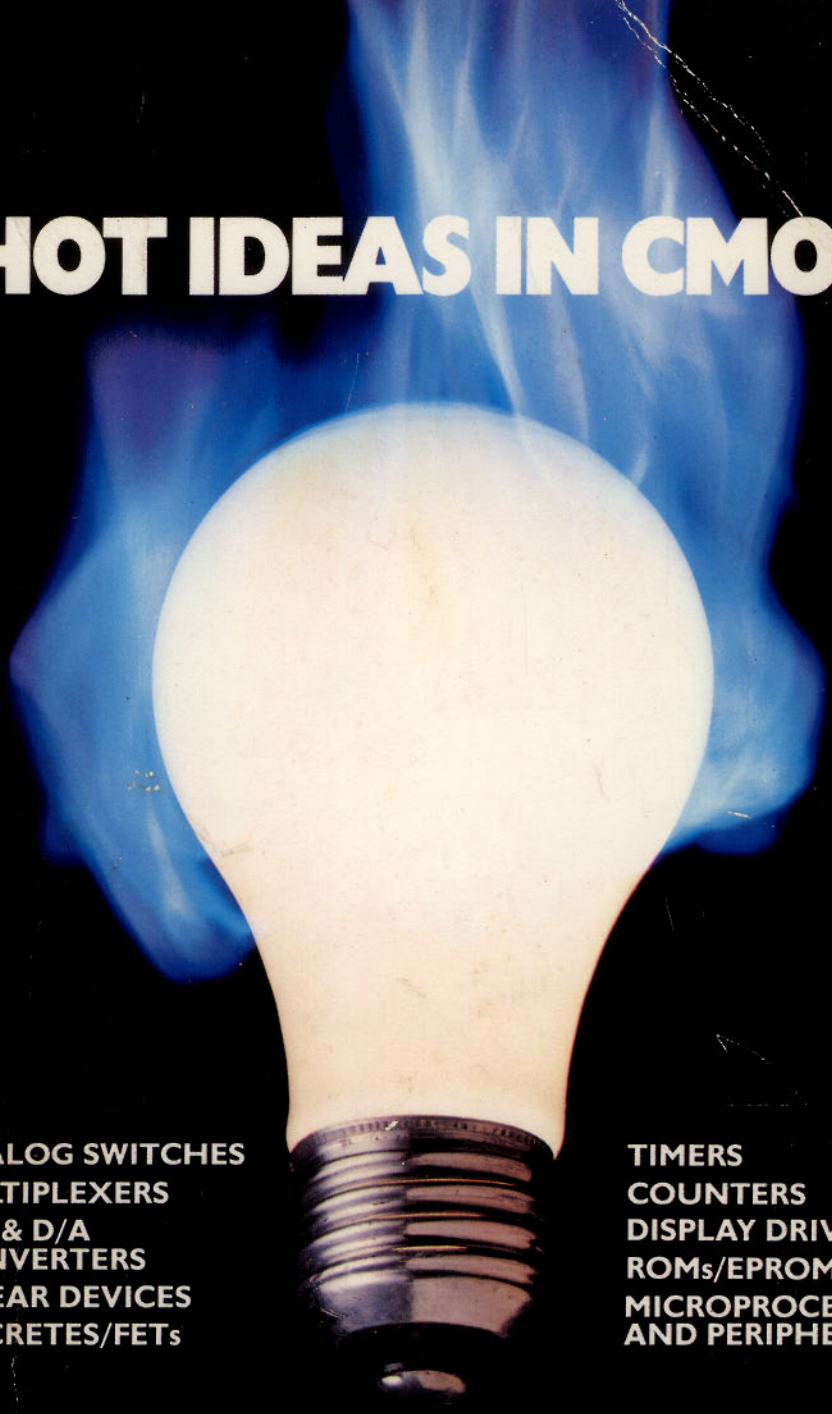
HOT IDEAS IN CMOS

ANALOG SWITCHES
MULTIPLEXERS
A/D & D/A CONVERTERS
LINEAR DEVICES
DISCRETES/FETs
TIMERS
COUNTERS
DISPLAY DRIVERS
ROMs/EPROMs
MICROPROCESSORS AND PERIPHERALS

INTERSIL



ANALOG SWITCHES
MULTIPLEXERS
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TIMERS
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INTERSIL

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ENGINEERING SOLUTIONS ON A CHIP FROM INTERSIL

Product offerings described in this data book reflect Intersil's commitment to industry leadership as a producer of advanced low-power analog and digital semiconductor components and data acquisition systems.

These components are fabricated using a wide variety of process technologies and are intended to provide state-of-the-art performance and maximum cost effectiveness.

Product areas in which Intersil demonstrates its innovative approach to providing engineering solutions on a chip include:

- **FIELD EFFECT AND DUAL MATCHED BIPOLAR TRANSISTORS**
  A complete line of high-performance junction FETs, dual JFETs, MOSFETs and matched dual bipolar devices.

- **DIGITAL**
  Very low-power CMOS ROMs and EPROMs, as well as high-speed HMOS ROMs; CMOS microprocessors, peripherals and UARTs.

- **ANALOG SWITCHES AND MULTIPLEXERS**
  The industry's broadest offering of highest-performance switches, including a video-RF switch with excellent isolation at 100 MHz, and multiplexers featuring the least error as well as unprecedented input overload protection.

- **ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS**
  3½- and 4½-digit display output (DVM) analog-to-digital converters; 12-, 14- and 16-bit microprocessor-compatible analog-to-digital converters; and high-speed precision digital-to-analog converters up to 14 bits.

- **LINEAR**
  A new set of low-power devices with unequalled performance—1-μV offset voltage op amps, 4-μA quiescent current regulators and supply monitors, 95-per-cent-efficient voltage converters and 1ppm/°C voltage references; a complete family of CMOS op amps; and a wide variety of special analog function circuits.

- **TIMERS, COUNTERS AND DISPLAY DRIVERS**
  A wide range of low-power counters, timers and multidigit LED, LCD and vacuum fluorescent display decoder/drivers, including those with full alphanumeric capability.

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PRODUCTION DATA SHEET
This is a full, final data sheet, and describes a mature product in full production. Although Intersil reserves the right to make changes in specifications contained in these data sheets at any time without notice, such changes are not common and are usually minor, generally relating to yield and processing improvements. These data sheets are not marked; others are marked preliminary.

PRELIMINARY DATA SHEET
A preliminary data sheet is issued in advance of the availability of production samples and generally indicates that at the time of printing, the device had not been fully characterized. In the case of a second-source part, the specifications are already determined, and a "preliminary" designation indicates the anticipated availability of the device.

ALPHANUMERIC INDEX
This part number index is arranged first by alpha sequence, (ie: ADCxxxx, DGxxx, Gxxx, ICLxxxx, ICMxxxx, etc.) then by numeric sequence (ie: LM100, LM101A, LM102, LM105, etc.) and ignoring package/temperature/pin number suffixes. The basic numbering sequence, is sorted by reading the part number characters from left to right. Reading the left character first (which is usually an alpha character), then the next character to the right and so forth.

BASE NUMBER INDEX
If only the basic part number is known, use the Base Number Index as a locator aid. The Base Number Index is organized in numeric sequence (with alpha prefixes appearing in bold type and numeric characters set in medium type). Devices are arranged in this index according to the numeric value of the first digit on the left, then the value of the second digit, then the third, and so on. For example, device number ICM7218 precedes ICL741, no package/temperature/pin number suffixes are included, but these may be obtained from the specific product data sheet.

FUNCTION INDEX
This is an index of Intersil device types categorized by product grouping and function. The first major subsection, DISCRETES, is further subdivided into categories for JFETs and Special Function devices.

All remaining major subsections (ANALOG SWITCHES/MULTIPLEXERS, DATA ACQUISITION, LINEAR, TIMERS/COUNTERS, TIMEKEEPING/DTMF, MEMORIES and MICROPROCESSORS/PERIPHERALS) are organized alphabetically by function. The Functional Index appears in its entirety in section A, and an appropriate subindex appears at the beginning of each major product section.

CROSS-REFERENCE GUIDES
Two cross-reference guides are provided: one for Discrete Devices and one for Integrated Circuits.

The Discrete Cross-Reference Guide indicates whether Intersil can provide the industry-standard type, or an Intersil preferred part instead.

The IC Alternate Source Cross-Reference Guide lists competitive manufacturer device types for which Intersil makes pin-for-pin replacements. In the left-hand column, the competitive device part number is organized alphabetically by manufacturer. The Intersil pin-for-pin replacement appears in the right hand column.

SELECTOR GUIDES
Selector guide tables appear at the front of each major product category subsection and provides a quick reference of key parameters for devices contained in that section.

DEVICE FUNCTION/PACKAGE CODES
Package dimensions and diagrams explaining device prefix and suffix codes appear in Appendix B.

DIE SELECTION CRITERIA
Many of Intersil's semiconductor products are available in die form. This subsection of Appendix B contains general information on criteria for transistor and integrated circuit die selection, including physical parameters, packaging for shipment, assembly, testing and purchase options.

HIGH-RELIABILITY PROCESSING
This subsection of Appendix B defines Intersil's commitment to 100 percent compliance with MIL-STD-883, MIL-STD-750, MIL-M-38510 and MIL-S-19500 specifications. It also outlines Intersil's programs for quality conformance, quality testing and limited use qualification and includes a glossary of military/aerospace Hi-Rel terms.

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†The ICL7136 is recommended for all applications which currently employ the ICL7126.

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*Not recommended for new designs. Use ICL8211/12 or ICL7665.

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**Obsolete product, refer to page A-9.

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The products listed below have been designed into circuits in the past, but are no longer likely to be the most economic choice for new designs.

These products are still available for use in existing designs. Data sheets for these products are available upon request.

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G116-19	LM107/307
G125-32	μA741
ICL7600/01	AD741K
ICL8052/7101	μA748
ICL8052/71C03	LH2101/2301
ICL8068/71C03	IH5101
ICL8052/53	LM4250
IH401	μA733
IMF5911/12	LM102/302
LD110/111	LM110/310
LD114	LH2110/2310
MM450/550	LH2111/2311
MM451/551	LM111/311
MM452/552	LM100/300
MM455/555	LM105/305
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LH0042	ICM7201

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AM9264	IM7364
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LH2301	LH2301
LH2311	LH2311
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LM105	LM105
LM107	LM107
LM108	LM108
LM110	LM110
LM111	LM111
LM301	LM301
LM302	LM302
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
723	µA723
733	µA733
741	µA741
748	µA748

AMI	Intersil
S68332	IM7332
S68364	IM7364

Analog Devices	Intersil
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AD108	LM108
AD301	LM301
AD308	LM308
AD503	AD503
AD590	AD590
AD741	µA741
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AD7506/MIL/CHIPS	IH6116M/D
AD7506JD	IH6116CJI
AD7506JD/883B	IH6116JI/883B
AD7506JN	IH6116CPI
AD7506KD	IH6116CJI
AD7506KD/883B	IH6116CJI/883B
AD7506KN	IH6116CPI
AD7506SD	IH6116MJI
AD7506SD/883B	IH6116MJI/883B
AD7506TD	IH6116MJI
AD7506TD/883B	IH6116MJI/883B
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AD7507/MIL/CHIPS	IH6216M/D
AD7507JD	IH6216CJI
AD7507JD/883B	IH6216CJI/883B
AD7507JN	IH6216CPI
AD7507KD	IH6216CJI
AD7507KD/883B	IH6216CJI/883B
AD7507KN	IH6216CPI
AD7507SD	IH6216MJI
AD7507SD/883B	IH6216MJI/883B
AD7507TD	IH6216MJI
AD7507TD/883B	IH6216MJI/883B
AD7520JD	AD7520JD
AD7502JN	AD7520JN
AD7520KD	AD7520KD
AD7520KN	AD7520KN
AD7520LD	AD7520LD
AD7520LN	AD7520LN
AD7520SD	AD7520SD
AD7520TD	AD7520TD
AD7520UD	AD7520UD
AD7521JD	AD7521JD
AD7521JN	AD7521JN
AD7521KD	AD7521KD
AD7521KN	AD7521KN
AD7521LD	AD7521LD
AD7521LN	AD7521LN
AD7521SD	AD7521SD
AD7521TD	AD7521TD
AD7521UD	AD7521UD
AD7523AD	AD7523AD
AD7523BD	AD7523BD
AD7523CD	AD7523CD
AD7523JN	AD7523JN
AD7523KN	AD7523KN
AD7523LN	AD7523LN
AD7523SD	AD7523SD
AD7523TD	AD7523TD
AD7523UD	AD7523UD
AD7530JD	AD7530JD
AD7530JN	AD7530JN
AD7530KD	AD7530KD
AD7530KN	AD7530KN
AD7530LD	AD7530LD
AD7530LN	AD7530LN
AD7531JD	AD7531JD
AD7531JN	AD7531JN
AD7531KD	AD7531KD
AD7531KN	AD7531KN
AD7531LD	AD7531LD
AD7531LN	AD7531LN
AD7533AD	AD7533AD
AD7533BD	AD7533BD
AD7533CD	AD7533CD
AD7533JN	AD7533JN
AD7533KN	AD7533KN
AD7533LN	AD7533LN
AD7533SD	AD7533SD
AD7533TD	AD7533TD
AD7533UD	AD7533UD
AD7541AD	AD7541AD
AD7541BD	AD7541BD
AD7541JN	AD7541JN
AD7541KN	AD7541KN
AD7541SD	AD7541SD
AD7541TD	AD7541TD

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DAC7523	AD7523
DAC7533	AD7533
DAC7541	AD7541
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E1151	ICM1115B

Exar	Intersil
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XR8038	ICL8038
XRL555	ICM7555
XRL556	ICM7556
XR2242	ICM7242

Fairchild	Intersil
µA101	LM101
µA102	LM102
µA105	LM105
µA107	LM107
µA108	LM108
µA110	LM110
µA111	LM111
µA301	LM301
µA302	LM302
µA305	LM305
µA307	LM307
µA308	LM308
µA310	LM310
µA311	LM311
µA723	µA723
µA733	µA733
µA740	µA740
µA741	µA741
µA748	µA748
µA777	µA777

GI	Intersil
9332	IM7332
9364	IM7364

GTE	Intersil
2114	2114
2332	IM7332
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Harris	Intersil
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HI1-0509A-5	IH5208IJE
HI1-0509A-8	IH5208MJE/883B
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HI1-0506-5	IH6116CJI
HI1-0506-8	IH6116MJI/883B
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HI1-0507-2	IH6216MJI
HI1-0507-5	IH6216CJI
HI1-0507-8	IH6216MJI/883B
HI3-0507-5	IH6216CPI
HI0-5040-6	IH5040C/D
HI1-5040-2	IH5040MJE
HI1-5040-5	IH5040CPE
HI1-5040-8	IH5040MJE/883B
HI0-5041-6	IH5041C/D
HI1-5041-2	IH5041MJE
HI1-5041-5	IH5041CPE
HI1-5041-8	IH5041MJE/883B
HI0-5042-6	IH5042C/D
HI1-5042-2	IH5042MJE
HI1-5042-5	IH5042CPE
HI1-5042-8	IH5042MJE/883B
HI0-5043-6	IH5043C/D
HI1-5043-2	IH5043MJE
HI1-5043-5	IH5043CPE
HI1-5043-8	IH5043MJE/883B
HI0-5044-6	IH044C/D
HI1-5044-2	IH5044MJE
HI1-5044-5	IH5044CPE
HI1-5044-8	IH5044MJE/883B
HI0-5045-6	IH5045C/D
HI1-5045-2	IH5045MJE
HI1-5045-5	IH5045CPE
HI1-5045-8	IH5045MJE/883B
HI0-5046-6	IH5046C/D
HI1-5046-2	IH5046MJE
HI1-5046-5	IH5046CPE
HI1-5046-8	IH5046MJE/883B
HI0-5047-6	IH5047C/D
HI1-5047-2	IH5047MJE
HI1-5047-5	IH5047CPE
HI1-5047-8	IH5047MJE/883B
HI0-5048-6	IH5048C/D
HI1-5048-2	IH5048MJE
HI1-5048-5	IH5048CJE,CPC
HI1-5048-8	IH5048MJE/883B
HI0-5049-6	IH5049C/D
HI1-5049-2	IH5049MJE
HI1-5049-5	IH5049CJE,CPE
HI1-5049-8	IH5049MJE/883B
HI0-5050-6	IH5050C/D
HI1-5050-2	IH5050MJE
HI1-5050-5	IH5050CJE,CPE
HI1-5050-8	IH5050MJE/883B
HI0-5051-6	IH5051C/D
HI1-5051-2	IH5051MJE
HI1-5051-5	IH5051CJE,CPE
HI1-5051-8	IH5051MJE/883B
LM101	LM101
LM4250	LM4250

MicroPower Systems	Intersil
MP7520JD	AD7520JD
MP7520JN	AD7520JN
MP7520KD	AD7520KD
MP7520KN	AD7520KN
MP7520LD	AD7520LD
MP7520LN	AD7502LN
MP7520SD	AD7520SD
MP7520TD	AD7520TD

IC Alternate Source Index (continued)

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MP7520UD	AD7520UD
MP7521JD	AD7521JD
MP7521JN	AD7521JN
MP7521KD	AD7521KD
MP7521KN	AD7521KN
MP7521LD	AD7521LD
MP7521LN	AD7521LN
MP7521SD	AD7521SD
MP7521TD	AD7521TD
MP7521UD	AD7521UD
MP7523JN	AD7523JN
MP7523KN	AD7523KN
MP7523LN	AD7523LN
MP7530JD	AD7530JD
MP7530JN	AD7530JN
MP7530KD	AD7530KD
MP7530KN	AD7530KN
MP7530LD	AD7530LD
MP7530LN	AD7530LN
MP7531JD	AD7531JD
MP7531JN	AD7531JN
MP7531KD	AD7531KD
MP7531KN	AD7531KN
MP7531LD	AD7531LD
MP7531LN	AD7531LN
MP7533AD	AD7533AD
MP7533BD	AD7533BD
MP7533CD	AD7533CD
MP7533JN	AD7533JN
MP7533KN	AD7533KN
MP7533LN	AD7533LN
MP7533SD	AD7533SD
MP7533TD	AD7533TD
MP7533UD	AD7533UD
MP7621AD	AD7541AD
MP7621BD	AD7541BD
MP7621JN	AD7541JN
MP7621KN	AD7541LN
MP7621SD	AD7541SD
MP7621TD	AD7541TD

Mitsubishi	**Intersil**
M58435P	ICM1115B

Motorola	**Intersil**
LM101	LM101
LM105	LM105
LM107	LM107
LM110	LM110
LM111	LM111
LM301	LM301
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
MCM68332	IM7332
MCM68364	IM7364
MC1723	μA723
MC1741	μA741
MC1748	μA748
MHW590	AD590

National Semiconductor	**Intersil**
AD7520JD (DAC1022LCD)	AD7520JD
AD7520JN (DAC1022LCN)	AD7520KD
AD7520KN (DAC1021LCD)	AD7520KD
AD7520KN (DAC1021LCN)	AD7520KN
AD7520LD (DAC1020LCD)	AD7520LD
AD7520LN (DAC1020LCN)	AD7520LN
AD7520SK (DAC1022LD)	AD7520SD
AD7520TD (DAC1021LD)	AD7520TD
AD7520UD (DAC1020LD)	AD7520UD
AD7521JD (DAC1222LCD)	AD7521JD
AD7521JN (DAC1222LCN)	AD7521JN
AD7521KD (DAC1221LCD)	AD7521KD
AD7521KN (DAC1221LCN)	AD7521KN
AD7521LD (DAC1220LCD)	AD7521LD
AD7521LN (DAC1220LCN)	AD7521LN
AD7521SD (DAC1222LD)	AD7521SD
AD7521TD (DAC1221LD)	AD7521TD
AD7521UD (DAC1220LD)	AD7521UD
AD7530JD (DAC1022LCD)	AD7530JD
AD7530JN (DAC1022LCN)	AD7530JN
AD7530KD (DAC1021LCD)	AD7530KD
AD7530KN (DAC1021LCN)	AD7530KN
AD7530LD (DAC1020LCD)	AD7530LD
AD7530LN (DAC1020LCN)	AD7530LN
AD7531JD (DAC1222LCD)	AD7531JD
AD7531JN (DAC1222LCN)	AD7531JN
AD7531KD (DAC1221LCD)	AD7531KD
AD7531KN (DAC1221LCN)	AD7531KN
AD7531LD (DAC1220LCD)	AD7531LD
AD7531LN (DAC1220LCN)	AD7531LN
AD7533AD (DAC1022LCD)	AD7533AD
AD7533BD (DAC1021LCD)	AD7533BD
AD7533CD (DAC1020LCD)	AD7533CD
AD7533JN (DAC1022LCN)	AD7533JN
AD7533KN (DAC1021LCN)	AD7533KN
AD7533LN (DAC1020LCN)	AD7533LN
AD7533SD (DAC1022LD)	AD7533SD
AD7533TD (DAC1021LC)	AD7533TD
AD7533UD (DAC1020LD)	AD7533UD
AH0139CD	DG139BK
AH0139D	DG139AK
AH0139D/883	DG139AK/883B
AH0142CD	DG142BK
AH0142D	DG142AK
AH0142D/883	DG142AK/883B
AH0143CD	DG143BK
AH0143D	DG143AK
AH0143D/883	DG143AK/883B
AH0144CD	DG144BK
AH0144D	DG144AK
AH0144D/883	DG144AK/883B
AD0145CD	DG145BK
AH0145D	DG145AK
AH0145D/883	DG145AK/883B
AH0146CD	DG146BK
AH0146D	DG146AK
AH0146D/883	DG146AK/883B
AH0161CD	DG161BK
AH0161D	DG161AK
AH0161D/83	DG161AK/883B
AH0162CD	DG162BK
AH0162D	DG162AK
AH0162D/883B	DG162AK/883B
AH0163CD	DG163BK
AH0163	DG163AK
AH0163D/883	DG163AK/883B
AH0164CD	DG164BK
AH0164D	DG164AK
AH0164D/883	DG164AK/883B
AH5009CN	IH5009CPD
AH5010CN	IH5010CPD
AH5011CN	IH5011CPE
AH5012CN	IH5012CPE
AN5013CN	IH5013CPD
AH5014CN	IH5014CPD
AH5015CN	IH5015CPE
AH5016CN	IH5016CPE
AM9709CN	IH5009CPD
AM97C09CN	IH5009CPD
AM9710CN	IH5010CPD
AM97C10CN	IH5010CPD
AM9711CN	IH5011CPE
AM97C11CN	IH5011CPE
AM9712CN	IH5012CPE
AM97C12CN	IH5012CPE
DM7555	ICM7555
DM7556	ICM7556
LF11201D	DG201AK
LF11201D/883	DG201AK/883B
LF11508D	IH6108MJE
LF11508D/883	IH6108MJE/883B
LF11509D	IH6208MJE
LF11509D/883	IH6208MJE/883B
LF13201	DG201
LH0042	LH0042
LH2108	LH2108
LH2110	LH2110
LH2111	LH2111
LH2301	LH2301
LH2308	LH2308
LH2310	LH2310
LH2311	LH2311
LM100	LM100
LM101	LM101
LM102	LM102
LM105	LM105
LM107	LM107
LM108	LM108
LM110	LM110
LM111	LM111
LM300	LM300
LM301	LM301
LM302	LM302
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
LM4250	LM4250
LM723	μA723
LM733	μA733
LM740	μA740
LM741	μA741
LM742	μA748
MM52132	IM7332
MM52164	IM7364
MM74C946	ICM7224

NEC	**Intersil**
μPD816C	ICM7038B
μPD820C	ICM1115B
μPD833G	ICM7223
μPD1963C	ICM7050
μPD2332	IM7332
μPD2364	IM7364

NPC	**Intersil**
SM5510	ICM1115B

OKI	**Intersil**
MSM503	AD503

Panasonic/Matsushita	**Intersil**
MN6091	ICM7038B
MN6093	ICM7051A

Phillips/Fasalec	**Intersil**
MB7B	ICM7245U
MB101	ICM7245B
MB103	ICM7245E
MB105	ICM7245U
MB107	ICM7245D
MB108	ICM7245E
MB143	ICM7245A
MB144	ICM7245F
MB510	ICM1115B

Plessey	**Intersil**
SC748	μA748

PMI	**Intersil**
PM308	LM308
SSS741	μA741

Raytheon	**Intersil**
LH2101	LH2101
LH2301	LH2301
LH2311	LH2311
LM101	LM101
LM105	LM105
LM107	LM107
LM108	LM108
LM301	LM301
LM305	LM305
LM307	LM307
LM308	LM308
LM311	LM311
RC723	μA723
RC733	μA733
RC741	μA741
RC748	μA748
RM723	μA723
RM741	μA741
RM748	μA748

RCA	**Intersil**
CA101	LM101
CA107	LM107
CA111	LM111
CA301	LM301
CA307	LM307
CA308	LM308
CA311	LM311
CA723	μA723
CA741	μA741
CA748	μA748
CD22015E	ICM7051A
CPD6402	IM6402

Samsong	**Intersil**
KS5240U01E	ICM7245U
KS5240B01J	ICM7245A
KS5240B01H	ICM7245B
KS5240B10H	ICM7245D
KS5240B12H	ICM7245E
KS5240B20H	ICM7245F

Sanyo	**Intersil**
LC7523	AD7523

Signetics	**Intersil**
μA723	μA723
μA733	μA733
μA740	μA740
μA741	μA741
μA748	μA748
LH2101	LH2101
LH2108	LH2108
LH2301	LH2301
LH2308	LH2308

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Silicon General	Intersil
µA777	µA777
SG101	LM101
SG105	LM105
SG107	LM107
SG108	LM108
SG110	LM110
SG111	LM111
SG301	LM301
SG305	LM305
SG307	LM307
SG308	LM308
SG311	LM311
SG4250	LM4250
SG723	µA723
SG733	µA733
SG741	µA741
SG748	µA748
SG7520	AD7520
SG7521	AD7521
SG7523	AD7523

Siliconix	Intersil
DF412	ICM7211
DG123AL	DG123AL
DG123AP	DG123AK
DG123BP	DG123BK
DG125AL	DG125AL
DG125AP	DG125AK
DG125BP	DG125BK
DG139AL	DG139AL
DG139AP	DG139AK
DG139BP	DG139BK
DG142AL	DG142AL
DG142AP	DG142AK
DG142BP	DG142BK
DG143AL	DG143AL
DG143AP	DG143AK
DG143BP	DG143BK
DG144AL	DG144AL
DG144AP	DG144AK
DG144AP	DG144BK
DG145AL	DG145AL
DG145AP	DG145AK
DG145BP	DG145BK
DG146AL	DG146AL
DG146AP	DG146AK
DG146BP	DG146BK
DG161AL	DG161AL
DG161AP	DG161AK
DG161BP	DG161BK
DG162AL	DG162AL
DG162AP	DG162AK
DG162BP	DG162BK
DG163AL	DG163AL
DG163AP	DG163AK
DG163BP	DG163BK
DG164AL	DG164AL
DG164AP	DG164AK
DG164BP	DG164BK
DG180AA	DG180AA
DG180AL	DG180AL
DG180AP	DG180AK
DG180BA	DG180BA
DG180BP	DG180BK
DG181AA	DG181AA
DG181AL	DG181AL
DG181AP	DG181AK
DG181BA	DG181BA
DG181BP	DG181BK
DG182AA	DG182AA
	DGM182AA
DG182AL	DG182AL
	DGM182AL
DG182AP	DG182AK
	DGM182AK
DG182BA	DG182BA
	DGM182BA
DG182BP	DG182BK
	DGM182BK
DG183AL	DG183AL
DG183AP	DG183AK
DG183BP	DG183BK
DG184AL	DG184AL
DG184AP	DG184AK
DG184BP	DG184BK
DG185AL	DG185AL
	DGM185AL
DG185AP	DG185AK
	DGM185AK
DG185BP	DG185BK
	DGM185BK
DG186AA	DG186AA
DG186AL	DG186AL
DG186AP	DG186AK
DG186BA	DG186BA
DG186BP	DG186BK
DG187AA	DG187AA
DG187AL	DG187AL
DG187AP	DG187AK
DG187BA	DG187BA
DG187BP	DG187BK
DG188AA	DG188AA
	DGM188AA
DG188AL	DG188AL
DG188AP	DG188AK
DG188BA	DG188BA
	DGM188BA
DG188BP	DG188BK
DG189AL	DG189AL
DG189AP	DG189AK
DG189BP	DG189BK
DG190AL	DG190AL
DG190AP	DG190AK
DG190BP	DG190BK
DG191AL	DG191AL
	DGM191AL
DG191AP	DG191AK
	DGM191AK
DG191BP	DG191BK
	DGM191BK
DG200AA	DG200AA
DG200AL	DG200AL
DG200AP	DG200AK
DG200BA	DG200BA
DG200BP	DG200BK
DG200CJ	DG200CJ
DG201AP	DG201AK
DG201BP	DG201BK
DG201CJ	DG201CJ
DG381AA	DGM182AA
DG381AK	DGM182AK
DG381AP	DGM182AK
DG381BA	DGM181BA
DG381BK	DGM181BK
DG381BP	DGM181BK
DG381CJ	DGM181CJ
DG384AK	DGM185AK
DG384AP	DGM185AK
DG384BK	DGM184BK
DG384BP	DGM184BK
DG384CJ	DGM184CJ
DG387AA	DGM188AA
DG387AK	DGM188AK
DG387AP	DGM188AK
DG387BA	DGM187BA
DG387BK	DGM187BK
DG387BP	DGM187BK
DG390AK	DGM191AK
DG390AP	DGM191AK
DG390BK	DGM190BK
DG390BP	DGM190BK
DG390CJ	DGM190CJ
DG503	AD503
DG506AR	IH6116MJI
DG506BR	IH6116CJI
DG506CJ	IH6116CPI
DG507AR	IH6216MJI
DG507BR	IH6216CJI
DG507CJ	IH6216CPI
DG508AP	IH6108MJE
DG508BP	IH6108CJE
DG508CJ	IH6108CPE
DG509AP	IH6208MJE
DG509BP	IH6208CJE
DG509CJ	IH6208CPE
D123AL	D123AL
D123AP	D123AK
D123BP	D123BK
D125AL	D125BJ
D125AP	D125AL
	D125AK
D125BP	D125BK
	D125BJ
D129AL	D129AL
D129AP	D129AK
D129BP	D129BK

Sprague	Intersil
UCN-4112M	ICM7051A
UCN-4113M	ICM7038B
UHP-503	AD503

Synertek	Intersil
SY2332	IM7332
SY2364	IM7364

TI	Intersil
µA723	µA723
µA733	µA733
µA741	µA741
µA748	µA748
µA777	µA777
LM101	LM101
LM105	LM105
LM107	LM107
LM111	LM111
LM301	LM301
LM305	LM305
LM307	LM307
LM311	LM311
SN74S188	DGM182BA
TL182CL	DGM182BA
TL182CN	DGM182CJ
TL182IL	DGM182BA
TL182IN	DGM182CJ
TL182ML	DGM182AA
TL185CJ	IH5045CJE
TL185CN	IH5045CPE
TL185IJ	IH5045CJE
TL185IN	IH5045CPE
TL185MJ	IH5045MJE
TL188CL	IH5042CTW
TL188CN	IH5042CPE
TL188IL	IH5042CTW
TL188IN	IH5042CPE
TL188ML	IH5042MTW
TL191CJ	IH5043CJE
TL191CN	IH5043CPE
TL191IJ	IH5043CJE
TL191IN	IH5043CPE
TL191MJ	IH5043MJE
TL503	AD503

Toshiba	Intersil
TC8031P	ICM7038A
TC8051P	ICM7038B
TC8056PA	ICM1115B
TC8057P	ICM7038D
TMM2114	2114
TMM2332	IM7332
TMM2364	IM7364

DISCRETE CROSS REFERENCE

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
100S	2N5458	2N2606	2N2607	2N3331	2N5270	2N3814	IT132
100U	2N3684	2N2607	2N2607	2N3332	2N5268	2N3815	IT132
102M	2N5686	2N2608	2N2608	2N3333	IT132	2N3816	IT130
102S	2N5457	2N2609	2N2609	2N3334	IT132	2N3816A	IT130A
103M	2N5457	2N2609JAN	2N2609JAN	2N3335	IT132	2N3817	IT130
103S	2N5459	2N2639	IT120	2N3336	IT132	2N3817A	IT130A
104M	2N5458	2N2640	IT122	2N3347	IT137	2N3819	2N5484
105M	2N5459	2N2641	IT122	2N3348	IT138	2N3820	2N2608
105U	2N4340	2N2642	IT120	2N3349	IT139	2N3821	2N3821
106M	2N5485	2N2643	IT122	2N3350	IT137	2N3822	2N3822
107M	2N5485	2N2644	IT122	2N3351	IT138	2N3823	2N3823
110U	2N3685	2N2652	IT120	2N3352	IT139	2N3824	2N3824
120U	2N3686	2N2652A	IT120	2N3365	2N4340	2N3907	IT120
125U	2N4339	2N2720	IT120	2N3366	2N4338	2N3908	IT120
1277A	2N3822	2N2721	IT122	2N3367	2N4338	2N3909	2N2609
1278A	2N3821	2N2722	IT120	2N3368	2N4341	2N3909A	2N2609
1279A	2N3821	2N2802	IT139	2N3369	2N4339	2N3921	2N3921
1280A	2N4224	2N2803	IT139	2N3370	2N4338	2N3922	2N3922
1281A	2N3822	2N2804	IT139	2N3376	2N2608	2N3949	IT132
1282A	2N4341	2N2805	IT139	2N3378	2N2608	2N3950	IT132
1283A	2N4340	2N2806	IT139	2N3380	2N2609	2N3954	2N3954
1284A	2N4222	2N2807	IT139	2N3382	2N3994	2N3954A	2N3954A
1285A	2N3821	2N2841	2N2607	2N3384	2N3993	2N3955	2N3955
1286A	2N4220	2N2842	2N2607	2N3386	2N5114	2N3955A	2N3955A
130U	2N3687	2N2843	2N2607	2N3409	IT122	2N3956	2N3956
1325A	2N4222	2N2844	2N2607	2N3410	IT122	2N3957	2N3957
135U	2N4339	2N2903	IT122	2N3411	IT122	2N3966	2N4416
14T	2N4224	2N2903A	IT120	2N3423	IT122	2N3967	2N4221
155U	2N4416	2N2910	IT122	2N3424	IT122	2N3967A	2N4221
1714A	2N4340	2N2913	IT122	2N3425	IT122	2N3968	2N3685
182S	2N4391	2N2914	IT120	2N3436	2N4341	2N3968A	2N3685
183S	2N3823	2N2915	IT120	2N3437	2N4340	2N3969	2N3686
197S	2N4338	2N2915A	IT120	2N3438	2N4338	2N3969A	2N3686
198S	2N4340	2N2916	IT120	2N3452	2N4220	2N3970	2N3970
199S	2N4341	2N2916A	IT120	2N3453	2N4338	2N3971	2N3971
2000M	2N3823	2N2917	IT122	2N3454	2N4338	2N3972	2N3972
2001M	2N3823	2N2918	IT122	2N3455	2N4340	2N3993	2N3993
200S	2N4392	2N2919	IT120	2N3456	2N4338	2N3993A	2N3993
200U	2N3824	2N2919A	IT120	2N3457	2N4338	2N3994	2N3994
201S	2N4391	2N2920	2N2920	2N3458	2N4341	2N3994A	2N3994
202S	2N4392	2N2920A	2N2920	2N3459	2N4339	2N4009	IT132
203S	2N3821	2N2936	IT120	2N3460	2N4338	2N4010	IT132
204S	2N3821	2N2937	IT120	2N3513	IT122	2N4011	IT132
2078A	2N3955	2N2972	IT122	2N3514	IT122	2N4015	IT139
2079A	2N3955	2N2973	IT122	2N3515	IT122	2N4016	IT137
2080A	2N3955A	2N2974	IT120	2N3516	IT122	2N4017	IT139
2081A	2N3955A	2N2975	IT120	2N3517	IT122	2N4018	IT139
2093M	2N3687	2N2976	IT120	2N3521	IT122	2N4019	IT139
2094M	2N3686	2N2977	IT120	2N3522	IT122	2N4020	IT139
2095M	2N3686	2N2978	IT120	2N3574	2N2607	2N4021	IT139
2098A	2N3954	2N2979	IT120	2N3575	2N2607	2N4022	IT139
2099A	2N3955A	2N2980	IT121	2N3578	2N2608	2N4023	IT137
210U	2N4416	2N2981	IT122	2N3587	IT122	2N4024	IT137
2130U	2N5452	2N2982	IT122	2N3608	3N172	2N4025	IT137
2132U	2N3955	2N3043	IT121	2N3680	IT120	2N4026	3N163
2134U	2N3956	2N3044	IT122	2N3684	2N3684	2N4038	2N4351
2136U	2N3957	2N3045	IT122	2N3684A	2N3684	2N4039	2N4351
2138U	2N3958	2N3046	IT121	2N3685	2N3685	2N4065	3N163
2139U	2N3958	2N3047	IT122	2N3685A	2N3685	2N4066	3N166
2147U	2N3958	2N3048	IT122	2N3686	2N3686	2N4067	3N166
2148U	2N3958	2N3049	IT139	2N3686A	2N3686	2N4082	2N3954
2149U	2N3958	2N3050	IT139	2N3687	2N3687	2N4083	2N3955
231S	2N3954	2N3051	IT139	2N3687A	2N3687	2N4084	2N3954
232S	2N3955	2N3052	IT129	2N3726	IT131	2N4085	2N3955
233S	2N3956	2N3059	IT139	2N3727	IT130	2N4091	2N4091
234S	2N3957	2N3066	2N4340	2N3728	IT122	2N4091A	2N4091
235S	2N3958	2N3067	2N4338	2N3729	IT121	2N4091JAN	2N4091JAN
241U	2N4869	2N3068	2N4338	2N3800	IT132	2N4091JANTX	2N4091JANTX
250U	2N4091	2N3069	2N4341	2N3801	IT132	2N4091JANTXV	2N4091JANTXV
251U	2N4392	2N3070	2N4339	2N3802	IT132	2N4092	2N4092
2N2060	IT120	2N3071	2N4338	2N3803	IT132	2N4092A	2N4092
2N2060A	IT121	2N3084	2N4339	2N3804	IT130	2N4092JAN	2N4092JAN
2N2060B	IT121	2N3085	2N4339	2N3804A	IT130A	2N4092JANTX	2N4092JANTX
2N2223	IT122	2N3086	2N4339	2N3805	IT130	2N4092JANTXV	2N4092JANTXV
2N2223A	IT121	2N3087	2N4339	2N3805A	IT130A	2N4093	2N4093
2N2386	2N2608	2N3088	2N4339	2N3806	IT122	2N4093A	2N4093
2N2386A	2N2608	2N3088A	2N4339	2N3807	IT122	2N4093JAN	2N4093JAN
2N2453	IT122	2N3089	2N4339	2N3808	IT122	2N4093JANTX	2N4093JANTX
2N2453A	IT121	2N3089A	2N4339	2N3809	IT122	2N4093JANTXV	2N4093JANTXV
2N2480	IT122	2N3113	2N2607	2N3810	2N3810	2N4100	2N4100
2N2480A	IT121	2N3277	2N2606	2N3810A	2N3810A	2N4117	2N4117
2N2497	2N2608	2N3278	2N2607	2N3811	2N3811	2N4117A	2N4117A
2N2498	2N2608	2N3328	2N5265	2N3811A	2N3811A	2N4118	2N4118
2N2499	2N2609	2N3329	2N5267	2N3812	IT132	2N4118A	2N4118A
2N2500	2N2608	2N3330	2N5268	2N3813	IT132	2N4119	2N4119

**CONSULT FACTORY

DISCRETE CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
2N4119A	2N4119A	2N5045	2N5453	2N5484	2N5484	2N6484	2N6484
2N4120	3N163	2N5046	2N5454	2N5485	2N5485	2N6485	2N6485
2N4139	2N3822	2N5047	2N5454	2N5486	2N5486	2N6502	IT122
2N4220	2N4220	2N5078	2N5397	2N5515	2N5515	2N6503	IT122
2N4220A	2N4220	2N5090	IT122	2N5516	2N5516	2N6550	2N4868A
2N4221	2N4221	2N5103	2N4416	2N5517	2N5517	2N6568	2N5432
2N4221A	2N4221	2N5104	2N4416	2N5518	2N5518	2SC294	IT122
2N4222	2N4222	2N5105	2N4416	2N5519	2N5519	2SJ11	2N2607
2N4222A	2N4222	2N5114	2N5114	2N5520	2N5520	2SJ12	2N2607
2N4223	2N4223	2N5114JAN	2N5114JAN	2N5521	2N5521	2SJ13	2N5270
2N4224	2N4224	2N5114JANTX	2N5114JANTX	2N5522	2N5522	2SJ15	2N2607
2N4267	3N163	2N5114JANTXV	2N5114JANTXV	2N5523	2N5523	2SJ16	2N2607
2N4268	3N161	2N5115	2N5115	2N5524	2N5524	2SJ47	**
2N4302	2N4302	2N5115JAN	2N5115JAN	2N5545	2N3954	2SJ48	**
2N4303	2N5459	2N5115JANTX	2N5115JANTX	2N5546	2N3955A	2SJ49	**
2N4304	2N5458	2N5115JANTXV	2N5115JANTXV	2N5547	2N3955	2SJ50	**
2N4338	2N4338	2N5116	2N5116	2N5549	2N4093	2SJ78	**
2N4339	2N4339	2N5116JAN	2N5116JAN	2N5555	J310	2SJ79	**
2N4340	2N4340	2N5116JANTX	2N5116JANTX	2N5556	2N3685	2SJ80	**
2N4341	2N4341	2N5116JANTXV	2N5116JANTXV	2N5557	2N3684	2SK11	2N5457
2N4342	2N5461	2N5117	2N5117	2N5558	2N3684	2SK12	2N5457
2N4343	2N5462	2N5118	2N5118	2N5561	U401	2SK13	2N5457
2N4351	2N4351	2N5119	2N5119	2N5562	U402	2SK132	**
2N4352	3N163	2N5120	IT131	2N5563	U404	2SK133	**
2N4353	3N172	2N5121	IT132	2N5564	IT550	2SK134	**
2N4360	2N5460	2N5122	IT132	2N5565	IT550	2SK135	**
2N4381	2N2609	2N5123	IT131	2N5566	IT550	2SK15	2N4868
2N4382	2N5115	2N5124	IT132	2N5592	2N3822	2SK17	2N5484
2N4391	2N4391	2N5125	IT132	2N5593	2N3822	2SK178	**
2N4392	2N4392	2N5158	2N5434	2N5594	2N3822	2SK179	**
2N4393	2N4393	2N5159	2N5433	2N5638	2N5638	2SK18	2N3821
2N4416	2N4416	2N5163	2N3822	2N5639	2N5639	2SK180	**
2N4416A	2N4416A	2N5196	2N5196	2N5640	2N5640	2SK19	ITE4416
2N4417	2N4416	2N5197	2N5197	2N5647	2N4117A	2SK23	2N5459
2N4445	2N5432	2N5198	2N5198	2N5648	2N4117A	2SK30	2N5458
2N4446	2N5434	2N5199	2N5199	2N5649	2N4117A	2SK32	2N3822
2N4447	2N5432	2N5245	ITE4416	2N5653	2N5638	2SK33	2N5397
2N4448	2N5434	2N5246	2N5484	2N5654	2N5639	2SK34	2N3822
2N4856	2N4856	2N5247	2N5486	2N5668	2N5484	2SK37	2N5484
2N4856A	2N4856	2N5248	2N5486	2N5669	2N5485	2SK41	2N5459
2N4856JAN	2N4856JAN	2N5254	IT132	2N5670	2N5486	2SK42	2N3822
2N4856JANTX	2N4856JANTX	2N5255	IT132	2N5793	IT129	2SK43	ITE4092
2N4856JANTXV	2N4856JANTXV	2N5256	IT130	2N5794	IT129	2SK44	ITE4416
2N4857	2N4857	2N5257	2N5457	2N5795	IT139	2SK46	2N5459
2N4857A	2N4857	2N5258	2N5458	2N5796	IT139	2SK48	2N3821
2N4857JAN	2N4857JAN	2N5259	2N5459	2N5797	2N2608	2SK49	2N5484
2N4857JANTX	2N4857JANTX	2N5265	2N2607	2N5798	2N2608	2SK50	ITE4416
2N4857JANTXV	2N4857JANTXV	2N5266	2N2607	2N5799	2N2608	2SK54	2N3822
2N4858	2N4858	2N5267	2N2608	2N5800	2N2608	2SK55	2N3822
2N4858A	2N4858	2N5268	2N2608	2N5801	2N4393	2SK56	2N5459
2N4858JAN	2N4858JAN	2N5269	2N2609	2N5802	2N4393	2SK61	2N5397
2N4858JANTX	2N4858JANTX	2N5270	2N2609	2N5803	2N4392	2SK65	J201
2N4858JANTXV	2N4858JANTXV	2N5277	2N4341	2N5843	IT130	2SK66	2N3821
2N4859	2N4859	2N5278	2N4341	2N5844	IT130	2SK68	2N3822
2N4859A	2N4859	2N5358	2N4220	2N5902	2N5902	2SK72	2N5196
2N4859JAN	2N4856JAN	2N5359	2N4220	2N5903	2N5903	3GS	2N3821
2N4859JANTX	2N4856JANTX	2N5360	2N4221	2N5904	2N5904	3N145	3N163
2N4860	2N4860	2N5361	2N4221	2N5905	2N5905	3N146	3N163
2N4860A	2N4860	2N5362	2N4222	2N5906	2N5906	3N147	3N189
2N4860JAN	2N4857JAN	2N5363	2N4222	2N5907	2N5907	3N148	3N189
2N4860JANTX	2N4857JANTX	2N5364	2N4222	2N5908	2N5908	3N149	3N161
2N4861	2N4861	2N5391	2N4867A	2N5909	2N5909	3N150	3N163
2N4861A	2N4861	2N5392	2N4868A	2N5911	2N5911	3N151	3N190
2N4861JAN	2N4858JAN	2N5393	2N4869A	2N5912	2N5912	3N155	3N163
2N4861JANTX	2N4858JANTX	2N5394	2N4869A	2N5949	2N5486	3N155A	3N163
2N4867	2N4867	2N5395	2N4869A	2N5950	2N5486	3N156	3N163
2N4867A	2N4867A	2N5396	2N4869A	2N5951	2N5486	3N156A	3N163
2N4868	2N4868	2N5397	2N5397	2N5952	2N5484	3N157	3N163
2N4868A	2N4868A	2N5398	2N5398	2N5953	2N5484	3N157A	3N163
2N4869	2N4869	2N5432	2N5432	2N6085	IT122	3N158	3N163
2N4869A	2N4869A	2N5433	2N5433	2N6086	IT122	3N158A	3N163
2N4878	2N4878	2N5434	2N5434	2N6087	IT121	3N160	3N161
2N4879	2N4879	2N5452	2N5452	2N6088	IT121	3N161	3N161
2N4880	2N4880	2N5453	2N5453	2N6089	IT122	3N163	3N163
2N4937	IT131	2N5454	2N5454	2N6090	IT121	3N164	3N164
2N4938	IT132	2N5457	2N5457	2N6091	IT121	3N165	3N165
2N4939	IT132	2N5458	2N5458	2N6092	IT121	3N166	3N166
2N4940	IT132	2N5459	2N5459	2N6441	IT122	3N167	3N161
2N4941	IT131	2N5460	2N5460	2N6442	IT122	3N168	3N161
2N4942	IT132	2N5461	2N5461	2N6443	IT122	3N169	3N170
2N4955	IT122	2N5462	2N5462	2N6444	IT122	3N170	3N170
2N4956	IT122	2N5463	2N5463	2N6445	IT121	3N171	3N171
2N4977	2N5433	2N5464	2N5464	2N6446	IT121	3N172	3N172
2N4978	2N5433	2N5465	2N5465	2N6447	IT121	3N173	3N173
2N4979	2N4859	2N5471	2N5265	2N6448	IT121	3N174	3N163
2N5018	2N5018	2N5472	2N5265	2N6451	U310	3N175	3N170
2N5019	2N5019	2N5473	2N5265	2N6452	U310	3N176	3N170
2N5020	2N2843	2N5474	2N5265	2N6453	U310	3N177	3N171
2N5021	2N2607	2N5475	2N5265	2N6454	U310	3N178	3N172
2N5033	2N5460	2N5476	2N5266	2N6483	2N6483	3N179	3N172

**CONSULT FACTORY

DISCRETE CROSS REFERENCE (cont.)

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
3N180	3N172	BCY89	IT122	BFX78	2N5397	CM652	2N5432
3N181	3N161	BF244	2N5486	BFX82	2N5019	CM653	2N5433
3N182	3N161	BF244A	2N5484	BFX83	2N5019	CM697	2N5433
3N183	3N161	BF244B	2N5485	BFX99	IT120A	CM800	2N5433
3N188	3N188	BF244C	2N5486	BFY20	IT122	CM856	2N5433
3N189	3N189	BF245	2N5486	BFY81	IT122	CM860	2N4868A
3N190	3N190	BF245A	2N4416	BFY82	IT122	CMX740	2N5432
3N191	3N191	BF245B	2N4416	BFY83	IT122	CP640	2N4091
3N207	3N190	BF245C	2N4416	BFY84	IT122	CP643	2N5434
3N208	3N188	BF246	2N5485	BFY85	IT122	CP650	2N5432
3SK22	2N5486	BF246A	2N5639	BFY86	IT122	CP651	2N5433
3SK23	2N5397	BF246B	2N5638	BFY91	IT122	CP652	2N5433
3SK28	2N5397	BF246C	2N5638	BFY92	IT122	CP653	2N5433
42T	2N4392	BF247	2N4091	BN209	IT122	D1101	2N3821
4360TP	2N5462	BF247A	2N4091	BSV22	2N4416	D1102	2N3821
5033TP	2N5460	BF247B	2N4091	BSV78	2N4856A	D1103	2N4338
588U	2N4416	BF247C	2N4091	BSV79	2N4857A	D1177	2N3821
58T	2N5457	BF256	2N5484	BSV8C	2N4858A	D1178	2N3821
59T	2N4416	BF256A	2N5484	BSX82	2N3822	D1179	2N4338
703U	2N4220	BF256B	2N4416	C21	2N3821	D1180	2N3822
704U	2N4220	BF256C	2N4416	C2306	2N5196	D1181	2N4338
705U	2N4224	BF320	2N5461	C38	2N4338	D1182	2N4338
707U	2N4860	BF320A	2N5460	C413N	2N5434	D1183	2N4341
714U	2N3822	BF320B	2N5461	C610	2N4392	D1184	2N4340
734EU	2N4416	BF320C	2N5462	C611	2N4221	D1185	2N4339
734U	2N5516	BF346	ITE4392	C612	2N4221	D1201	2N4224
751U	2N4340	BF347	J201	C613	2N4221	D1202	2N3821
752U	2N4340	BF348	J310	C614	2N4220	D1203	2N4420
753U	2N4341	BF800	2N4867	C615	2N4221	D1301	2N4222
754U	2N4340	BF801	2N4867	C620	2N4220	D1302	2N4220
755U	2N4341	BF802	2N4338	C621	2N4220	D1303	2N4220
756U	2N4340	BF804	2N4338	C622	2N4220	D1420	2N4868
A190	ITE4416	BF805	2N4869	C623	2N4220	D1421	2N3822
A191	ITE4416	BF806	2N4869	C624	2N4220	D1422	2N4869
A192	2N4416	BF808	2N4868	C625	2N4220	D2T2218	IT129
A193	2N5484	BF810	2N4858	C650	2N4220	D2T2218A	IT129
A194	2N5484	BF811	2N4858	C651	2N4220	D2T2219	IT129
A195	2N5484	BF815	2N4858	C652	2N4220	D2T2219A	IT129
A196	ITE4416	BF816	2N4858	C653	2N4220	D2T2904	IT139
A197	ITE4391	BF817	2N4858	C6690	2N4341	D2T2904A	IT139
A198	ITE4392	BF818	2N4858	C6691	2N4341	D2T2905	IT139
A199	ITE4393	BFQ10	U401	C6692	2N4339	D2T2905A	IT139
A5T3821	2N5484	BFQ11	U401	C673	2N4341	D2T918	IT129
A5T3822	2N5484	BFQ12	U402	C674	2N4341	DA102	2N5196
A5T3823	2N4416	BFQ13	U403	C680	2N4338	DA402	2N5196
A5T3824	2N4341	BFQ14	U404	C680A	2N4338	DN3066A	2N3821
A5T5460	2N5460	BFQ15	U405	C681	2N4338	DN3067A	2N4338
A5T5461	2N5461	BFQ16	U406	C681A	2N4338	DN3068A	2N4338
A5T5462	2N5462	BFQ23	IT5912	C682	2N4339	DN3069A	2N3822
AD3954	2N3954	BFQ26	U403	C682A	2N4339	DN3070A	2N3821
AD3954A	2N3954A	BFQ44	IT5912	C683	2N4339	DN3071A	2N4338
AD3955	2N3955	BFQ45	IT5912	C683A	2N4339	DN3365A	2N4220
AD3956	2N3956	BFQ49A	2N3055	C684	2N4220	DN3365B	2N4091
AD3958	2N3958	BFQ49B	2N3958	C684A	2N4220	DN3366A	2N3686
AD5905	2N5905	BFQ49C	2N3958	C685	2N4220	DN3366B	2N4091
AD5906	2N5906	BFS21	2N5199	C685A	2N4220	DN3367A	2N3687
AD5907	2N5907	BFS21A	2N5199	C80	2N4338	DN3367B	2N4091
AD5908	2N5908	BFS67	2N3821	C81	2N4338	DN3368A	2N4341
AD5909	2N5909	BFS67P	2N5459	C84	2N4338	DN3368B	2N4221
AD810	2N4878	BFS68	2N3823	C85	2N4338	DN3369A	2N4339
AD811	2N4878	BFS68P	2N4416	C91	2N4858	DN3369B	2N4220
AD812	2N4878	BFS70	2N3821	C92	2N4091	DN3370A	2N4338
AD813	2N4878	BFS71	2N3822	C93	2N4393	DN3370B	2N4338
AD814	IT124	BFS72	2N3823	C94	2N5457	DN3436A	2N4341
AD815	IT124	BFS73	2N3821	C94E	2N5457	DN3436B	2N4222
AD816	IT120A	BFS74	2N4856	C95	2N5457	DN3437A	2N4340
AD818	IT140	BFS75	2N4857	C95E	2N5459	DN3437B	2N4220
AD820	IT132	BFS76	2N4858	C96E	2N5484	DN3438A	2N4338
AD821	IT130A	BFS77	2N4859	C97E	2N3822	DN3438B	2N4339
AD822	IT130A	BFS78	2N4860	C98E	2N3822	DN3458A	2N4341
AD830	2N5520	BFS79	2N4861	CC4445	2N5432	DN3458B	2N4222
AD831	2N5521	BFS80	2N4416A	CC4446	2N5434	DN3459A	2N4339
AD832	2N5522	BFT10	2N5397	CC697	2N4856	DN3459B	2N4220
AD833	2N5523	BFT11	2N5019	CF2386	2N5458	DN3460A	2N4338
AD833A	2N5524	BFW10	2N3823	CF24	2N3824	DN3460B	2N4220
AD835	2N3954	BFW11	2N3822	CFM13026	2N4858	DNX1	2N4338
AD836	2N3955	BFW12	2N4416	CM600	2N4092	DNX2	2N4338
AD837	2N3955	BFW13	2N4867	CM601	2N4091	DNX3	2N4338
AD838	2N3956	BFW39	IT129	CM602	2N4091	DNX4	2N4869
AD839	2N3957	BFW39A	IT120	CM603	2N4091	DNX5	2N4868
AD840	2N5520	BFW54	2N3822	CM640	2N4093	DNX6	2N4338
AD841	2N5521	BFW55	2N3822	CM641	2N4093	DNX7	2N4416
AD842	2N5523	BFW56	2N4860	CM642	2N4093	DNX8	2N4416
BC264	2N5458	BFW61	2N4224	CM643	2N4092	DNX9	2N4339
BC264A	2N5457	BFX11	IT132	CM644	2N4092	DU4339	2N5397
BC264B	2N5458	BFX15	IT122	CM645	2N4092	DU4340	2N5398
BC264C	2N5458	BFX36	IT131	CM646	2N4092	E100	2N5458
BC264D	2N4416	BFX70	IT122	CM647	2N4091	E101	J204
BCY87	IT121	BFX71	IT122	CM650	2N5432	E102	2N5457
BCY88	IT122	BFX72	IT122	CM651	2N5433	E103	2N5459

**CONSULT FACTORY

DISCRETE CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
E105	J105	FF400	2N5457	IT127	IT127	ITE2977	IT120
E106	J106	FM1100	2N3954A	IT128	IT128	ITE2978	IT120
E107	J107	FM1100A	2N5906	IT129	IT129	ITE2979	IT120
E108	J105	FM1101A	2N5906	IT130	IT130	ITE3066	2N3685
E109	J106	FM1102	2N3954	IT130A	IT130A	ITE3067	2N3686
E110	J107	FM1102A	2N5906	IT131	IT131	ITE3068	2N3687
E111	J111	FM1103	2N3955	IT132	IT132	ITE3347	IT137
E111A	J111	FM1103A	2N5908	IT135	IT135	ITE3348	IT138
E112	J112	FM1104	2N3957	IT137	IT137	ITE3349	IT139
E112A	J112	FM1104A	2N5909	IT138	IT138	ITE3350	IT137
E113	J113	FM1105	2N3954A	IT139	IT139	ITE3351	IT138
E113A	J113	FM1105A	IT500	IT140	IT140	ITE3680	IT120
E114	J204	FM1106	2N3954A	IT1700	IT1700	ITE3800	IT132
E174	J174	FM1106A	IT500	IT1701	3N172	ITE3802	IT132
E175	J175	FM1107	2N3954	IT1702	3N163	ITE3804	IT130
E176	J176	FM1107A	IT500	IT1750	IT1750	ITE3806	IT132
E177	J177	FM1108	2N3955	IT2700	3N165	ITE3807	IT132
E201	J201	FM1108A	IT502	IT2701	3N165	ITE3808	IT132
E202	J202	FM1109	2N3957	IT400	2N4392	ITE3809	IT132
E203	J203	FM1109A	IT503	IT500	IT500	ITE3810	IT130
E204	J204	FM1110	2N3955	IT500P	IT500	ITE3811	IT130
E210	2N5397	FM1110A	2N5908	IT501	IT501	ITE3907	IT120
E211	2N5397	FM1111	2N3957	IT501P	IT501	ITE3908	IT120
E212	2N5397	FM1111A	2N5909	IT502	IT502	ITE4017	IT139
E230	2N4867	FM1112	2N5196	IT502P	IT502	ITE4018	IT139
E231	2N4868	FM1200	2N3954	IT503	IT503	ITE4019	IT139
E232	2N4869	FM1201	2N3954	IT503P	IT503	ITE4020	IT139
E270	J270	FM1202	2N3954	IT504	IT504	ITE4021	IT139
E271	J271	FM1203	2N3955A	IT505	IT505	ITE4022	IT139
E300	2N5397	FM1204	2N3955	IT550	IT550	ITE4023	IT137
E304	2N5486	FM1205	2N3954	IT5911	IT5911	ITE4024	IT137
E305	2N5484	FM1206	2N3954	IT5912	IT5912	ITE4025	IT137
E308	J308	FM1207	2N3954	ITC2972	IT122	ITE4091	ITE4091
E309	J309	FM1208	2N3955A	ITC2973	IT122	ITE4092	ITE4092
E310	J310	FM1209	2N3955	ITC2974	IT120	ITE4093	ITE4093
E311	J310	FM1210	2N3955A	ITC2975	IT120	ITE4117	2N4117
E312	2N5397	FM1211	IT5911	ITC2976	IT120	ITE4118	2N4118
E400	2N3955	FM3954	2N3954	ITC2977	IT120	ITE4119	2N4119
E401	2N3955	FM3954A	2N3954A	ITC2978	IT120	ITE4338	2N4338
E402	2N3957	FM3955	2N3955	ITC2979	IT120	ITE4339	2N4339
E410	2N3955	FM3955A	2N3955A	ITC3347	IT137	ITE4340	2N4340
E411	IT5911	FM3956	2N3956	ITC3348	IT138	ITE4341	2N4341
E412	IT5911	FM3957	2N3957	ITC3349	IT139	ITE4391	ITE4391
E413	2N5454	FM3958	IT5911	ITC3350	IT137	ITE4392	ITE4392
E414	2N3956	FP4339	2N4339	ITC3351	IT138	ITE4393	ITE4393
E415	2N3957	FP4340	2N4340	ITC3352	IT139	ITE4416	ITE4416
E420	IT5911	FT0654A	2N5486	ITC3800	IT132	ITE4867	2N4867
E421	IT5912	FT0654B	2N5486	ITC3802	IT132	ITE4868	2N4868
E430	J309(X2)	FT0654C	2N4221	ITC3804	IT130	ITE4869	2N4869
E431	J310(X2)	FT0654D	2N4221	ITC3806	IT132	J100	2N5458
ESM25	U401	FT3820	2N5019	ITC3807	IT132	J101	2N4338
ESM25A	U401	FT3820	2N5460	ITC3808	IT132	J102	2N5457
ESM4091	2N4091	FT3909	2N5019	ITC3809	IT132	J103	2N5459
ESM4092	2N4092	FT703	3N161	ITC3810	IT130	J105	J105
ESM4093	2N4093	FT704	3N163	ITC3811	IT130	J105-18	J105
ESM4302	2N5457	GET5457	2N5457	ITC4017	IT139	J106	J106
ESM4303	2N5459	GET5458	2N5458	ITC4018	IT139	J106-18	J106
ESM4304	2N5458	GET5459	2N5459	ITC4019	IT139	J107	J107
ESM4445	2N5432	HA7807	IT132	ITC4020	IT139	J107-18	J107
ESM4446	2N5434	HA7809	IT132	ITC4021	IT139	J108	J105
ESM4447	2N5432	HDIG1030	3N163	ITC4022	IT139	J108-18	J105
ESM4448	2N5434	HEP801	2N3822	ITC4023	IT137	J109	J106
FE0654A	2N4386	HEP802	2N5484	ITC4024	IT137	J109-18	J106
FE0654B	2N5485	HEP803	2N5019	ITC4025	IT137	J110	J107
FE100	2N3821	HEPF0021	2N5484	ITE2453	IT120	J110-18	J107
FE100A	2N3821	HEPF1035	J176	ITE2639	IT120	J111	J111
FE102	2N4119	HEPF2004	2N5484	ITE2640	IT122	J111-18	J111
FE102A	2N4119	HEPF2005	2N5459	ITE2641	IT122	J111A	J111
FE104	2N4118	ID100	ID100	ITE2642	IT120	J111A-18	J111
FE104A	2N4118	ID101	ID101	ITE2643	IT122	J112	J112
FE1600	2N4092	IMF3954	2N3954	ITE2644	IT122	J112-18	J112
FE200	2N3821	IMF3954A	2N3954A	ITE2720	IT120	J113A	J112
FE202	2N3821	IMF3955	2N3955	ITE2721	IT122	J113A-18	J112
FE204	2N3821	IMF3955A	2N3955A	ITE2722	IT120	J113	J113
FE300	2N3822	IMF3956	2N3956	ITE2903	IT122	J113-18	J113
FE302	2N3821	IMF3957	2N3957	ITE2913	IT122	J113A	J113
FE304	2N3821	IMF3958	2N3958	ITE2914	IT122	J113A-18	J113
FE3819	2N5484	IMF5911	IMF5911	ITE2915	IT120	J114	2N5555
FE4302	2N5457	IMF5912	IMF5912	ITE2916	IT120	J1401	IT501
FE4303	2N5459	IMF6485	IMF6485	ITE2917	IT122	J1402	IT502
FE4304	2N5458	IT100	IT100	ITE2918	IT122	J1403	IT503
FE5245	2N4416	IT101	IT101	ITE2919	IT120	J1404	IT503
FE5246	2N5484	IT108	ITE4416	ITE2920	IT120	J1405	IT504
FE5247	2N5486	IT109	ITE4416	ITE2936	IT120	J1406	IT505
FE5457	2N5457	IT120	IT120	ITE2937	IT120	J174	J174
FE5458	2N5458	IT120A	IT120A	ITE2972	IT122	J174-18	J174
FE5459	2N5459	IT121	IT121	ITE2973	IT122	J175	J175
FE5484	2N5484	IT122	IT122	ITE2974	IT120	J175-18	J175
FE5485	2N5485	IT124	IT124	ITE2975	IT120	J176	J176
FE5486	2N5486	IT126	IT126	ITE2976	IT120	J176-18	J176

**CONSULT FACTORY

DISCRETE CROSS REFERENCE (cont.)

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
J177	J177	K309-18	J309	LS5105	2N5486	MD7002B	IT122
J177-18	J177	K310-18	J310	LS5245	ITE4416	MD7003	IT132
J201	J201	KE3684	2N3684	LS5246	2N5484	MD7003A	IT132
J201-18	J201	KE3685	2N3685	LS5247	2N5486	MD7003B	IT132
J202	J202	KE3686	2N3686	LS5248	2N5486	MD7004	IT129
J202-18	J202	KE3687	2N3687	LS5358	J204	MD7007	IT129
J203	J203	KE3823	2N3823	LS5359	J204	MD7007A	IT129
J203-18	J203	KE3970	ITE4391	LS5360	J202	MD7007B	IT129
J204	J204	KE3971	ITE4392	LS5361	J202	MD708	IT129
J204-18	J204	KE3972	ITE4393	LS5362	J203	MD708A	IT129
J210	2N5397	KE4091	ITE4091	LS5363	J203	MD708B	IT129
J211	2N5397	KE4092	ITE4092	LS5364	J203	MD8001	IT120
J212	2N5397	KE4093	ITE4093	LS5391	2N4867A	MD8002	IT120
J230	2N4867	KE4220	2N5457	LS5392	2N4868A	MD8003	IT122
J231	2N4868	KE4221	2N5459	LS5393	2N4869A	MD918	IT122
J232	2N4869	KE4222	2N5459	LS5394	2N4869A	MD918A	IT122
J270	J270	KE4223	J204	LS5395	2N4869A	MD918B	IT122
J270-18	J270	KE4391	ITE4391	LS5396	2N4869A	MD982	IT139
J271	J271	KE4392	ITE4392	LS5457	2N5457	MD984	IT139
J271-18	J271	KE4393	ITE4393	LS5458	2N5458	MEF103	2N5457
J300	2N5397	KE4416	ITE4416	LS5459	2N5459	MEF104	2N5459
J304	2N5486	KE4856	ITE4391	LS5484	2N5484	MEF3069	2N4341
J305	2N5484	KE4857	ITE4392	LS5485	2N5485	MEF3070	2N4339
J308	J308	KE4858	ITE4393	LS5486	2N5486	MEF3458	2N4341
J309	J309	KE4859	ITE4391	LS5556	2N3685	MEF3459	2N4339
J310	J310	KE4860	ITE4392	LS5557	2N3684	MEF3460	2N4338
J315	2N5397	KE4861	ITE4393	LS5558	2N3684	MEF3684	2N3684
J316	U309	KE510	ITE4393	LS5638	2N5638	MEF3685	2N3685
J317	U310	KE5103	J204	LS5639	2N5639	MEF3686	2N3686
J3970	ITE4391	KE5104	ITE4416	LS5640	2N5640	MEF3687	2N3687
J3971	ITE4392	KE5105	ITE4416	M103	3N161	MEF3821	2N3821
J3972	ITE4393	KE511	ITE4392	M104	3N161	MEF3822	2N3822
J401	IT501	KH5196	2N5196	M106	3N166	MEF3823	2N3823
J402	IT502	KH5197	2N5197	M107	3N189	MEF3954	2N3954
J403	IT503	KH5198	2N5198	M108	3N191	MEF3955	2N3955
J404	IT503	KH5199	2N5199	M113	3N161	MEF3956	2N3956
J405	IT504	LDF603	2N4221	M114	3N161	MEF3957	2N3957
J406	IT505	LDF604	2N4221	M116	M116	MEF3958	2N3958
J4091	ITE4091	LDF605	2N4221	M117	2N4351	MEF4223	2N4223
J4092	ITE4092	LM114	IT120	M119	3N161	MEF4224	2N4224
J4093	ITE4093	LM114A	IT120A	M163	3N163	MEF4391	ITE4391
J410	IT502	LM114AH	IT120A	M164	3N164	MEF4392	ITE4392
J411	IT503	LM114H	IT120	M511	3N172	MEF4393	ITE4393
J412	IT503	LM115	IT120	M511A	3N172	MEF4416	ITE4416
J420	IT5911	LM115A	IT120A	M517	3N163	MEF4856	2N4856
J421	IT5912	LM115AH	IT120A	MA7807	IT132	MEF4857	2N4857
J4220	J204	LM115H	IT120	MA7809	IT132	MEF4858	2N4858
J4221	J202	LM194	IT120A	MAT-01AH	IT140	MEF4859	2N4859
J4222	J203	LM394	IT120A	MAT-01FH	IT140	MEF4860	2N4860
J4223	J202	LS3069	2N5458	MAT-01GH	IT140	MEF4861	2N4861
J4224	J202	LS3070	2N5458	MAT-01H	IT140	MEF5103	ITE4416
J430	J309(X2)	LS3071	2N5458	MD1120	IT122	MEF5104	ITE4416
J4302	2N4302	LS3458	J204	MD1121	IT122	MEF5105	ITE4416
J4303	2N5459	LS3459	J204	MD1122	IT122	MEF5245	ITE4416
J4304	2N5458	LS3460	J204	MD1123	IT139	MEF5246	2N5484
J431	J310(X2)	LS3684	2N3684	MD1129	IT129	MEF5247	2N5486
J433	2N5457	LS3685	2N3685	MD1130	IT139	MEF5248	2N5486
J4338	2N5457	LS3686	2N3686	MD2218	IT129	MEF5284	2N5484
J4339	2N5457	LS3687	2N3687	MD2218A	IT129	MEF5285	2N5485
J4391	ITE4391	LS3819	2N5484	MD2219	IT129	MEF5286	2N5486
J4392	ITE4392	LS3821	2N5457	MD2219A	IT129	MEF5561	U401
J4393	ITE4393	LS3822	2N5458	MD2369	IT129	MEF5562	U402
J4416	ITE4416	LS3823	2N5458	MD2369A	IT129	MEF5563	U403
J4856	ITE4856	LS3921	2N3921	MD2369B	IT122	MEM511	3N172
J4857	ITE4857	LS3922	2N3922	MD2904	IT139	MEM511A	3N172
J4858	ITE4858	LS3966	ITE4416	MD2904A	IT139	MEM511C	3N172
J4859	ITE4859	LS3967	ITE4416	MD2905	IT139	MEM517	3N172
J4860	ITE4860	LS3968	ITE4416	MD2905A	IT139	MEM517A	3N172
J4861	ITE4861	LS3969	ITE4416	MD2974	IT120	MEM517B	3N172
J4867	2N4867	LS4220	J204	MD2975	IT120	MEM517C	3N172
J4867A	2N4867A	LS4221	J202	MD2978	IT120	MEM550	3N189
J4867RR	2N4867	LS4222	J203	MD2979	IT120	MEM550C	3N189
J4868	2N4868	LS4223	J202	MD3008	IT120	MEM550F	3N189
J4868A	2N4868A	LS4224	J202	MD3250	IT132	MEM551	3N190
J4868RR	2N4868	LS4338	2N5457	MD3250A	IT131	MEM551C	3N189
J4869	2N4869	LS4339	2N5457	MD3251	IT132	MEM556	3N172
J4869A	2N4869A	LS4340	2N5457	MD3251A	IT131	MEM556C	3N172
J4869RR	2N4869	LS4341	2N5458	MD3409	IT129	MEM560	3N161
J5103	2N5484	LS4391	ITE4391	MD3410	IT129	MEM560C	3N161
J5104	2N5485	LS4392	ITE4392	MD3467	IT139	MEM561	3N163
J5105	2N5486	LS4393	ITE4393	MD3725	IT129	MEM561C	3N163
J6163	2N5486	LS4416	ITE4416	MD3762	IT139	MEM562	2N4351
K114-18	2N5555	LS4856	ITE4091	MD4957	IT132	MEM562C	2N4351
K210-18	2N5397	LS4857	ITE4092	MD5000	IT132	MEM563	2N4351
K211-18	2N5397	LS4858	ITE4093	MD5000A	IT132	MEM563C	2N4351
K212-18	2N5397	LS4859	ITE4091	MD5000B	IT132	MEM711	M116
K300-18	2N5397	LS4860	ITE4092	MD7000	IT129	MEM712	M116
K304-18	2N5486	LS4861	ITE4093	MD7001	IT139	MEM712A	M116
K305-18	2N5484	LS5103	2N5484	MD7002	IT122	MEM713	3N170
K308-18	J308	LS5104	2N5485	MD7002A	IT122	MEM806	3N163

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
MEM806A	3N163	MP840	2N5520	NKT80111	2N4220	SA2718	IT122
MEM807	3N172	MP841	2N5521	NKT80112	2N4220	SA2719	IT120
MEM807A	3N172	MP842	2N5523	NKT80113	2N3821	SA2720	IT121
MEM814	3N161	MPF102	2N5486	NKT80211	2N4339	SA2721	IT122
MEM816	3N172	MPF103	2N5457	NKT80212	2N4339	SA2722	IT120
MEM817	3N172	MPF104	2N5458	NKT80213	2N4339	SA2723	IT121
MEM823	MFE823	MPF105	2N5459	NKT80214	2N4339	SA2724	IT122
MEM954	3N188	MPF106	2N5485	NKT80215	2N4339	SA2726	IT122
MEM954A	3N188	MPF107	2N5486	NKT80216	2N4339	SA2727	IT122
MEM9548	3N188	MPF108	2N5486	NKT80421	2N4220	SA2738	IT120A
MEM955	3N190	MPF109	2N5484	NKT80422	2N4220	SA2739	IT120
MEM955A	3N190	MPF111	2N5458	NKT80423	2N4220	SDF1001	2N5432
MEM955B	3N190	MPF112	2N5458	NKT80424	2N4220	SDF1002	2N5433
MF510	2N4092	MPF161	2N5398	NPC108	2N5484	SDF1003	2N5434
MF803	2N4338	MPF208	2N3821	NPC211N	2N4338	SDF500	2N5520
MF818	2N4858	MPF209	2N3821	NPC212N	2N4338	SDF501	2N5520
MFE2000	2N4416	MPF256	ITE4416	NPC213N	2N4338	SDF502	2N5520
MFE2001	2N4416	MPF4391	ITE4391	NPC214N	2N4339	SDF503	2N5520
MFE2004	2N4093	MPF4392	ITE4392	NPC215N	2N4339	SDF504	2N5520
MFE2005	2N4092	MPF4393	ITE4393	NPC216N	2N4339	SDF505	2N5520
MFE2006	2N4091	MPF820	J310	NPD5564	IT550	SDF506	2N5520
MFE2007	2N4860	MPF970	J175	NPD5565	IT550	SDF507	2N5520
MFE2008	2N4859	MPF971	J175	NPD5566	IT550	SDF508	2N5520
MFE2009	2N4859	MTF101	2N5484	NPD8301	2N3954	SDF509	2N5520
MFE2010	2N4859	MTF102	2N5484	NPD8302	2N3955	SDF510	2N3954
MFE2011	2N5433	MTF103	2N5457	NPD8303	2N3956	SDF512	2N3954
MFE2012	2N5433	MTF104	2N5459	OT3	2N4338	SDF513	2N3954
MFE2012	2N5434	ND5700	IT120A	P1004	2N5116	SDF514	2N3954
MFE2093	2N4338	ND5701	IT120A	P1005	2N5115	SDF661	IT122
MFE2094	2N4339	ND5702	IT120	P1027	2N5267	SDF662	IT122
MFE2095	2N4340	NDF9401	IT500	P1028	2N5270	SDF663	IT122
MFE2133	2N4860	NDF9402	IT501	P1029	2N5270	SE33819	2N5484
MFE2912	2N5433	NDF9403	IT502	P1069E	2N2609	SFT601	2N4338
MFE3002	3N170	NDF9404	IT503	P1086E	2N5115	SFT602	2N4338
MFE3003	3N164	NDF9405	IT504	P1087E	2N5516	SFT603	2N4339
MFE3020	3N166	NDF9406	IT500	P1117E	2N5640	SFT604	2N4339
MFE3021	3N166	NDF9407	IT501	P1118E	2N5641	SL301AT	IT129
MFE4007	2N3686	NDF9408	IT502	P1119E	2N5640	SL301BT	IT129
MFE4008	2N3686	NDF9409	IT503	PF510	2N5115	SL301CT	IT129
MFE4009	2N3685	NDF9410	IT504	PF5101	2N4867	SL301ET	IT129
MFE4010	2N2608	NF3819	2N5484	PF5102	2N4867	SL360C	IT129
MFE4011	2N2608	NF4302	2N5457	PF5103	2N4867	SL362C	IT129
MFE4012	2N2609	NF4303	2N5459	PF511	2N5114	SU2000	2N4340
MFE823	IT1700	NF4304	2N5458	PF5301	2N4118A	SU2020	2N3954
MK10	2N4416	NF4445	2N5432	PF5301-1	2N4117A	SU2021	2N3954
MMF1	2N5197	NF4446	2N5433	PF5301-2	2N4118A	SU2022	2N3954
MMF2	2N3921	NF4447	2N5433	PF5301-3	2N4118A	SU2023	2N3954
MMF3	2N5198	NF4448	2N5433	PL1091	2N3823	SU2024	2N3954
MMF4	2N3922	NF500	2N4224	PL1092	2N3823	SU2025	2N3954
MMF5	2N5199	NF501	2N4224	PL1093	2N3823	SU2026	2N3954
MMF6	2N3955A	NF506	2N4416	PL1094	2N3823	SU2027	2N3954
MMT3823	2N3823	NF5101	2N4867	PN3684	2N3684	SU2028	2N3954
MP301	IT124	NF5102	2N4867	PN3685	2N3685	SU2029	2N3954
MP302	IT124	NF5103	2N4867	PN3686	2N3686	SU2029	2N5197
MP303	IT124	NF511	2N4860	PN3687	2N3687	SU2030	2N3954
MP310	2N4045	NF5163	2N4341	PN4091	ITE4091	SU2030	2N3955
MP311	2N4045	NF520	2N3684	PN4092	ITE4092	SU2031	2N3954
MP312	2N4044	NF521	2N3685	PN4093	ITE4093	SU2031	2N5198
MP313	IT124	NF522	2N3686	PN4220	J204	SU2032	2N3954
MP318	IT120A	NF523	2N3865	PN4221	J202	SU2033	2N3954
MP350	IT132	NF530	2N4341	PN4222	J203	SU2034	2N3954
MP351	IT130	NF5301	2N4118A	PN4223	J204	SU2034	2N3955
MP352	IT130	NF5301-1	2N4117A	PN4224	J202	SU2035	2N3954
MP358	IT130A	NF5301-2	2N4118A	PN4342	2N5461	SU2035	2N3955
MP360	IT132	NF5301-3	2N4118A	PN4360	2N5460	SU2074	2N3954
MP361	IT130A	NF531	2N4339	PN4391	ITE4391	SU2075	2N3954
MP362	IT130A	NF532	2N4341	PN4392	ITE4392	SU2076	2N3954
MP3954	2N3954	NF533	2N4339	PN4416	ITE4416	SU2077	2N3954
MP3954A	2N3954A	NF5457	2N5457	PN4856	2N4856	SU2077	2N3955
MP3955	2N3955	NF5458	2N5458	PN4857	2N4857	SU2078	2N3955
MP3956	2N3956	NF5459	2N5459	PN4858	2N4858	SU2079	2N3955
MP3957	2N3957	NF5484	2N5484	PN4859	2N4859	SU2080	U404
MP3958	2N3958	NF5485	2N5485	PN4860	2N4860	SU2081	U404
MP5905	2N5905	NF5486	2N5486	PN4861	2N4861	SU2098	2N5197
MP5906	2N5906	NF5555	2N5484	PN5033	2N5460	SU2098A	2N5197
MP5907	2N5907	NF5638	2N5638	PTC151	2N5484	SU2098B	2N5196
MP5908	2N5908	NF5639	2N5639	PTC152	2N5485	SU2099	2N5197
MP5909	2N5909	NF5640	2N5640	SA2253	IT122	SU2099A	2N5197
MP5911	2N5911	NF5653	2N4860	SA2254	IT122	SU2365	2N3954
MP5912	2N5912	NF5654	2N4861	SA2255	IT122	SU2365A	2N3954
MP804	2N5520	NF580	2N5432	SA2644	IT120	SU2366	2N3955
MP830	2N5520	NF581	2N5432	SA2648	IT120	SU2366A	2N3955
MP831	2N5521	NF582	2N5433	SA2710	IT120	SU2367	2N3955
MP832	2N5522	NF583	2N5434	SA2711	IT120	SU2367A	2N3955
MP833	2N5523	NF584	2N5433	SA2712	IT121	SU2368	2N3956
MP835	2N3954	NF585	2N4859	SA2713	IT121	SU2368A	2N3956
MP836	2N3955	NF6451	U310	SA2714	IT122	SU2369	2N3957
MP837	2N3955	NF6452	U310	SA2715	IT120	SU2369A	2N3957
MP838	2N3956	NF6453	U310	SA2716	IT120	SU2410	2N5907
MP839	2N3957	NF6454	U310	SA2717	IT121	SU2411	2N5908

CONSULT FACTORY

DISCRETE CROSS REFERENCE (cont.)

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
SU2412	2N5909	TD5909A	2N5909	U183	2N3824	U405	U405
SU2652	U401	TD5911	IT5911	U1837E	2N5486	U406	U406
SU2652M	U401	TD5911A	IT5911	U184	2N5397	U410	2N3955
SU2653	U401	TD5912	IT5912	U1897E	U1897	U411	2N3956
SU2653M	U401	TD5912A	IT5912	U1898E	U1898	U412	2N3958
SU2654	U401	TD700	IT122	U1899E	U1899	U421	2N5908
SU2654M	U401	TD701	IT122	U197	2N4338	U422	2N5908
SU2655	U402	TD709	IT122	U198	2N4340	U423	2N5909
SU2655M	U402	TD710	IT122	U199	2N4341	U424	2N5908
SU2656	U404	TD711	IT122	U1994E	2N4416	U425	2N5908
SU2656M	U404	TD713	IT122	U200	2N4861	U426	2N5909
SX3819	2N5484	TIS14	2N4340	U201	2N4860	U430	J309(X2)
SX3820	2N2608	TIS25	2N3954	U202	2N4859	U431	J310(X2)
TD100	IT129	TIS26	2N3954	U2047E	2N4416	U440	IT5911
TD101	IT129	TIS27	2N3955	U221	2N4391	U441	IT5912
TD102	IT129	TIS34	2N5486	U222	2N4391	UC100	2N3684
TD200	IT129	TIS41	2N4859	U231	U231	UC110	2N3685
TD201	IT129	TIS42	2N4393	U232	U232	UC115	2N4340
TD202	IT129	TIS58	2N5484	U233	U233	UC120	2N3686
TD2219	IT129	TIS59	2N5486	U234	U234	UC130	2N3687
TD224	IT122	TIS68	2N3955A	U235	U235	UC155	2N4416
TD225	IT122	TIS69	2N3955A	U240	2N5432	UC1700	3N163
TD226	IT122	TIS70	2N3956	U241	2N5433	UC1764	3N163
TD227	IT122	TIS73	ITE4391	U242	2N5432	UC20	2N3686
TD228	IT122	TIS74	ITE4392	U243	2N5433	UC200	2N3824
TD229	IT122	TIS75	ITE4393	U244	2N5433	UC201	2N3824
TD230	IT121	TIS88	2N4416	U248	2N5902	UC21	2N3687
TD231	IT121	TIS88A	2N4416	U248A	2N5906	UC210	2N4416
TD232	IT122	TIXS33	2N4392	U249	2N5903	UC2130	2N5452
TD233	IT122	TIXS35	2N4857	U249A	2N5907	UC2132	2N5453
TD234	IT122	TIXS36	2N4391	U250	2N5904	UC2134	2N5454
TD235	IT122	TIXS41	2N4859	U250A	2N5908	UC2136	2N5454
TD236	IT122	TIXS42	2N5639	U251	2N5905	UC2138	2N5454
TD237	IT122	TIXS59	2N5459	U251A	2N5909	UC2139	2N3958
TD238	IT122	TIXS78	2N4341	U252	IT5911	UC2147	2N3958
TD239	IT122	TIXS79	2N4341	U253	IT5912	UC2148	2N3958
TD240	IT121	TN4117	2N4117	U254	2N4859	UC2149	2N3958
TD241	IT121	TN4117A	2N4117A	U255	2N4860	UC220	2N3822
TD242	IT120A	TN4118	2N4118	U256	2N4861	UC240	2N4869
TD243	IT120A	TN4118A	2N4118A	U257	U257	UC241	2N4869
TD244	IT129	TN4119	2N4119	U257/TO-71	U257/TO-71	UC250	2N4091
TD245	IT129	TN4119A	2N4119A	U266	2N4856	UC251	2N4392
TD246	IT129	TN4338	2N4338	U273	2N4118A	UC2766	3N166
TD247	IT129	TN4339	2N4339	U273A	2N4118A	UC300	2N2608
TD248	IT129	TN4340	2N4340	U274	2N4119A	UC310	2N2607
TD250	IT120A	TN4341	2N4341	U274A	2N4119A	UC320	2N2607
TD2905	IT139	TN5277	2N4341	U275	2N4119A	UC330	2N2607
TD400	IT139	TN5278	2N4341	U275A	2N4119A	UC340	2N2607
TD401	IT139	TP5114	2N5114	U280	2N5452	UC40	2N2608
TD402	IT139	TP5115	2N5115	U281	2N5453	UC400	2N5270
TD500	IT139	TP5116	2N5116	U282	2N5453	UC401	2N5116
TD501	IT139	U110	2N2608	U283	2N5453	UC41	2N2608
TD502	IT139	U111	2N2608	U284	2N5454	UC410	2N5268
TD509	IT132	U112	2N2608	U285	2N5454	UC420	2N5267
TD510	IT132	U113	2N2608	U290	2N5432	UC450	2N5114
TD511	IT132	U114	2N2608	U291	2N5434	UC451	2N5116
TD512	IT132	U1177	2N4220	U295	2N5432	UC588	2N4416
TD513	IT132	U1178	2N3821	U296	2N5434	UC703	2N4220
TD514	IT132	U1179	2N3821	U300	2N5114	UC704	2N4220
TD517	IT132	U1180	2N4221	U3000	2N4341	UC705	2N4224
TD518	IT132	U1181	2N4220	U3001	2N4339	UC707	2N4860
TD519	IT132	U1182	2N3821	U3002	2N4338	UC714	2N3822
TD520	IT139	U1277	2N3684	U301	2N5115	UC714E	2N4341
TD521	IT139	U1278	2N3685	U3010	2N4341	UC734	2N4416
TD522	IT139	U1279	2N3686	U3011	2N4340	UC734E	2N4416
TD523	IT139	U1280	2N3684	U3012	2N4338	UC751	2N4340
TD524	IT139	U1281	2N3822	U304	U304	UC752	2N4340
TD525	IT132	U1282	2N4341	U305	U305	UC753	2N4341
TD526	IT132	U1283	2N4340	U306	U306	UC754	2N4340
TD527	IT131	U1284	2N4341	U308	U308	UC755	2N4341
TD528	IT131	U1285	2N4220	U309	U309	UC756	2N4340
TD5432	2N5432	U1286	2N4341	U310	U310	UC805	2N5270
TD5433	2N5433	U1287	2N4092	U311	U310	UC807	2N5115
TD5434	2N5434	U1321	2N4860	U312	2N5397	UC814	2N5270
TD550	IT129	U1322	2N3822	U314	2N5555	UC851	2N2608
TD5902	2N5902	U1323	2N3822	U315	2N5397	UC853	2N2608
TD5902A	2N5902	U1324	2N3687	U316	U309	UC854	2N2608
TD5903	2N5903	U1325	2N3686	U317	U310	UC855	2N2609
TD5903A	2N5903	U133	2N2608	U320	2N5433	UT100	2N5397
TD5904	2N5904	U1420	2N3821	U321	2N5434	UT101	2N5397
TD5904A	2N5904	U1421	2N3822	U322	2N5433	UXC2910	IT126
TD5905	2N5905	U1422	2N3822	U328	**	VCR10N	2N4869
TD5905A	2N5905	U146	2N2608	U329	**	VCR11N	VNR11N
TD5906	2N5906	U147	2N2608	U330	**	VCR12N	2N3958
TD5906A	2N5906	U148	2N2608	U331	**	VCR13N	2N3958
TD5907	2N5907	U149	2N2609	U350	**	VCR20N	2N4341
TD5907A	2N5907	U168	2N2609	U401	U401	VCR2N	VCR2N
TD5908	2N5908	U1714	2N4340	U402	U402	VCR3P	VCR2P
TD5908A	2N5908	U1715	2N4340	U403	U403	VCR4N	VCR4N
TD5909	2N5909	U182	2N4857	U404	U404	VCR5P	VCR5P

**CONSULT FACTORY

DISCRETE CROSS REFERENCE (cont.)

A

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
VCR6P	VCR6P						
VCR7N	VCR7N						
VF28	2N4392						
VF811	2N4858						
VF815	2N4858						
VFW40	IT122						
VFW40A	IT120						
W245A	ITE4416						
W245B	ITE4416						
W245C	ITE4416						
W300	2N5398						
W300A	2N5397						
W300B	2N5397						
W300C	2N5397						
W300D	2N5398						
WK5457	2N5457						
WK5458	2N5458						
WK5459	2N5459						
ZDT40	IT129						
ZDT41	IT129						
ZDT42	IT129						
ZDT44	IT129						
ZDT45	IT129						

**CONSULT FACTORY

ANALOG SWITCH CROSS REFERENCE

A

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
AD7506/COM/CHIPS	IH6116C/D	AH5010CN	IH5010CPD	DG180AP	DG180AK	DG200AK	DG200AK
AD7506/MIL/CHIPS	IH6116M/D	AH5012CN	IH5012CPE	DG180BA	DG180BA	DG200AL	DG200AL
AD7506JD	IH6116CJI	AH5013CN	IH5013CPD	DG180BP	DG180BK	DG200AP	DG200AK
AD7506JD/883B	IH6116CJI/883B	AH5014CN	IH5014CPD	DG181AA	DG181AA	DG200BA	DG200BA
AD7506JN	IH6116CPI	AH5015CN	IH5015CPE	DG181AA	DGM181AA	DG200BK	DG200BK
AD7506KD	IH6116CJI	AH5016CN	IH5016CPE	DG181AL	DG181AL	DG200BP	DG200BK
AD7506KD/883B	IH6116CJI/883B	AM5011CN	IH5011CPE	DG181AL	DGM181AL	DG200CJ	DG200CJ
AD7506KN	IH6116CPI	D123AL	D123AL	DG181AP	DG181AK	DG201AK	DG201AK
AD7506SD	IH6116MJI	D123AP	D123AK	DG181AP	DGM181AK	DG201AP	DG201AK
AD7506SD/883B	IH6116MJI/883B	D123BP	D123BJ	DG181BA	DG181BA	DG201BK	DG201BK
AD7506TD	IH6116MJI	D123BP	D123BK	DG181BA	DGM181BA	DG201CJ	DG201CJ
AD7506TD/883B	IH6116MJI/883B	D125AL	D125AL	DG181BP	DG181BK	DG210BP	DG201BK
AD7507/COM/CHIPS	IH6216C/D	D125AP	D125AP	DG181BP	DGM181BK	DG281AA	IH182MTW
AD7507/MIL/CHIPS	IH6216M/D	D125BP	D125BK	DG181BP	DGM181CJ	DG281AP	IH182MJD
AD7507JD	IH6216CJI	D129AL	D129AL	DG182AA	DG182AA	DG281BA	IH182CTW
AD7507JD/883B	IH6216CJI/883B	D129AP	D129AK	DG182AA	DGM182AA	DG281BP	IH182CJD
AD7507JN	IH6216CPI	D129BP	D129BK	DG182AL	DG182AL	DG284AP	IH185MJE
AD7507KD	IH6216CJI	DG123AL	DG123AL	DG182AL	DGM182AL	DG284BP	IH185CJE
AD7507KD/883B	IH6216CJI/883B	DG123AP	DG123AK	DG182AP	DG182AK	DG287AA	IH188MTW
AD7507KN	IH6216CPI	DG123BP	DG123BK	DG182AP	DGM182AK	DG287AP	IH188MJD
AD7507SD	IH6216M/D	DG125AL	DG125AL	DG182BA	DG182BA	DG287BA	IH188CTW
AD7507SD/883B	IH6216MJI/883B	DG125AP	DG125AK	DG182BA	DGM182BA	DG287BP	IH188CJD
AD7507TD	IH6216MJI	DG125BP	DG125BK	DG182BP	DG182BK	DG290AP	IH191MJE
AD7507TD/883B	IH6216MJI/883B	DG126AK	DG126AK	DG182BP	DGM182BK	DG290BP	IH191CJE
AH0126CD	DG126BK	DG126AL	DG126AL	DG182BP	DGM182CJ	DG381AA	DGM182AA
AH0126D	DG126AK	DG126BP	DG126BK	DG183AL	DG183AL	DG381AK	DGM182AK
AH0126D/883	DG126AK/883B	DG129AL	DG129AL	DG183AP	DG183AK	DG381AP	DGM182AK
AH0129CD	DG129BK	DG129AP	DG129AK	DG183BP	DG183BK	DG381BA	DGM181BA
AH0129D	DG129AK	DG129BP	DG129BK	DG184AL	DG184AL	DG381BK	DGM181BK
AH0129D/883	DG129AK/883B	DG133AL	DG133AL	DG184AL	DGM184AL	DG381BP	DGM181BK
AH0133CD	DG133BK	DG133AP	DG133AK	DG184AP	DG184AK	DG381CJ	DGM181CJ
AH0133D	DG133AK	DG133BP	DG133BK	DG184AP	DGM184AK	DG384AK	DGM185AK
AH0133D/883	DG133AK/883B	DG134AL	DG134AL	DG184BP	DG184BK	DG384AP	DGM185AK
AH0134CD	DG134BK	DG134AP	DG134AK	DG184BP	DGM184BK	DG384BK	DGM184BK
AH0134D	DG134AK	DG134BP	DG134BK	DG184BP	DGM184CJ	DG384BP	DGM184BK
AH0134D/883	DG134AK/883B	DG139AL	DG139AL	DG185AL	DG185AL	DG384CJ	DGM184CJ
AH0139CD	DG139BK	DG139AP	DG139AK	DG185AL	DGM185AL	DG387AA	DGM188AA
AH0139D	DG139AK	DG139BP	DG139BK	DG185AP	DG185AK	DG387AK	DGM188AK
AH0139D/883	DG139AK/883B	DG140AL	DG140AL	DG185AP	DGM185AK	DG387AP	DGM188AK
AH0140CD	DG140BK	DG140AP	DG140AK	DG185BP	DG185BK	DG387BA	DGM187BA
AH0140D	DG140AK	DG140BP	DG140BK	DG185BP	DGM185BK	DG387BK	DGM187BK
AH0140D/883	DG140AK/883B	DG141AL	DG141AL	DG185BP	DGM185CJ	DG387BP	DGM187BK
AH0141CD	DG141BK	DG141AP	DG141AK	DG186AA	DG186AA	DG390AK	DGM191AK
AH0141D	DG141AK	DG141BP	DG141BK	DG186AL	DG186AL	DG390AP	DGM191AK
AH0141D/883	DG141AK/883B	DG142AL	DG142AL	DG186AP	DG186AK	DG390BK	DGM190BK
AH0142CD	DG142BK	DG142AP	DG142AK	DG186BA	DG186BA	DG390BP	DGM190BK
AH0142D	DG142AK	DG142BP	DG142BK	DG186BP	DG186BK	DG390CJ	DGM190CJ
AH0142D/883	DG142AK/883B	DG143AL	DG143AL	DG187AA	DG187AA	DG5040AK	IH5040MJE
AH0143CD	DG143BK	DG143AP	DG143AK	DG187AA	DGM187AA	DG5040AL	IH5040MFD
AH0143D	DG143AK	DG143BP	DG143BK	DG187AL	DG187AL	DG5040CJ	IH5040CPE
AH0143D/883	DG143AK/883B	DG144AL	DG144AL	DG187AL	DGM187AL	DG5040CK	IH5040CJE
AH0144CD	DG144BK	DG144AP	DG144AK	DG187AP	DG187AK	DG5041AA	IH5041MTW
AH0144D	DG144AK	DG144BP	DG144BK	DG187AP	DGM187AK	DG5041AK	IH5041MJE
AH0144D/883	DG144AK/883B	DG145AL	DG145AL	DG187BA	DG187BA	DG5041AL	IH5041MFD
AH0145CD	DG145BK	DG145AP	DG145AK	DG187BA	DGM187BA	DG5041CJ	IH5041CPE
AH0145D	DG145AK	DG145BP	DG145BK	DG187BP	DG187BK	DG5041CK	IH5041CJE
AH0145D/883	DG145AK/883B	DG146AL	DG146AL	DG187BP	DGM187BK	DG5042AA	IH5042MTW
AH0146CD	DG145BK	DG146AP	DG146AK	DG188AA	DG188AA	DG5042AK	IH5042MJE
AH0146D	DG146AK	DG146BP	DG146BK	DG188AA	DGM188AA	DG5042AL	IH5042MFD
AH0146D/883	DG146AK/883B	DG151AL	DG151AL	DG188AL	DG188AL	DG5042CJ	IH5042CPE
AH0151CD	DG151BK	DG151AP	DG151AK	DG188AL	DGM188AL	DG5042CK	IH5042CJE
AH0151D/883	DG151AK/883B	DG151BP	DG151BK	DG188AP	DG188AK	DG5043AK	IH5043MJE
AH0152CD	DG152BK	DG152AL	DG152AL	DG188AP	DGM188AK	DG5043AL	IH5043MFD
AH0152D	DG152AK	DG152AP	DG152AK	DG188AP	DGM188BK	DG5043CJ	IH5043CPE
AH0152D/883	DG152AK/883B	DG152BP	DG152BK	DG188BA	DG188BA	DG5043CK	IH5043CJE
AH0153CD	DG153BK	DG153AL	DG153AL	DG188BA	DGM188BA	DG5044AA	IH5044MTW
AH0153D	DG153AK	DG153AP	DG153AK	DG188BP	DG188BK	DG5044AK	IH5044MJE
AH0153D/883	DG153AK/883B	DG153BP	DG153BK	DG189AL	DG189AL	DG5044AL	IH5044MFD
AH0154CD	DG154BK	DG154AL	DG154AL	DG189AP	DG189AK	DG5044CJ	IH5044CPE
AH0154D	DG154AK	DG154AP	DG154AK	DG189BP	DG189BK	DG5044CK	IH5044CJE
AH0154D/883	DG143AK/883B	DG154BP	DG154BK	DG190AL	DG190AL	DG5045AK	IH5045MJE
AH0155D	DG151AK	DG161AL	DG161AL	DG190AL	DGM190AL	DG5045AL	IH5045MFD
AH0161CD	DG161BK	DG161AP	DG161AK	DG190AP	DG190AK	DG5045CJ	IH5045CPE
AH0161D	DG161AK	DG161BP	DG161BK	DG190AP	DGM190AK	DG5045CK	IH5045CJE
AH0161D/883	DG161AK/883B	DG162AL	DG162AL	DG190BP	DG190BK	DG506AR	IH6116MJI
AH0162CD	DG162BK	DG162AP	DG162AK	DG190BP	DGM190BK	DG506BR	IH6116CJI
AH0162D	DG162AK	DG162BP	DG162BK	DG190BP	DGM190CJ	DG506CJ	IH6116CPI
AH0162D/883B	DG162AK/883B	DG163AL	DG163AL	DG191AL	DG191AL	DG507AR	IH6216MJI
AH0163CD	DG163BK	DG163AP	DG163AK	DG191AL	DGM191AL	DG507BR	IH6216CJI
AH0163D	DG163AK	DG163BP	DG163BK	DG191AP	DG191AK	DG507CJ	IH6216CPI
AH0163D/883	DG163AK/883B	DG164AL	DG164AL	DG191AP	DGM191AK	DG508AP	IH6108MJE
AH0164CD	DG164BK	DG164AP	DG164AK	DG191BP	DG191BK	DG508BP	IH6108CJE
AH0164D	DG164AK	DG164BP	DG164BK	DG191BP	DGM191BK	DG508CJ	IH6108CPE
AH0164D/P83	DG164AK/883B	DG180AA	DG180AA	DG191BP	DGM191CJ	DG509AP	IH5208MJE
AH5009CN	IH5009CPD	DG180AL	DG180AL	DG200AA	DG200AA	DG509BP	IH6208CJE

**CONSULT FACTORY

ANALOG SWITCH CROSS REFERENCE (cont.)

A

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
DG509CJ	IH6208CPE	HI1-5041-5	IH5041CJE	TL182CN	DGM182CJ		
DGM111AL	DG111AL	HI1-5041-8	IH5041MJE/883B	TL182IL	DGM182BA		
DGM111AP	DG111AK	HI1-5042-2	IH5042MJE	TL182IN	DGM182CJ		
DGM111BP	DG111BK	HI1-5042-5	IH5042CJE	TL182ML	DGM182AA		
G115AP	G115AK	HI1-5042-8	IH5142MJE/883B	TL185CJ	IH5045CJE		
G115BP	G115BJ	HI1-5043-2	IH5143MJE	TL185CN	IH5045CPE		
G115BP	G115BK	HI1-5043-5	IH5143CJE	TL185IJ	IH5045CJE		
G116AL	G116AL	HI1-5043-8	IH5143MJE/883B	TL185IN	IH5045CPE		
G116AP	G116AK	HI1-5044-2	IH5144MJE	TL185MJ	IH5045MJE		
G116BP	G116BJ	HI1-5044-5	IH5144CJE	TL188CL	IH5042CTW		
G116BP	G116BK	HI1-5044-8	IH5144MJE/883B	TL188CN	IH5042CPE		
G117AL	G117AL	HI1-5045-2	IH5145MJE	TL188IL	IH5042CTW		
G118AL	G118AL	HI1-5045-5	IH5145CJE	TL188IN	IH5042CPE		
G118AP	G118AK	HI1-5045-8	IH5145MJE/883B	TL188ML	IH5042MTW		
G119AL	G119AL	HI1-5046-2	IH5046MJE	TL191CJ	IH5043CJE		
G123AL	G123AL	HI1-5046-5	IH5046CJE	TL191CN	IH5043CPE		
G123AP	G123AK	HI1-5046-8	IH5046MJE/883B	TL191IJ	IH5043CJE		
HI0-0201-6	DG201C/D	HI1-5047-2	IH5047MJE	TL191IN	IH5043CPE		
HI0-0381-6	DGM181C/D	HI1-5047-5	IH5047CJE	TL191MJ	IH5043MJE		
HI0-0384-6	DGM184C/D	HI1-5047-8	IH5047MJE/883B				
HI0-0387-6	DGM187C/D	HI1-5049-2	IH5149MJE				
HI0-0390-6	DGM190C/D	HI1-5049-5	IH5149CJE				
HI0-0506-6	IH6116C/D	HI1-5049-8	IH5149MJE/883B				
HI0-0506A-6	IH5116C/D	HI1-5050-2	IH5150MJE				
HI0-0507-6	IH6216C/D	HI1-5050-5	IH5150CJE				
HI0-0507A-6	IH5216C/D	HI1-5050-8	IH5150MJE/883B				
HI0-0508-6	IH6108C/D	HI1-5051-2	IH5151MJE				
HI0-0508A-6	IH5108C/D	HI1-5051-5	IH5151CJE				
HI0-0509-6	IH6208C/D	HI1-5051-8	IH5151MJE/883B				
HI0-0509A-6	IH5208C/D	HI2-0200-2	DG200AA				
HI0-5040-6	IH5140C/D	HI2-0200-4	DG200BA				
HI0-5041-6	IH5141C/D	HI2-0200-5	DG200BA				
HI0-5042-6	IH5142C/D	HI2-0200-8	DG200AA/883B				
HI0-5043-6	IH5143C/D	HI2-0381-2	DGM182AA				
HI0-5044-6	IH5144C/D	HI2-0381-5	DGM181BA				
HI0-5045-6	IH5145C/D	HI2-0381-8	DGM181AA/883B				
HI0-5046-6	IH5046C/D	HI2-0387-2	DGM188AA				
HI0-5047-6	IH5047C/D	HI2-0387-5	DGM187BA				
HI0-5049-6	IH5149C/D	HI2-0387-8	DGM188AA/883B				
HI0-5050-6	IH5150C/D	HI3-0200-5	DG200CJ				
HI0-5051-6	IH5051C/D	HI3-0201-5	DG201CJ				
HI1-0200-2	DG200AK	HI3-0381-5	DGM181CJ				
HI1-0200-4	DG200BK	HI3-0384-5	DGM184CJ				
HI1-0200-5	DG200BK	HI3-0390-5	DGM190CJ				
HI1-0200-6	DG200C/D	HI3-0506-5	IH6116CPI				
HI1-0200-8	DG200AK/883B	HI3-0506A-5	IH5116CPI				
HI1-0201-2	DG201AK	HI3-0507-5	IH6216CPI				
HI1-0201-4	DG201BK	HI3-0507A-5	IH5216CPI				
HI1-0201-5	DG201BK	HI3-0508-5	IH6108CPE				
HI1-0201-8	DG201AK/883B	HI3-0508A-5	IH5108CPE				
HI1-0381-2	DGM182AK	HI3-0509-5	IH6208CPE				
HI1-0381-5	DGM181BK	HI3-0509A-5	IH5208CPE				
HI1-0381-8	DGM182AK/883B	LF11201D	DG201AK				
HI1-0384-2	DGM185AK	LF11201D/883	DG201AK/883B				
HI1-0384-5	DGM184BK	LF11202D	IH202MJE				
HI1-0384-8	DGM185AK/883B	LF11202D/883	IH202MJE/883B				
HI1-0387-2	DGM188AK	LF11508D	IH6108MJE				
HI1-0387-5	DGM187BK	LF11508D/883	IH6108MJE/883B				
HI1-0387-8	DGM188AK/883B	LF11509D	IH6208MJE				
HI1-0390-2	DGM191AK	LF11509D/883	IH6208MJE/883B				
HI1-0390-5	DGM190BK	LF13201D	DG201BK				
HI1-0390-8	DGM191AK/883B	LF13201N	DG201CJ				
HI1-0506-2	IH6116MJI	LF13202D	IH202CJE				
HI1-0506-5	IH6116CJI	LF13508D	IH6108CJE				
HI1-0506-8	IH6116MJI/883B	LF13508N	IH6108CPE				
HI1-0506A-2	IH5116MJI	LF13509D	IH6208CJE				
HI1-0506A-5	IH5116IJI	LF13509N	IH6208CPE				
HI1-0506A-8	IH5116MJI/883B	MM450H	MM450H				
HI1-0507-2	IH6216MJI	MM451H	MM451H				
HI1-0507-5	IH6216CJI	MM452D	MM452J				
HI1-0507-8	IH6216MJI/883B	MM452F	MM452F				
HI1-0507A-2	IH5216MJI	MM455H	MM455H				
HI1-0507A-5	IH5216IJI	MM550H	MM550H				
HI1-0507A-8	IH5216MJI/883B	MM551H	MM551H				
HI1-0508-2	IH6108MJE	MM552D	MM552J				
HI1-0508-5	IH6108CJE	MM552F	MM552F				
HI1-0508-8	IH6108MJE/883B	MM555H	MM555H				
HI1-0508A-2	IH5108MJE	SJM181BCC	JM38510/11101BCC				
HI1-0508A-5	IH5108IJE	SJM181BIC	JM38510/11101BIC				
HI1-0508A-8	IH5108MJE/883B	SJM182BCC	JM38510/11102BCC				
HI1-0509-2	IH6208MJE	SJM182BIC	JM38510/11102BIC				
HI1-0509-5	IH6208CJE	SJM184BEC	JM38510/11103BEC				
HI1-0509-8	IH6208MJE/883B	SJM185BEC	JM38510/11104BEC				
HI1-0509A-2	IH5208MJE	SJM187BCC	JM38510/11105BCC				
HI1-0509A-5	IH5208IJE	SJM187BIC	JM38510/11105BIC				
HI1-0509A-8	IH5208MJE/883B	SJM188BCC	JM38510/11106BCC				
HI1-5040-2	IH5040MJE	SJM188BIC	JM38510/11106BIC				
HI1-5040-5	IH5040CJE	SJM190BEC	JM38510/11107BEC				
HI1-5040-8	IH5040MJE/883B	SJM191BEC	JM38510/11108BEC				
HI1-5041-2	IH5041MJE	TL182CL	DGM182BA				

**CONSULT FACTORY

DATA ACQUISITION CROSS REFERENCE

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
AD7520JD	AD7520JD	MP7521LN	AD7521LN				
AD7520JN	AD7520JN	MP7521SD	AD7521SD				
AD7520KD	AD7520KD	MP7521TD	AD7521TD				
AD7520KN	AD7520KN	MP7521UD	AD7521UD				
AD7520LD	AD7520LD	MP7523JN	AD7523JN				
AD7520LN	AD7520LN	MP7523KN	AD7523KN				
AD7520SD	AD7520SD	MP7523LN	AD7523LN				
AD7520TD	AD7520TD	MP7621AD	AD7541AD				
AD7520UD	AD7520UD	MP7621BD	AD7541BD				
AD7521JD	AD7521JD	MP7621JN	AD7541JN				
AD7521JN	AD7521JN	MP7621KN	AD7541KN				
AD7521KD	AD7521KD	MP7621SD	AD7541SD				
AD7521KN	AD7521KN	MP7621TD	AD7541TD				
AD7521LD	AD7521LD						
AD7521LN	AD7521LN						
AD7521SD	AD7521SD						
AD7521TD	AD7521TD						
AD7521UD	AD7521UD						
AD7523AD	AD7523AD						
AD7523BD	AD7523BD						
AD7523CD	AD7523CD						
AD7523JN	AD7523JN						
AD7523KN	AD7523KN						
AD7523LN	AD7523LN						
AD7523SD	AD7523SD						
AD7523TD	AD7523TD						
AD7523UD	AD7523UD						
AD7530JD	AD7530JD						
AD7530JN	AD7530JN						
AD7530KD	AD7530KD						
AD7530KN	AD7530KN						
AD7530LD	AD7530LD						
AD7530LN	AD7530LN						
AD7531JD	AD7531JD						
AD7531JN	AD7531JN						
AD7531KD	AD7531KD						
AD7531KN	AD7531KN						
AD7531LD	AD7531LD						
AD7531LN	AD7531LN						
AD7533AD	AD7533AD						
AD7533BD	AD7533BD						
AD7533CD	AD7533CD						
AD7533JN	AD7533JN						
AD7533KN	AD7533KN						
AD7533LN	AD7533LN						
AD7533SD	AD7533SD						
AD7533TD	AD7533TD						
AD7533UD	AD7533UD						
AD7541AD	AD7541AD						
AD7541BD	AD7541BD						
AD7541JN	AD7541JN						
AD7541KN	AD7541KN						
AD7541SD	AD7541SD						
AD7541TD	AD7541TD						
DAC1020LCD	AD7520LD						
DAC1020LD	AD7520UD						
DAC1021LCD	AD7520KD						
DAC1021LD	AD7520TD						
DAC1022LCD	AD7520JD						
DAC1022LD	AD7520SD						
DAC1218LCD	AD7541BD						
DAC1218LCN	AD7541KN						
DAC1218LCN	AD7541LN						
DAC1219LCD	AD7541AD						
DAC1219LCN	AD7541JN						
DAC1220LCD	AD7521LD						
DAC1220LD	AD7521UD						
DAC1221LCD	AD7521KD						
DAC1221LD	AD7521TD						
DAC1222LCD	AD7521JD						
DAC1222LD	AD7521SD						
MP7520JD	AD7520JD						
MP7520JN	AD7520JN						
MP7520KD	AD7520KD						
MP7520KN	AD7520KN						
MP7520LD	AD7520LD						
MP7520LN	AD7520LN						
MP7520SD	AD7520SD						
MP7520TD	AD7520TD						
MP7520UD	AD7520UD						
MP7521JD	AD7521JD						
MP7521JN	AD7521JN						
MP7521KD	AD7521KD						
MP7521KN	AD7521KN						
MP7521LD	AD7521LD						

**CONSULT FACTORY

WATCH & CLOCK CROSS REFERENCE

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
CD22001H	ICM1424C						
CD22015E	ICM7051A						
E1115	ICM1115A						
E1151	ICM1115B						
E1426	ICM7050U						
HD43871	ICM7050G						
HD43871	ICM7050H						
KS5183	ICM7269						
KS5240B01H	ICM7245B						
KS5240B01J	ICM7245A						
KS5240B10H	ICM7245D						
KS5240B12H	ICM7245E						
KS5240B20H	ICM7245F						
KS5240U01E	ICM7245U						
M5001	ICM7269						
M58434P	ICM7038D						
M58435P	ICM1115B						
M58436-001P	ICM7050G						
M58437-001P	ICM7070L						
MB101	ICM7245B						
MB103	ICM7245E						
MB105	ICM7245U						
MB107	ICM7245D						
MB108	ICM7245E						
MB143	ICM7245A						
MB144	ICM7245F						
MB510	ICM1115B						
MB511	ICM7050H						
MB512	ICM7050H						
MB513	ICM7050G						
MB521	ITS9068						
MB522	ITS9068						
MB531	ICM7050H						
MB533	ICM7050H						
MB541	ICM7052						
MB542	ICM7052						
MB7B	ICM7245U						
MCC1444D	ICM1424C						
MCC1448J	ICM7210						
MJ41	ICM1424C						
MJ6	ICM7220						
MN6091	ICM7038B						
MN6092A	ICM7038E						
MN6093	ICM7051A						
MN6252	ICM7050G						
MSM5001	ICM7269						
MSM5011	ICM1424C						
MSM5977	ICM1424C						
S1424	ICM1424C						
SCL54301	ICM1424C						
SCL5478	ICM7269						
SM5011	ICM7050G						
SM5510	ICM1115B						
SM5530B	ICM7070P						
TC8031P	ICM7038A						
TC8032P	ICM7038F						
TC8051P	ICM7038B						
TC8052P	ICM7038E						
TC8056PA	ICM1115B						
TC8057P	ICM7038D						
UCN-4111M	ICM7038C						
UCN-4112M	ICM7051A						
UCN-4113M	ICM7038B						
UPD1952P	ICM7220MFA						
UPD1962C	ICM7050G						
UPD1963C	ICM7050						
UPD815C	ICM7038E						
UPD816C	ICM7038B						
UPD820C	ICM1115B						
UPD833G	ICM7223						

**CONSULT FACTORY

LINEAR CROSS REFERENCE

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
723	UA723	MC1741	UA741				
733	UA733	MC1748	UA748				
741	UA741	MHW590	AD590				
748	UA748	MPS5010	ICL8069				
AD101	LM101	NE590	AD590				
AD108	LM108	NE592	NE592				
AD301	LM301	OP-05	OP-05				
AD308	LM308	OP-07	OP-07				
AD503	AD503	OP-08	OP-08				
AD532	AD532	PM308	LM308				
AD534	AD534	RC723	UA723				
AD590	AD590	RC733	UA733				
AD741	UA741	RC741	UA741				
AM2502	AM2502	RC748	UA748				
AM2503	AM2503	RM723	UA723				
AM2504	AM2504	RM741	UA741				
AM5402	HA2505	RM748	UA748				
AM5402	HA2525	SC748	UA748				
CA101	LM101	SG101	LM101				
CA107	LM107	SG105	LM105				
CA111	LM111	SG107	LM107				
CA301	LM301	SG108	LM108				
CA307	LM307	SG110	LM110				
CA308	LM308	SG111	LM111				
CA311	LM311	SG2502	AM2502				
CA723	UA723	SG2503	AM2503				
CA741	UA741	SG301	LM301				
CA748	UA748	SG305	LM305				
DG503	AD503	SG307	LM307				
DM2502	AM2502	SG308	LM308				
DM2503	AM2503	SG311	LM311				
DM2504	AM2504	SG4250	LM4250				
HA2500	HA2500	SG723	UA723				
HA2502	HA2502	SG733	UA733				
HA2505	HA2505	SG741	UA741				
HA2507	HA2507	SG748	UA748				
HA2510	HA2510	SSS741	UA741				
HA2512	HA2512	SU536	SU536				
HA2515	HA2515	TL503	AD503				
HA2517	HA2517	TL592	NE592				
HA2520	HA2520	TT-590	AD590				
HA2522	HA2522	UA101	LM101				
HA2525	HA2525	UA102	LM102				
HA2527	HA2527	UA105	LM105				
HA2600	HA2600	UA107	LM107				
HA2602	HA2602	UA108	LM108				
HA2605	HA2605	UA110	LM110				
HA2607	HA2607	UA111	LM111				
HA2620	HA2620	UA301	LM301				
HA2622	HA2622	UA302	LM302				
HA2625	HA2625	UA305	LM305				
HA2627	HA2627	UA307	LM307				
HA2720	ICL8021	UA308	LM308				
LH0042	LH0042	UA310	LM310				
LH2101	LH2101	UA311	LM311				
LH2108	LH2108	UA723	UA723				
LH2110	LH2110	UA733	UA733				
LH2111	LH2111	UA740	UA740				
LH2301	LH2301	UA741	UA741				
LH2308	LH2308	UA748	UA748				
LH2310	LH2310	UA777	UA777				
LH2311	LH2311	UHP-503	AD503				
LM100	LM100	VR-8069	ICL8069				
LM101	LM101	WG-8038	ICL8038				
LM102	LM102	XR8038	ICL8038				
LM105	LM105						
LM107	LM107						
LM108	LM108						
LM110	LM110						
LM111	LM111						
LM300	LM300						
LM301	LM301						
LM302	LM302						
LM305	LM305						
LM307	LM307						
LM308	LM308						
LM310	LM310						
LM311	LM311						
LM4250	LM4250						
LM723	UA723						
LM733	UA733						
LM740	UA740						
LM741	UA741						
LM748	UA748						
MC1723	UA723						

**CONSULT FACTORY

Discretes

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2N4091-93 1-22
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2N4856-61 1-32
2N5432-34 1-42
2N5638-40 1-49
ITE4091-3 1-22
ITE4391-3 1-30
J105-7 1-77
J111-13 1-78
U200-2 1-85
U1897-99 1-92

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2N3993/4 1-19
2N5018/19 1-36
2N5114-16 1-37
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J174-77 1-79

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2N3684-87 1-10
2N3821/22 1-13
2N3823 1-14
2N3824 1-15
2N4117-19 1-25
2N4220-22 1-26
2N4223/24 1-27
2N4338-41 1-28
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2N5397/98 1-41
2N5457-59 1-44
2N5484-86 1-46
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2N2607-9 1-9
2N5460-65 1-45
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2N3921/22 1-16
2N3954-58 1-17
2N5196-99 1-40
2N5452-54 1-43
2N5515-24 1-47
2N5902-9 1-50
2N5911/12 1-51
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Switches — Junction FET

Ordering Information Preferred Part Number	Package	$r_{DS(on)}$ max Ω	V_p min/max V	I_{GSS} max pA	BV_{GSS} min V	$I_{D(off)}$ max pA	I_{DSS} min/max mA		t_{total} max ns	C_{iss} max pF	C_{rss} max pF
N-channel: Generally requires driver circuit to translate the popular logic levels to voltages required to drive the JFET.											
2N3970	TO-18	30	−4.0	−10.0	(−250)	−40	250	50	150	50	25	6.0
2N3971	TO-18	60	−2.0	−5.0	(−250)	−40	250	25	75	90	25	6.0
2N3972	TO-18	100	−0.5	−3.0	(−250)	−40	250	5	30	180	25	6.0
2N4091	TO-18	30	−5.0	−10.0	−200	−40	200	30		65	16	5.0
2N4092	TO-18	50	−2.0	−7.0	−200	−40	200	15		95	16	5.0
2N4093	TO-18	80	−1.0	−5.0	−200	−40	200	8		140	16	5.0
2N4391	TO-18	30	−4.0	−10.0	−100	−40	100	50	150	55	14	3.5
2N4392	TO-18	60	−2.0	−5.0	−100	−40	100	25	75	75	14	3.5
2N4393	TO-18	100	−0.5	−3.0	−100	−40	100	5	30	100	14	3.5
2N4856	TO-18	25	−4.0	−10.0	−250	−40	250	50		34	18	8.0
2N4857	TO-18	40	−2.0	−6.0	−250	−40	250	20	100	60	18	8.0
2N4858	TO-18	60	−0.8	−4.0	−250	−40	250	8	80	120	18	8.0
2N4859	TO-18	25	−4.0	−10.0	−250	−30	250	50		34	18	8.0
2N4860	TO-18	40	−2.0	−6.0	−250	−30	250	20	100	60	18	8.0
2N4861	TO-18	60	−0.8	−4.0	−250	−30	250	8	80	120	18	8.0
2N5432	TO-52	5	−4.0	−10.0	−200	−25	200	150		41	30	15.0
2N5433	TO-52	7	−3.0	−9.0	−200	−25	200	100		41	30	15.0
2N5434	TO-52	10	−1.0	−4.0	−200	−25	200	30		41	30	15.0
2N5638	TO-92	30		−12.0	−1nA	−30	1nA	50		24	10	4.0
2N5639	TO-92	60		−8.0	−1nA	−30	1nA	25		44	10	4.0
2N5640	TO-92	100		−6.0	−1nA	−30	1nA	5		63	10	4.0
ITE4091	TO-92	30	−5.0	−10.0	−200	−40	200	30		65	16	5.0
ITE4092	TO-92	50	−2.0	−7.0	−200	−40	200	15		95	16	5.0
ITE4093	TO-92	80	−1.0	−5.0	−200	−40	200	8		140	16	5.0
ITE4391	TO-92	30	−4.0	−10.0	−100	−40	100	50	150	55	14	3.5
ITE4392	TO-92	60	−2.0	−5.0	−100	−40	100	25	75	75	14	3.5
ITE4393	TO-92	100	−0.5	−3.0	−100	−40	100	5	30	100	14	3.5
J105	TO-92	3	−4.5	−10.0	−3nA	−25	3nA	500	—	60	(70)	(3.5)
J106	TO-92	6	−2.0	−6.0	−3nA	−25	3nA	200	—	60	(70)	(3.5)
J107	TO-92	8	−0.5	−4.5	−3nA	−25	3nA	100	—	60	(70)	(3.5)
J111	TO-92	30	−3.0	−10.0	−1nA	−35	1nA	20		48	(16)	(5.0)
J112	TO-92	50	−1.0	−5.0	−1nA	−35	1nA	5		48	(16)	(5.0)
J113	TO-92	100	−0.5	−3.0	−1nA	−35	1nA	2		48	(16)	(5.0)
P-channel:												
2N3993	TO-72	150	4.0	9.5	1.2nA	25	1.2nA	−10.0			16	4.5
2N3994	TO-72	300	1.0	5.5	1.2nA	25	1.2nA	−2.0			16	4.5
2N5114	TO-18	75	5.0	10.0	500	30	500	−30.0	−90	37	25	7.0
2N5115	TO-18	100	3.0	6.0	500	30	500	−15.0	−60	68	25	7.0
2N5116	TO-18	150	1.0	4.0	500	30	500	−5.0	−25	102	25	7.0
IT100	TO-18	75	2.0	4.5	200	35	100	−10.0			35	12.0
IT101	TO-18	60	4.0	10.0	200	35	100	−20.0			35	12.0
J174	TO-92	85	5.0	10.0	1nA	30	−1nA	−20.0	−100	22	(25)	(8.0)
J175	TO-92	125	3.0	6.0	1nA	30	−1nA	−7.0	−60	45	(25)	(8.0)
J176	TO-92	250	1.0	4.0	1nA	30	−1nA	−2.0	−25	70	(25)	(8.0)
J177	TO-92	300	0.8	2.25	1nA	30	−1nA	−1.5	−20	90	(25)	(8.0)
J270	TO-92	—	0.5	2.0	200	30	—	−2.0	−15	—	32 typ.	4.0 typ.
J271	TO-92	—	1.5	4.5	200	30	—	−6.0	−50	—	32 typ.	4.0 typ.
P1086	TO-92	75	—	10.0	2nA	30	−10nA	−10.0	—	100	45	10.0
P1087	TO-92	150	—	5.0	2nA	30	−10nA	−5.0	—	215	45	10.0

( ) Approximate Value

Switches and Amplifiers — MOSFET

Ordering Information Preferred Part Number	Package	$V_{GS(TH)}$ $V_{GS(OFF)}$ min/max V	BV_{GSS} min V	I_{DSS} max pA	I_{GSS} max pA	G_{fs} min μmho	$r_{DS(ON)}$ max Ω	I_D $I_{D(ON)}$ min/max mA	
P-Channel Enhancement: Gen. used where max isolation between signal source and logic drive required: sw. "On" resistance varies with signal amplitiude.									
3N161	TO-72	−1.5	−5.0	−25	−10nA	−100.0	3500.0	(125)	−40	−120	Diode Protected
3N163	TO-72	−2.0	−5.0	−40	−200	−10.0	2000.0	250	−5	−30	
3N164	TO-72	−2.0	−5.0	−30	−400	−10.0	2000.0	300	−3	−30	
3N172	TO-72	−2.0	−5.0	−40	−400	−200.0	(2000.0)	250	−5	−30	Diode Protected
3N173	TO-72	−2.0	−5.0	−30	−10nA	−500.0	(1000.0)	350	−5	−30	Diode Protected
IT1700	TO-72	−2.0	−5.0	−40	−200	−10.0	2000.0	400	−2	—	
N-Channel Enhancement: Can switch positive signals directly from TTL logic; gen. requires driver or translator circuit to switch bipolar signals.									
2N4351	TO-72	1.0	5.0	25	10nA	10.0	1000.0	300	3		
3N170	TO-72	1.0	2.0	25	10nA	10.0	1000.0	200	10		
3N171	TO-72	1.5	3.0	25	10nA	10.0	1000.0	200	10		
IT1750	TO-72	0.5	3.0	25	10nA	10.0	3000.0	50	10	100	
M116	TO-72	1.0	5.0	30	(10nA)	100.0	(1000.0)	100	—		Diode Protected

Amplifiers — N-Channel Junction FET

Ordering Information Preferred Part Number	Package	g_{fs} min μmho	I_{DSS} min/max mA		V_P min/max V		I_{GSS} max pA	BV_{GSS} min V	C_{iss} max pF	C_{rss} max pF	e_n max nv/√Hz
2N3684	TO-72	2000	2.5	7.5	−2.0	−5.0	−100	−50	4	1.2	140 @ 100Hz
2N3685	TO-72	1500	1.0	3.0	−1.0	−3.5	−100	−50	4	1.2	140 @ 100Hz
2N3686	TO-72	1000	0.4	1.2	−0.6	−2.0	−100	−50	4	1.2	140 @ 100Hz
2N3687	TO-72	500	0.1	0.5	−0.3	−1.2	−100	−50	4	1.2	140 @ 100Hz
2N3821	TO-72	1500	0.5	2.5		−4.0	−100	−50	6	3.0	200 @ 10Hz
2N3822	TO-72	3000	2.0	10.0		−6.0	−100	−50	6	3.0	200 @ 10Hz
2N3823	TO-72	3500	4.0	20.0		−8.0	−500	−30	6	2.0	—
2N3824	TO-72	—	—	—		(−8.0)	−100	−50	6	3.0	—
2N4117	TO-72	70	0.03	0.09	−0.6	−1.8	−10	−40	3	1.5	—
2N4117A	TO-72	70	0.03	0.09	−0.6	−1.8	−1	−40	3	1.5	—
2N4118	TO-72	80	0.08	0.24	−1.0	−3.0	−10	−40	3	1.5	—
2N4118A	TO-72	80	0.08	0.24	−1.0	−3.0	−1	−40	3	1.5	—
2N4119	TO-72	100	0.2	0.6	−2.0	−6.0	−10	−40	3	1.5	—
2N4119A	TO-72	100	0.2	0.6	−2.0	−6.0	−1	−40	3	1.5	—
2N4220	TO-72	1000	0.5	0.3		−4.0	−100	−30	6	2.0	—
2N4221	TO-72	2000	2.0	6.0		−6.0	−100	−30	6	2.0	—
2N4222	TO-72	2500	5.0	15.0		−8.0	−100	−30	6	2.0	—
2N4223	TO-72	3000	3.0	18.0	−0.1	−8.0	−250	−30	6	2.0	—
2N4224	TO-72	2000	2.0	20.0	−0.1	−8.0	−500	−30	6	2.0	—
2N4338	TO-18	600	0.2	0.6	−0.3	−1.0	−100	−50	7	3.0	65 @ 1kHz
2N4339	TO-18	800	0.5	1.5	−0.6	−1.8	−100	−50	7	3.0	65 @ 1kHz
2N4340	TO-18	1300	1.2	3.6	−1.0	−3.0	−100	−50	7	3.0	65 @ 1kHz
2N4341	TO-18	2000	3.0	9.0	−2.0	−6.0	−100	−50	7	3.0	65 @ 1kHz
2N4416	TO-72	4500	5.0	15.0		−6.0	−100	−30	4	2.0	—
2N4867	TO-72	700	0.4	1.2	−0.7	−2.0	−250	−40	25	5.0	10 @ 1kHz
2N4867A	TO-72	700	0.4	1.2	−0.7	−2.0	−250	−40	25	5.0	5 @ 1kHz
2N4868	TO-72	1000	1.0	3.0	−1.0	−3.0	−250	−40	25	5.0	10 @ 1kHz
2N4868A	TO-72	1000	1.0	3.0	−1.0	−3.0	−250	−40	25	5.0	5 @ 1kHz
2N4869	TO-72	1300	2.5	7.5	−1.8	−5.0	−250	−40	25	5.0	10 @ 1kHz
2N4869A	TO-72	1300	2.5	7.5	−1.8	−5.0	−250	−40	25	5.0	5 @ 1kHz
2N5397	TO-72	6000	10.0	30.0	−1.0	−6.0	−100	−25	5	1.2	3.5dB @ 450MHz
2N5398	TO-72	5500	5.0	40.0	−1.0	−6.0	−100	−25	5.5	1.3	—
2N5457	TO-92	1000	1.0	5.0	−0.1	−6.0	−1nA	−25	7	3.0	—
2N5458	TO-92	1500	2.0	9.0	−1.0	−7.0	−1nA	−25	7	3.0	—
2N5459	TO-92	2000	4.0	16.0	−2.0	−8.0	−1nA	−25	7	3.0	—

Amplifiers — N-Channel Junction FET (continued)

Ordering Information Preferred Part Number	Package	g_{fs} min μmho	I_{DSS} min/max mA		V_P min/max V		I_{GSS} max pA	BV_{GSS} min V	C_{iss} max pF	C_{rss} max pF	e_n max nv/√Hz
2N5484	TO-92	3000	1.0	5.0	−0.3	−3.0	−1nA	−25	5	1.0	120 @ 1kHz
2N5485	TO-92	3500	4.0	10.0	−0.5	−4.0	−1nA	−25	5	1.0	120 @ 1kHz
2N5486	TO-92	4000	8.0	20.0	−2.0	−6.0	−1nA	−25	5	1.0	120 @ 1kHz
ITE4416	TO-92	4500	5.0	15.0		−6.0	−100	−30	4	2.0	—
J201	TO-92	500	0.2	1.0	−0.3	−1.5	−100	−40	4	1.0	5 @ 1kHz
J202	TO-92	1000	0.9	4.5	−0.8	−4.0	−100	−40	4	1.0	5 @ 1kHz
J203	TO-92	1500	4.0	20.0	−2.0	−10.0	−100	−40	4	1.0	5 @ 1kHz
J204	TO-92	1500	1.2	typ.	−0.5	−2.0	−100	−25	4	1.0	10 @ 1kHz
J308	TO-92	8000	12.0	60.0	−1.0	−6.5	−1nA	−25	(8)	(5.0)	—
J309	TO-92	10,000	12.0	30.0	−1.0	−4.0	−1nA	−25	(8)	(5.0)	—
J310	TO-92	8000	24.0	60.0	−2.0	−6.5	−1nA	−25	(8)	(5.0)	—
U308	TO-52	10,000	12.0	60.0	−1.0	−6.0	−150	−25	7 typ.	4.0 typ.	10 @ 100Hz typ.
U309	TO-52	10,000	12.0	30.0	−1.0	−4.0	−150	−25	7 typ.	4.0 typ.	10 @ 100Hz typ.
U310	TO-52	10,000	24.0	60.0	−2.5	−6.0	−150	−25	7 typ.	4.0 typ.	10 @ 100Hz typ.

Amplifiers — P-Channel Junction FET

Ordering Information Preferred Part Number	Package	g_{fs} min μmho	I_{DSS} min/max mA		V_P min/max V		I_{GSS} max nA	BV_{GSS} min V	C_{iss} max pF	C_{rss} max pF	e_n max nv/√Hz
2N2607	TO-18	330	−0.3	−1.5	1.0	4.0	3	30	10	—	400 @ 1kHz
2N2608	TO-18	1000	−0.9	−4.5	1.0	4.0	10	30	17	—	140 @ 1kHz
2N2609	TO-18	2500	−2.0	−10.0	1.0	4.0	30	30	30	—	140 @ 1kHz
2N5460	TO-92	1000	−1.0	−5.0	0.75	6.0	5	40	7	2	115 @ 100Hz
2N5461	TO-92	1500	−2.0	−9.0	1.0	7.5	5	40	7	2	115 @ 100Hz
2N5462	TO-92	2000	−4.0	−16.0	1.8	9.0	5	40	7	2	115 @ 100Hz
2N5463	TO-92	1000	−1.0	−5.0	0.75	6.0	5	60	7	2	115 @ 100Hz
2N5464	TO-92	1500	−2.0	−9.0	1.0	7.5	5	60	7	2	115 @ 100Hz
2N5465	TO-92	2000	−4.0	−16.0	1.8	9.0	5	60	7	2	115 @ 100Hz
U304	TO-18	—	−30.0	−90.0	5.0	10.0	.5	30	27	7	—
J305	TO-18	—	−15.0	−60.0	3.0	6.0	.5	30	27	7	—
U306	TO-18	—	−5.0	−25.0	1.0	4.0	.5	30	27	7	—

Differential Amplifiers — Dual Monolithic N-Channel Junction FET

Preferred Part Number	Package	V_{GSI-2} max mV	ΔV_{GS} max μV/°C	I_G max pA	BV_{GSS} min V	V_P min/max V		g_{fs} min/max μmho		I_{DSS} min/max mA		e_n max nV/√Hz
2N3921	TO-71	5	10	−250	−50	−	−3.0	1500	7500	1.0	10.0	—
2N3922	TO-71	5	25	−250	−50	−	−3.0	1500	7500	1.0	10.0	—
2N3954	TO-71	5	10	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3954A	TO-71	5	5	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3955	TO-71	10	25	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3955A	TO-71	15	15	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3956	TO-71	15	50	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3957	TO-71	20	75	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3958	TO-71	25	100	−50	−50	−1.0	−4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N5196	TO-71	5	5	−15	−50	−0.7	−4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5197	TO-71	5	10	−15	−50	−0.7	−4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5198	TO-71	10	20	−15	−50	−0.7	−4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5199	TO-71	15	40	−15	−50	−0.7	−4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5452	TO-71	5	5	IGSS −100	−50	−1.0	−4.5	1000	4000	0.5	5.0	20 @ 1kHz
2N5453	TO-71	10	10	IGSS −100	−50	−1.0	−4.5	1000	4000	0.5	5.0	20 @ 1kHz
2N5454	TO-71	15	25	IGSS −100	−50	−1.0	−4.5	1000	4000	0.5	5.0	20 @ 1kHz
2N5515	TO-71	5	5	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5516	TO-71	5	10	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5517	TO-71	10	20	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5518	TO-71	15	40	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5519	TO-71	15	80	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5520	TO-71	5	5	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5521	TO-71	5	10	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5522	TO-71	10	20	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5523	TO-71	15	40	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5524	TO-71	15	80	−100	−40	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5902	TO-99	5	5	−3	−40	−0.6	−4.5	70	250	0.3	0.5	200 @ 1kHz
2N5903	TO-99	5	10	−3	−40	−0.6	−4.5	70	250	0.03	.05	200 @ 1kHz
2N5904	TO-99	10	20	−3	−40	−0.6	−4.5	70	250	0.03	.05	200 @ 1kHz
2N5905	TO-99	15	40	−3	−40	−0.6	−4.5	70	250	0.03	.05	200 @ 1kHz
2N5906	TO-99	5	5	−1	−40	−0.6	−4.5	70	250	0.03	.05	100 @ 1kHz
2N5907	TO-99	5	10	−1	−40	−0.6	−4.5	70	250	0.03	.05	100 @ 1kHz
2N5908	TO-99	10	20	−1	−40	−0.6	−4.5	70	250	0.03	.05	100 @ 1kHz
2N5909	TO-99	15	40	−1	−40	−0.6	−4.5	70	250	0.03	.05	100 @ 1kHz
2N5911	TO-99	10	20	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
2N5912	TO-99	15	40	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
2N6483	TO-71	5	5	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	10 @ 10Hz
2N6484	TO-71	10	10	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	10 @ 10Hz
2N6485	TO-71	15	25	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	10 @ 10Hz
IMF6485	TO-71	25	40	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10Hz
IT500	TO-52	5	5	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10Hz
IT501	TO-52	5	10	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10Hz
IT502	TO-52	10	20	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10Hz
IT503	TO-52	15	40	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10Hz
IT504	TO-52	25	100	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10Hz
IT505	TO-52	50	200	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10Hz
IT5911	TO-71	10	20	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
IT5912	TO-71	15	40	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
U257	TO-99	100	—	IGSS −100	−25	−1.0	−5.0	5000	10000	5.0	40.0	30 @ 10kHz
U401	TO-71	5	10	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10Hz
U402	TO-71	10	10	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10Hz
U403	TO-71	10	25	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10Hz
U404	TO-71	15	25	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10Hz
U405	TO-71	20	40	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10Hz
U406	TO-71	40	80	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10Hz
U421	TO-99	10	10	0.1	−60	−0.4	−2.0	300	800		60-1000μA	20 @ 10Hz
U422	TO-99	15	25	0.1	−60	−0.4	−2.0	300	800		60-1000μA	20 @ 10Hz
U423	TO-99	25	40	0.1	−60	−0.4	−2.0	300	800		60-1000μA	20 @ 10Hz
U424	TO-99	10	10	0.5	−60	−0.4	−3.0	300	1000		60-1000μA	20 @ 10Hz
U425	TO-99	15	25	0.5	−60	−0.4	−3.0	300	1000		60-1000μA	20 @ 10Hz
U426	TO-99	25	40	0.5	−60	−0.4	−3.0	300	1000		60-1000μA	20 @ 10Hz

Differential Amplifiers — Dual Monolithic P-Channel MOSFETS (Enhancement)

Ordering Information Preferred Part Number	Package	$V_{GS(TH)}$ min/max V		BV_{DSS} min/max V	I_{DSS} max pA	I_{GSS} max pA	G_{fs} min μmho	$I_{DS(ON)}$ min/max mA		$r_{DS(ON)}$ max Ω	$V_{GS\ 1-2}$ max mV	
3N165	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300	100	
3N166	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300		
3N188	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	100	Zener Protected
3N189	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300		Zener Protected
3N190	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	100	Zener Protected
3N191	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300		

Differential Amplifiers — Dual NPN Bipolar Transistors

Ordering Information Preferred Part Number	Package	$V_{BE\ 1-2}$ mV max	ΔV_{BE} μV/°C max	h_{FE} @ $I_C = 10\mu A$ $V_{CE} = 5V$ min	$I_{B\ 1-2}$ @ $I_C = 10\mu A$ $V_{CE} = 5V$ nA max	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz@I_C min	C_{obo} pF max	Structure
2N4044	TO-78	3	3	200	5	60	.1	2	200 @ 1mA	0.8	Dielec. Isol.
2N4045	TO-78	5	10	80	25	45	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4100	TO-78	5	5	150	10	55	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4878	TO-71	3	3	200	5	60	.1	2	200 @ 1mA	0.8	Dielec. Isol.
2N4879	TO-71	5	5	150	10	55	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4880	TO-71	5	10	80	25	45	.1	3	150 @ 1mA	0.8	Dielec. Isol.
IT120	TO-78 TO-71	2	5	200	5	45	1	2 typ.	220 @ 1mA	2	Junc. Isol.
IT120A	TO-78 TO-71	1	3	200	2.5	45	1	2 typ.	220 @ 1mA	2	Jur.c. Isol.
IT121	TO-78 TO-71	3	10	80	25	45	1	2 typ.	180 @ 1mA	2	Junc. Isol.
IT122	TO-78 TO-71	5	20	80	25	45	1	2 typ.	180 @ 1mA	2	Junc. Isol.
IT124	TO-78	5	15	1500	0.6 @ V_{CE} = 1V	2	.1	3	100 @ 100μA	0.8	Junc. Isol.
IT126	TO-78 TO-71	1	3	200	2.5	60	.1	1 typ.	250 @ 10mA	4	Dielec. Isol.
IT127	TO-78 TO-71	2	5	200	5	60	.1	1 typ.	250 @ 10mA	4	Dielec. Isol.
IT128	TO-78 TO-71	3	10	150	10	45	.1	1 typ.	200 @ 10mA	4	Dielec. Isol.
IT129	TO-78 TO-71	5	20	100	20	45	.1	1 typ.	150 @ 10mA	4	Dielec. Isol.

Differential Amplifiers — Dual PNP Bipolar Transistors

Ordering Information

Preferred Part Number	Package	$V_{BE\ 1\text{-}2}$ mV max	ΔV_{BE} µV/°C max	h_{FE} @ $I_C = 10\mu A$ $V_{CE} = 5V$ min	$I_C = 10\mu A$ $V_{CE} = 5V$ nA max	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz@I_C min	C_{obo} pF max	Structure
2N5117	TO-78	3	3	100	10	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.
2N5118	TO-78	5	5	100	15	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.
2N5119	TO--78	5	10	50	40	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.
IT130	TO-78 TO-71	2	5	200	5	−45	1	2 typ.	110 @ 1mA	2	Junc. Isol.
IT130A	TO-78 TO-71	1	3	200	2.5	−60	.1	2 typ.	110 @ 1mA	2	Junc. Isol.
IT131	TO-78 TO-71	5	10	80	10	−45	1	2 typ.	90 @ 1mA	2	Junc. Isol.
IT132	TO-78 TO-71	10	20	80	25	−45	1	2 typ.	90 @ 1mA	2	Junc. Isol.
IT136	TO-78 TO-71	1	3	150	2.5	−60	.1	2 typ.	150 @ 10mA	4	Dielec. Isol.
IT137	TO-78 TO-71	2	5	150	5	−60	.1	2 typ.	150 @ 10mA	4	Dielec. Isol.
IT138	TO-78 TO-71	3	10	120	10	−55	.1	2 typ.	180 @ 10mA		Dielec. Isol.
IT139	TO-78 TO-71	5	20	70	20	−45	.1	2 typ.	100 @ 10mA	4	Dielec. Isol.

Specialty Items

ID-100
ID-101

This product is a diode combination used to protect those P-channel MOSFET duals which are not diode protected. Their chief characteristic is < 1 pA leakage when voltage across them is less than 5 mV. If voltage across diodes is adjusted to 0V ±0.1mV, leakage is less than 0.01 pA.

VCR2N
VCR3P
VCR4N
VCR5P
VCR7N
VCR11N (Dual)

The VCR family consists of three terminal variable resistors where the resistance value between two of the terminals is controlled by the voltage potential applied to the third.

Note: Intersil offers the following military qualified devices:*

N-channel switches	N-channel amplifiers	P-channel switches	P-channel amplifiers
2N4091 JAN, JANTX, JANTXV	2N3821 JAN, JANTX, JANTXV	2N5114 JAN, JANTX, JANTXV	2N2609 JAN
2N4092 JAN, JANTX, JANTXV	2N3823 JAN, JANTX, JANTXV	2N5115 JAN, JANTX, JANTXV	
2N4093 JAN, JANTX, JANTXV		2N5116 JAN, JANTX, JANTXV	
2N4856 JAN, JANTX, JANTXV			
2N4857 JAN, JANTX, JANTXV			
2N4858 JAN, JANTX, JANTXV			

*JAN processing consists of a sample Group B pulled from the production run.
JANTX processing consists of JAN processing plus 100% electrical read and record, and 100% burn-in.
JANTVX processing consists of JANTX processing plus 100% pre-cap visual and on-shore assembly.

DISCRETE SELECTOR GUIDE

	Detailed Application	Important Parameters	Recommended Part Numbers							
			Single N-Channel JFET	Single P-Channel JFET	Dual N-Channel JFET	Single N-Channel MOSFET	Single P-Channel MOSFET	Dual P-Channel MOSFET	Dual NPN Bipolar	Dual PNP Bipolar
Amplifiers	Audio	low noise	2N4220, 2N3821	2N2607 2N5460	2N3958 IT505	2N4351 3N170-1	3N163 3N164		2N4044 2N4878	IT130
	Buffer	low leakage, high gain	2N4221	2N2609 2N5462	2N5905 IT505	M116 IT1750	3N172 IT1700		IT120	IT136
	Differential	good matching & drift	—	—	2N3954 U401	—	—	3N165	IT126	2N3810
	Fet Input Op Amp		—	—	2N5515	—	—		—	—
	High Impedance	low leakage	2N4117A	IT100 J176 2N5116	2N5905 IT505 U426	IT1750	IT1700		—	—
	High Frequency	high gain, low capacitance	U308 2N5397	2N5114 J176	2N5912 IT5912	2N4351	3N163 3N164	3N188	2N4044 2N4878 IT120	IT130 IT136
	Low Supply Voltage	low pinch-off voltage	2N4338 2N3687	2N5265 J177	U406 2N3958	3N170-1			IT126 IT140	2N3810
	Low Noise	low noise	2N4867A	2N5116 J176	2N5519 2N5199	M116	3N172		2N4044	IT130
	Preamplifier	high gain	2N5397 U310	2N5116 J176	IT550 U406				2N4044 2N4878 IT120	IT130 IT136
	Video	high gain, low capacitance	2N4393 ITE4393	IT100	IT5912 2N5912				IT126	2N3810
Mixers	VHF	RF parameters,	U310 2N5397	IT100 J174	2N6485	—	—	—	—	—
	UHF	high g_{fs}/C_{iss}	J310 2N5484	2N5114	IT5912 2N5912					
Switches	Commutators	low C_{rss}	2N4391 ITE4391	2N3993-4 IT100-1	IT550	IT1750	IT1700			
	Sample and Hold			2N5114-6			3N163	3N165		
	Analog Gates	fast switching,	2N4091-3 2N4391-3	2N5114-6	2N5912				—	—
	Digital	low $r_{DS(on)}$	ITE4391-3	J174-7	IT5912	3N170-1	3N164	3N188		
	Chopper		2N5432-4	IT100-1			3N172			
	Integrator Reset	low $r_{DS(on)}$, high I_{DSS}	J111-3 J105-7							
Voltage Control Resistors	Gain Control Amplitude Stability Attenuators	high $V_{GS(off)}$	VCR2N VCR4N VCR7N	VCR3P	VCR11N	—	—	—	—	—
Protection Diodes	Signal Clipping and Clamping	low leakage current	—	—	—	—	—	—	ID100-1	IT139

2N2607-2N2609
2N2609 JAN
P-Channel JFET

APPLICATIONS

- Low-level Choppers
- Data Switches
- Commutators

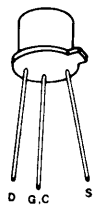
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage	30 V
Gate-Drain Voltage	30 V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature Soldering, 10 sec	+300°C
Power Dissipation	300 mW
Derate above 25°C	2 mW/°C

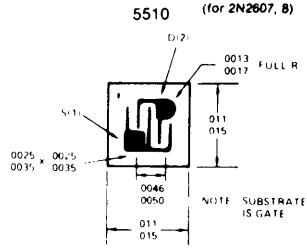
PIN CONFIGURATION

TO-18

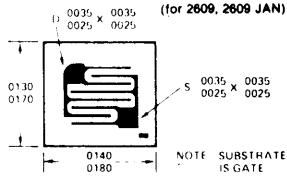


CHIP TOPOGRAPHY

5510 (for 2N2607, 8)



5503 (for 2609, 2609 JAN)



ORDERING INFORMATION*

TO-18	WAFER	DICE
2N2607	2N2607/W	2N2607/D
2N2608	2N2608/W	2N2608/D
2N2609	2N2609/W	2N2609/D
2N2609 JAN	—	—

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		2N2607		2N2608		2N2609		Unit	Test Conditions	
		Min	Max	Min	Max	Min	Max			
I_{GSSR}	Gate Reverse Current		3		10		30	nA	V_{GS} = 30 V, V_{DS} = 0	
			3		10		30	μA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150° C	
BV_{GSS}	Gate-Drain Breakdown Voltage	30		30		30		V	I_G = 1 μA, V_{DS} = 0	
V_P	Gate-Source Pinch-Off Voltage	1	4	1	4	1	4	V	V_{DS} = -5 V, I_D = -1 μA	
I_{DSS}	Drain Current at Zero Gate Voltage	-0.30	-1.50	-0.90	-4.50	-2	-10	mA	V_{DS} = -5 V, V_{GS} = 0	
g_{fs}	Small-Signal Common-Source Forward Transconductance	330		1000		2500		μmho	V_{DS} = -5 V, V_{GS} = 0, f = 1 kHz	
C_{iss}	Common-Source Input Capacitance		10		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V, f = 140 kHz	
NF	Noise Figure		3					dB	V_{DS} = -5 V, V_{GS} = 0, f = 1 kHz	R_G = 10 MΩ
					3		3			R_G = 1 MΩ

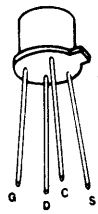
2N3684-2N3687
N-Channel JFET

FEATURES
- **Low Noise**
- **High Input Impedance**
- **Low Capacitance**

APPLICATIONS
- Low Level Choppers
- Data Switches
- Multiplexers
- Low Noise Amplifiers

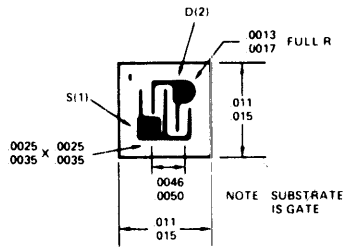
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5010*



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3684	2N3684/W	2N3684/D
2N3685	2N3685/W	2N3685/D
2N3686	2N3686/W	2N3686/D
2N3687	2N3687/W	2N3687/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3684		2N3685		2N3686		2N3687		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	-50		-50		-50		-50		V	V_{DS} = 0, I_G = 1.0 μA
V_P	Pinch-Off Voltage	2.0	5.0	1.0	3.5	0.6	2.0	0.3	1.2	V	V_{DS} = 20 V, I_D = 0.001 μA
I_{GSS}	Total Gate Leakage Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0
	T_A = 150°C		-0.5		-0.5		-0.5		-0.5	μA	
I_{DSS}	Saturation Current, Drain-to-Source	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA	V_{GS} = 0, V_{DS} = 20 V
$\|Y_{fs}\|$	Forward Transadmittance	2000	3000	1500	2500	1000	2000	500	1500	μmhos	
G_{os}	Common Source Output Conductance		50		25		10		5	μmhos	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
C_{iss}	Common Source Input Capacitance		4.0		4.0		4.0		4.0	pF	
C_{rss}	Common Source Short Circuit Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF	
$r_{DS(on)}$	On Resistance		600		800		1200		2400	Ohms	V_{DS} = 0, V_{GS} = 0
NF	Noise Figure		0.5		0.5		0.5		0.5	dB	f = 100 Hz, R_G = 10 MΩ NBW = 6 Hz, V_{DS} = 10V V_{GS} = 0V

2N3810/A, 2N3811/A Monolithic Dual Matched PNP Transistor

1

ABSOLUTE MAXIMUM RATINGS

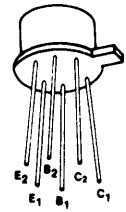
(T_A = 25°C unless otherwise noted)

Emitter-Base Voltage (Note 1) ..... -5V
Collector-Base or Collector-Emitter Voltage (Note 1) ... -60V
Collector Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	500 mW	600 mW
Derate above 25°C	2.9 mW/°C	3.4 mW/°C

PIN CONFIGURATION

TO-78



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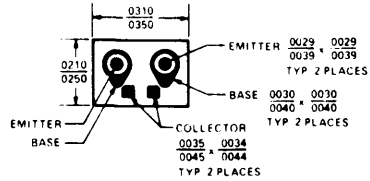
CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-78	WAFER	DICE
2N3810	2N3810/W	2N3810/D
2N3810A		
2N3811	2N3811/W	2N3811/D
2N3811A		

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	PARAMETER	2N3810/A MIN	2N3810/A MAX	2N3811/A MIN	2N3811/A MAX	UNITS	TEST CONDITIONS
BV_{CBO}	Collector-Base Breakdown Voltage	-60		-60		V	I_C = -10 μA, I_E = 0
BV_{CEO}	Collector-Emitter Breakdown Voltage (Note 2	-60		-60		V	I_C = -10 mA, I_B = 0
BV_{EBO}	Emitter-Base Breakdown Voltage	-5		-5		V	I_E = -10 μA, I_C = 0
$I_{C(off)}$	Collector Cutoff Current		-10		-10	nA	V_{CB} = -50V, I_E = 0
	T_A = +150°C		-10		-10	μA	
$I_{E(off)}$	Emitter Cutoff Current		-20		-20	nA	V_{BE} = 4V, I_C = 0
h_{FE}	Static Forward Current Transfer Ratio (Note 2	100		225			V_{CE} = -5V, I_C = -10μA
		150	450	300	900		V_{CE} = -5V, I_C = -100μA to -1 mA
		125		250			V_{CE} = -5V, I_C = 10 mA
	T_A = -55°C	75		150			V_{CE} = -5V, I_C = 100 μA
$V_{BE(sat)}$	Base-Emitter Saturation Voltage (Note 2		-0.7		-0.7	V	V_{CE} = -5V, I_B = -10μA
			-0.8		-0.8		I_C = -100 μA, I_B = -100 μA
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 2		-0.2		-0.2		I_B = -10 μA, I_C = -100 μA
			-0.25		-0.25		I_B = -100 μA, I_C = -1 mA
h_{ie}	Input Impedance	3	30	10	40	kΩ	V_{CE} = -10V, I_C = -1 mA, f = 1 KHz
h_{fe}	Forward Current Transfer Ratio	150	600	300	900		
h_{re}	Reverse Voltage Transfer Ratio		0.25		0.25		
h_{oe}	Output Admittance	5	60	5	60	μmho	
$\|h_{fe}\|$	Magnitude of small signal current gain	1	5	1	5		V_{CE} = -5V, I_C = -1mA, f = 100 MHz
		1		1			I_C = -500 μA, f = 30 MHz

NOTES:

1. Per transistor.
2. Pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	PARAMETER		2N3810/A MIN	2N3810/A MAX	2N3811/A MIN	2N3811/A MAX	UNITS	TEST CONDITIONS	
C_{obo}	Output Capacitance			4		4	pF	V_{CB} = -5V, I_E = 0, f = 100 MHz	
C_{ibo}	Input Capacitance			8		8		V_{CB} = -0.5V, I_C = 0, f = 100 KHz	
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio		0.9	1.0	0.9	1.0		V_{CE} = -5V, I_C = 100 μA	
		A devices	0.95	1.0	0.95	1.0			
$\lvert V_{BE_1}-V_{BE_2}\rvert$	Base-Emitter Voltage Differential			-5		-5	mV	V_{CE} = -5V	I_C = 10 μA to 10 mA
		A devices		-2.5		-2.5			I_C = 100 μA
				-3		-3			
		A devices		-1.5		-1.5			
$\frac{\Delta V_{BE_1}-V_{BE_2}}{\Delta T}$	Base-Emitter Voltage Differential Gradient			10		10	μV/°C	V_{CE} = -5, I_C = 100 μA	
		A devices		5		5			
NF	Spot Noise Figure			7		4	dB	V_{CE} = -10V, I_C = -100 μA, R_G = 3kΩ, f = 100 Hz, Noise Bandwidth = 20Hz	
				3		1.5		V_{CE} = -10V, I_C = -100 μA, R_G = 3kΩ, f = 1kHz, Noise Bandwidth = 200 kHz	
				2.5		1.5		V_{CE} = -10V, I_C = -100μA, R_G = 3 kΩ f = 10 kHz, Noise Bandwidth = 2 kHz	
				3.5		2.5		V_{CE} = -10V, I_C = -100 μA, R_G = 3kΩ, Noise Bandwidth = 15.7 kHz (Note 3)	

NOTES:

3 3 dB down at 10 Hz and 10 kHz.

2N3821, 2N3822
N-Channel JFET

FEATURES

- **Low Capacitance**
- **Up to 6500 μmho Transconductance**

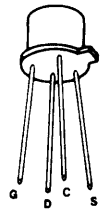
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage	-50V
Gate-Drain Voltage	-50V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

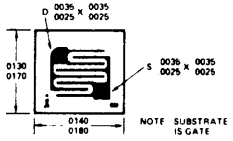
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5003



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3821 MIN	2N3821 MAX	2N3822 MIN	2N3822 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
	T_A = 150°C		-0.1		-0.1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		V_{DS} = 15 V, I_D = 0.5 nA	
V_{GS}	Gate-Source Voltage	-0.5	-2				V_{DS} = 15 V, I_D = 50 μA	
				-1	-4		V_{DS} = 15 V, I_D = 200 μA	
I_{DSS}	Saturation Drain Current	0.5	2.5	2	10	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward **Transconductance (Note 1)**	1500	4500	3000	6500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
$\|y_{fs}\|$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
g_{os}	Common-Source Output **Conductance (Note 1)**		10		20			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
NF	Noise Figure		5		5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
$\overline{e_n}$	Equivalent Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

Note 1: These parameters are measured during a 2 msec interval 100 msec after DC power is applied.

2N3823
N-Channel JFET

1

FEATURES

- **Low Noise**
- **Low Capacitance**
- **Transductance up to 6500 μmho**

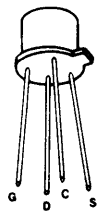
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

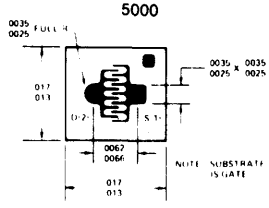
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5000



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3823	2N3823/W	2N3823/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.5	nA	V_{GS} = -20V, V_{DS} = 0	
	T_A = 150°C		-0.5	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = 1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-8		V_{DS} = 15V, I_D = 0.5 nA	
V_{GS}	Gate-Source Voltage	-1.0	-7.5		V_{DS} = 15V, I_D = 400 μA	
I_{DSS}	Saturation Drain Current	4	20	mA	V_{DS} = 15V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	3,500	6,500	μmho	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz (Note 1)
$\|Y_{fs}\|$	Common-Source Forward Transadmittance	3,200				f = 100 MHz
g_{os}	Common-Source Output Transconductance		35			f = 1 kHz (Note 1)
g_{iss}	Common-Source Input Conductance		800			f = 200 MHz
g_{oss}	Common-Source Output Conductance		200			
C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Noise Figure		2.5	dB	V_{DS} = 15V, V_{GS} = 0 R_G = 1 kΩ	f = 100 MHz

NOTE 1: These parameters are measured during a 2 msec interval 100 msec after DC power is applied.

2N3824
N-Channel JFET

FEATURES

- $r_{ds} < 250$ ohms
- $I_{D(off)} < 0.1$ nA

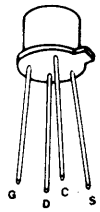
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Load Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

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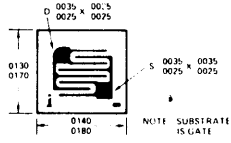


ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3824	2N3824/W	2N3824/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETER			MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current			-0.1	nA	V_{GS} = -30V, V_{DS} = 0	
		T_A = 150°C		-0.1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage		-50		V	I_G = 1 μA, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current			0.1	nA	V_{DS} = 15V, V_{GS} = -8V	
		T_A = 150°C		0.1	μA		
$r_{ds(on)}$	Drain-Source ON Resistance			250	Ω	V_{GS} = 0V, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance			6	pF	V_{DS} = 15V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			3		V_{GS} = -8V, V_{DS} = 0	

2N3921, 2N3922
Monolithic Dual N-Channel JFET

1

FEATURES

- **Low Drain Current**
- **High Output Impedance**
- **Matched V_{GS}, ΔV_{GS}, and g_{fs}**

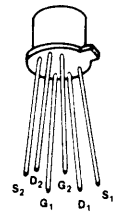
ABSOLUTE MAXIMUM RATINGS

(T_A = 25° C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65° C to +200° C
Operating Temperature Range ..... -55° C to +150° C
Load Temperature (Soldering, 10 sec.) ..... +300° C
Power Dissipation ..... 300 mW
Derate above 25° C ..... 1.7 mW/° C

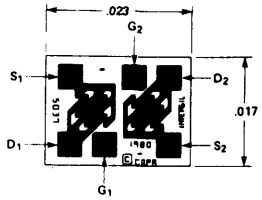
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6037



ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N3921	2N3921/W	2N3921/D
2N3922	2N3922/W	2N3922/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: (25° C unless otherwise noted)

PARAMETER			MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current	T_A = 100° C		−1 −1	nA μA	V_{GS} = −30V, V_{DS} = 0	
BV_{DGO}	Drain-Gate Breakdown Voltage		50		V	I_D = 1 μA, I_S = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage			−3		V_{DS} = 10V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage		−0.2	−2.7		V_{DS} = 10V, I_D = 100μA	
I_G	Gate Operating Current			−250	pA	V_{DG} = 10V, I_D = 700μA	
		T_A = 100° C		−25	nA		
I_{DSS}	Saturation Drain Current (Note 1)		1	10	mA	V_{DS} = 10V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 2)		1500	7500	μmho	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance			35			
C_{iss}	Common-Source Input Capacitance			18	pF		
C_{rss}	Common-Source Reverse Transfer Capacitance			6			
g_{fs}	Common-Source Forward Transconductance		1500		μmho	V_{DG} = 10V, I_D = 700 μA	f = 1 kHz
g_{oss}	Common-Source Output Conductance			20			
NF	Spot Noise Figure			2	dB	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz, R_G = 1 meg

MATCHING CHARACTERISTICS		2N3921 MIN	2N3921 MAX	2N3922 MIN	2N3922 MAX	UNIT	TEST CONDITIONS	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5	mV	V_{DG} = 10V, I_D = 700 μA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		10		25	μV/° C		T_A = 0° C T_B = 100° C
g_{fs2}	Transconductance Ratio	0.95	1.0	0.95	1.0			f = 1 kHz

NOTES: 1. Per transistor.
2. Pulse test duration = 2 ms.

2N3954-2N3958 Monolithic Dual N-Channel JFET

FEATURES

- **Low Offset and Drift**
- **Low Capacitance**
- **Low Noise**
- **Superior Tracking Ability**
- **Low Output Conductance**

ABSOLUTE MAXIMUM RATINGS

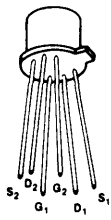
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain
Breakdown Voltage (Note 1) 50V
Any Pin to Case Voltage 100V
Gate Current (Note 1) ..... 50 mA
Storage Temperature .. -65°C to +200°C
Operating Temperature -55°C to +150°C
Lead Temperature
(Soldering, 10 sec.) ..... +300°C

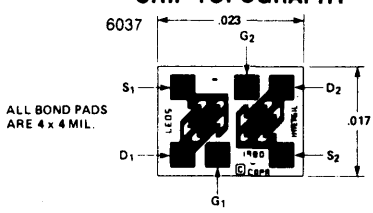
	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	2.8 mW/°C	4.3 mW/°C

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-100		-100		-100		-100		-100		-100		-100	pA	V_{GS} = -30 V,	
	T_A = 125°C		-500		-500		-500		-500		-500		-500		-500	nA	V_{DS} = 0	
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		-50		V	V_{DS} = 0 I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		2.0		2.0		2.0	V	V_{DS} = 0 I_G = 1 mA	
V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2	V	V_{DS} = 20 V	I_D = 50 μA
		-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.4	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	V		I_D = 200 μA
I_G	Gate Operating Current		-50		-50		-50		-50		-50		-50		-50	pA	V_{DS} = 20 V,	
	T_A = 125°C		-250		-250		-250		-250		-250		-250		-250	nA	I_D = 200 μA	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		1000		1000		1000		1000				f = 200 MHz
g_{os}	Common-Source Output Conductance		35		35		35		35		35		35		35	μmho		f = 1 kHz
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2		1.2		1.2		1.2	pF		f = 1 MHz
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		1.5		1.5		1.5	pF	V_{DG} = 10 V, I_S = 0	f = 1 MHz
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V V_{GS} = 0 R_G = 10 MΩ	f = 100 Hz
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0		V_{DS} = 20 V V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0		15		20		25	mV		
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		4.0		6.0		8.0	mV	V_{DS} = 20 V, I_D = 200 μA	T = 25°C to -55°C
			1.0		0.5		2.5		1.5		5.0		7.5		10.0			T = 25°C to 125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0			f = 1 kHz

NOTE 1: Per transistor.

2N3970-2N3972
N-Channel JFET

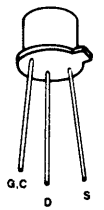
1

FEATURES

- **Low $r_{DS(on)}$**
- **$I_{D(off)}$ < 250 pA**
- **Fast Switching**

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

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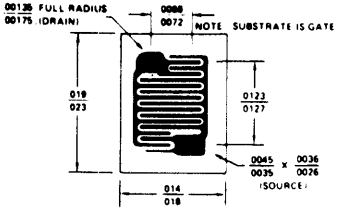


ORDERING INFORMATION*

TO-18	WAFER	DICE
2N3970	2N3970/W	2N3970/D
2N3971	2N3971/W	2N3971/D
2N3972	2N3972/W	2N3972/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS

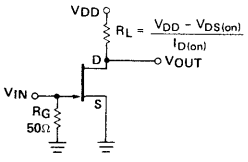
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipaton	1.8W
Derate above 25°C	10 mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	PARAMETER	2N3970 MIN	2N3970 MAX	2N3971 MIN	2N3971 MAX	2N3972 MIN	2N3972 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate Reverse Breakdown Voltage	-40		-40		-40		V	I_G = -1μA, V_{DS} = 0	
I_{DGO}	Drain Reverse Current		250		250		250	pA	V_{DG} = 20V, I_S = 0	
	T_A = 150°C		500		500		500	nA		
$I_{D(off)}$	Drain Cutoff Current		250		250		250	pA	V_{DG} = 20V, V_{GS} = -12V	
	T_A = 150°C		500		500		500	nA		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	V_{DS} = 20V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Pulse width 300μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	V_{DS} = 20V, V_{GS} = 0	
$V_{DS(on)}$	Drain-Source ON Voltage						2	V	V_{GS} = 0	I_D = 5 mA
					1.5					I_D = 10 mA
			1							I_D = 20 mA
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA	
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		6		6		6		V_{DS} = 0, V_{GS} = -12V	
t_d	Turn-On Delay Time		10		15		40	ns	V_{DD} = 10V, $V_{GS(on)}$ = 0	
t_r	Rise Time		10		15		40		$I_{D(on)}$ / $V_{GS(off)}$ / R_L	
t_{off}	Turn-Off Time		30		60		100		2N3970: 20 mA / -10V / 450Ω	
									2N3971: 10 mA / -5V / 850Ω	
									2N3972: 5 mA / -3V / 1.6KΩ	



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

2N3993, 2N3994
P-Channel JFET

FEATURES

- Low $r_{DS(on)}$
- High Y_{fs}/C_{iss} Ratio (High-Frequency Figure-of-Merit)

APPLICATIONS

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ±10 VAC. Can be driven direct from T^2L or CMOS logic.

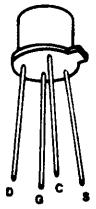
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

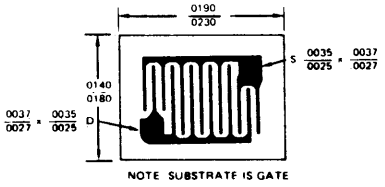
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5508



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3993	2N3993/W	2N3993/D
2N3994	2N3994/W	2N3994/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

SYMBOL	PARAMETER	2N3993		2N3994		UNIT	TEST CONDITIONS (Note 3)
		MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	25		25		V	I_G = 1 μA, V_{DS} = 0
I_{DGO}	Drain Reverse Current		-1.2		-1.2	nA	V_{DG} = -15 V, I_S = 0
			-1.2		-1.2	μA	V_{DG} = -15 V, I_S = 0, T_A = 150°C
I_{DSS}	Zero-Gate-Voltage Drain Current	-10		-2		mA	V_{DS} = -10 V, V_{GS} = 0, (See Note 1)
$I_{D(off)}$	Drain Cutoff Current				-1.2	nA	V_{DS} = -10 V, V_{GS} = 6 V
					-1	μA	V_{DS} = -10 V, V_{GS} = 6 V, T_A = 150°C
			-1.2			nA	V_{DS} = -10 V, V_{GS} = 10 V
			-1			μA	V_{DS} = -10 V, V_{GS} = 10 V, T_A = 150°C
$V_{GS(off)}$	Gate-Source Voltage	4	9.5	1	5.5	V	V_{DS} = -10 V, I_D = -1 μA
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance		150		300	Ω	V_{GS} = 0, I_D = 0, f = 1 kHz
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	6	12	4	10	mmho	V_{DS} = -10 V, V_{GS} = 0, f = 1 kHz, (See Note 1)
C_{iss}	Common-Source Short-Circuit Input Capacitance		16		16	pF	V_{DS} = -10 V, V_{GS} = 0, f = 1 MHz, (See Note 2)
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance				5	pF	V_{DS} = 0, V_{GS} = 6 V, f = 1 MHz
			4.5			pF	V_{DS} = 0, V_{GS} = 10 V, f = 1 MHz

NOTES: 1. These parameters must be measured using pulse techniques. t_p = 100 ms, duty cycle ≤ 10%.
2. This parameter must be measured with bias voltage applied for less than 5 seconds to avoid overheating.
3. The case should be connected to the source for all measurements.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

Dielectrically Isolated Dual NPN Transistor

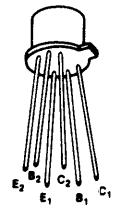
1

FEATURES

- **High Gain at Low Current**
- **Low Output Capacitance**
- **Good h_{FE} Match**
- **Tight V_{BE} Tracking**
- **Dielectrically Isolated Matched Pairs for Differential Amplifiers.**

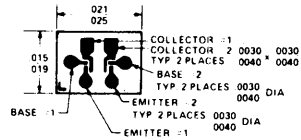
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4000



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)
- 2N4044, 2N4878 ..... 60V
- 2N4100, 2N4879 ..... 55V
- 2N4045, 2N4880 ..... 45V

Collector-Collector Voltage 100V
Emitter-Base Voltage (Note 2) 7V
Collector Current (Note 1) ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C (mW/°C)	1.7	2.9	2.3	4.3

ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200	600	150	600	80	800		I_C = 10 μA, V_{CE} = 5V
		225		175		100			I_C = 1.0 mA, V_{CE} = 5 V
	T_A = -55°C	75		50		30		V	I_C = 10 μA, V_{CE} = 5 V
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		I_C = 1.0 mA, I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45 V, 30 V*
	T_A = 150°C		0.1		0.1		0.1*	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5 V
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	I_E = 0, V_{CB} = 5 V

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
C_{te}	Emitter Transition Capacitance		1		1		1	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C_1, C_2}	Collector to Collector Capacitance		0.8		0.8		0.8	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		5		5		5	pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		55		45		V	$I_C = 1mA$, $I_B = 0$
f_t	Current Gain Bandwidth Product	200		150		150		MHz	$I_C = 1mA$, $V_{CE} = 10V$
f_t	Current Gain Bandwidth Product	20		15		15		MHz	$I_C = 10\mu A$, $V_{CE} = 10V$
NF	Narrow Band Noise Figure		2		3		3	dB	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_G = 10$ kohms, f = 1kHz, BW = 200 Hz
BV_{CBO}	Collector Base Breakdown Voltage	60		55		45		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		V	$I_E = 10\mu A$, $I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A$ to 1mA, $V_{CE} = 5V$
$\lvert V_{BE_1}-V_{BE_2}\rvert$	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\mu A$, $V_{CE} = 5V$
$\lvert I_{B_1}-I_{B_2}\rvert$	Base Current Differential		5		10		25	nA	$I_C = 10\mu A$, $V_{CE} = 5V$
$\lvert\Delta(V_{BE_1}-V_{BE_2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10	μV/°C	$I_C = 10\mu A$, $V_{CE} = 5V$, $T_A = -55°C$ to $+125°C$
$\lvert\Delta(I_{B_1}-I_{B_2})\rvert/\Delta T$	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	

SMALL SIGNAL CHARACTERISTICS

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	ohms	$I_C = 1mA$, $V_{CB} = 5V$
h_{rb}	Voltage Feedback Ratio	43	x 10^{-3}	
h_{fe}	Small Signal Current Gain	250		$I_C = 1mA$, $V_{CE} = 5V$
h_{ob}	Output Conductance	60	μmhos	
h_{ie}	Input Resistance	9.6	k ohms	
h_{re}	Voltage Feedback Ratio	42	x 10^{-3}	
h_{oe}	Output Conductance	12	μmhos	

NOTES:
1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μamps.
3. The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

ITE4091-ITE4093
2N4091-2N4093, JANTX*
N-Channel JFET

1

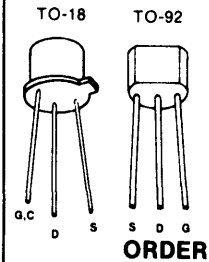
FEATURES
- **Low $r_{DS(on)}$**
- **$I_{D(OFF)}$ < 100 pA (JAN TX Types)**
- **Fast Switching**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

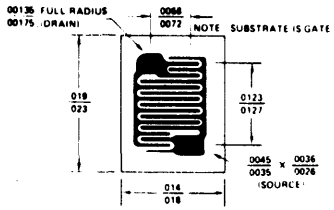
Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	TO-18	TO-92
Power Dissipation	1.8W	360 mW
Derate above 25°C	1.7 mW/°C ..	3.0 mW/°C

PIN CONFIGURATIONS



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	TO-18†	WAFER	DICE
ITE 4091	2N4091	2N4091/W	2N4091/D
ITE 4091A	2N4091A		
ITE 4092	2N4092	2N4092/W	2N4092/D
ITE 4092A	2N4092A		
ITE 4093	2N4093	2N4093/W	2N4093/D
ITE 4093A	2N4093A		

†add JANTX to these part numbers if JANTX processing is desired.

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N/ITE 4091		2N/ITE 4092		2N/ITE 4093		Unit	Test Conditions	
		Min.	Max.	Min.	Max.	Min.	Max.			
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1μA, V_{DS} = 0	
I_{DGO}	Drain Reverse Current		200		200		200	pA		
	(Not JANTX Specified) T_A = 150°C		400		400		400	nA	V_{GD} = -20V, I_S = 0	
I_{GSS}	Gate Reverse Current		-100		-100		-100	pA		
	(JANTX, ITE devices only); T_A = 150°C		-200		-200		-200	nA	V_{GS} = -20V, V_{DS} = 0	
$I_{D(OFF)}$	JANTX; T_A = 25°C		100		100		100	pA	V_{DS} = 20V	V_{GS} = -12V (4091)
			200		200		200			V_{GS} = -8V (4092)
										V_{GS} = -6V (4093)
	Drain Cutoff Current		200		200		200			
	JANTX, T_A = 150°C		400		400		400	nA		
V_P	Gate-Source Pinch-Off Voltage	-5	-10	-2	-7	-1	-5	V	V_{DS} = 20V, I_D = 1 nA	
I_{DSS}	Drain Current at Zero Gate Voltge	30		15		8		mA	V_{DS} = 20V, V_{GS} = 0, Pulse Test Duraton = 2 ms	
$V_{DS(ON)}$	Drain-Source ON Voltage						0.2	V	V_{GS} = 0	I_D = 2.5 mA
					0.2					I_D = 4 mA
			0.2							I_D = 6.6 mA
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	V_{GS} = 0, I_D = 1 mA	
$r_{ds(on)}$	Static Drain Source ON Resistance		30		50		80	Ω	V_{GS} = 0, I_D = 0, f = 1 kHz	
C_{iss}	Common-Source Input Capacitance		16		16		16	pF	V_{DS} = 20V, V_{GS} = 0, f = 1 MHz	
C_{rss}	JANTX Only		5		5		5			
	Common-Source Reverse Transfer Capacitance		5		5		5		V_{DS} = 0, V_{GS} = -20V, f = 1 MHz	
$t_{d(ON)}$	Turn-ON Delay Time		15		15		20	ns	V_{DD} = 3V, $V_{GS(ON)}$ = 0	
t_r	Rise Time		10		20		40			
t_{off}	Turn-OFF Time		40		60		80			

	$I_{D(on)}$	$V_{GS(off)}$	R_1
4091	6.6 mA	-12V	425Ω
4092	4 mA	-8V	700Ω
4093	2.5 mA	-6V	1120Ω

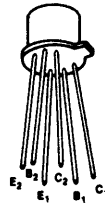
2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor

FEATURES

- **High Gain at Low Current**
- **Low Output Capacitance**
- **Good h_{FE} Match**
- **Tight V_{BE} Tracking**
- **Dielectrically Isolated Matched Pairs for Differential Amplifiers.**

PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

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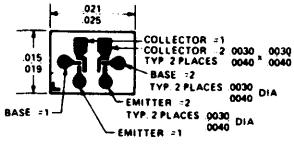


ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)
- 2N4044, 2N4878 ..... 60V
- 2N4100, 2N4879 ..... 55V
- 2N4045, 2N4880 ..... 45V

Collector-Collector Voltage 100V
Emitter-Base Voltage (Note 2) 7V
Collector Current (Note 1) ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C (mW/°C)	1.7	2.9	2.3	4.3

ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200	600	150	600	80	800	V	I_C = 10 μA, V_{CE} = 5V
		225		175		100			I_C = 1.0 mA, V_{CE} = 5 V
	T_A = -55°C	75		50		30			I_C = 10 μA, V_{CE} = 5 V
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		I_C = 1.0 mA, I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45 V, 30 V*
	T_A = 150°C		0.1		0.1		0.1*	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5 V
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	I_E = 0, V_{CB} = 5 V

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
C_{te}	Emitter Transition Capacitance		1		1		1	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C_1, C_2}	Collector to Collector Capacitance		0.8		0.8		0.8	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		5		5		5	pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		55		45		V	$I_C = 1mA$, $I_B = 0$
f_t	Current Gain Bandwidth Product	200		150		150		MHz	$I_C = 1mA$, $V_{CE} = 10V$
f_t	Current Gain Bandwidth Product	20		15		15		MHz	$I_C = 10\mu A$, $V_{CE} = 10V$
NF	Narrow Band Noise Figure		2		3		3	dB	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_G = 10$ kohms, f = 1kHz, BW = 200 Hz
BV_{CBO}	Collector Base Breakdown Voltage	60		55		45		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		V	$I_E = 10\mu A$, $I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A$ to 1mA, $V_{CE} = 5V$
$\lvert V_{BE_1}\text{-}V_{BE_2}\rvert$	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\mu A$, $V_{CE} = 5V$
$\lvert I_{B_1}\text{-}I_{B_2}\rvert$	Base Current Differential		5		10		25	nA	$I_C = 10\mu A$, $V_{CE} = 5V$
$\lvert\Delta(V_{BE_1}\text{-}V_{BE_2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10	$\mu V/°C$	$I_C = 10\mu A$, $V_{CE} = 5V$, $T_A = -55°C$ to $+125°C$
$\lvert\Delta(I_{B_1}\text{-}I_{B_2})\rvert/\Delta T$	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	

SMALL SIGNAL CHARACTERISTICS

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	ohms	$I_C = 1mA$, $V_{CB} = 5V$
h_{rb}	Voltage Feedback Ratio	43	x 10^{-3}	
h_{fe}	Small Signal Current Gain	250		$I_C = 1mA$, $V_{CE} = 5V$
h_{ob}	Output Conductance	60	μmhos	
h_{ie}	Input Resistance	9.6	k ohms	
h_{re}	Voltage Feedback Ratio	42	x 10^{-3}	
h_{oe}	Output Conductance	12	μmhos	

NOTES:
1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μamps.
3. The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

2N4117-19, 2N4117A-19A
N-Channel JFET

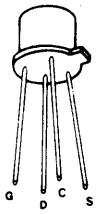
FEATURES
- **Low Leakage**
- **Low Capacitance**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

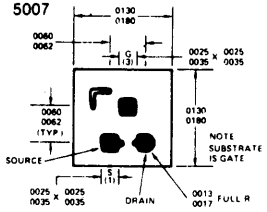
Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 1.7 mW/°c

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	—	—
2N4118	2N4118/W	2N4118/D
2N4118A	—	—
2N4119	2N4119/W	2N4119/D
2N4119A	—	—

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0
I_{GSSR}	Gate Reverse Current		-10		-10		-10	pA	V_{GS} = -20 V, V_{DS} = 0
	A devices		-1		-1		-1		
	T_A = +100°C		-25		-25		-25	nA	
	A devices		-2.5		-2.5		-2.5		
V_{GS} (off)	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V	V_{DS} = 10 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	V_{DS} = 10 V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μmho	V_{DS} = 10 V, f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	60		70		90			V_{GS} = 0, f = 30 MHz
g_{os}	Common-Source Output Conductance		3		5		10		V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		3		3		3	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5		V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz

NOTE: 1. Pulse test: Pulse duration of 2 ms used during test.

2N4220-2N4222
N-Channel JFET

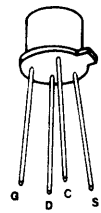
FEATURES
- C_{rss} < 2 pF
- Moderately High Forward Transconductance

1

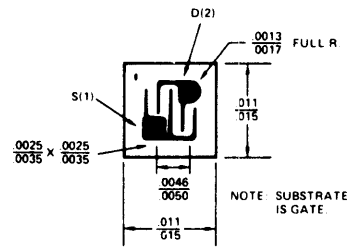
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -30V
Gate Current ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 1.7 mW/°C

PIN CONFIGURATION
TO-72



CHIP TOPOGRAPHY
5010*



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4220		2N4221		2N4222		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
	T_A = 150°C		-0.1		-0.1		-0.1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		V_{DS} = 15 V, I_D = 0.1 nA	
V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V	V_{DS} = 15V | I_D = 50 μA (2N4220); I_D = 200 μA (2N4221); I_D = 500 μA (2N4222)	
I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	2000	5000	2500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
$\|y_{fs}\|$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 1)		10		20		40			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			

NOTE 1: Pulse test duration 2 ms.

2N4223, 2N4224
N-Channel JFET

FEATURES

- **NF = 3 dB Typical at 200 MHz**
- **C_{rss} < 2 pF**

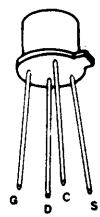
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -30V
Gate Current ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 1.7 mW/°C

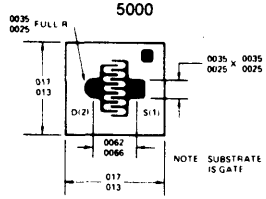
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5000



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4223	2N4223/W	2N4223/D
2N4224	2N4224/W	2N4224/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4223 MIN	2N4223 MAX	2N4224 MIN	2N4224 MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
	T_A = +150°C		-0.25		-0.5	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15V	I_D = 0.25 nA (2N4223) I_D = 0.5 nA (2N4224)
V_{GS}	Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5	V	V_{DS} = 15V	I_D = 0.3 mA (2N4223) I_D = 0.2 mA (2N4224)
I_{DSS}	Saturation Drain Current (Note 1)	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	3000	7000	2000	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
$\|Y_{fs}\|$	Common-Source Forward Transadmittance	2700		1700		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
G_{ps}	Small Signal Power Gain	10						
NF	Noise Figure		5			dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1kΩ	f = 200 MHz

Note 1: Pulse test, duration 2 msec.

2N4338-2N4341
N-Channel JFET

FEATURES

- **Exceptionally High Figure of Merit**
- **Radiation Immunity**
- **Extremely Low Noise and Capacitance**
- **High Input Impedance**

APPLICATIONS

- Low-level Choppers
- Data Switches
- Multiplexers and Low Noise Amplifiers

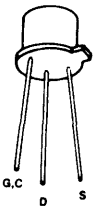
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -50V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 1.7 mW/°C

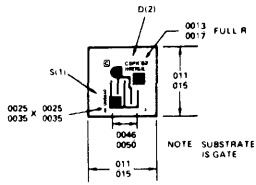
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5040



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N4338	2N4338/W	2N4338/D
2N4339	2N4339/W	2N4339/D
2N4340	2N4340/W	2N4340/D
2N4341	2N4341/W	2N4341/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4338		2N4339		2N4340		2N4341		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
	T_A = 150°C		-0.1		-0.1		-0.1		-0.1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 15 V, I_D = 0.1 μA	
$I_{D(off)}$	Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	V_{DS} = 15V, V_{GS} = ( )	
I_{DSS}	Saturation Drain Current	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	600	1800	800	2400	1300	3000	2000	4000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		5		15		30		60			
$r_{DS(on)}$	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, I_{DS} = 0	
C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

INTERSIL

2N4351
N-Channel Enhancement Mode MOS FET

FEATURES

- **Low ON Resistance**
- **Low Capacitance**
- **High Gain**
- **High Gate Breakdown Voltage**
- **Low Threshold Voltage**

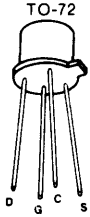
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source Voltage or Drain-Gate Voltage	25V
Peak Gate-Source Voltage (Note 1)	±125V
Drain Current	100 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3 mW/°C

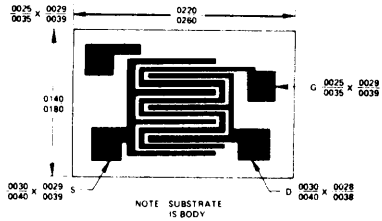
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1003



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4351	2N4351/W	2N4351/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-Source Breakdown Voltage	25		V	I_D = 10 μA, V_{GS} = 0
I_{GSS}	Gate Leakage Current		10	pA	V_{GS} = ±30 V, V_{DS} = 0
I_{DSS}	Zero-Gate-Voltage Drain Current		10	nA	V_{DS} = 10 V, V_{GS} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	1	5	V	V_{DS} = 10 V, I_D = 10 μA
$I_{D(on)}$	"ON" Drain Current	3		mA	V_{GS} = 10 V, V_{DS} = 10 V
$V_{DS(on)}$	Drain-Source "ON" Voltage		1	V	I_D = 2 mA, V_{GS} = 10 V
$r_{DS(on)}$	Drain-Source Resistance		300	ohms	V_{GS} = 10 V, I_D = 0, f = 1 kHz
$\|y_{fs}\|$	Forward Transfer Admittance	1000		μmho	V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz
C_{rss}	Reverse Transfer Capacitance		1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 140 kHz
C_{iss}	Input Capacitance		5.0		V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz
$C_{d(sub)}$	Drain-Substrate Capacitance		5.0		$V_{D(SUB)}$ = 10 V, f = 140 kHz
$t_{d(on)}$	Turn-On Delay		45	ns	FIGURE 1 - SWITCHING CIRCUIT and WAVEFORMS
t_r	Rise Time		65		
$t_{d(off)}$	Turn-Off Delay		60		
t_f	Fall Time		100		

Note 1. Device must not be tested at ±125V more than once or longer than 300 ms.

ITE4391-ITE4393
2N4391-2N4393
N-Channel JFET

FEATURES

- $r_{ds(on)}$ < 30 ohms (2N4391)
- $I_{D(off)}$ < 100 pA
- Switches ±10 VAC with ±15V Supplies (2N4392, 2N4393)

ABSOLUTE MAXIMUM RATINGS

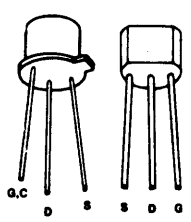
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	TO-18	TO-92
Power Dissipation	1.8W	360 mW
Derate above 25°C	1.7 mW/°C	3.0 mW/°C

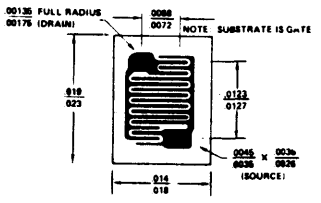
PIN CONFIGURATIONS

TO-18 TO-92



CHIP TOPOGRAPHY

5001



ORDERING INFORMATION*

TO-92	TO-18	WAFER	DICE
ITE 4391	2N4391	2N4391/W	2N4391/D
ITE 4392	2N4392	2N4392/W	2N4392/D
ITE 4393	2N4393	2N4393/W	2N4393/D

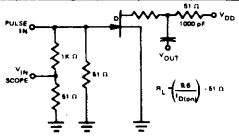
*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		4391 MIN	4391 MAX	4392 MIN	4392 MAX	4393 MIN	4393 MAX	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0
	T_A = 150°C		-200		-200		-200	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = 1 μA, V_{DS} = 0
$I_{D(off)}$	Drain Cutoff Current		100		100		100	pA	V_{DS} = 20 V; V_{GS} = -5 V (4393), V_{GS} = -7 V (4392), V_{GS} = -12 V (4391)
	T_A = 150°C		200		200		200	nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0
$V_{DS(on)}$	Drain Source ON Voltage		0.4		0.4		0.4	V	V_{GS} = 0; I_D = 3 mA (4393), I_D = 6 mA (4392), I_D = 12 mA (4391)
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0; V_{GS} = -5 V
					3.5				V_{GS} = -7 V
			3.5						V_{GS} = -12 V
t_d	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0
t_r	Rise Time		5		5		5		
t_{off}	Turn-OFF Delay Time		20		35		50		
t_f	Fall Time		15		20		30		

	$I_{D(on)}$	$V_{GS(off)}$
4391	12 mA	-12 V
4392	6	-7
4393	3	-5

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%



INPUT PULSE
RISE TIME ≤ 0.5 ns
FALL TIME ≤ 0.5 ns
PULSE DUTY CYCLE 1%

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 50 Ω

ITE4416, 2N4416/A
N-Channel JFET

FEATURES

- **Low Noise**
- **Low Feedback Capacitance**
- **Low Output Capacitance**
- **High Transconductance**
- **High Power Gain**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage
- 2N4416, ITE4416 ..... -30V
- 2N4416A ..... -35V

Gate Current ..... 10 mA

Storage Temperature Range
- 2N4416/2N4416A ..... -65°C to +200°C
- ITE4416 ..... -55°C to +125°C

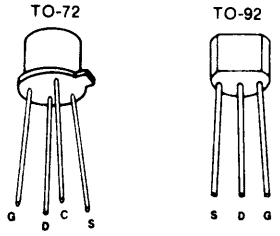
Operating Temperature Range
- 2N4416/2N4416A ..... -65°C to +200°C
- ITE4416 ..... -55°C to +125°C

Lead Temperature (Soldering, 10 sec.) ..... +300°C

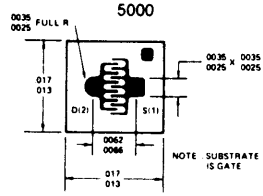
Power Dissipation ..... 300 mW

Derate above 25°C .....
- 2N4416/2N4416A ..... 1.7 mW/°C
- ITE4416 ..... 3.0 mW/°C

PIN CONFIGURATIONS



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	TO-72	WAFER	DICE
ITE 4416	2N4416	2N4416/W	2N4416/D
—	2N4416A	2N4416A/W	2N4416A/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER			MIN	MAX	UNIT	TEST CONDITIONS	
$V_{GS(f)}$	Gate- Source Forward Voltage			1	V	I_G = 1 mA, V_{DS} = 0	
I_{GSS}	Gate Reverse Current			-0.1	nA	V_{GS} = -20 V, V_{DS} = 0	
		T_A = 150°C		-0.1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	2N4416/ITE4416	-30		V	I_G = -1 μA, V_{DS} = 0	
		2N4416A	-35				
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N4416/ITE4416		-6		V_{DS} = 15 V, I_D = 1 nA	
		2N4416A	-2.5	-6			
I_{DSS}	Drain Current at Zero Gate Voltage		5	15	mA	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance		4500	7500	μmho		
g_{os}	Common-Source Output Conductance			50	μmho		
C_{rss}	Common-Source Reverse Transfer Capacitance			0.8	pF		
C_{iss}	Common-Source Input Capacitance			4	pF		f = 1 MHz
C_{oss}	Common-Source Output Capacitance			2			

PARAMETER		100 MHz		400 MHz		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
b_{iss}	Common-Source Input Susceptance		2500		10,000		
g_{oss}	Common-Source Output Conductance		75		100		
b_{oss}	Common-Source Output Susceptance		1000		4000		
g_{fs}	Common-Source Forward Transconductance			4000			
G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
NF	Noise Figure		2		4		V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ

2N4856-2N4861
2N4856-2N4858 JAN, JTX, JTXV*
N-Channel JFET

1

FEATURES

- Low $r_{DS(on)}$
- $I_{D(off)}$<250 pA
- Switches ±10V Signals with ±15V Supplies (2N4858, 2N4861)

ABSOLUTE MAXIMUM RATINGS

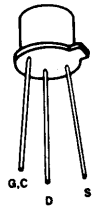
(T_A = 25° C unless otherwise noted)

Gate-Source or Gate-Drain Voltage
- 2N4856-58 ..... -40V
- 2N4859-61 ..... -30V

Gate Current ..... 50 mA
Storage Temperature ..... -65° C to +200° C
Operating Temperature Range ... -55° C to +150° C
Led Temperature (Soldering, 10 sec.) .... +300° C
Power Dissipation 1.8W
Derate above 25° C ..... 10 mW/° C

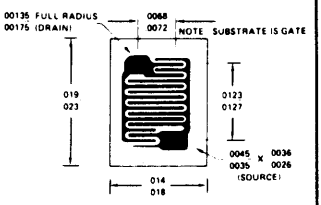
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5001



ORDERING INFORMATION*

TO-18	WAFER	DICE
2N4856 †	2N4856/W	2N4856/D
2N4857 †	2N4857/W	2N4857/D
2N4858 †	2N4858/W	2N4858/D
2N4859	2N4859/W	2N4859/D
2N4860	2N4860/W	2N4860/D
2N4861	2N4861/W	2N4861/D

† add JAN, JTX, JTXV, to basic part number to specify these devices.

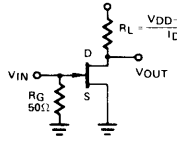
*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

(25° C unless otherwise noted)

PARAMETER			2N4856,59 MIN	2N4856,59 MAX	2N4857,60 MIN	2N4857,60 MAX	2N4858,61 MIN	2N4858,61 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
		2N4859-61	-30		-30		-30				
I_{GSSR}	Gate Reverse Current			-250		-250		-250	pA	V_{GS} = -20 V, V_{DS} = 0	
		T_A = 150° C		-500		-500		-500	nA	V_{GS} = -15 V, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	V_{DS} = 15 V, V_{GS} = -10 V	
		T_A = 150° C		500		500		500	nA		
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	V_{DS} = 15 V, I_D = 0.5 nA	
I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	V_{DS} = 15 V, V_{GS} = 0	
$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	V_{GS} = 0, I_D = ( )	
$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance			18		18		18	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
t_d	Turn-ON Delay Time			6		6		10	ns	V_{DD} = 10 V, R_L = 464 Ω (2N4856,59) 953 Ω (2N4857,60) 1910 Ω (2N4858,61); $V_{GS(on)}$ = 0; $V_{GS(off)}$ = -10V, I_D = 20 mA (2N4856, 9); $V_{GS(off)}$ = -6V, I_D = 10 mA (2N4857, 60); $V_{GS(off)}$ = -4V, I_D = 5 mA (2N4858, 61)	
t_r	Rise Time			3		4		10			
t_{off}	Turn-OFF Time			25		50		100			

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 100 ns
PULSE DUTY CYCLE ≤ 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pf

2N4867/A-2N4869/A
N-Channel JFET

FEATURES

- **Low Noise Voltage**
- **Low Leakage**
- **High Gain**

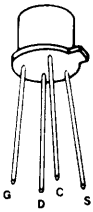
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec. ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 1.7 mW/°c

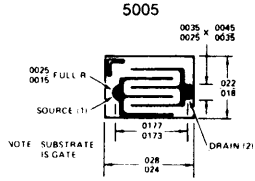
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5005



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0	
	T_A = 150°C		-0.25		-0.25		-0.25	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20 V, I_D = 1 μA	
I_{DSS}	Saturation Drain Current (Note 1)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		1.5		4		10			
C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25		25		25			
$\bar{e}_n$	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/√Hz	V_{DS} = 10 V, V_{GS} = 0	f = 10 Hz
			10		10		10			f = 1KHz
	A devices		10		10		10			f = 10 Hz
			5		5		5			f = 1 kHz
NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0 R_{gen} = 20K, (2N4867 Series) R_{gen} = 5K, (2N4867A Series)	f = 1 kHz

NOTE: 1. Pulse test duration = 2 ms.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor

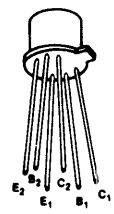
1

FEATURES

- **High Gain at Low Current**
- **Low Output Capacitance**
- **Good h_{FE} Match**
- **Tight V_{BE} Tracking**
- **Dielectrically Isolated Matched Pairs for Differential Amplifiers.**

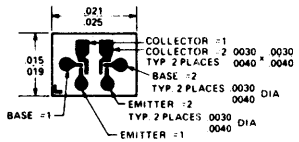
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4000



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)
- 2N4044, 2N4878 ..... 60V
- 2N4100, 2N4879 ..... 55V
- 2N4045, 2N4880 ..... 45V

Collector-Collector Voltage 100V
Emitter-Base Voltage (Note 2) 7V
Collector Current (Note 1) ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C (mW/°C)	1.7	2.9	2.3	4.3

ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200	600	150	600	80	800		I_C = 10 μA, V_{CE} = 5V
		225		175		100			I_C = 1.0 mA, V_{CE} = 5 V
	T_A = -55°C	75		50		30		V	I_C = 10 μA, V_{CE} = 5 V
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		I_C = 1.0 mA, I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45 V, 30 V*
	T_A = 150°C		0.1		0.1		0.1*	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5 V
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	I_E = 0, V_{CB} = 5 V

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
C_{te}	Emitter Transition Capacitance		1		1		1	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C_1, C_2}	Collector to Collector Capacitance		0.8		0.8		0.8	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		5		5		5	pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		55		45		V	I_C = 1mA, $I_B = 0$
f_t	Current Gain Bandwidth Product	200		150		150		MHz	I_C = 1mA, V_{CE} = 10V
f_t	Current Gain Bandwidth Product	20		15		15		MHz	I_C = 10μA, V_{CE} = 10V
NF	Narrow Band Noise Figure		2		3		3	dB	I_C = 10μA, V_{CE} = 5V, R_G = 10 kohms; f = 1kHz, BW = 200 Hz
BV_{CBO}	Collector Base Breakdown Voltage	60		55		45		V	I_C = 10μA, $I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		V	I_E = 10μA, $I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		I_C = 10μA to 1mA, V_{CE} = 5V
$\lvert V_{BE_1}-V_{BE_2}\rvert$	Base Emitter Voltage Differential		3		5		5	mV	I_C = 10μA, V_{CE} = 5V
$\lvert I_{B_1}-I_{B_2}\rvert$	Base Current Differential		5		10		25	nA	I_C = 10μA, V_{CE} = 5V
$\lvert\Delta(V_{BE_1}-V_{BE_2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10	μV/°C	I_C = 10μA, V_{CE} = 5V, T_A = −55°C to +125°C
$\lvert\Delta(I_{B_1}-I_{B_2})\rvert/\Delta T$	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	

SMALL SIGNAL CHARACTERISTICS

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	ohms	I_C = 1mA, V_{CB} = 5V
h_{rb}	Voltage Feedback Ratio	43	x 10^{-3}	
h_{fe}	Small Signal Current Gain	250		I_C = 1mA, V_{CE} = 5V
h_{ob}	Output Conductance	60	μmhos	
h_{ie}	Input Resistance	9.6	k ohms	
h_{re}	Voltage Feedback Ratio	42	x 10^{-3}	
h_{oe}	Output Conductance	12	μmhos	

NOTES:
1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μamps.
3. The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

2N5018, 2N5019
P-Channel JFET

FEATURES
- **Low Insertion Loss**
- **No Offset or Error Voltages Generated by Closed Switch**
- **Purely Resistive**

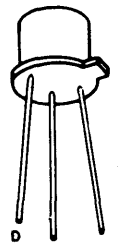
APPLICATIONS
- Analog Switches
- Commutators
- Choppers

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ... +300°C
Power Dissipation ..... 500 mW
Derate above 25°C ..... 3 mW/°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

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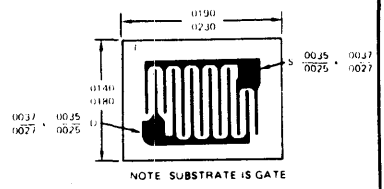


ORDERING INFORMATION*

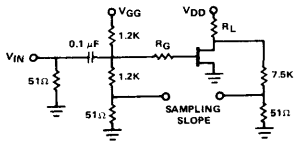
TO-18	WAFER	DICE
2N5018	2N5018/W	2N5018/D
2N5019	2N5019/W	2N5019/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		2N5018 Min	2N5018 Max	2N5019 Min	2N5019 Max	Unit	Test Conditions
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0
I_{GSSR}	Gate Reverse Current		2		2	nA	V_{GS} = 15 V, V_{DS} = 0
$I_{D(off)}$	Drain Cutoff Current		-10		-10	nA	V_{DS} = -15 V, V_{GS} = 12 V (2N5018)
	T_A = 150°C		-10		-10	μA	V_{DS} = -15 V, V_{GS} = 7 V (2N5019)
I_{DGO}	Drain Reverse Current		-2		-2	nA	V_{DG} = -15 V, I_S = 0
	T_A = 150°C		-3		-3	μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	V_{DS} = -15 V, I_D = -1 μA
I_{DSS}	Saturation Drain Current	-10		-5		mA	V_{DS} = -20 V, V_{GS} = 0
$V_{DS(on)}$	Drain-Source ON Voltage		-0.5		-0.5	V	V_{GS} = 0, I_D = -6 mA (2N5018), I_D = -3 mA (2N5019)
$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	I_D = -1 mA, V_{GS} = 0
$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	I_D = 0, V_{GS} = 0, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		45		45	pF	V_{DS} = -15 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		10		10	pF	V_{DS} = 0, V_{GS} = 12 V (2N5018), V_{GS} = 7 V (2N5019), f = 1 MHz
$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = -6 V, $V_{GS(on)}$ = 0
t_r	Rise Time		20		75	ns	
$t_{d(off)}$	Turn-Off Delay Time		15		25	ns	2N5018: $V_{GS(off)}$ 12 V, $I_{D(on)}$ -6 mA, R_L 910Ω
t_f	Fall Time		50		100	ns	2N5019: $V_{GS(off)}$ 7V, $I_{D(on)}$ -3 mA, R_L 1.8KΩ

NOTE 1: Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 100 ns
REPLETION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

2N5114-2N5116 JAN, JTX P-Channel JFET

1

FEATURES

- **Low ON Resistance**
- **$I_{D(off)}$ < 500 pA**
- **Switches directly from T^2L Logic**

GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and ±10 VAC signals can be handled using only +5V logic (T^2L or CMOS).

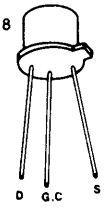
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

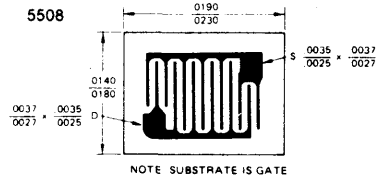
Gate-Drain or Gate-Source Voltage 30V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ... +300°C
Power Dissipation ..... 500 mW
Derate above 25°C ..... 3 mW/°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY



NOTE SUBSTRATE IS GATE

ORDERING INFORMATION*

TO18 †	WAFER	DICE
2N5114	2N5114/W	2N5114/D
2N5115	2N5115/W	2N5115/D
2N5116	2N5116/W	2N5116/D

†add JAN, JTX to basic part number to specify these devices

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

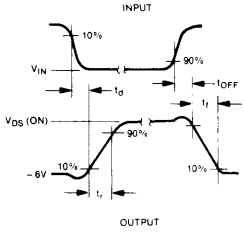
PARAMETER		2N5114		2N5115		2N5116		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 μA, V_{DS} = 0
I_{GSSR}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0
	T_A = 150°C		1.0		1.0		1.0	μA	
$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15 V, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V
	T_A = 150°C		-1.0		-1.0		-1.0	μA	
V_P	Gate-Source Pinch-Off Voltage	5	10	3	6	1	4	V	V_{DS} = -15 V, I_D = -1 nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	-30	-90	-15	-60	-5	-25	mA	V_{GS} = 0, V_{DS} = 2N5114 = -18 V, 2N5115 = -15 V, 2N5116 = -15 V
V_{GSSF}	Forward Gate Source Voltage		-1		-1		-1	V	I_G = -1 mA, V_{DS} = 0
$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6	V	V_{GS} = 0, I_D = 2N5114 = -15 mA, 2N5115 = - 7 mA, 2N5116 = - 3 mA
$r_{DS(on)}$	Static Drain-Source ON Resistance		75		100		150	Ω	V_{GS} = 0, I_D = -1 mA
$r_{ds(on)}$	Small Signal Drain-Source ON Resistance		75		100		150	Ω	V_{GS} = 0, I_D = 0, f = 1 kHz
	Jan TX only		75		100		175	Ω	
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	V_{DS} = -15 V, V_{GS} = 0, f = 1 MHz
	Jan TX only		25		25		27	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7	pF	V_{DS} = 0, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V, f = 1 MHz

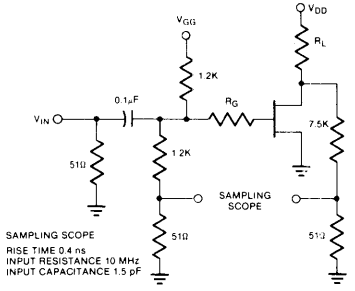
Note 1. Pulse test; duration = 2 ms.

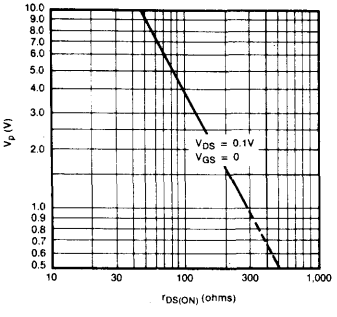
SWITCHING CHARACTERISTICS (25°C unless otherwise noted)

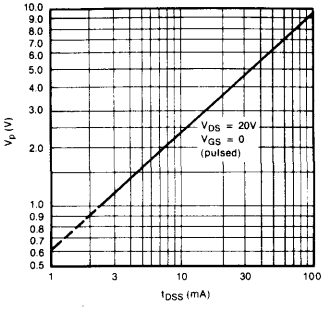
PARAMETER	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	UNIT
	MAX	MAX	MAX	MAX	MAX	MAX	
t_d Turn-ON Delay Time	6	10	12	6	10	25	
t_r Rise Time	10	20	30	10	20	35	ns
t_{off} Turn-OFF Delay Time	6	8	19	6	8	29	
t_f Fall Time	15	30	50	(not JAN TX specified)			

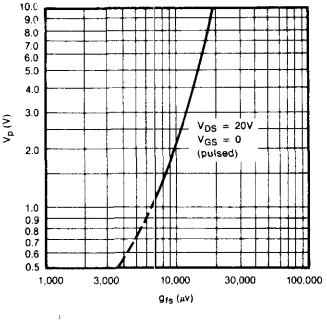
TEST CONDITIONS			
	2N5114	2N5115	2N5116
V_{DD}	−10V	−6V	−6V
V_{GG}	20V	12V	8V
R_L	430Ω	910Ω	2 KΩ
R_G	100Ω	220Ω	390Ω
$I_{D(ON)}$	−15mA	−7mA	−3mA
V_{IN}	−12V	−7V	−5V











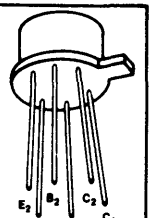
2N5117-2N5119 Dielectrically Isolated Dual PNP Transistor

FEATURES

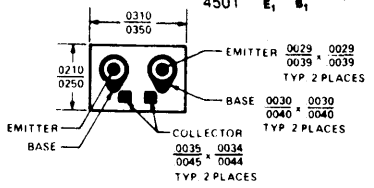
- **High Gain at Low Current**
- **Low Output Capacitance**
- **Good h_{FE} Match**
- **Tight V_{BE} Tracking**
- **Dielectrically Isolated Matched Pairs for Differential Amplifiers.**

PIN CONFIGURATION

TO-78



CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1) 45V
Emitter-Base Voltage (Notes 1 and 2) 7V
Collector-Collector Voltage 100V
Collector Current (Note 1) ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	400 mW	750 mW
Derate above 25°C	2.3 mW/°C	4.3 mW/°C

ORDERING INFORMATION*

TO-78	WAFER	DICE
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

*When ordering wafer/dice refer to Appendix B-23

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 2N5118 MIN	2N5117 2N5118 MAX	2N5119 MIN	2N5119 MAX	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	100	300	50			I_C = 10 μA, V_{CE} = 5.0 V
		100		50			I_C = 500 μA, V_{CE} = 5.0 V
	T_A = -55°C	30		20			I_C = 10 μA, V_{CE} = 5.0 V
I_{CBO}	Collector Cutoff Current		0.1		0.1	nA	I_E = 0, V_{CB} = 30 V
	T_A = 150°C		0.1		0.1	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1	nA	I_C = 0, V_{EB} = 5.0 V
$I_{C_1-C_2}$	Collector-Collector Leakage		5.0		5.0	pA	V_{CC} = 100 V
GBW	Current Gain Bandwith Product	100		100		MHz	I_C = 500 μA, V_{CE} = 10 V
C_{ob}	Output Capacitance		0.8		0.8	pF	I_E = 0, V_{CB} = 5.0 V
C_{te}	Emitter Transition Capacitance		1.0		1.0		I_C = 0, V_{EB} = 0.5 V
$C_{C_1-C_2}$	Collector-Collector Capacitance		0.8		0.8		V_{CC} = 0
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	45		45		V	I_C = 1.0 mA, I_B = 0
NF	Narrow Band Noise Figure		4.0		4.0	dB	I_C = 10 μA, V_{CE} = 5.0 V, BW = 200 Hz, f = 1 KHz, R_G = 10 KΩ
BV_{CBO}	Collector Base Breakdown Voltage	45		45		V	I_C = 10 μA, I_E = 0
BV_{EBO}	Emitter Base Breakdown Voltage	7.0		7.0		V	I_E = 10 μA, I_C = 0

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 MIN	2N5117 MAX	2N5118 MIN	2N5118 MAX	2N5119 MIN	2N5119 MAX	UNIT	TEST CONDITIONS	
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1.0						I_C = 10 μA to 500 μA, V_{CE} = 5 V	
				0.85	1.0	0.8	1.0		I_C = 10 μA, V_{CE} = 5.0 V	
$V_{BE_1}-V_{BE_2}$	Base-Emitter Voltage Differential		3.0					mV	I_C = 10 μA to 500 μA, V_{CE} = 5 V	
					5.0		5.0			
$I_{B_1}-I_{B_2}$	Base Current Differential		10.0		15		40	nA		
$\Delta(V_{BE_1}-V_{BE_2})/\Delta T$	Base Voltage Differential Change with Temperature		3.0		5.0		10	μV/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = -55°C to +125°C
$\Delta(I_{B_1}-I_{B_2})/\Delta T$	Base-Current Differential Change with Temperature		0.3		0.5		1.0	nA/°C		T_A = -55°C to +125°C

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA.
3. Lower of two h_{FE} readings is defined as h_{FE_1}.

2N5196-2N5199
Dual Monolithic N-Channel JFET

1

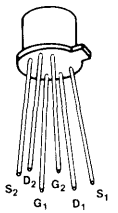
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDE
Power Dissipation	250 mW ...	500 mW
Derate above 25°C	2.6 mW/°C ..	4.3 mW/°C

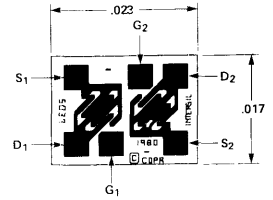
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

6037



ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
	T_A = 150°C		-50	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-3.8			
I_G	Gate Operating Current		-15	pA	V_{DG} = 20 V, I_D = 200 μA	
	T_A = 125°C		-15	nA		
I_{DSS}	Saturation Drain Current (Note 2)	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	700	**1600**		V_{DG} = 20 V, I_D = 200 μA	
g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
$\overline{e_n}$	Equivalent Input Noise Voltage		20	$\frac{\mu nV}{\sqrt{Hz}}$		f = 1 kHz

PARAMETER		2N5196		2N5197		2N5198		2N5199		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 2)	0.95	1	0.95	1	0.95	1	0.95	1		V_{DS} = 20 V, V_{GS} = 0 V	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	0.97	1	0.97	1	0.95	1	0.95	1		V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 3)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			5		10		20		40			T_A = -55°C, T_B = 25°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

NOTES: 1. Per transistor.
2. Pulse test required, pulsewidth = 300 μs, duty cycle < 3%.
3. Measured at endpoints T_A and T_B.

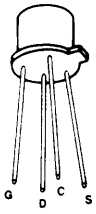
2N5397, 2N5398
N-Channel JFET

FEATURES

- G_{ps} = 15 dB Minimum (Common Gate) at 450 MHz
- Low Noise
- Low Capacitance

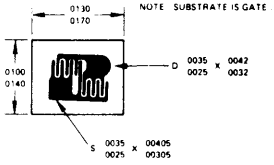
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5011



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N5397	2N5397/W	2N5397/D
2N5398	2N5398/W	2N5398/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5397		2N5398		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
	T_A = +150°C		-0.1		-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		V	V_{DS} = 0, I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-6.0	-1.0	-6.0	V	V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	**Saturation Drain Current (Note 1)**	10	30	5	40	mA	V_{DS} = 10 V, V_{DS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1	V	V_{DS} = 0, I_G = 1 mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	6000	10,000			μmho	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
				5500	10,000		V_{DS} = 10 V, V_{GS} = 0	
g_{oss}	Common-Source Output Conductance		200				V_{DS} = 10 V, I_D = 10 mA	
					400		V_{DS} = 10 V, V_{GS} = 0	
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			pF	V_{DS} = 10 V, I_D = 10 mA	f = 1 MHz
					1.3		V_{DS} = 10 V, V_{GS} = 0	
C_{iss}	Common-Source Input Capacitance		5.0				V_{DG} = 10 V, I_D = 10 mA	
					5.5		V_{DS} = 10 V, V_{GS} = 0	
g_{iss}	Common-Source Input Conductance		2000			μmho	V_{DG} = 10 V, I_D = 10 mA	f = 450 MHz
					3000		V_{DG} = 10 V, V_{GS} = 0	
g_{oss}	Common-Source Output Conductance		400				V_{DG} = 10 V, I_D = 10 mA	
					500		V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	5500	9000				V_{DG} = 10 V, I_D = 10 mA	
				5000	10,000		V_{DS} = 10 V, V_{GS} = 0	
G_{ps}	Common-Source Power Gain (neutralized)	15				dB	V_{DG} = 10 V, I_D = 10 mA	
NF	Common-Source, Spot Noise Figure (neutralized)		3.5					

Note 1: Pulse test duration = 2ms

2N5432-2N5434
N-Channel JFET

FEATURES

- Low $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

1

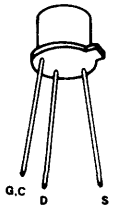
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage	-25V
Gate-Drain Voltage	-25V
Gate Current	100mA
Drain Current	400 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2.3 mW/°C

PIN CONFIGURATION

TO-52



CHIP TOPOGRAPHY

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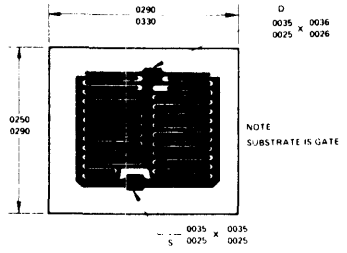


ORDERING INFORMATION*

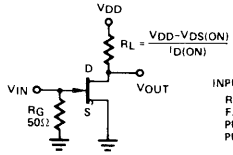
TO-52	WAFER	DICE
2N5432	2N5432/W	2N5432/D
2N5433	2N5433/W	2N5433/D
2N5434	2N5434/W	2N5434/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5432		2N5433		2N5434		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-200		-200		-200	pA	V_{GS} = -15 V, V_{DS} = 0	
	T_A = 150°C		-200		-200		-200	nA		
BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = -10 V	
	T_A = 150°C		200		200		200	nA		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V_{DS} = 5 V, I_D = 3 nA	
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
t_d	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1 5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -12 V, $I_{D(on)}$ = 10 mA	
t_r	Rise Time		1		1		1			
t_{off}	Turn-OFF Delay Time		6		6		6			
t_f	Fall Time		30		30		30			

NOTE: 1. Pulse test required, pulsewidth 300 μs, duty cycle ⩽ 3%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

R_L = 1450Ω (2N5432)
1430Ω (2N5433)
1400Ω (2N5434)

2N5452-2N5454 Dual Monolithic N-Channel JFET

FEATURES

- **Low Offset Voltage**
- **Low Drift**
- **Low Capacitance**
- **Low Output Conductance**

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

ABSOLUTE MAXIMUM RATINGS

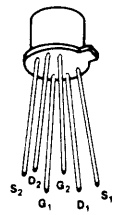
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate Drain Voltage (Note 1) ..... -50V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	2.9 mW/°C	4.3 mW/°C

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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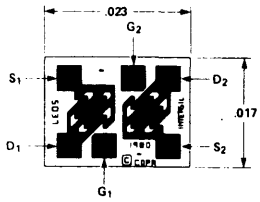


ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETER		2N5452 MIN	2N5452 MAX	2N5453 MIN	2N5453 MAX	2N5454 MIN	2N5454 MAX	UNITS	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
	T_A = 150°C		-200		-200		-200	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5		V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2		V_{DS} = 20 V, I_D = 50 μA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2		V_{DS} = 0, I_G = 1 mA	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000				f = 100 MHz
g_{os}	Common-Source Output Conductance		3.0		3.0		3.0			f = 1 kHz
			1.0		1.0		1.0		V_{DS} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0		V_{DS} = 20 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
			0.5		1.0		2.5			T = 25°C to +125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.95	1.0			
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		f = 1 kHz

NOTE: 1. Per transistor.

2N5457-2N5459
N-Channel JFET

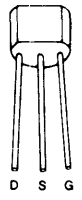
ABSOLUTE MAXIMUM RATINGS
(TA = 25°C unless otherwise noted)

Drain-Gate Voltage	25V
Drain-Source Voltage	25V
Continuous Forward Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

1

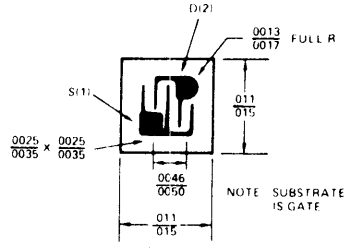
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5010*



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5457	2N5457/W	2N5457/D
2N5458	2N5458/W	2N5458/D
2N5459	2N5459/W	2N5459/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNITS	TEST CONDITIONS
BV_{GSS}	Gate-Source Breakdown Voltage		-25	-60		V	I_G = -10 μA, V_{DS} = 0
I_{GSS}	Gate Reverse Current			.05	-1.0	nA	V_{GS} = -15 V, V_{DS} = 0
					-200		V_{GS} = -15 V, V_{DS} = 0, T_A = 100°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N5457	-0.5		-6.0	V	V_{DS} = 15 V, I_D = 10 nA
		2N5458	-1.0		-7.0		
		2N5459	-2.0		-8.0		
V_{GS}	Gate-Source Voltage	2N5457		2.5		V	V_{DS} = 15 V, I_D = 100 μA
		2N5458		3.5			V_{DS} = 15 V, I_D = 200 μA
		2N5459		4.5			V_{DS} = 15 V, I_D = 400 μA
I_{DSS}	Zero-Gate-Voltage Drain Current	2N5457	1.0	3.0	5.0	mA	V_{DS} = 15 V, V_{GS} = 0
		2N5458	2.0	6.0	9.0		
		2N5459	4.0	9.0	16		
$\|y_{fs}\|$	Forward Transfer Admittance	2N5457	1000	3000	5000	μmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz
		2N5458	1500	4000	5500		
		2N5459	2000	4500	6000		
$\|y_{os}\|$	Output Admittance			10	50	μmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz
C_{iss}	Input Capacitance			4.5	7.0	pF	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			1.5	3.0	pF	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz
NF	Noise Figure				3.0	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MHz BW = 1 Hz, f = 1 KHz

Pulse test required. PW ≤ 630 ms, duty cycle ≤ 10%

2N5460-2N5465
P-Channel JFET

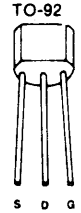
1

ABSOLUTE MAXIMUM RATINGS
(TA = 25°C unless otherwise noted)

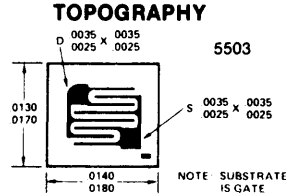
Drain-Gate or Source-Gate Voltage
- 2N5460 - 2N5462 ..... 40V
- 2N5463 - 2N5465 ..... 60V

Gate Current ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 310 mW
- Derate above 25°C ..... 2.8 mW/°C

PIN CONFIGURATION
TO-92



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

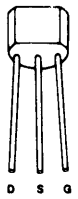
	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	2N5460, 2N5461, 2N5462	40			V	I_G = 10 μAdc, V_{DS} = 0	
		2N5463, 2N5464, 2N5465	60					
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N5460, 2N5463	0.75		6.0	V	V_{DS} = 15 Vdc, I_D = 1.0 μAdc	
		2N5461, 2N5464	1.0		7.5			
		2N5462, 2N5465	1.8		9.0			
I_{GSSR}	Gate Reverse Current	2N5460, 2N5461, 2N5462			5.0	nA	V_{DS} = 0	V_{GS} = 20V
		2N5463, 2N5464, 2N5465			5.0			V_{GS} = 30V
	T_A = 100°C	2N5460, 2N5461, 2N5462			1.0	μA		V_{GS} = 20V
		2N5463, 2N5464, 2N5465			1.0			V_{GS} = 30V
I_{DSS}	Zero-Gate Voltage Drain Current	2N5460, 2N5463	-1.0		-5.0	mA	V_{DS} = -15V	V_{GS} = 0
		2N5461, 2N5464	-2.0		-9.0			
		2N5462, 2N5465	-4.0		-16			
V_{GS}	Gate-Source Voltage	2N5460, 2N5463	0.5		4.0	V		I_D = 0.1 mA
		2N5461, 2N5464	0.8		4.5			I_D = -0.2 mA
		2N5462, 2N5465	1.5		6.0			I_D = -0.4 mA
g_{fs}	Forward Transadmittance	2N5460, 2N5463	1000		4000	μmho	V_{DS} = -15V, V_{GS} = 0V	f = 1.0 kHz
		2N5461, 2N5464	1500		5000			
		2N5462, 2N5465	2000		6000			
g_{os}	Output Admittance				75	μmho		
C_{iss}	Input Capacitance			5.0	7	pF		
C_{rss}	Reverse Transfer Capacitance			1.0	2.0	pF		
NF	Common-Source Noise Figure			1.0	2.5	dB		f = 100 Hz, BW = 1.0 Hz, R_G = 1.0 MΩ
$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			60	115	$nV/\sqrt{Hz}$		

2N5484-2N5486
N-Channel JFET

FEATURES
- **Up to 400 MHz Operation**
- **Economy Packaging**
- **C_{rss} < 1.0 pF**

1

PIN CONFIGURATION
TO-92



CHIP TOPOGRAPHY
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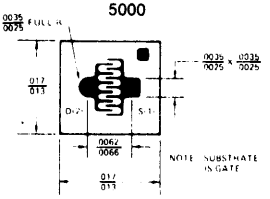


ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Drain-Gate Voltage	25V
Source Gate Voltage	25V
Drain Current	30 mA
Forward Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	310 mW
Derate above 25°C	2.8 mW/°C

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5484	2N5484/W	2N5484/D
2N5485	2N5485/W	2N5485/D
2N5486	2N5486/W	2N5486/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5484		2N5485		2N5486		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -20 V, V_{DS} = 0	
	T_A = 100°C		-200		-200		-200			
BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0		V_{DS} = 15 V, I_D = 10 nA	
I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
g_{fs}	Common-Source Forward Transconductance	3000	6000	3500	7000	4000	8000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		50		60		75			
$Re(y_{fs})$	Common-Source Forward Transconductance	2500								f = 100 MHz
				3000		3500				f = 400 MHz
$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
					100		100			f = 400 MHz
$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
					1000		1000			f = 400 MHz
C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
			3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz
					2.0		2.0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	f = 400 MHz
					4.0		4.0			
G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f = 100 MHz
				18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	f = 400 MHz
				10	20	10	20			

NOTE: Pulse test required. Pulse width = 300μs, duty cycle ≤ 3%.

2N5515-2N5524 Monolithic Dual N-Channel JFET

FEATURES

- **Tight Temperature Tracking**
- **Tight Matching**
- **High Common Mode Rejection**
- **Low Noise**

ABSOLUTE MAXIMUM RATINGS

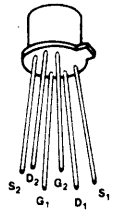
(T_A = 25°C unless otherwise specified)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current (Note 1)	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/°C	7.7 mW/°C

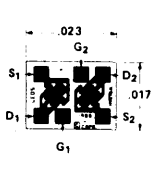
PIN CONFIGURATION

TO-71

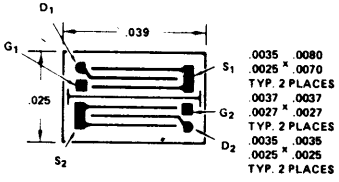


CHIP TOPOGRAPHY

(2N5515-19)
6037



(2N5520-24)
6019



ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520		
2N5521		
2N5522		
2N5523		
2N5524		

*When ordering wafer/dice refer to Appendix B-23.

NOTE: Per transistor.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER			MIN	MAX	UNITS	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current			-250	pA	V_{GS} = -30 V, V_{DS} = 0	
		T_A = 150°C		-250	nA		
BV_{GSS}	Gate-Source Breakdown Voltage		-40		V	I_G = -1 μA, V_{DS} = 0	
V_P	Gate-Source Pinch-Off Voltage		-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)		0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)		1000	4000	μmho		f = 1 kHz
g_{oss}	Common-Source Output Conductance			10			
C_{rss}	Common-Source Reverse Transfer Capacitance			5	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance			25			
$\bar{e}_n$	Equivalent Input Noise Voltage	2N5515-19		30	$nV/\sqrt{Hz}$	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
		2N5520-24		15			f = 1 kHz
		2N5515-24		10			
I_G	Gate Current			-100	pA		
		T_A = 125°C		-100	nA		
V_{GS}	Gate Source Voltage		-0.2	-3.8	V		
g_{fs}	Common-Source Forward Transconductance (Note 1)		500	1000	μmho		f = 1 kHz
g_{oss}	Common-Source Output Conductance			1	μmho		

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{DSS1}	Drain Current Ratio at	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1		V_{DS} = 20 V, V_{GS} = 0
I_{DSS2}	Zero Gate Voltage (Note 1)												
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current (+125°C)		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA
g_{fs1}	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1		V_{DG} = 20 V, I_D = 200 μA f = 1 KHz
g_{fs2}	(Note 1)												
$\lvert g_{oss1} - g_{oss2} \rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = -55°C to +125°C)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA
CMRR	Common Mode Rejection Ratio (Note 2)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA

NOTES:

1. Pulse duration of 28 ms used during test.
2. CMRR = 20 $Log_{10} \Delta V_{DD} / \Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V)

2N5638-2N5640
N-Channel JFET

FEATURES

- **Economy Packaging**
- **Fast Switching**
- **Low Drain-Source 'ON' Resistance**

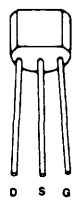
ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise specified)

Drain-Source Voltage	30V
Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Forward Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	310 mW
Derate above 25°C	2.8 mW/°C

PIN CONFIGURATION

TO-92



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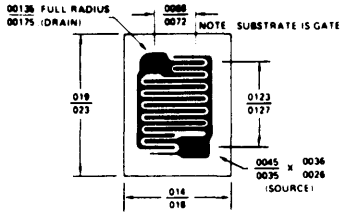


ORDERING INFORMATION*

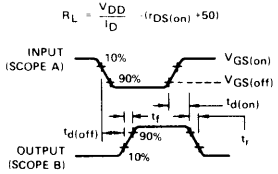
TO-92	WAFER	DICE
2N5638	2N5638/W	2N5638/D
2N5639	2N5639/W	2N5638/D
2N5640	2N5640/W	2N5640/D

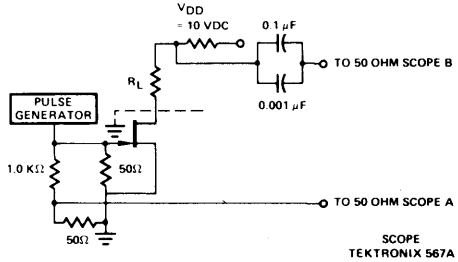
*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5638		2N5639		2N5640		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate Reverse Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
I_{GSSR}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
	T_A = 100°C		-1.0		-1.0		-1.0	μA		
$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = -12 V (2N5638)	
	T_A = 100°C		1.0		1.0		1.0	μA	V_{GS} = -8 V (2N5639), V_{GS} = -6 V (2N5640)	
I_{DSS}	Saturation Drain Current	50		25		5.0		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	V_{GS} = 0, I_D = 12 mA (2N5638), I_D = 6 mA (2N5639), I_D = 3 mA (2N5640)	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	I_D = 1 mA, V_{GS} = 0	
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		10		10		10	pF	V_{GS} = -12 V, V_{DS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	ns	V_{DD} = 10 V $I_{D(on)}$ = 12 mA (2N5638)	
t_r	Rise Time		5.0		8.0		10		$V_{GS(on)}$ = 0 $I_{D(on)}$ = 6 mA (2N5639)	
t_d	Turn-OFF Delay Time		5.0		10		15		$V_{GS(off)}$ = -10 V $I_{D(on)}$ = 3 mA (2N5640)	
t_f	Fall Time		10		20		30		R_G = 50 Ω	

NOTE: 1. Pulse test; PW ≤ 300μs, duty cycle ≤ 3.0%.





2N5902-2N5909 Monolithic Dual N-Channel JFET

FEATURES
- **Tight Tracking**
- **Good Matching**

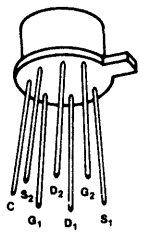
1

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40V
Gate Current (Note 1) ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	367 mW	500 mW
Derate above 25°C	3 mW/°C	4 mW/°C

PIN CONFIGURATION
TO-99



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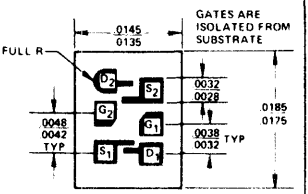


ORDERING INFORMATION*

TO-99	WAFER	DICE	TO-99	WAFER	DICE
2N5902	2N5902/W	2N5902/D	2N5906	2N5906/W	2N5906/D
2N5903	2N5903/W	2N5903/D	2N5907	2N5907/W	2N5907/D
2N5904	2N5904/W	2N5904/D	2N5908	2N5908/W	2N5908/D
2N5905	2N5905/W	2N5905/D	2N5909	2N5905/W	2N5909/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5902-5 MIN	2N5902-5 MAX	2N5906-9 MIN	2N5906-9 MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-5		-2	pA	V_{GS} = -20 V, V_{DS} = 0	
	T_A = 125°C		-10		-5	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate Source Voltage		-4		-4			
I_G	Gate Operating Current		-3		-1	pA	V_{DG} = 10 V, I_D = 30 μA	
	T_A = 125°C		-3		-1	nA		
I_{DSS}	Saturation Drain Current	30	500	30	500	μA		
g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		5		5			
C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
g_{os}	Common-Source Output Conductance		1		1			
$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 MΩ

PARAMETER		2N5902-6 MIN	2N5902-6 MAX	2N5903-7 MIN	2N5903-7 MAX	2N5904-8 MIN	2N5904-8 MAX	2N5905-9 MIN	2N5905-9 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	V_{DG} = 10 V, I_D = 30 μA, T_A = 125°C	2N5902-5
			0.2		0.2		0.2		0.2			2N5906-9
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1		V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{BS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			5		10		20		40			T_A = -55°C, T_B = 25°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

NOTE 1: Per transistor.

2N5911, 2N5912
IT5911, IT5912
Monolithic Dual N-Channel JFET

FEATURES

- **Tight Tracking**
- **Low Insertion Loss**
- **Good Matching**

ABSOLUTE MAXIMUM RATINGS

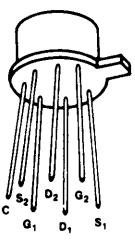
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate Source Voltage ..... -25V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

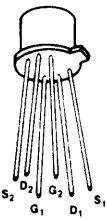
	TO-71		TO-99	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	300 mW	500 mW	300 mW	500 mW
Derate above 25°C	1.7 mW/°C	2.9 mW/°C	3.0 mW/°C	4.0 mW/°C

PIN CONFIGURATION

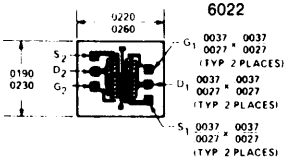
TO-99



TO-71



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-71	TO-99	WAFER	DICE
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
	T_A = 150°C		-250	nA		
BV_{GSS}	Gate Reverse Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.3	-4			
I_G	Gate Operating Current		-100	pA	V_{DG} = 10 V, I_D = 5 mA	
	T_A = 125°C		-100	nA		
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ⩽ 3%)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
g_{os}	Common-Source Output Conductance		100			f = 1 kHz
g_{oss}	Common-Source Output Conductance		150			f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100KΩ

PARAMETER		IT, 2N5911		IT, 2N5912		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0 (Pulsewidth 300 μs, duty cycle ⩽ 3%)	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		20		40	μV/°C		T_A = 25°C T_B = 125°C
			20		40			T_A = -55°C T_B = 25°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1			f = 1 kHz

2N6483-2N6485
Monolithic Low Noise Dual N-Channel JFET

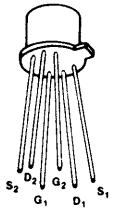
FEATURES

- **Ultra Low Noise**
- **High CMRR**
- **Low Offset**
- **Tight Tracking**

1

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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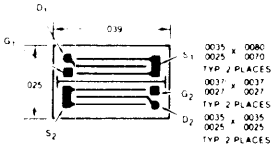


ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate-Gate Voltage ..... ±50V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C ..	3.8 mw/°C	7.7 mW/°C

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		200	pA	V_{GS} = 30 V, V_{DS} = 0
	T_A = 150°C		200	nA	
BV_{GSS}	Gate Source Breakdown Voltage	50		V	I_G = 1 µA, V_{DS} = 0
V_p	Gate Source Pinch Off Voltage	0.7	4.0		V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0
g_{fs}	Common Source Forward Transconductance (Note 2)	1000	4000	µmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz
g_{oss}	Common Source Output Conductance		10		
C_{iss}	Common Source Input Capacitance		20	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common Source Reverse Transfer Capacitance		3.5		
I_G	Gate Current		100	pA	V_{GD} = 20 V, I_D = 200 µA,
	T_A = 150°C		100	nA	
V_{GS}	Gate Source Voltage	0.2	3.8	V	V_{DG} = 20 V, I_D = 200 µA
g_{fs}	Common Source Forward Transconductance	500	1500	µmho	V_{DG} = 20 V, I_D = 200 µA, f = 1 KHz
g_{os}	Common Source Output Conductance		1		V_{DG} = 20 V, I_D = 200 µA
$\bar{e}_n$	Equivalent Input Noise Voltage		10	nV/√Hz	V_{DS} = 20 V, I_D = 200 µA, f = 10 Hz
			5		V_{DS} = 20 V, I_D = 200 µA, f = 1 KHz

NOTES: 1. Per transistor.
2. Pulse test required; pulse width = 2 ms.

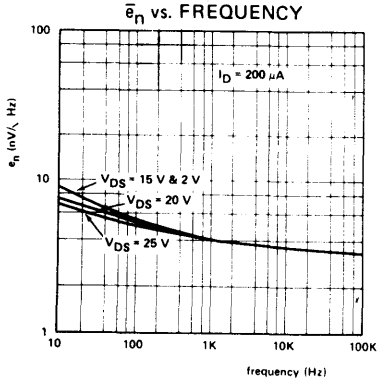
MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1		V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125°C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1		V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = -55°C to +125°C
CMRR	Common Mode Rejection Ratio	100		100		90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

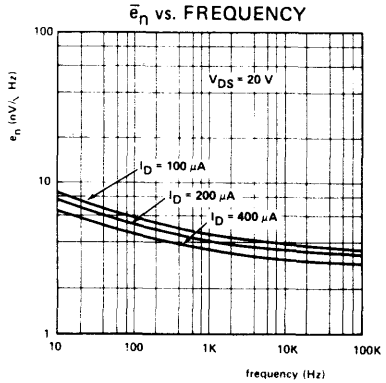
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V), not included in JEDEC registration

TYPICAL OPERATING CHARACTERISTICS

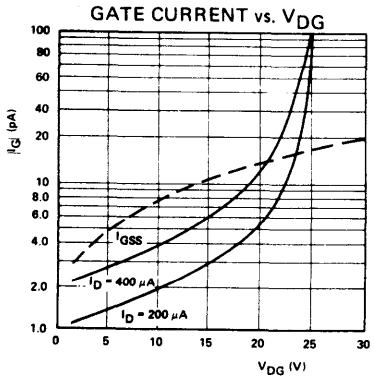
$\bar{e}_n$ vs. FREQUENCY



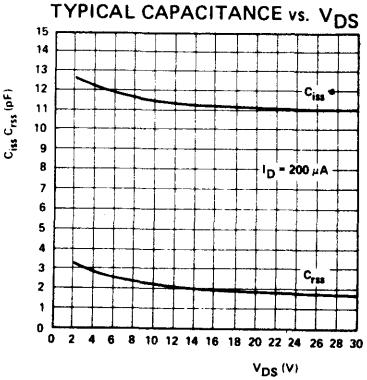
$\bar{e}_n$ vs. FREQUENCY



GATE CURRENT vs. V_{DG}



TYPICAL CAPACITANCE vs. V_{DS}



IMF6485
Monolithic Low Noise Dual N-Channel JFET

FEATURES

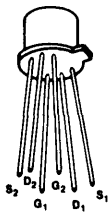
- **Ultra Low Noise**
- **High CMRR**
- **Low Offset**
- **Tight Tracking**

GENERAL DESCRIPTION

This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.

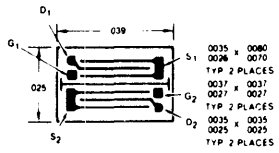
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6019



ORDERING INFORMATION*

TO-71	WAFER	DICE
IMF6485	IMF6485/W	IMF6485/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate-Gate Voltage ..... ±50V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/°C	7.7 mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200	pA	V_{GS} = -30 V, V_{DS} = 0,
	T_A = 150°C		-200	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 µA, V_{DS} = 0
V_p	Gate-Source Pinch-Off Voltage	-0.7	-4.0		V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	µmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz
g_{oss}	Common-Source Output Conductance		10		V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz
C_{iss}	Common-Source Input Capacitance		20	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
I_G	Gate Current		100	pA	V_{GD} = 20 V, I_D = 200 µA,
	T_A = 150°C		100	nA	
V_{GS}	Gate-Source Voltage	0.2	-3.8	V	V_{DG} = 20 V, I_D = 200 µA
g_{fs}	Common-Source Forward Transconductance	500	1500	µmho	V_{DG} = 20 V, I_D = 200 µA, f = 1 KHz
g_{os}	Common-Source Output Conductance		1		V_{DG} = 20 V, I_D = 200 µA
$\bar{e}_n$	Equivalent Input Noise Voltage		15	nV/√Hz	V_{DS} = 20 V, I_D = 200 µA, f = 10 Hz
			10		V_{DS} = 20 V, I_D = 200 µA, f = 1 KHz

NOTES:
1. Per transistor.
2. Pulse test required; pulse width = 2 ms.

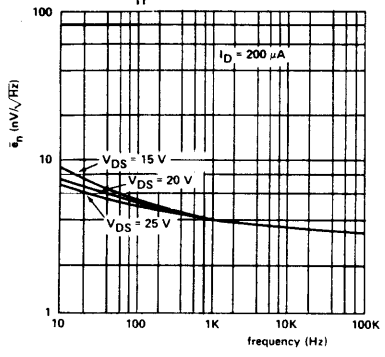
MATCHING CHARACTERISTICS (@ 25° C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1		V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G_1} - I_{G_2} \rvert$	Differential Gate Current		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125° C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.95	1		V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		25	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{CG} = 20 V, I_D = 200 μA T_A = -55°C to +125° C
CMRR	Common Mode Rejection Ratio	90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

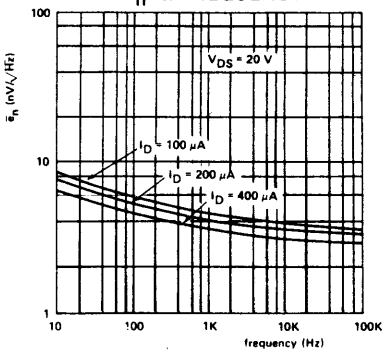
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V)

TYPICAL OPERATING CHARACTERISTICS

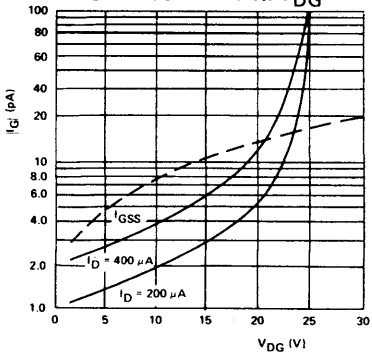
$\bar{e}_n$ vs. FREQUENCY



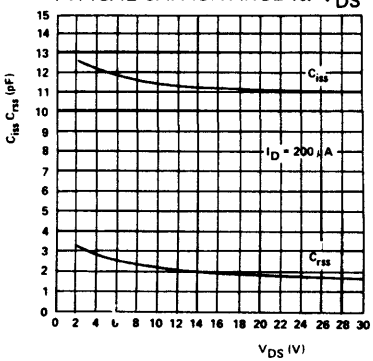
$\bar{e}_n$ vs. FREQUENCY



GATE CURRENT vs. V_{DG}



TYPICAL CAPACITANCE vs. V_{DS}



INTERSIL

3N161
Diode Protected P-Channel Enhancement Mode MOSFET

FEATURES

- **Channel Cut Off with Zero Gate Voltage**
- **Square-Law Transfer Characteristic Reduces Distortion**
- **Independent Substrate Connection Provides Flexibilty in Biasing**
- **Internally Connected Diode Protects Gate from Damage due to Overvoltage**

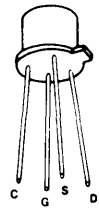
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

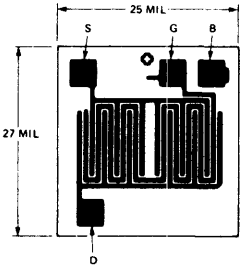
Drain-Source or Drain-Gate Voltage	40V
Drain Current	50 mA
Gate Forward Current	10 μA
Gate Reverse Current	1 mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3.0 mW/°C

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY 1507



ORDERING INFORMATION*

TO-72	WAFER	DICE
3N161	3N161/W	3N161/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
I_{GSSF}	Forward Gate-Terminal Current		-100		pA	V_{GS} = -25 V, V_{DS} = 0	
	T_A = +100°C			-1	nA		
BV_{GSS}	Forward Gate-Source Breakdown Voltage	-25			V	I_G -0.1 mA, V_{DS} = 0,	
I_{DSS}	Zero-Gate-Voltage Drain Current			-10	nA	V_{DS} = -15 V, V_{GS} = 0	
				-10	μA	V_{DS} = -25 V, V_{GS} = 0	
$V_{GS(th)}$	Gate-Source Threshold Voltage	-1.5		-5	V	V_{DS} = -15V, I_D = -10 μA	
V_{GS}	Gate-Source Voltage	-4.5		-8		V_{DS} = -15 V, I_D = -8 mA	
$I_{D(on)}$	On-State Drain Current	-40		-120	mA	V_{DS} = -15 V, V_{GS} = -15 V	
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	3500		6500	μmho	V_{DS} = -15 V, I_D = -8 mA	f = 1 kHz
$\|y_{os}\|$	Small-Signal Common-Source Output Admittance			250			
C_{iss}	Common-Source Short-Circuit Input Capacitance			10	pF		f = 1 MHz
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			4			

3N163, 3N164
P-Channel Enhancement Mode MOS FET

FEATURES
- **Very High Input Impedance**
- **High Gate Breakdown**
- **Fast Switching**
- **Low Capacitance**

ABSOLUTE MAXIMUM RATINGS (Note 1)
(TA = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage
- 3N163 ..... 40V
- 3N164 ..... 30V

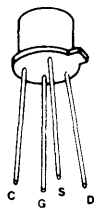
Static Gate-Source Voltage
- 3N163 ..... ±40V
- 3N164 ..... ±30V

Transient Gate-Source Voltage (Note 2) ..... ±125V
Drain Current ..... 50 mA
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 375 mW
Derate above +25°C ..... 3.0 mW/°C

NOTES:
1. See handling precautions on 3N170 data sheet.
2. Devices must not be tested at ±125V more than once, nor for longer than 300 ms.

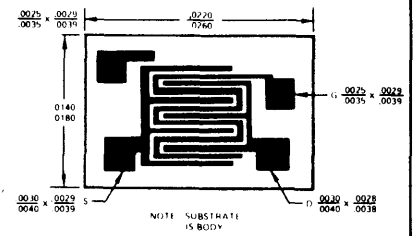
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1503



ORDERING INFORMATION*

TO-72	WAFER	DICE
3N163	3N163/W	3N163/D
3N164	3N164/W	3N164/D

*When ordering wafer/dice refer to Appendix B-23.

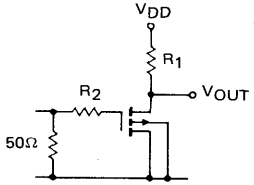
ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

Symbol	Parameter	3N163 MIN	3N163 MAX	3N164 MIN	3N164 MAX	UNITS	TEST CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current		10		10	pA	V_{GS} = -40V (3N163), V_{GS} = -30V (3N164)
I_{GSSF}	Gate Forward Current		-10		-10	pA	V_{GS} = -40V (3N163), V_{GS} = -30V (3N164)
	T_A = +125°C		-25		-25		
BV_{DSS}	Drain Source Breakdown Voltage	-40		-30		V	I_D = -10 µA, V_{GS} = 0
BV_{SDS}	Source Drain Breakdown Voltage	-40		-30		V	I_S = 10 µA, V_{GD} = 0, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 µA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = -15V, I_D = -10 µA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	V	V_{DS} = -15V, I_D = -0.5 mA
I_{DSS}	Zero Gate Voltage Drain Current		200		400	pA	V_{DS} = -15V, V_{GS} = 0
I_{SDS}	Source Drain Current		400		800	pA	V_{SD} = 15V, V_{GS} = V_{DB} = 0
$r_{DS(on)}$	Drain Source on Resistance		250		300	ohms	V_{GS} = -20V, I_D = -100 µA
$I_{D(on)}$	On Drain Current	-5.0	-30.0	-3.0	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
g_{fs}	Forward Transconductance	2000	4000	1000	4000	µmhos	V_{DS} = -15V, I_D = -10 mA, f = 1 KHz
g_{os}	Output Admittance		250		250	µmhos	V_{DS} = -15V, I_D = -10 mA, f = 1 KHz
C_{iss}	Input Capacitance Output Shorted		2.5		2.5	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz

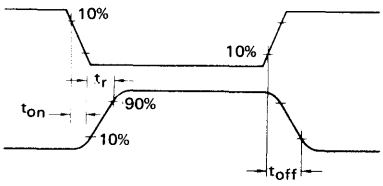
SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0)

t_{on}	Turn-On Delay Time		12		12	ns	V_{DD} = -15V
t_r	Rise Time		24		24	ns	$I_{D(on)}$ = -10 mA
t_{off}	Turn-Off Time		50		50	ns	R_G = R_L = 1.4 kΩ

SWITCHING TIME CIRCUIT



SWITCHING WAVEFORM



3N165, 3N166
Dual P-Channel Enhancement Mode MOS FET

FEATURES

- **Very High Impedance**
- **High Gate Breakdown**
- **Low Capacitance**

ABSOLUTE MAXIMUM RATINGS (Note 1)

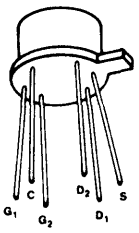
(T_A = 25°C unless otherwise specified)

Drain-Source or Drain-Gate Voltage (Note 2)
- 3N165 ..... 40V
- 3N166 ..... 30V

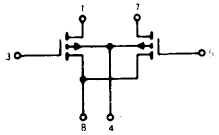
Transient Gate-Source Voltage (Note 3) ..... ±125
Gate-Gate Voltage ..... ±80V
Drain Current (Note 2) ..... 50 mA
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation
- One Side ..... 300 mW
- Both Sides ..... 525 mW
- Total Derating above 25°C ..... 4.2 mW/°C

PIN CONFIGURATION

TO-99

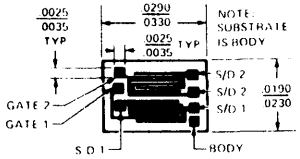


DEVICE SCHEMATIC



CHIP TOPOGRAPHY

2506



ORDERING INFORMATION*

TO-99	WAFER	DICE
3N165	3N165/W	3N165/D
3N166	3N166/W	3N166/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless notes)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current		10	pA	V_{GS} = 40V
I_{GSSF}	Gate Forward Leakage Current		-10		V_{GS} = -40V
	T_A = +125°C		-25		
I_{DSS}	Drain to Source Leakage Current		-200		V_{DS} = -20V
I_{SDS}	Source to Drain Leakage Current		-400		V_{SD} = -20, V_{DB} = 0
$I_{D(on)}$	On Drain Current	-5	-30	mA	V_{DS} = -15V, V_{GS} = -10V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	V	V_{DS} = -15V, I_D = -10μA
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5		V_{DS} = V_{GS}, I_D = -10μA
$r_{DS(on)}$	Drain Source ON Resistance		300	ohms	V_{GS} = -20V, I_D = -100μA
g_{fs}	Forward Transconductance	1500	3000	μmhos	V_{DS} = -15V, I_D = -10mA, f = 1kHz
g_{os}	Output Admittance		300		
C_{iss}	Input Capacitance		3.0	pF	V_{DS} = -15V, I_D = -10mA, f = 1MHz
C_{rss}	Reverse Transfer Capacitance		0.7		
C_{oss}	Output Capacitance		3.0		
$R_E(Y_{fs})$	Common Source Forward Transconductance	1200		μmhos	V_{DS} = -15V, I_D = -10mA, f = 100MHz

MATCHING CHARACTERISTICS 3N165

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS} = -15V, I_D = -1500μA, f = 1KHz
V_{GS1-2}	Gate-Source Threshold Voltage Differential		100	mV	V_{DS} = -15V, I_D = -500μA
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature		100	μV/°C	V_{DS} = -15V, I_D = -500μA T_A = -55°C to +25°C
			100		

Note 1: See handling precautions on 3N170 data sheet.
Note 2: Per transistor.
Note 3: Devices must not be tested at ±125V more than once, nor for longer than 300 ms.

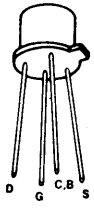
3N170, 3N171
N-Channel Enhancement Mode MOS FET

FEATURES
- **Low Switching Voltages**
- **Fast Switching Times**
- **Low Drain-Source Resistance**
- **Low Reverse Transfer Capacitance**

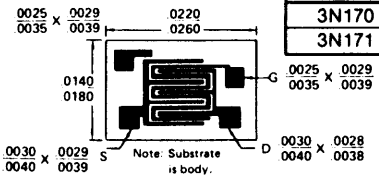
ABSOLUTE MAXIMUM RATINGS
(TA = 25°C unless otherwise noted)

Drain-Gate Voltage	±35V
Drain-Source Voltage	25V
Gate-Source Voltage	±35V
Drain Current	30 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION
TO-72



CHIP TOPOGRAPHY
1003



HANDLING PRECAUTIONS
MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanant damage to the devices.

ORDERING INFORMATION*

TO-72	WAFER	DICE
3N170	3N170/W	3N170/D
3N171	3N170/W	3N170/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connectored to source.

	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-Source Breakdown Voltage		25		V	I_D = 10 μA, V_{GS} = 0
I_{GSS}	Gate Leakage Current			10	pA	V_{GS} = -35 V, V_{DS} = 0
		T_A = 125°C		100		
I_{DSS}	Zero-Gate-Voltage Drain Current			10	nA	V_{DS} = 10 V, V_{GS} = 0
		T_A = 125°C		1.0	μA	
$V_{GS(th)}$	Gate-Source Threshold Voltage	3N170	1.0	2.0	V	V_{DS} = 10 V, I_D = 10 μA
		3N171	1.5	3.0		
$I_{D(on)}$	"ON" Drain Current		10		mA	V_{GS} = 10 V, V_{DS} = 10 V
$V_{DS(on)}$	Drain-Source "ON" Voltage			2.0	V	I_D = 10 mA, V_{GS} = 10 V
$r_{ds(on)}$	Drain-Source ON Resistance			200	Ω	V_{GS} = 10 V, I_D = 0, f = 1.0 kHz
$\|Y_{fs}\|$	Forward Transfer Admittance		1000		μmhos	V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz
C_{rss}	Reverse Transfer Capacitance			1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz
C_{iss}	Input Capacitance			5.0		V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
$C_{d(sub)}$	Drain-Substrate Capacitance			5.0		$V_{D(SUB)}$ = 10 V, f = 1.0 MHz
$t_{d(on)}$	Turn-On Delay Time			3.0	ns	V_{DD} = 10 V, $I_{D(on)}$ = 10 mA, $V_{GS(on)}$ = 10 V, $V_{GS(off)}$ = 0, R_G = 50 Ω
t_r	Rise Time			10		
$t_{d(off)}$	Turn-Off Delay Time			3.0		
t_f	Fall Time			15		

3N172, 3N173 Diode Protected P-Channel Enhancement Mode MOS FET

FEATURES
- **High Input Impedance**
- **Diode Protected Gate**

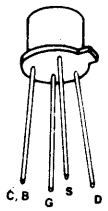
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage
- 3N172 ..... 40V
- 3N173 ..... 30V

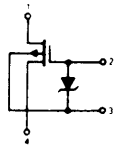
Drain Current ..... 50 mA
Gate Forward Current ..... 10 μA
Gate Reverse Current ..... 1 mA
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 375 mW
Derate above 25°C ..... 3.0 mW/°C

PIN CONFIGURATION

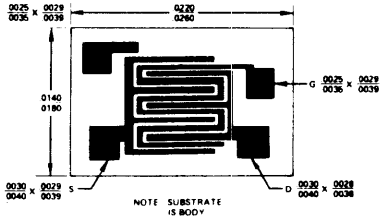
TO-72



DEVICE SCHEMATIC



CHIP TOPOGRAPHY 1503Z



ORDERING INFORMATION*

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

PARAMETER		3N172		3N173		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSSR}	Gate Reverse Current		-200		-500	pA	V_{GS} = -20V
	T_A = +125°C		-0.5		-1.0	μA	
BV_{GSS}	Gate Breakdown Voltage	-40	-125	-30	-125	V	I_D = -10 μA
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30			I_D = -10 μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			I_S = -10 μA, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		V_{DS} = V_{GS}, I_D = -10 μA
		-2.0	-5.0	-2.0	-5.0		V_{DS} = -15V, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-2.5	-6.5		V_{DS} = -15V, I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-0.4		-10	nA	V_{DS} = -15V, V_{GS} = 0
I_{SDS}	Zero Gate Voltage Source Current		-0.4		-10		V_{SD} = -15V, V_{DB} = 0, V_{GD} = 0
$r_{DS(on)}$	Drain Source On Resistance		250		350	ohms	V_{GS} = -20V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30	-5.0	-30	mA	V_{DS} = -15V, V_{GS} = -10V

3N188-3N191
Dual P-Channel Enhancement Mode MOSFET

FEATURES

- **Very High Input Impedance**
- **High Gate Breakdown 3N190-3N191**
- **Zener Protected gate 3N188-3N189**
- **Low Capacitance**

ABSOLUTE MAXIMUM RATINGS

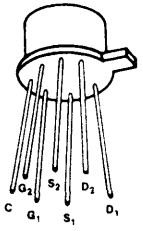
(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage (Note 1)
- 3N188, 3N189 ..... 40V
- 3N190, 3N191 ..... 30V

Transient Gate-Source Voltage (Notes 1 and 2) .. ±125V
Gate-Gate Voltagae ..... ±80V
Drain Current (Note 1) ..... 50 mA
Storage Temperature ..... -65°C to +200°C
Operating Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation
- One Side ..... 300 mW
- Both Sides ..... 525 mW
- Total Derating above 25°C ..... 4.2 mW/°C

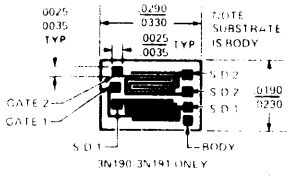
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

2506



NOTE: Body is connected to case.

ORDERING INFORMATION*

TO-99	WAFER	DICE
3N188	—	—
3N189	—	—
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C and V_{BS} = 0 unless otherwise noted)

PARAMETER		3N188 3N189 MIN	3N188 3N189 MAX	3N190 3N191 MIN	3N190 3N191 MAX	UNITS	TEST CONDITIONS
I_{GSSR}	Gate Reverse Current				10	pA	V_{GS} = 40V
I_{GSSF}	Gate Forward Current		-200		-10		V_{GS} = -40V
	T_A = 125°C		-200		-25		
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-40		V	I_D = -10μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-40			I_S = -10μA, V_{BD} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		V_{DS} = -15V, I_D = -10 μA
		-2.0	-5.0	-2.0	-5.0		V_{DS} = V_{GS}, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5		V_{DS} = -15V I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-200		-200	pA	V_{DS} = -15V
I_{SDS}	Source Drain Current		-400		-400		V_{SD} = -15V, V_{DB} = 0
$r_{DS(on)}$	Drain-Source on Resistance		300		300	ohms	V_{DS} = -20V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30.0	-5.0	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
$\|y_{fs}\|$	Forward Transconductance (Note 3)	1500	4000	1500	4000	μmhos	V_{DS} = -15V, I_D = -5 mA, f = 1kHz
Y_{os}	Output Admittance		300		300		
C_{iss}	Input Capacitance Output Shorted		4.5		4.5	pF	V_{DS} = -15V, I_D = -5 mA, f = 1MHz
C_{rss}	Reverse Transfer Capacitance		1.5		1.0		
C_{oss}	Output Capacitance Input Shorted		3.0		3.0		

SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		MIN	MAX	UNITS	TEST CONDITIONS
$t_{d(on)}$	Turn On Delay Time		15	ns	V_{DD} = -15V, I_D = -5 mA
t_r	Rise Time		30		R_G = R_L = 1.4 kΩ
t_{off}	Turn Off Time		50		

MATCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted) 3N188 and 3N190

		MIN	MAX	UNITS	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.85	1.0		V_{DS} = -15V, I_D = -500 μA, f = 1 kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential		100	mV	V_{DS} = -15V, I_D = -500 μA
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)		100	μV/°C	V_{DS} = -15V, I_D = -500 μA, T = -55°C to + 25°C
$\frac{\Delta VGS1-2}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)		100	μV/°C	V_{DS} = -15V, I_D = -500μA T = +25°C to +125°C

NOTES:
1. Per transistor
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
4. Measured at end points, T_A and T_B.

INTERSIL

FEATURES

- I_R = 0.1 pA (typical)
- BV_R > 30 V
- C_{rss} = 0.75 pF (typical)

1

GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

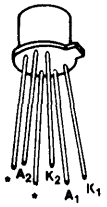
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Diode Reverse Voltage	30V
Diode to Diode Voltage	±50V
Forward Current	20 mA
Reverse Current	100 μA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

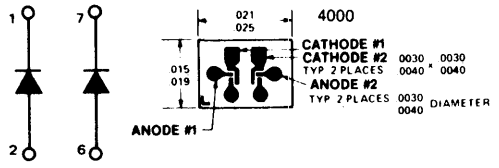
PIN CONFIGURATIONS

TO-71
TO-78



*These leads must not be tied together nor connected to the circuit in any way.

CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO78	TO71	WAFER	CHIP
ID100	ID101	ID100/W	ID100/D

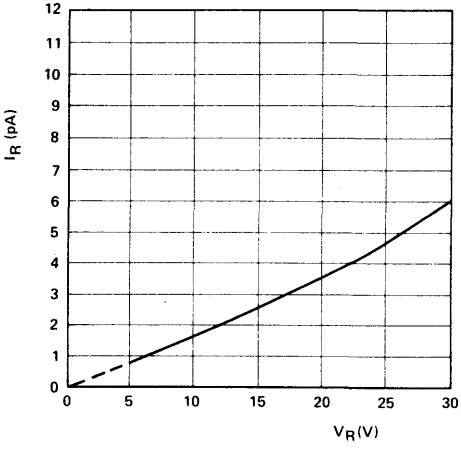
*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

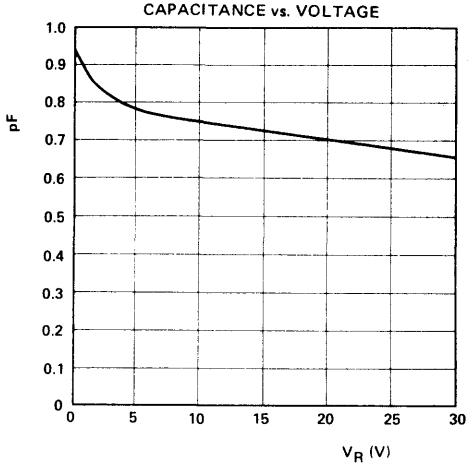
PARAMETER		ID100, ID101 MIN.	ID100, ID101 TYP.	ID100, ID101 MAX.	UNITS	TEST CONDITIONS
V_F	Forward Voltage Drop	0.8		1.1	V	I_F = 10 mA
BV_R	Reverse Breakdown Voltage	30			V	I_R = 1 μA
I_R	Reverse Leakage Current		0.1		pA	V_R = 1 V
			2.0	10		
	T_A = 125°C			10	nA	V_R = 10 V
$\lvert I_{R_1} - I_{R_2} \rvert$	Differential Leakage Current			3	pA	
C_{rss}	Total Reverse Capacitance		0.75	1	pF	V_R = 10 V, f = 1 MHz

TYPICAL CHARACTERISTICS OF ID100/ID101

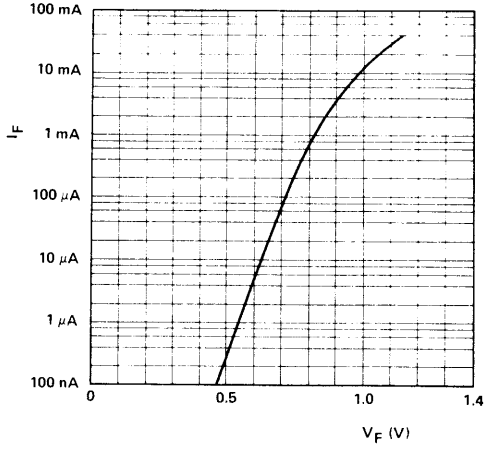
REVERSE CURRENT vs. VOLTAGE



CAPACITANCE vs. VOLTAGE



FORWARD CURRENT vs. VOLTAGE



IT100, IT101
P-Channel JFET

1

FEATURES

- **Interfaces Directly w/T^2L Logic Elements**
- **$r_{DS(on)}$ < 75Ω for 5V Logic Drive**
- **$I_{D(off)}$ < 100 pA**

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with T^2L logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of ±15 V can be switched. The FET is OFF for hi level inputs (+5 V or +15 V) and ON for low level inputs (< 0.5 V for IT100;< 1.5 V for IT101.

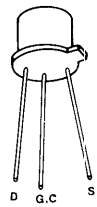
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source Voltage	35V
Gate-Drain Voltage	35V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

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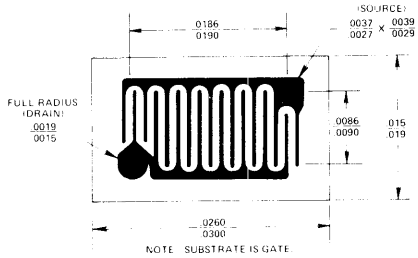


ORDERING INFORMATION*

TO-18	WAFER	DICE
IT100	IT100/W	IT100/D
IT101	IT101/W	IT101/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT100		IT101		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{DSS}	Drain Current	-10		-20		mA	V_{GS} = 0, V_{DS} = -15 V
V_P	Pinch Off Voltage	2	4.5	4	10	V	I_D = 1 nA, V_{DS} = -15 V
BV_{GSS}	Gate-Source Breakdown Voltage	35		35			I_G = 1 μA, V_{DS} = 0
I_{GSSR}	Gate Reverse Current		200		200	pA	V_{GS} = 20 V, V_{DS} = 0
g_{fs}	Transconductance	8		8		mmho	V_{GS} = 0, V_{DS} = -15 V
g_{os}	Output Conductance		1		1		
$I_{D(off)}$	Drain (OFF) Leakage		-100		-100	pA	V_{DS} = -10 V, V_{GS} = 15 V
$r_{DS(on)}$	Drain-Source "ON" Resistance		75		60	Ω	V_{GS} = 0, V_{DS} = -0.1 V
C_{iss}	Input Capacitance		35		35	pF	V_{DG} = -20 V, V_{GS} = 0
C_{rss}	Reverse Transfer Capacitance		12		12		V_{DG} = -10 V, I_S = 0

IT120-IT122 Monolithic Dual NPN Transistor

FEATURES

- **High h_{FE} at Low Current**
- **Low Output Capacitance**
- **Good Matching**
- **Tight V_{BE} Tracking**

ABSOLUTE MAXIMUM RATINGS

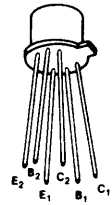
(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	50 mA
Collector-Collector Voltage	60V
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Power Dissipation ...	TO-71 ONE SIDE	TO-71 BOTH SIDES	TO-78 ONE SIDE	TO-78 BOTH SIDES
	400 mW	750 mW	300 mW	500 mW
Derate Above 25°C	1.7 mW/°C	2.9 mW/°C	2.3 mW/°C	4.3 mW/°C

PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

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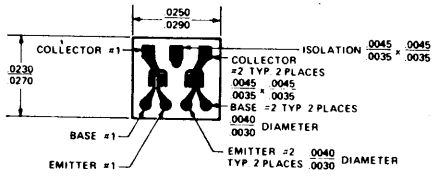


ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT120	IT120-TO71	IT120/W	IT120/D
IT121	IT121-TO71	IT121/W	IT121/D
IT122	IT122-TO71	IT122/W	IT122/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

(25°C unless otherwise noted)

PARAMETER		IT120A MIN	IT120A MAX	IT120 MIN	IT120 MAX	IT121 MIN	IT121 MAX	IT122 MIN	IT122 MAX	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	200		200		80		80			I_C = 10 μA, V_{CE} = 5.0 V
		225		225		100		100			I_C = 1.0 mA, V_{CE} = 5.0 V
	T_A = -55°C	75		75		30		30			
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7		I_C = 10 μA, V_{CE} = 5.0 V
$V_{CE(SAT)}$	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	I_C = 0.5 mA, I_B = 0.05 mA
I_{CBO}	Collector Cutoff Current		1.0		1.0		1.0		1.0	nA	I_E = 0, V_{CB} = 45 V
	T_A = +150°C		10		10		10		10	μA	
I_{EBO}	Emitter Cutoff Current		1.0		1.0		1.0		1.0	nA	I_C = 0, V_{EB} = 5.0 V
C_{obo}	Output Capacitance		2.0		2.0		2.0		2.0		I_E = 0, V_{CB} = 5.0 V, f = 1 MHz
C_{te}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	I_C = 0, V_{EB} = 0.5 V, f = 1 MHz
C_{C_1,C_2}	Collector to Collector Capacitance		4.0		4.0		4.0		4.0		V_{CC} = 0
I_{C_1,C_2}	Collector to Collector Leakage Current		10		10		10		10	nA	V_{CC} = ±60 V
$V_{CEO(SUST)}$	Collector to Emitter Sustaining Voltage	45		45		45		45		V	I_C = 1.0 mA, I_B = 0
GBW	Current Gain Bandwidth Product	10		10		7		7		MHz	I_C = 10 μA, V_{CE} = 5 V
		220		220		180		180			I_C = 1 mA, V_{CE} = 5 V
$\lvert V_{BE_1}-V_{BE_2}\rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert I_{B_1}-I_{B_2}\rvert$	Base Current Differential		2.5		5		25		25	nA	
$\Delta(V_{BE_1}-V_{BE_2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	T_A = -55°C to +125°C, I_C = 10 μA, V_{CE} = 5.0 V

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA.

IT124
Monolithic Dual Super-Beta NPN Transistor

1

FEATURES

- **Very High Gain**
- **Low Output Capacitance**
- **Tight V_{BE} Matching**
- **High GBW**

ABSOLUTE MAXIMUM RATINGS

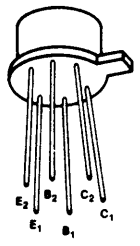
(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1) 2V
Collector-Emitter Voltage (Note 1) 2V
Emitter-Base Voltage (Notes 1 and 2) 7V
Collector-Current (Note 1) ..... 10 mA
Collector-Collector Voltage 100V
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

	TO-78 ONE SIDE	TO-78 BOTH SIDES
Power Dissipation	300 mW	500 mW
Derate above 25°C	1.7 mW/°C	4.3 mW/°C

PIN CONFIGURATION

TO-78



CHIP TOPOGRAPHY

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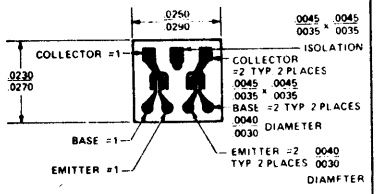


ORDERING INFORMATION*

TO-78	WAFER	DICE
IT124	IT124/W	IT124/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1500			I_C = 1μA, V_{CE} = 1V
		1500			I_C = 10μA, V_{CE} = 1V
	T_A = -55°C	600			
V_{BE}(ON)	Emitter-Base "ON" Voltage		0.7	V	
V_{CE}(SAT)	Collector Saturation Voltage		0.5		I_C = 1mA, I_B = 0.1mA
I_{CBO}	Collector Cutoff Current		100	pA	I_E = 0, V_{CB} = 1V
	T_A = +150°C		100	nA	
I_{EBO}	Emitter Cutoff Current		100	pA	I_C = 0, V_{EB} = 5V
C_{obo}	Output Capacitance		0.8	pF	I_E = 0, V_{CB} = 1V, f = 1 MHz
C_{te}	Emitter Transition Capacitance		1.0		I_C = 0, V_{EB} = 0.5V, f = 1 MHz
$C_{C_1C_2}$	Collector to Collector Capacitance		0.8		V_{CC} = 0
$I_{C_1C_2}$	Collector to Collector Leakage Current		250	pA	V_{CC} = ±50V
GBW	Current Gain Bandwidth Product	10		MHz	I_C = 10μA, V_{CE} = 1V
		100			I_C = 100μA, V_{CE} = 1V
NF	Narrow Band Noise Figure		3	dB	I_C = 10μA, V_{CE} = 3V, f = 1 KHz, R_G = 10 Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	I_C = 10μA, I_E = 0
BV_{EBO} (Note 2)	Emitter-Base Breakdown Voltage	7			I_E = 10μA, I_C = 0
V_{CEO}(SUST)	Collector-Emitter Sustaining Voltage	2			I_C = 1mA, I_B = 0

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	2	5	mV	I_C = 10μA, V_{CE} = 1V
$\Delta\lvert(V_{BE1}-V_{BE2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature	5	15	μV/°C	I_C = 10μA, V_{CE} = 1V T = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential		.6	nA	T_C = 10μA, V_{CE} = 1V

NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.

IT126-IT129
Monolithic Dual NPN Transistor

FEATURES
- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectric Isolated Matched Pairs for Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

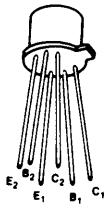
Collector-Base Voltage (Note 1)
- IT126, IT127 ..... 60V
- IT128 ..... 55V
- IT129 ..... 45V

Collector-Emitter Voltage (Note 1)
- IT126, IT127 ..... 60V
- IT128 ..... 55V
- IT129 ..... 45V

Emitter-Base Voltage (Notes 1 and 2) 7.0V
Collector Current (Note 1) ..... 100 mA
Collector-Collector Voltage 70V
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	TO71		TO78	
	One Side	Both Sides	One Side	Both Sides
Power Dissipation Total Dissipation at 25°C Cast Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7 mW/°C	2.9 mW/°C	2.5 mW/°C	4.3 mW/°C

PIN CONFIGURATION TO-71 TO-78



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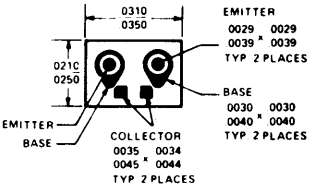


ORDERING INFORMATION*

TO78	TO-71	WAFER	DICE
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-TO71	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT128/W	IT128/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT126		IT127		IT128		IT129		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			I_C = 10 μA, V_{CE} = 5V
		200	800	200	800	150	800	100			I_C = 1.0 mA, V_{CE} = 5V
		230		230		170		115			I_C = 10 mA, V_{CE} = 5V
		100		100		75		50			I_C = 50 mA, V_{CE} = 5V
	T_A = -55°C	75		75		60		40			I_C = 1 mA, V_{CE} = 5V
$V_{BE(on)}$	Emitter-Base On Voltage		.9		.9		.9		.9	V	I_C = 10 mA, V_{CE} = 5V
			1.0		1.0		1.0		1.0		I_C = 50 mA, V_{CE} = 5V
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3		I_C = 10 mA, I_B = 1 mA
			1.0		1.0		1.0		1.0		I_C = 50 mA, I_B = 5 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45V, 30V*
	T_A = +150°C		0.1		0.1		0.1		0.1*	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5V
C_{obo}	Output Capacitance		3		3		3		3	pF	I_E = 0, V_{CB} = 20V
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	± 100		± 100		± 100		± 100		V	I_C = ±1 μA
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45			I_C = 1 mA, I_B = 0
BV_{CBO}	Collector Base Breakdown Voltage	60		60		55		45			I_C = 10 μA, I_E = 0
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		7			I_E = 10 μA, I_C = 0
MATCHING CHARACTERISTICS											
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 1 ma, V_{CE} = 5V
$\Delta(\lvert V_{BE_1} - V_{BE_2} \rvert)/\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	I_C = 1 mA, V_{CE} = 5V T_A = -55°C to +125°C
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		10		20	nA	I_C = 10 μA, V_{CE} = 5V
			25		.5		1.0		2.0	μA	I_C = 1 mA, V_{CE} = 5V

NOTES:
1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μ Amps.

IT130-IT132 Monolithic Dual PNP Transistor

FEATURES

- **High h_{FE} at Low Current**
- **Low Output Capacitance**
- **Tight I_B Match**
- **Tight V_{BE} Tracking**

ABSOLUTE MAXIMUM RATINGS

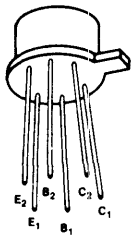
(T_A = 25°C unless otherwise specified)

Collector-Base Voltage (Note 1) 45V
Collector-Emitter Voltage (Note 1) 45V
Emitter Base Voltage (Notes 1 and 2) 7V
Collector Current (Note 1) ..... 50 mA
Collector-Collector Voltage 60V
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	400 mW	750 mW	300 mW	500 mW
	2.3 mW/°C	4.3 mW/°C	1.7 mW/°C	4.3 mW/°C

PIN CONFIGURATIONS

TO-71
TO-78



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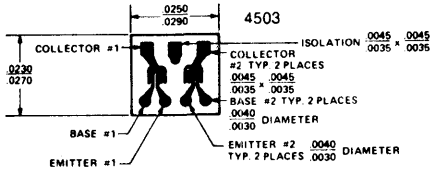


ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			I_C = 10 μA, V_{CE} = 5.0 V
		225		225		100		100			I_C = 1.0 mA, V_{CE} = 5.0 V
	T_A = -55°C	75		75		30		30			I_C = 10 μA, V_{CE} = 5.0 V
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	I_C = 10 μA, V_{CE} = 5.0 V
$V_{CE(SAT)}$	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	I_C = 0.5 mA, I_B = 0.05 mA
I_{CBO}	Collector Cutoff Current		-1.0		-1.0		-1.0		-1.0	nA	I_E = 0, V_{CB} = 45 V
	T_A = +150°C		-10		-10		-10		-10	μA	
I_{EBO}	Emitter Cutoff Current		-1.0		-1.0		-1.0		-1.0	nA	I_C = 0, V_{EB} = 5.0 V
C_{ob}	Output Capacitance		2.0		2.0		2.0		2.0	pF	I_E = 0, V_{CB} = 5.0 V
C_{te}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	I_C = 0, V_{EB} = 0.5 V
$C_{C_1-C_2}$	Collector to Collector Capacitance		4.0		4.0		4.0		4.0		V_{CC} = 0
$I_{C_1-C_2}$	Collector to Collector Leakage Current		10		10		10		10	nA	V_{CC} = ±60 V
$V_{CEO(SUST)}$	Collector to Emitter Sustaining Voltage	-45		-45		-45		-45		V	I_C = 1.0 mA, I_B = 0
GBW	Current Gain Bandwidth Product	5		5		4		4		MHz	I_C = 10 μA, V_{CE} = 5 V
		110		110		90		90		MHz	I_C = 1 mA, V_{CE} = 5 V
$\lvert V_{BE_1}-V_{BE_2}\rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 10 μA, V_{CE} = 5.0 V
$\lvert I_{B_1}-I_{B_2}\rvert$	Base Current Differential		2.5		5		25		25	nA	I_C = 10 μA, V_{CE} = 5.0 V
$\Delta(V_{BE_1}-V_{BE_2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	T_A = -55°C to +125°C, I_C = 10 μA, V_{CE} = 5.0 V

NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0V, and the reverse base-to-emitter current must never exceed 10 μA.

IT136-IT139
Monolithic Dual PNP Transistor

FEATURES
- **High Gain at Low Current**
- **Low Output Capacitance**
- **Tight I_B Match**
- **Tight V_{BE} Tracking**
- **Dielectrically Isolated Matched Pairs for Differential Amplifiers**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1)
- IT136, IT137 ..... 60V
- IT138 ..... 55V
- IT139 ..... 45V

Collector-Emitter Voltage (Note 1)
- IT136, IT137 ..... 60V
- IT138 ..... 55V
- IT139 ..... 45V

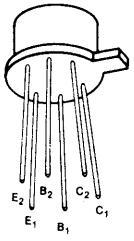
Emitter-Base Voltage (Notes 1 and 2) 7V
Collector Current (Note 1) ..... 100 mA
Collector-Collector Voltage 70V
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

	TO78 ONE SIDE	TO78 BOTH SIDES
Power Dissipation	0.4 Watt	0.75 Watt
Derate above 25°C	2.3 mW/°C	4.3 mW/°C

	TO71 ONE SIDE	TO71 BOTH SIDES
Power Dissipation	0.3 Watt	0.5 Watt
Derate above 25°C	1.7 mW/°C	2.9 mW/°C

PIN CONFIGURATION

TO-71
TO-78



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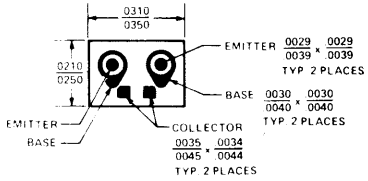
CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

*When ordering wafer/dice refer to Appendix B-23.

INTERSIL

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			I_C = 10 μA, V_{CE} = 5V
		150	800	150	800	100	800	70	800		I_C = 1.0 mA, V_{CE} = 5V
		125		125		80		50			I_C = 10 mA, V_{CE} = 5V
		65		60		40		25			I_C = 50 mA, V_{CE} = 5V
	T_A = 55°C	75		75		60		40			I_C = 1 mA, V_{CE} = 5V
$V_{BE(on)}$	Emitter - Base On Voltage		.9		.9		.9		.9	V	I_C = 10 mA, V_{CE} = 5V
			1.0		1.0		1.0		1.0		I_C = 50 mA, V_{CE} = 5V
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3		I_C = 1 mA, I_B = .1 mA
			.6		.6		.6		.6		I_C = 10 mA, I_B = 1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45V, 30V*
	T_A = +150°C		0.1		0.1		0.1		0.1*	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5V
C_{obo}	Output Capacitance		3		3		3		3	pF	I_E=0, V_{CB}=20V, f=1 MHz

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	± 100		± 100		± 100		± 100		V	I_C = ±1 μA
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45			I_C = 1 mA, I_B = 0
BV_{CBO}	Collector Base Breakdown Voltage	60		60		55		45			I_C = 10 μA, I_E = 0
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		7			I_E = 10 μA, I_C = 0

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 1 ma , V_{CE} = 5V
$\Delta\lvert(V_{BE_1} - V_{BE_2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	I_C = 1 mA, V_{CE} = 5V T_A = -55°C to +125°C
$\lvert I_{B1} - I_{B2} \rvert$	Base Current Differential		2.5		5		10		20	nA	I_C = 10 μA, V_{CE} = 5V
			.25		.5		1.0		2.0	μA	I_C = 1 mA, V_{CE} = 5V

NOTES: 1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA

IT500-IT505 Monolithic Dual Cascoded N-Channel JFET

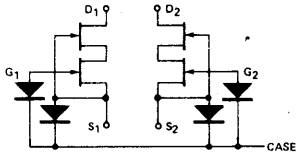
FEATURES

- C_{MRR} > 120 dB
- I_G < 5pA @ 50V_{DG}
- C_{rss} < 0.5 pF
- g_{os} > .025 μmhos

GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common mode rejection ratio.

1



ABSOLUTE MAXIMUM RATINGS

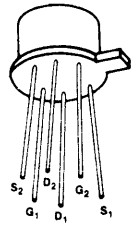
(T_A = 25° C unless otherwise specified)

Drain-Source and Drain-Gate Voltages (Note 1)	60V
Drain Current (Note 1)	50 mA
Gate-Gate Voltage	±60V
Storage Temperature	-65° C to +200° C
Operating Temperature	-55° C to +150° C
Lead Temperature (Soldering, 10 sec.)	+300° C

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25° C	3.8 mW/° C	7.7 mW/° C

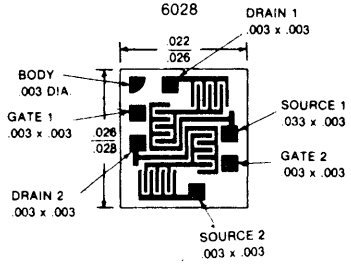
PIN CONFIGURATION

TO-71
low profile



CHIP TOPOGRAPHY

(Note 2)



ORDERING INFORMATION*

TO-78	WAFER	DICE
IT500	IT500/W	IT500/D
IT501	IT501/W	IT501/D
IT502	IT502/W	IT502/D
IT503	IT503/W	IT503/D
IT504	IT504/W	IT504/D
IT505	IT505/W	IT505/D

*When ordering wafer/dice refer to Appendix B-23.

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

Symbol	Characteristics	Min	Max	Unit	Test Conditions
I_{GSSR}	Gate Reverse Current		-100	pA	V_{GS} = -20V, V_{DS} = 0
	T_A = 125°C		-5	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-60		V	I_G = -1 μA, V_{DS} = 0
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20V, I_D = 1 nA
V_{GS}	Gate-Source Voltage	-0.2	-3.8		
I_G	Gate Operating Current		-5	pA	V_{DG} = 50V, I_D = 200 μA
	T_A = 125°C		-5	nA	
I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V_{DS} = 20V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	1600		V_{DG} = 20V, I_D = 200 μA
g_{os}	Common-Source Output Conductance		1		V_{DS} = 20V, V_{GS} = 0
g_{os}	Common-Source Output Conductance		0.025		V_{DS} = 20V, I_D = 200 μA
$C_{g_1g_2}$	Gate to Gate Capacitance		3.5	pF	V_{G1} = V_{G2} = 10V
C_{iss}	Common-Source Input Capacitance		7	pF	V_{DS} = 20V, V_{GS} = 0
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)		0.5		
NF	Spot Noise Figure		0.5	dB	
$\bar{e}_n$	Equivalent Input Noise Voltage		0.035	$\frac{\mu V}{\sqrt{Hz}}$	
			0.010		

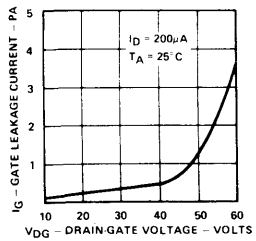
Symbol	Characteristics	IT500		IT501		IT502		IT503		IT504		IT505		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
I_{G1}-I_{G2}	Differential Gate Current		5		5		5		5		10		15	nA	V_{DG} = 20V, I_D = 200 μA + 125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1		V_{DS} = 20V, V_{GS} = 0V
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1		f = 1 kHz
V_{GS1}-V_{GS2}	Differential Gate-Source Voltage		5		5		10		15		25		50	mV	
$\frac{\triangle V_{GS1}\text{-}V_{GS2}}{\triangle T}$	Gate-Source Differential Voltage		5		10		20		40		100		200	μV/°C	V_{DG} = 20V, I_D = 200 μA, T_A = 25°C, T_B = 125°C
	Change with Temp. (Note 2)		5		10		20		40		100		200		T_A = -55°C, T_B = 25°C
C_{MRR}**	Common Mode Rejection Ratio	120		120		120		120		120		120		dB	$\triangle V_{DD}$ = 10V, I_D = 200 μA

** $C_{MRR} = 20 \log_{10} \triangle V_{DD} / \triangle [V_{gs1} - V_{gs2}]$, $\triangle V_{DD}$ = 10/-20V

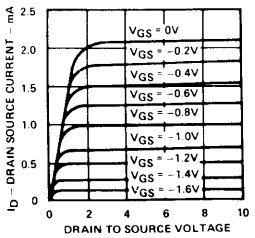
NOTES: 1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤3%. 2. Measured at end points, T_A and T_B.
3. With case guarded C_{rss} is typically < 0.15 pF.

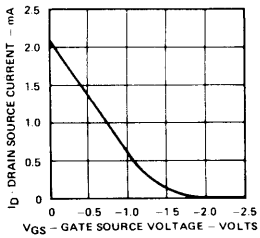
TYPICAL PERFORMANCE CURVES

GATE LEAKAGE

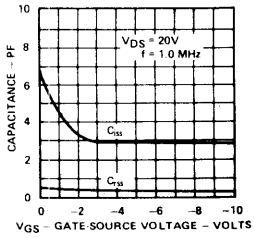


OUTPUT CHARACTERISTICS





TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE



A050 Using the IT500 Family to Improve the Input Bias Current of BIFET OPAMPS

1

INTRODUCTION

The LF156 family of BIFET OPAMPS is very popular because of the combination of high slew rate (typically 12V/μs @ unity gain) and moderate offset voltage (about 2mV). Input bias current, however, varies directly with input voltage, rising from 30pA @ V_{IN} = -10V, to 50 pA @ V_{IN} = 0V, and finally to 80pA @ V_{IN} = +10V. This can be improved markedly by using one of the IT500 series to drive the inputs of the LF156.

The IT500, like the others in its family, is a dual cascoded n-channel JFET pair, featuring a typical input bias current of <1pA with inputs ranging from -15V to +15V; actual I_G is guaranteed to be less than 5pA @ V_{DG} = 50V.

Figure 1 shows an IT500 being used to drive the inputs of an LF156. This greatly reduces the input bias current, and in no way affects the already superior slew rate; the offset voltage is not significantly degraded because of the excellent matching of the IT500.

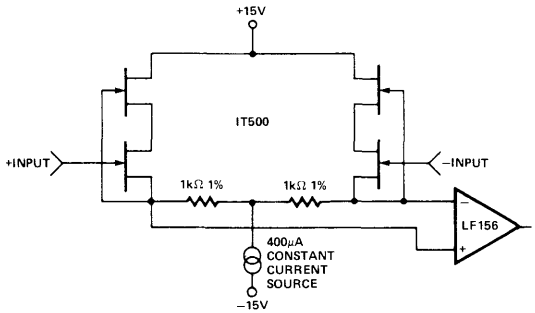


FIGURE 1. INPUT DRIVE CIRCUIT USING IT500

The constant current source can be designed with any transistor pair having a high beta @ I_C = 400μA. See Figure 2.

An added bonus of the IT500 is its CMRR > 100dB, compared to the LF156 CMRR of 85dB.

This configuration is ideal for electrometer circuits, with good measurement accuracy down to 10pA of input current (< 10% error with 10pA of input current). A 10MΩ glass feedback resistor connected between the -INPUT and OPAMP OUTPUT does the trick. Other possible applications include sample and hold amplifiers, instrumentation amplifiers, etc.

Although this application note has dealt solely with the LF156, all present day BIFET OPAMPS exhibit the same I_{BIAS} vs. V_{IN} dependancy, and all will benefit from using the IT500 as a preamplifier.

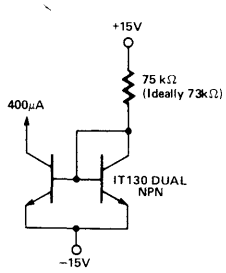


FIGURE 2. CONSTANT CURRENT SOURCE

IT550
Dual N-Channel JFET

1

FEATURES

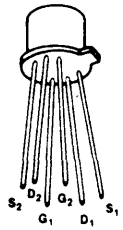
- **Specified Matching Characteristics**
- **High Gain**
- **Low "ON" Resistance**

ABSOLUTE MAXIMUM RATINGS
(25°C Unless otherwise noted)

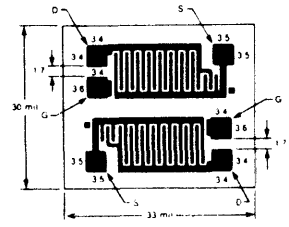
Gate-Drain or Gate-Source Voltage	-40V
Gate Current	50 mA
Gate-Gate Voltage	±80V
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

	One Side	Both Sides
Power Dissipation	325mW	650mW
Derate above 25°C	2.2mW/°C	3.3mW/°C

PIN CONFIGURATION
TO-71



CHIP TOPOGRAPHY
6033



ORDERING INFORMATION*

TO-71	WAFER	DICE
IT550	IT550/W	IT550/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS (25°C unless otherwise noted)

SYMBOL	PARAMETERS	TEST CONDITIONS		MIN.	MAX.	UNIT
I_{GSSR}	Gate-Reverse Current	V_{GS} = −20V, V_{DS} = 0			−100	pA
	T_A = 150°C				−200	mA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1nA		−0.5	−3	
$V_{GS(f)}$	Gate-Source Voltage	V_{DS} = 0V, I_G = 2mA			1.0	
I_{DSS}	Saturation Drain Current (Note 1)	V_{DS} = 15V, V_{GS} = 0		5	30	mA
$r_{DS(on)}$	Static Drain Source ON Resistance	I_D = 1mA, V_{GS} = 0			100	Ω
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DG} = 15V, I_D = 2mA	f = 1kHz	7500	12,500	μmho
			f = 100MHz	7000		
g_{os}	Common-Source Output Conductance		f = 1kHz		45	
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1MHz		3	pF
C_{iss}	Common-Source Input Capacitance				12	
NF	Spot Noise Figure		f = 10Hz, R_g = 1M		1.0	dB
e_n	Equivalent Short Circuit Input Noise Voltage		f = 10Hz		50	$\frac{nV}{\sqrt{Hz}}$

SYMBOL	PARAMETERS	CONDITIONS	IT550 MIN.	IT550 MAX.	UNIT
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	V_{DS} = 15V, V_{GS} = 0	0.95	1	—
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DS} = 15V, I_D = 2mA (T_A = −55°C to +125°C)		50	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)			100	μV/°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	V_{DS} = 15V, I_D = 2mA f = 1kHz	0.90	1	—

NOTES:
1. Pulse test required; pulse width 300μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator
3. Measured at end points T_A and T_B

IT1700
P-Channel Enhancement Mode MOSFET

FEATURES

- **Low ON-Resistance**
- **High Gain**
- **Low Noise Voltage**
- **High Input Impedance**
- **Low Leakage**

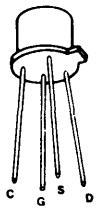
ABSOLUTE MAXIMUM RATINGS

(T_A = 25° C unless otherwise noted)

Drain-Source and Gate-Source Voltage ..... -40 V
Peak Gate-Source Voltage (Note 1)..... ±125 V
Drain Current ..... 50 mA
Storage Temperature ..... -65° C to +200° C
Operating Temperature Range ... -55° C to +150° C
Lead Temperature (Soldering, 10 sec) ..... +300° C
Power Dissipation ..... 375 mW
Derate above 25° C ..... 3 mW/° C

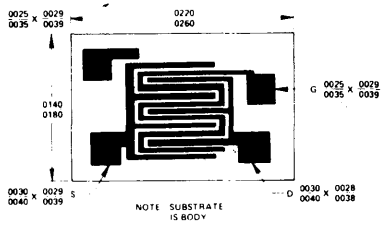
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1503



ORDERING INFORMATION*

TO-72	WAFER	DICE
IT1700	IT1700/W	IT1700/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted), V_{BS} = 0 unless otherwise noted.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40		V	V_{GS} = 0, I_D = -10 μA
BV_{SDS}	Source to Drain Breakdown Voltage	-40		V	V_{GS} = 0, I_D = -10 μA
I_{GSS}	Gate Leakage Current		(See note 2)		
I_{DSS}	Drain to Source Leakage Current		200	pA	V_{GS} = 0, V_{DS} = -20 V
I_{DSS} (150° C)	Drain to Source Leakage Current		0.4	μA	
I_{SDS}	Source to Drain Leakage Current		400	pA	
I_{SDS} (150° C)	Source to Drain Leakage Current		0.8	μA	
$V_{GS(th)}$	Gate Threshold Voltage	-2	-5	V	V_{GS} = V_{DS}, I_D = -10 μA
r_{DS} (on)	Static Drain to Source "on" Resistance		400	ohms	V_{GS} = -10 V, V_{DS} = 0
I_{DS} (on)	Drain to Source "on" Current	2		mA	V_{GS} = -10 V, V_{DS} = -15 V
g_{fs}	Forward Transconductance Common Source	2000	4000	μmhos	V_{DS} = -15 V, I_D = -10 mA f = 1 kHz
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance		5	pF	V_{DS} = -15V, I_D = -10 mA f = 1 MHz
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance		1.2	pF	V_{DG} = -15 V, I_D = 0 f = 1 MHz
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance		3.5	pF	V_{DS} = -15 V, I_D = -10 mA f = 1 MHz

NOTES: 1. Device must not be tested at ±125V more than once nor longer than 300 ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10 pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

IT1750
N-Channel Enhancement Mode MOSFET

FEATURES

- **Low ON Resistance**
- **Low C_{dg}**
- **High Gain**
- **Low Threshold Voltage**

1

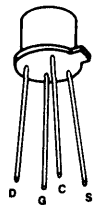
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage	25V
Peak Gate-Source Voltage (Note 1)	±125V
Drain Current	100 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	375 mW
Derate above 25°C	3 mW/°C

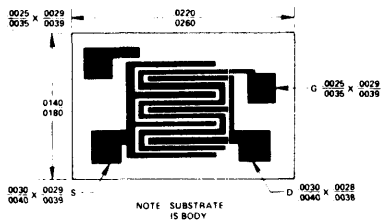
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1003



ORDERING INFORMATION*

TO-72	WAFER	DICE
IT1750	IT1750/W	IT1750/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Body connected to Source and V_{BS} = 0 unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GS(th)}$	Gate to Source Threshold Voltage	0.50	1.5	3.0	V	V_{DS} = V_{GS}, I_D = 10 μA
I_{DSS}	Drain Leakage Current		0.1	10	nA	V_{DS} = 10 V, V_{GS} = 0
I_{GSS}	Gate Leakage Current		See note 2.			
BV_{DSS}	Drain Breakdown Voltage	25			V	I_D = 10 μA, V_{GS} = 0
$r_{DS(on)}$	Drain To Source on Resistance		25	50	ohms	V_{GS} = 20 V
$I_{D(on)}$	Drain Current	10	50		mA	V_{DS} = V_{GS} = 10 V
Y_{fs}	Forward Transadmittance	3,000			μmhos	V_{DS} = 10 V, I_D = 10 mA, f = 1 KHz
C_{iss}	Total Gate Input Capacitance		5.0	6.0	pF	I_D = 10 mA, V_{DS} = 10 V, f = 1 MHz
C_{dg}	Gate to Drain Capacitance		1.3	1.6	pF	V_{DG} = 10 V, f = 1 MHz

NOTES:

1. Devices must not be tested at ±125V more than once nor longer than 300 ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

J105-J107
N-Channel JFET

1

FEATURES
- Low $r_{DS(on)}$

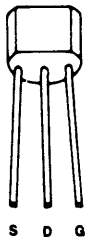
APPLICATIONS
- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -25V
Gate Current ..... 50 mA
Storage Temperature Range .. -65°C to +200°C
Operating Temperature Range -55°C to +150°C
Lead Temperature (Soldering, 10 sec.)...+300°C
Power Dissipation ..... 360 mW
Derate above 25°C ..... 3.3 mW/°C

PIN CONFIGURATION

TO-92



ORDERING INFORMATION*

J105	TO-92 only
J106	TO-92 only
J107	TO-92 only

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted

PARAMETER		J105			J106			J107			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate-Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS}=0V, V_{GS}=-15V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	V_{DS}=5V, I_D=1 μA	
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS}=0V, I_G=-1 μA	
I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	V_{DS}=15V, V_{GS}=0V	
$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS}=5V, V_{GS}=-10V	
$r_{DS(on)}$	Drain source ON Resistance			3			6			8	Ω	V_{DS}≤0.1V, V_{GS}=0V	
$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	V_{DS}=0V, V_{GS}=-10V	f=1 MHz
$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35			
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		V_{DS}=V_{GS}=0V	
$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions	
t_r	Rise Time		20			20			20				
$t_{d(off)}$	Turn Off Delay Time		15			15			15				
t_f	Fall Time		20			20			20				

Switching Time Test Conditions	J105	J106	J107
V_{DD}	1.5V	1.5V	1.5V
$V_{GS(off)}$	-12V	-7V	-5V
R_L	50Ω	50Ω	50Ω

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration =300 μs; duty cycle≤3%.

J111-J113
N-Channel JFET

1

FEATURES

- **Low Cost**
- **Automated Insertion Package**
- **Low Insertion Loss**
- **No Offset or Error Voltage Generated by Closed Switch**
  - **Purely Resistive**
  - **High Isolation Resistance from Driver**
- **Fast Switching**
- **Short Sample and Hold Aperture Time**

APPLICATIONS

- Analog Switches
- Choppers
- Commutators

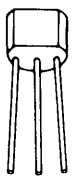
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -35V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 310 mW
Derate Above 25°C ..... 2.8 mW/°C

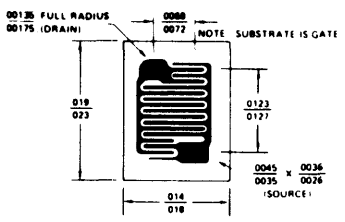
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5001



ORDERING INFORMATION*

TO-92	WAFER	DICE
J111	J111/W	J111/D
J112	J112/W	J112/D
J113	J113/W	J113/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	PARAMETERS	J111 MIN	J111 TYP	J111 MAX	J112 MIN	J112 TYP	J112 MAX	J113 MIN	J113 TYP	J113 MAX	UNIT	TEST CONDITIONS
I_{GSSR}	Gate Reverse Current (Note 1)			-1			-1			-1	nA	V_{DS} = 0V, V_{GS} = -15V
$V_{GS(off)}$	Gate Source Cutoff Voltage	-3		-10	-1		-5	-0.5		-3	V	V_{DS} = 5V, I_D = 1μA
BV_{GSS}	Gate Source Breakdown Voltage	-35			-35			-35				V_{DS} = 0V, I_G = -1μA
I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	V_{DS} = 15V, V_{GS} = 0V
$I_{D(off)}$	Drain Cutoff Current (Note 1)			1			1			1	nA	V_{DS} = 5V, V_{GS} = -10V
$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	V_{DS} = 0.1V, V_{GS} = 0V
$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0V, V_{GS} = -10V; f = 1 MHz
$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5		
$C_{dg(on)}$ $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28		V_{DS} = V_{GS} = 0; f = 1 MHz
$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions
t_r	Rise Time		6			6			6			
$t_{d(off)}$	Turn Off Delay Time		20			20			20			
t_f	Fall Time		15			15			15			

	J111	J112	J113
V_{DD}	10V	10V	10V
$V_{GS(off)}$	-12V	-7V	-5V
R_L	0.8kΩ	1.6kΩ	3.2kΩ

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300μs; duty cycle ≤ 3%.

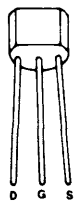
J174-J177
P-Channel JFET

FEATURES
- **Low Insertion Loss**
- **No Offset or Error Generated by Closed Switch**
  - **Purely Resistive**
  - **High Isolation Resistance from Driver**
- **Short Sample and Hold Aperture Time**
- **Fast Switching**

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

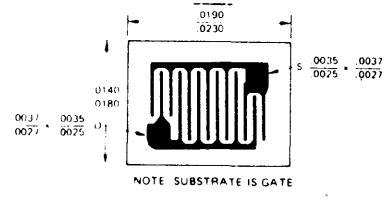
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY (Note 1)

5508



ORDERING INFORMATION*

TO-92	WAFER	DICE
J17X	J17X/W	J17X/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1)	30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	350 mW
Derate above 25°C	3.5 mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS		J174			J175			J176			J177			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSSR}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15V, I_D = -10nA	
BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1μA	
I_{DSS}	Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V_{DS} = -15V, V_{GS} = 0	
$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15V, V_{GS} = 10V	
$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1V	
$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10V	f = 1 MHz
$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5				
$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance		40			40			40			40			V_{DS} = V_{GS} = 0	
$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions	
t_r	Rise Time		5			10			20			25				
$t_{d(off)}$	Turn Off Delay Time		5			10			15			20				
t_f	Fall Time		10			20			20			25				

Switching Time Test Conditions	J174	J175	J176	J177
V_{DD}	-10V	-6V	-6V	-6V
$V_{GS(off)}$	12V	8V	6V	3V
R_L	560Ω	12KΩ	5.6KΩ	10KΩ
$V_{GS(on)}$	0V	0V	0V	0V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration ≤300μs; duty cycle ≤ 3%.

J201-J204
N-Channel JFET

1

FEATURES
- **High Input Impedance**
- **Low I_{GSS}**

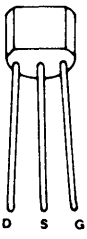
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current ..... 50 mA
Storage Temperature Range .. -65°C to +200°C
Operating Temperature Range -55°C to +150°C
Lead Temperature (Soldering, 10 sec.)...+300°C
Power Dissipation ..... 360 mW
Derate above 25°C ..... 3.3mW/°C

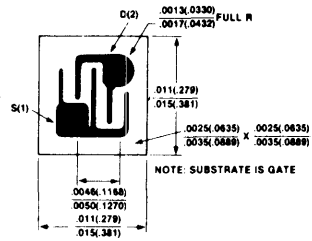
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5010*



ORDERING INFORMATION*

TO-92	WAFER	DICE
J201	J201/W	J201/D
J202	J202/W	J202/D
J203	J203/W	J203/D
J204	J204/W	J204/D

*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	PARAMETERS	J201			J202			J203			J204			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current (Note 2)			-100			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -20V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	-0.5		-2.0	V	V_{DS} = 20V, I_D = 10 nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			-25			V	V_{DS} = 0, I_G = -1μA	
I_{DSS}	Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20		1.2		mA	V_{DS} = 20V, V_{GS} = 0	
I_G	Gate Current (Note 1)		-3.5			-3.5			-3.5			-3.5		pA	V_{DG} = 20V, I_D = 200μA	
g_{fs}	Common-Source Forward Transconductance(Note 2)	500			1,000			1,500				1500		μmho	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz
g_{os}	Common Source Output Conductance		1			3.5			10			2.5				
C_{iss}	Common-Source Input Capacitance		4			4			4			4		pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1			1				
$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		5			5			5			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2ms.

	PARAMETERS		J204 MIN	J204 TYP	J204 MAX	UNIT	TEST CONDITIONS	
STATIC	I_{GSS}	Gate Reverse Current (Note 2)			−100	pA	V_{DS} = 0, V_{GS} = −20V	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−2.0	V	V_{DS} = 20V, ID = 10nA	
	BV_{GSS}	Gate-Source Breakdown Voltage	−25				V_{DS} = 0, I_G = −μA	
	I_{DSS}	Saturation Drain Current (Note 3)		1.2		mA	V_{DS} = 20V, V_{GS} = 0	
	I_G	Gate Current (Note 1)		−3.5		pA	V_{DG} = 20V, I_D 200μA	
DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)		1500		μmho	V_{DS} = 20V, V_{GS} = 0	f = 1kHz
	g_{os}	Common Source Output Conductance		2.5		μmho	V_{DS} = 20V, V_{GS} = 0	f = 1kHz
	C_{iss}	Common-Source Input Capacitance		4		pF	V_{DS} = 20V, V_{GS} = 0	f = 1MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		1		pF	V_{DS} = 20V, V_{GS} = 0	f = 1MHz
	e_n	Equivalent Short-Circuit Input Noise Voltage		10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10V, V_{GS} = 0	f = 1kHz

J308-J310
N-Channel JFET

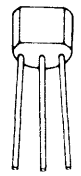
FEATURES
- **Industry Standard Part in Low Cost Plastic Package**
- **High Power Gain**
- **Low Noise**
- **Dynamic Range Greater than 100 dB**
- **Easily Matched to 75Ω Input**

1

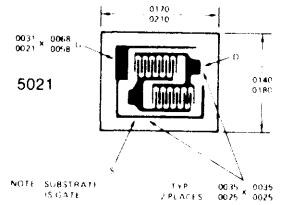
APPLICATIONS
- VHF/UHF Amplifiers
- Oscillators
- Mixers

PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	WAFER	DICE
J30X	J30X/W	J30X/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted

PARAMETER		J308			J309			J310			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1μA, V_{DS} = 0	
I_{GSSR}	Gate Reverse Current			-1.0			-1.0			-1.0	nA	V_{GS} = -15V,	
	T_A = 125°C			-1.0			-1.0			-1.0	μA	V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.5	-1.0		-4.0	-2.0		-6.5	V	V_{DS} = 10V, I_D = 1nA	
I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	V_{DS} = 0, I_G = 1 mA	
g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	μmhos	V_{DS} = 10V, I_D = 10mA	f = 1 kHz
g_{os}	Common-Source Output Conductance			200			200			200			
g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
g_{og}	Common Gate Output Conductance		150			150			150				
C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	V_{DS} = 0, V_{GS} = -10V	f = 1 MHz
C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
e_n	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz
$Re_{(Yfs)}$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10V, I_D = 10mA	f = 105 MHz
$Re_{(Yfg)}$	Common-Gate Input Conductance		14			14			14				
$Re_{(Yis)}$	Common-Source Input Conductance		0.4			0.4			0.4				
$Re_{(Yos)}$	Common-Source Output Conductance		0.15			0.15			0.15				
G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
NF	Noise Figure		1.5			1.5			1.5				
G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
NF	Noise Figure		2.7			2.7			2.7				

NOTE: 1. Pulse test PW 300 μs, duty cycle ≤ 3%.

LM114/H, LM114A/AH Monolithic Dual NPN Transistor

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10μA collector current. Typical collector-base capacitance is only 1.6 pF at 5V.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

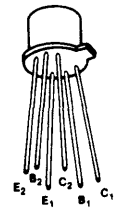
Collector-Base Voltage (1)	45V
Collector-Emitter Voltage (1)	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (1)	6V
Collector Current (1)	20mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	800mW
Derate above 25°C	14mW/°C

FEATURES

- Low offset voltage
- Low drift
- High current gain
- Tight beta match
- High breakdown voltage
- Matching guaranteed over a 0V to 45V collector-base voltage range
- CMRR > 100 dB

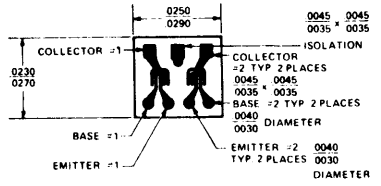
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4003



ORDERING INFORMATION*

TO-71	TO-78	WAFER	DICE
LM114	LM114H	LM114/W	LM114/D
LM114A	LM114AH		

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	MAXIMUM LIMITS LM114A, AH	MAXIMUM LIMITS LM114, H	UNITS	CONDITIONS
Offset Voltage	0.5	2.0	mV	$1\mu A \le I_C \le 100\mu A$
Offset Current	2.0	10	nA	$I_C = 10\mu A$
Bias Current	0.5	40	nA	$I_C = 1\mu A$
	20			$I_C = 10\mu A$
	3.0			$I_C = 1\mu A$
Offset Voltage Change	0.2	1.5	mV	$0V \le V_{CB} \le V_{MAX}$, $I_C = 10\mu A$
Offset Current Change	1.0	4.0	nA	
Offset Voltage Drift	2.0	10	μV/°C	$-55°C \le T_A \le +125°$, $I_C = 10\mu A$
Offset Current	12	50	nA	
Bias Current	60	150		
Collector-Base Leakage Current	10	50	pA	$V_{CB} = V_{MAX}$
T_A = 125°C	10	50	nA	
Collector-Emitter Leakage Current	50	200	pA	$V_{CE} = V_{MAX}$, $V_{EB} = 0V$
T_A = 125°C	50	200	nA	
Collector-Collector Leakage Current	100	300	pA	$V_{CC} = V_{MAX}$
T_A = 125°C	100	300	nA	

Note 1: Per transistor.

Note 2: These specifications apply for T_A = +25°C and $0V \le V_{CB} \le V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, V_{MAX} = 30V.

M116
Diode Protected N-Channel Enhancement Mode MOSFET

1

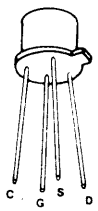
FEATURES
- Low I_{GSS}
- Integrated Zener Clamp for Gate Protection

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

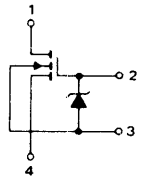
Drain to Source Voltage	30V
Gate to Drain Voltage	30V
Drain Current	50 mA
Gate Zener Current	±0.1 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2.2 mW/°C

PIN CONFIGURATION

TO-72

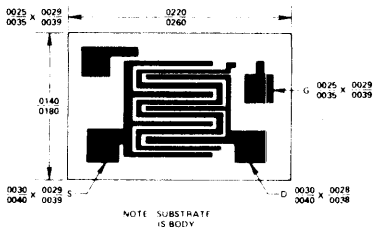


DEVICE SCHEMATIC



CHIP TOPOGRAPHY

1003



ORDERING INFORMATION*

TO-72	WAFER	DICE
M116	M116/W	M116/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		M116 MIN	M116 MAX	UNITS	TEST CONDITIONS
$r_{DS(on)}$	Drain Source ON Resistance		100	Ω	V_{GS} = 20 V, I_D = 100 μA, V_{BS} = 0
			200		V_{GS} = 10 V, I_D = 100 μA, V_{BS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	1	5	V	V_{GS} = V_{DS}, I_D = 10 μA, V_{BS} = 0
BV_{DSS}	Drain-Source Breakdown Voltage	30			I_D = 1 μA, V_{GS} = V_{BS} = 0
BV_{SDS}	Source-Drain Breakdown Voltage	30			I_S = 1 μA, V_{GD} = V_{BD} = 0
BV_{GBS}	Gate-Body Breakdown Voltage	30	60		I_G = 10 μA, V_{SB} = V_{DB} = 0
$I_{D(OFF)}$	Drain Cutoff Current		10	nA	V_{DS} = 20 V, V_{GS} = V_{BS} = 0
$I_{S(OFF)}$	Source Cutoff Current		10		V_{SD} = 20 V, V_{GD} = V_{BD} = 0
I_{GSS}	Gate-Body Leakage		100	pA	V_{GS} = 20 V, V_{DS} = V_{BS} = 0
C_{gs}	Gate-Source		2.5	pF	V_{GB} = V_{DB} = V_{SB} = 0, f = 1 MHz Body Guarded
C_{gd}	Gate-Drain Capacitance		2.5		
C_{db}	Drain-Body Capacitance		7		V_{GB} = 0, V_{DB} = 10 V, f = 1 MHz
C_{iss}	Input Capacitance		10		V_{GB} = 0, V_{DB} = 10 V, V_{BS} = 0 f = 1 MHz

U200-U202
N-Channel JFET

FEATURES

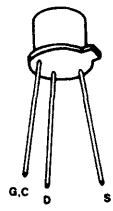
- **Low Insertion Loss**
- **Good OFF Isolation**

APPLICATIONS

- Analog Switches
- Commutators
- Choppers

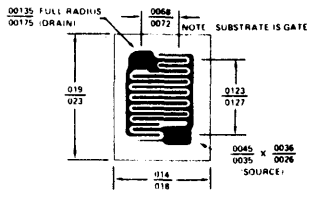
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5001



ORDERING INFORMATION*

TO-18	WAFER	DICE
U200	U200/W	U200/D
U201	U201/W	U201/D
U202	U202/W	U202/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -30V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Total Device Dissipation 1.8W
Derate above 25°C ..... 10 mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Parameter		U200		U201		U202		Unit	Test Conditions	
		Min	Max	Min	Max	Min	Max			
I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	V_{GSS} = 20 V, V_{DS} = 0	
	T_A = 150°C		-1		-1		-1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = 1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		V_{DS} = 20 V, I_D = 10 nA	
$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	V_{DS} = 10 V, V_{GS} = -12 V	
	T_A = 150°C		1		1		1	μA		
I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	V_{DS} = 20 V, V_{GS} = 0	
$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common Source Reverse Transfer Capacitance		8		8		8		V_{DS} = 0, V_{GS} = -12 V	

NOTE 1: Pulse test required, pulsewidth = 300 μsec, duty cycle ≤3%.

INTERSIL

U231-U235
Monolithic Dual N-Channel JFET

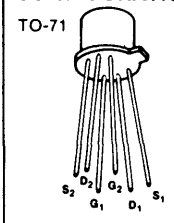
FEATURES
- **Good Matching Characteristics**

APPLICATIONS
- Differential Amplifiers
- Low and Maximum Frequency Amplifiers

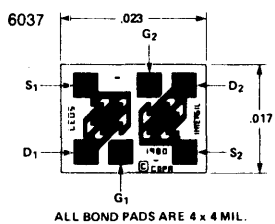
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) ..... -50V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Load Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 1.7 mW/°C

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-71	WAFER	DICE
U23X	U23X/W	U23X/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted.

Parameter		Min	Max	Unit	Test Conditions	
I_{GSSR}	Gate Reverse Current		-100	pA	V_{GS} = -30V, V_{DS} = 0	
	T_A = 150°C		-500	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = 1μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 20V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.3	-4.0			
I_G	Gate Operating Current		-50	pA	V_{DG} = 20V, I_D = 200μA	
	T_A = 125°C		-250	nA		
I_{DSS}	Saturation Drain Current (Note 2)	0.5	5.0	mA	V_{DS} = 20V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000	μmho	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz
		1000				f = 100 MHz
g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		V_{DG} = 20V, I_D = 200μA	
g_{os}	Common-Source Output Capacitance		35		V_{DS} = 20V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		10		V_{DG} = 20V, I_D = 200μA	
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

Matching Characteristics		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	10	10	10	10	10	nA	V_{DG} = 20V, I_D = 200μA	125°C
$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 2)	5	5	5	10	15	%	V_{DS} = 20V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV	V_{DG} = 20V, I_D = 200μA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)	10	25	50	75	100	μV/°C		T_A = 25°C, T_B = 125°C
		10	25	50	75	100			T_A = -55°C, T_B = 25°C
$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 2)	3	5	5	10	15	%		f = 1 kHz
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance	5	5	5	5	5	μmho		

NOTES:
1. Per transistor.
2. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.

U257
Monolithic Dual N-Channel JFET

FEATURES
- g_{fs} > 5000 μmho from DC to 100 MHz
- Matched V_{GS}, g_{fs} and g_{os}

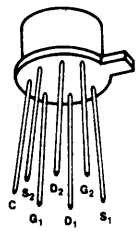
ABSOLUTE MAXIMUM RATINGS
(T$_A$ = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -25V
Gate Current (Note 1) ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/°C	7.7 mW/°C

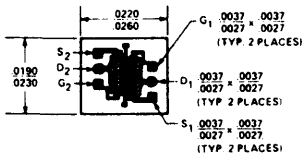
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

6022



ORDERING INFORMATION*

TO-99	WAFER	DICE
U257	U257/W	U257/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-100	pA	V_{GS} = 15 V, V_{DS} = 0	
	T_A = 150°C		-250	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 2)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
g_{os}	Common-Source Output Conductance		150		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		150		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\overline{e_n}$	Equivalent Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 2)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.85	1			f = 1 kHz
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTES:
1. Per transistor.
2. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

U304-U306
P-Channel JFET

FEATURES
- **Low ON Resistance**
- **$I_{D(off)}$ <500 pA**
- **Switches directly from T^2L Logic (U306)**

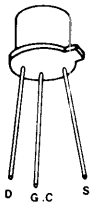
1

APPLICATIONS
- Analog Switches
- Commutators
- Choppers

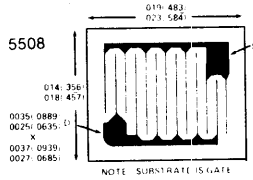
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current ..... 50 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Power Dissipation ..... 350 mW
Derate above 25°C ..... 2.8 mW/°C

PIN CONFIGURATION
TO-18



CHIP TOPOGRAPHY (Note 1)



ORDERING INFORMATION*

TO-18	WAFER	DICE
U304	U304/W	U304/D
U305	U305/W	U305/D
U306	U306/W	U306/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted.

Parameter		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions
I_{GSSR}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20V, V_{DS} = 0
	T_A = 150°C		1.0		1.0		1.0	µA	
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 µA, V_{DS} = 0
$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	V_{DS} = -15V, I_D = -1µA
$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6	V	V_{GS} = 0, I_D = -15mA(U304), I_D = -7mA (U305), I_D = -3mA (U306)
I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	V_{DS} = -15V, V_{GS} = 0
$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15V, V_{GS} = 12V (U304) V_{GS} = 7V (U305) V_{GS} = 5V (U306)
	T_A = 150°C		-1.0		-1.0		-1.0	µA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0V, I_D = -1mA
$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0V, I_D = 0 f = 1 kHz
C_{iss}	Common-Source Input Capacitance		27		27		27	pF	V_{DS} = -15V, V_{GS} = 0
C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7	pF	V_{DS} = 0, V_{GS} = 12V (U304) V_{GS} = 7V (U305), V_{GS} = 5V (U306) f = 1 MHz

	U304	U305	U306
V_{DD}	-10V	-6V	-6V
$V_{GS(off)}$	12V	7V	5V
R_L	580Ω	743Ω	1800Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15mA	-7mA	-3mA

$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns	
t_r	Rise Time		15		25		35	ns	
$t_{d(off)}$	Turn-OFF Delay Time		10		15		20	ns	
t_f	Fall Time		25		40		60	ns	

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300µs, duty cycle ≤3%.

U308-U310
N-Channel JFET

FEATURES

- **Industry Standard Part in Low Cost Plastic Package**
- **High Power Gain**
- **Low Noise**
- **Dynamic Range Greater than 100 dB**
- **Easily Matched to 75Ω Input**

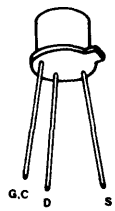
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

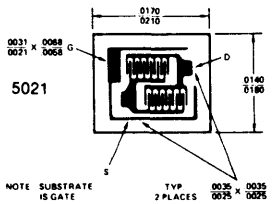
Gate-Drain or Gate-Source Voltage	-25V
Gate Current	20 mA
Storage Temperature	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Led Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	500 mW
Derate above 25°C	4mW/°C

PIN CONFIGURATIONS

TO-52



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-52	WAFER	DICE
U308	U308/W	U308/D
U309	U309/W	U309/D
U310	U310/W	U310/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	U308			U309			U310			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSSR}	Gate Reverse Current			-150			-150			-150	pA	V_{GS} = -15 V	
	T_A = 125°C			-150			-150			-150	nA	V_{GS} = 0	
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
g_{ogs}	Common-Gate Output Conductance			150			150			150	μmho		
C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = -10 V, V_{DS} = 10 V	f = 1 MHz
C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
			14			14			14				f = 450 MHz
g_{ogs}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 100 MHz
			0.32			0.32			0.32				f = 450 MHz
G_{pg}	Common-Gate Power Gain		16			16			16		dB		f = 100 MHz
			11			11			11				f = 450 MHz
NF	Noise Figure		1.5			1.5			1.5				f = 100 MHz
			2.7			2.7			2.7				f = 450 MHz

NOTE: Pulse test duration = 2 ms.

U401-U406
Monolithic Dual N-Channel JFET

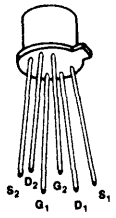
FEATURES

- **Minimum System Error and Calibration**
- **Low Drift with Temperature**
- **Operates from Low Power Supply Voltages**
- **High Output Impedance**

1

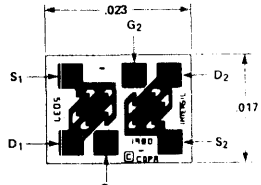
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6037



ORDERING INFORMATION*

TO-71	WAFER	DICE
U40X	U40X/W	U40X/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) 50V
Gate Current (Note 1) ..... 10 mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	300 mW	500 mW
Derate above 25°C ..	2.6 mW/°C	5 mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25° unless otherwise noted.

Parameters		U401		U402		U403		U404		U405		U406		Unit	Test Conditions	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		V	V_{DS} = 0, I_G = -1μA	
I_{GSS}	Gate Reverse Current (Note 2)		-25		-25		-25		-25		-25		-25	pA	V_{DS} = 0, V_{GS} = -30V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	V	V_{DS} = 15V, I_D = 1 nA	
$V_{GS(on)}$	Gate-Source Voltage (on)		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3		V_{DG} = 15V, I_D = 200μA	
I_{DSS}	Saturation Drain Current (Note 3)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10V, V_{GS} = 0	
I_G	Operationg Gate Current (Note 2) T_A = 125°C		-15		-15		-15		-15		-15		-15	pA	V_{DG} = 15V, I_D = 200μA	
			-10		-10		-10		-10		-10		-10	nA		
BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1μA	
g_{fs}	Common-Source Forward Transconductance (Note 3)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
g'_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600			f = 1 kHz
g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0		V_{DG} = 15V, I_D = 200μA	
C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
e_n	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15V, V_{GS} = 0	f = 10 Hz
CMRR	Common-Mode Rejection Ratio (Note 4)	95		95		95		95		90				dB	V_{DG} = 10 to 20V, I_D = 200μA	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10V, I_D = 200μA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 5)		10		10		25		25		40		80	μV/°C	V_{DG} = 10V, I_D = 200μA	T_A = -55°C, T_B = +25°C, I_D = 200μA T_C = +125°C

NOTES:

1. Per transistor.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
4. Measured at end points, T_A and T_B.
5. $CMRR = 20 \log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS_1}-V_{GS_2}\rvert}\right]$, ΔV_{DD} = 10 V.

U1897-U1899
N-Channel JFET

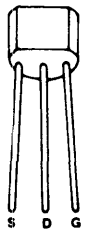
FEATURES
- **Low Insertion Loss**
- **No Error or Offset Voltage Generated by Closed Switch**

APPLICATIONS
Analog Switches, Choppers

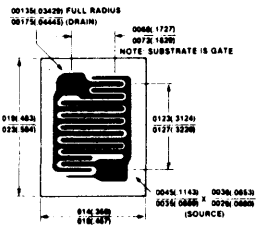
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... -40V
Forward Gate Current ..... 10 mA
Storage Temperature Range .. -65°C to +200°C
Operating Temperature Range..-55°C to +150°C
Lead Temperature (Soldering, 10 sec)... +300°C
Power Dissipation ..... 350 mW
Derate above 25°C ..... 3.5 mW/°C

PIN CONFIGURATION
TO-92



CHIP TOPOGRAPHY
5001



ORDERING INFORMATION*

TO-92	TO-92-18	WAFER	DICE
U1897	U1897-18	U1897/W	U1897/D
U1898	U1898-18	U1898/W	U1898/D
U1899	U1899-18	U1899/W	U1899/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted

	PARAMETERS	U1897 MIN	U1897 MAX	U1898 MIN	U1898 MAX	U1899 MIN	U1899 MAX	UNIT	TEST CONDITIONS
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1μA, V_{DS} = 0
I_{GSSR}	Gate Reverse Current		-400		-400		-400	pA	V_{GS} = -20V, V_{DS} = 0
I_{DGO}	Drain-Gate Leakage Current		200		200		200	pA	V_{DG} = 20V, I_S = 0
I_{SGO}	Source-Gate Leakage Current		200		200		200	pA	V_{SG} = 20V, I_D = 0
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 20V, V_{GS} = -12V (U1897)
	T_A = 85°C		10		10		10	nA	V_{GS} = -8V (U1898) V_{GS} = -6V (U1899)
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5.0	-10	-2.0	-7.0	-1.0	-5.0	V	V_{DS} = 20V, I_D = 1 na
I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	V_{DS} = 20V, V_{GS} = 0
$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	V_{GS} = 0, I_D = 6.6mA (U1897) I_D = 4.0mA (U1898) I_D = 2.5mA (U1899)
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	I_D = 1mA, V_{GS} = 0
C_{dg}	Drain-Gate Capacitance		5		5		5	pF	V_{DG} = 20V, I_S = 0 f = 1 MHz
C_{sg}	Source-Gate Capacitance		5		5		5	pF	V_{SG} = 20V, I_D = 0 f = 1 MHz
C_{iss}	Common-Source Input Capacitance		16		16		16	pF	V_{DS} = 20V, V_{GS} = 0 f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5	pF	V_{DS} = 20V, V_{GS} = 0 f = 1 MHz
$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions
t_r	Rise Time		10		20		40	ns	
t_{off}	Turn OFF Time		40		60		80	ns	

Switching Time Test Conditions	U1897	U1898	U1899
V_{DD}	3V	3V	3V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	-12V	-8V	-6V
R_L	425Ω	770Ω	1120Ω
$I_{D(on)}$	6.6mA	4mA	2.5mA

NOTE: 1. Pulse test pulsewidth = 300 μs; duty cycle < 3%

VCR2N/3P/4N/7N Voltage Controlled Resistors

1

APPLICATIONS

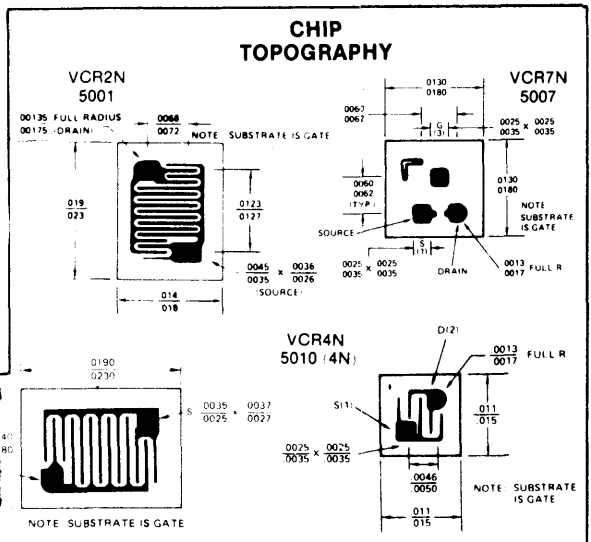
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

ABSOLUTE MAXIMUM RATINGS

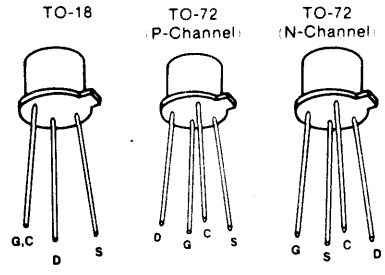
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 15V
Gate Current ..... 10 mA
Storage Temperature Range .. -65°C to +200°C
Operating Temperature Range...-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)...+300°C
Power Dissipation .....300 mW
Derate above 25°C ..... 2 mW/°C

CHIP TOPOGRAPHY



PIN CONFIGURATIONS



ORDERING INFORMATION*

TO-18	TO-72	WAFER	DICE
VCR2N	—	VCR2N/W	VCR2N/D
VCR4N	—	VCR4N/W	VCR4N/D
—	VCR3P	VCR3P/W	VCR3P/D
—	VCR7N	VCR7N/W	VCR7N/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

	Parameter		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15V, V_{DS} = 0	
	BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5		I_D = 1 μA, V_{DS} = 10V	
	$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10V, I_S = 0	f = 1 MHz
	C_{sgo}	Source-Gate Capacitance		7.5		3		1.5		V_{GS} = -10V, I_D = 0	

P-Channel VCR FETs

	Parameter		VCR3P		Unit	Test Conditions	
STATIC	I_{GSS}	Gate Reverse Current		20	nA	V_{GS} = 15V, V_{DS} = 0	
	BV_{GSS}	Gate-Source Breakdown Voltage	15		V	I_G = 1μA, V_{DS} = 0	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7		I_D = -1μA, V_{DS} = -10V	
	$r_{ds(on)}$	Drain-Source ON Resistance	70	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
DY	C_{dgo}	Drain-Gate Capacitance		6	pF	V_{GD} = 10V, I_S = 0	f = 1 MHz
	C_{sgo}	Source-Gate Capacitance		6		V_{GS} = 10V, I_D = 0	

JFETS AS VOLTAGE CONTROLLED RESISTORS

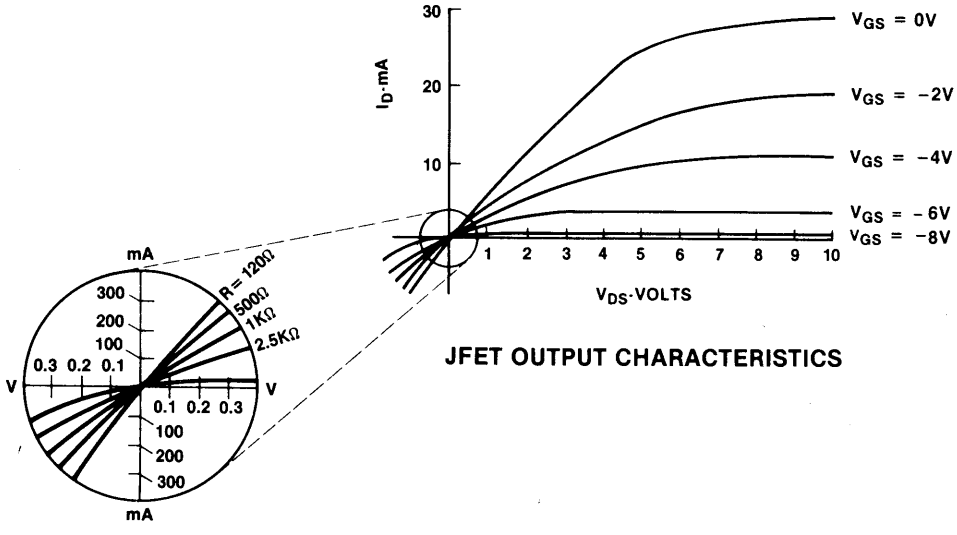
The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of VDS = 0 for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about 100kΩ.

Best gate control voltage for best linearity is up to about $0.8V_{PK}$; ON resistance increases rapidly beyond this point.



JFET OUTPUT CHARACTERISTICS

JFET OUTPUT CHARACTERISTICS ENLARGED AROUND V_{DS} = 0

FIGURE 1

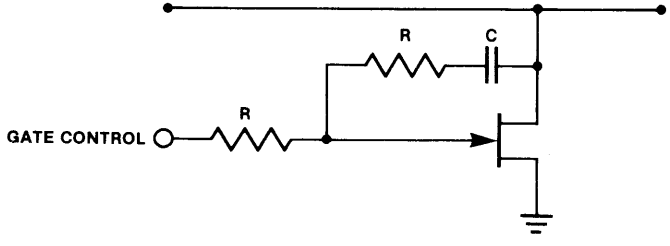


FIGURE 2

Digital

Memory

	Page
NMOS ROMs	
IM7332	2-18
IM7364	2-21
CMOS EPROMs	
IM6653/4	2-11

Peripherals

IM6402/3	2-3
82C43	2-24

Gate Arrays

IGC10000	2-28

DIGITAL

ROMs

Organization	Max Access Time (ns)	I_{DD} Max(mA)	No. Pins	Package*	Temp Range*
4096 x 8 IM7332	300	80	24	J,P	C
8192 x 8 IM7364	350	150	24	J,P	C

EPROMs

Organization	Max Access Time (ns)	V_{CC} (V)	I_{CC} Max (mA) Operating	I_{CC} Max (μA) Standby	No. Pins	Package*	Temp Range
1024 x 4							
IM6653	550	5	6	140	24	J	I,M
IM6653A	300	10	12	140	24	J	I,M
512 x 8							
IM6654	550	5	6	140	24	J	I,M
IM6654A	300	10	12	140	24	J	I,M

PERIPHERAL

IM8048 Peripheral

IM82C43 — CMOS I/O Expander

*Package and Temperature Key

F—Flatpack
J—Ceramic Dual In-Line
P—Plastic Dual In-Line
D-Ceramic Side Brazed (Not Recommended for High Volume)

C—Commercial, 0°C to +70°C
I—Industrial, -40°C to +85°C
M—Military, -55°C to +125°C

UARTS

Part Number	Max. Clock Frequency	XTAL Frequency	V Supply	I_{CC} Max.
IM6402	1.0 MHz	—	5.0	1.2 mA
IM6402A	4.0 MHz	—	4-11	9.0 mA
IM6402-1	2.0 MHz	—	5.0	1.9 mA
IM6403	2.46 MHz	2.46 MHz	5.0	3.7 mA
IM6403A	6.0 MHz	6.0 MHz	4-11	13.0 mA
IM6403-1	3.58 MHz	3.58 MHz	5.0	5.5 mA

GATE ARRAYS

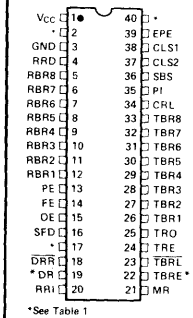
Part Number	Delay	Input Nand Gate Equivalent	I/O Cells	V_{CC}
IGC10408	6 ns	408	34	3-9V
IGC10756	6 ns	756	44	3-9V
IGC11500	6 ns	1500	62	3-9V
IGC12001	6 ns	2001	70	3-9V

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- **Low Power — Less Than 10mW Typ. at 2MHz**
- **Operation Up to 4MHz Clock (IM6402A)**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UART's (IM6402)**
- **On-Chip Oscillator with External Crystal (IM6403)**
- **Operating Voltage —**
  IM6402-1/03-1: 5V
  IM6402A/03A: 4-11V
  IM6402/03: 5V

PIN CONFIGURATION (outline dwg DL, PL)



*See Table 1

TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT CLOCK
2	N/C	Divide Control	Divide Control
17	RRC	XTAL	External Clock Input
19	Tri-State	Always Active	Always Active
22	Tri-State	Always Active	Always Active
40	TRC	XTAL	GND

GENERAL DESCRIPTION

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 6.

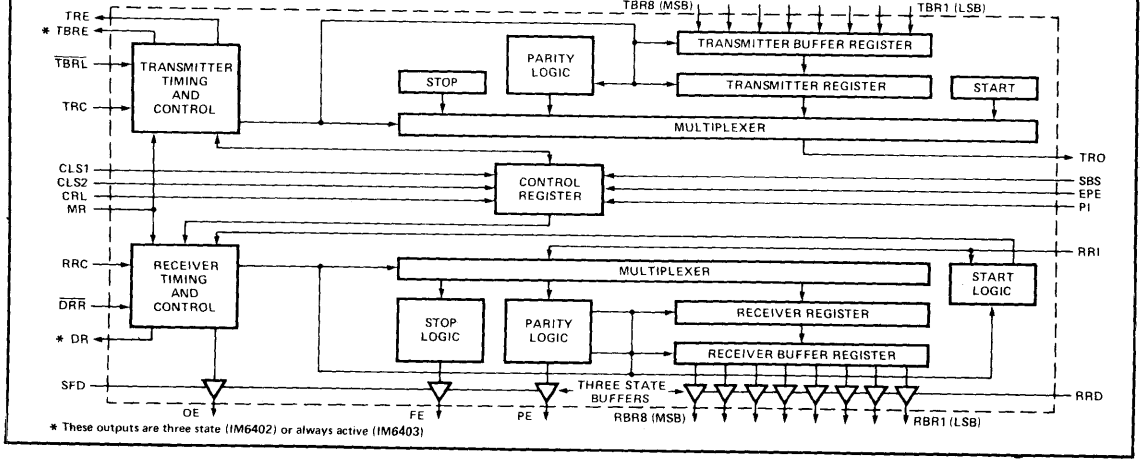
The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 1.

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-IPL
CERAMIC PKG	IM6402-1/03-1IDL	IM6402/03-AIDL	IM6402/03IDL
MILITARY TEMP.	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP. WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

FUNCTIONAL BLOCK DIAGRAM



* These outputs are three state (IM6402) or always active (IM6403)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
IM6402/03 ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-5.0		5.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL}=1.6mA			0.45	V
6	I_{OLK}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-5.0		5.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	800	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 500 KHz			1.2	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 2.46MHz			3.7	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.		1.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403				2.46	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
4	t_{mr}	Pulse Width MR		600	200		ns
5	t_{ds}	Input Data Setup Time		75	20		ns
6	t_{dh}	Input Data Hold Time		90	40		ns
7	t_{en}	Output Enable Time			80	190	ns

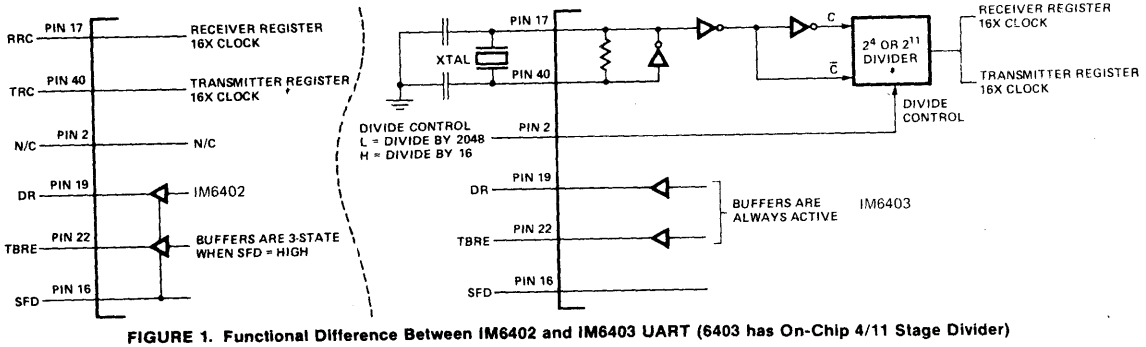


FIGURE 1. Functional Difference Between IM6402 and IM6403 UART (6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three Inputs (RRC, TRC, pin 2) as shown in Figure 1. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 10). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402AI/03AI ..... -40°C to +85°C
- Military IM6402AM/03AM ..... -55°C to +125°C

Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.0V to 11.0V, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		5.0	500	µA
8	I_{CC}	Power Supply Current IM6402A Dynamic	f_c = 4MHz			9.0	mA
9	I_{CC}	Power Supply Current IM6403A Dynamic	$f_{crystal}$ = 3.58MHz			13.0	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10.0V ± 5%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_c	Clock Frequency IM6402A	See Timing Diagrams (Figures 2,3,4)	D.C.		4.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403A				6.0	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
4	t_{mr}	Pulse Width MR		400	200		ns
5	t_{ds}	Input Data Setup Time		40	0		ns
6	t_{dh}	Input Data Hold Time		30	30		ns
7	t_{en}	Output Enable Time			40	70	ns

TIMING DIAGRAMS

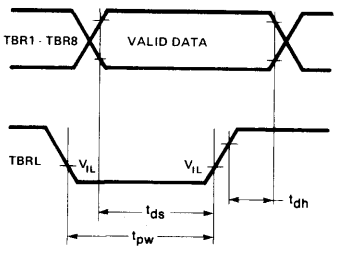


FIGURE 2. Data Input Cycle

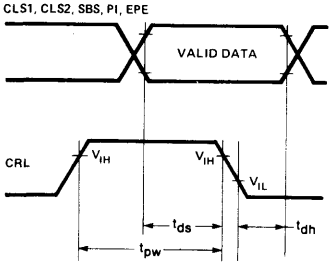


FIGURE 3. Control Register Load Cycle

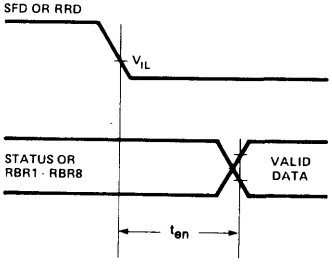


FIGURE 4. Status Flag Enable Time or Data Output Enable Time

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402-1I/03-1I ..... -40°C to +85°C
- Military IM6402-1M/03-1M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

2

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = Industrial or Military

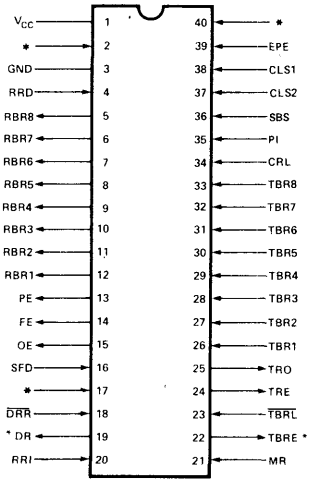
	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH}=-0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	100	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 2MHz			1.9	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 3.58MHz			5.5	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.		2.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403				3.58	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
4	t_{mr}	Pulse Width MR		400	200		ns
5	t_{ds}	Input Data Setup Time		50	20		ns
6	t_{dh}	Input Data Hold Time		60	40		ns
7	t_{en}	Output Enable Time			80	160	ns



*DIFFERS BETWEEN IM6402 AND IM6403.

FIGURE 5. Pin Configuration

IM6403 FUNCTIONAL PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$: active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, *TBRE* to a high impedance state. See Block Diagram and Figure 4. *IM6402 only.
17	IM6402-RRC IM6403-XTAL or EXT CLK IN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 2.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.

IM6403 FUNCTIONAL PIN DEFINITION
(Continued)

PIN	SYMBOL	DESCRIPTION
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 3.

IM6403 FUNCTIONAL PIN DEFINITION
(Continued)

PIN	SYMBOL	DESCRIPTION
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL or GND	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TABLE 2. Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 6) on the TROutput terminal.

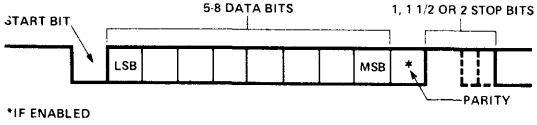


FIGURE 6. Serial Data Format

Transmitter timing is shown in Figure 7. Ⓐ Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{\text{TBR}}$Load input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{\text{TBR}}$L. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. Ⓑ The rising edge of $\overline{\text{TBR}}$L clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock, which is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins.

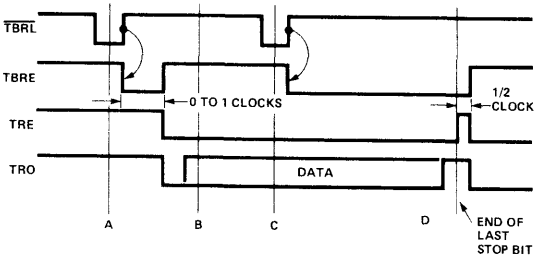


FIGURE 7. Transmitter Timing (Not to Scale)

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 8.

Ⓐ A low level on $\overline{\text{DRR}}$eset clears the DReady line. Ⓑ During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. Ⓒ 1/2 clock cycle later, DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

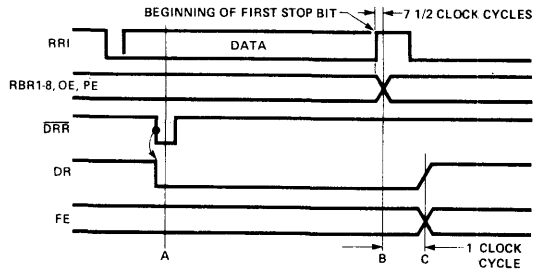


FIGURE 8. Receiver Timing (Not to Scale)

START BIT DETECTION

The receiver uses a 16X clock for timing (see Figure 9.) The start bit Ⓐ could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

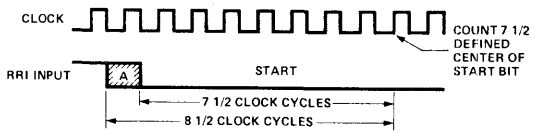


FIGURE 9. Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 10 shows how the IM6403 can be interfaced to an IM6100 microcomputer system with the aid of an IM6101 Programmable Interface Element (PIE). The PIE interprets Input/Output transfer (IOT) instructions from the processor and generates read and write pulses to the UART. The SENSE lines on the PIE are also employed to allow the processor to detect UART status. In particular, the processor must know when the Receive Buffer Register has accumulated a character (DR active), and when the Transmit Buffer Register can accept another character to be transmitted.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs should be committed.

The baud rate at which the transmitter and receiver will operate is determined by the external crystal and DIVIDE CONTROL pin on the IM6403. The internal divider can be set to reduce the crystal frequency by either 16 (PIN 2:HIGH) or 2048 (PIN 2:LOW) times. The frequency out of the internal divider should be 16 times the desired baud rate. To generate 110 baud, this example will use a 3.579545MHz color TV crystal

and DIVIDE CONTROL set low. The IM6402 may use different receive (RRC) and transmit (TRC) clock rates, but requires an external clock generator.

To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM6100 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not re-trigger RESET. A long reset pulse after power-up (~100ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

2

The IM6402 supports the processor's bi-directional data bus quite easily by tying the TBR and RBR buses together. A read command from the processor will enable the RECEIVER BUFFER REGISTER onto the bus by using the RECEIVER REGISTER DISABLE (RRD) pin. A write command from the processor clocks data from the bus into the TRANSMITTER BUFFER REGISTER using $\overline{TBRL}$. Figure 10 shows a NAND gate driving $\overline{TBRL}$ from the $\overline{WRITE_2}$ pin on the PIE. This gate is used to generate a rising edge to $\overline{TBRL}$ at the point where data is stable on the bus, and to hold $\overline{TBRL}$ high until the UART actually transfers the data to it's internal buffer. If $\overline{TBRL}$ were allowed to return low before TBRE went high, the intended output data would be overwritten, since the TBR is a transparent latch.

Although not shown in this example, the error flags (PE, FE, OE) could be read by the processor, using the other READ line from the PIE. Since an IM6403 is used, TBRE and DR are not affected by the STATUS FLAGS DISABLE pin, thus, the three error flags can be tied to the data bus and gated by connecting SFD to $\overline{READ_2}$.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The $\overline{OE}$ pin will stay high until the next received stop bit after a $\overline{DRR}$ is performed.

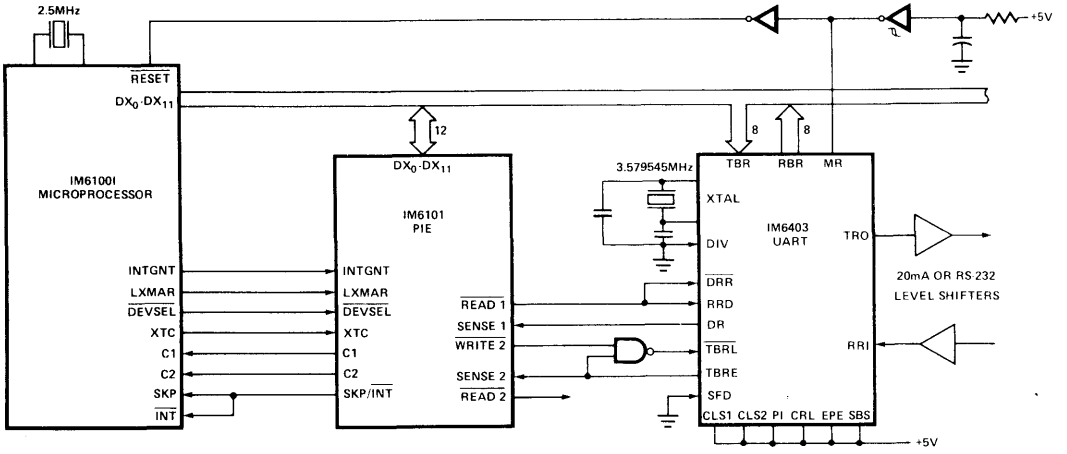


FIGURE 10. 110 Baud Serial Interface for IM6100 System

IM6653/IM6654
4096 Bit CMOS
UV Erasable PROM

FEATURES

- **Organization — IM6653: 1024 x 4**
  IM6654: 512 x 8
- **Low Power — 770μW Maximum Standby**
- **High Speed**
  — 300ns 10V Access Time for IM6653/54 AI
  — 450ns 5V Access Time for IM6653/54-1I
- **Single +5V supply operation**
- **UV erasable**
- **Synchronous operation for low power dissipation**
- **Three-state outputs and chip select for easy system expansion**
- **Full −55°C to +125°C MIL range devices— IM6653/54 M, IM6653A/64A M**

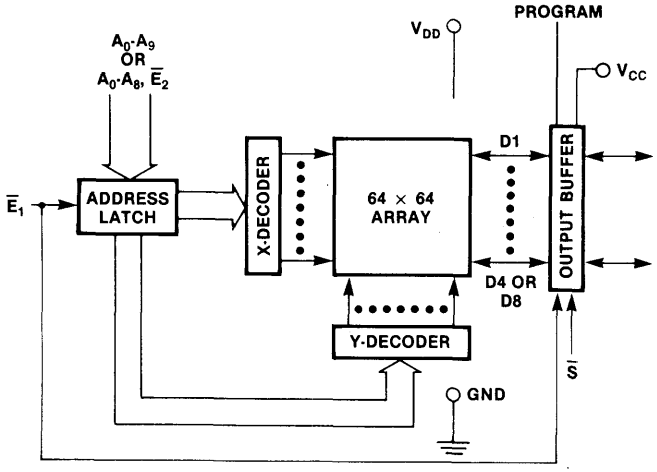
GENERAL DESCRIPTION

The Intersil IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

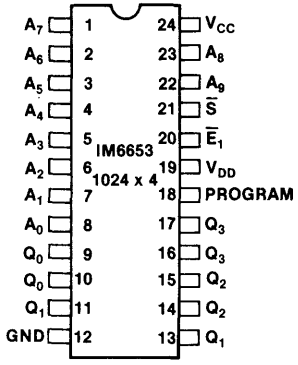
2

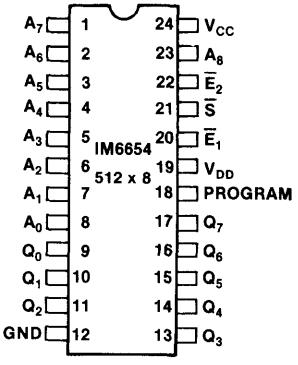
BLOCK DIAGRAM



PIN CONFIGURATION

(outline dwg JG/W)





ORDERING INFORMATION

24 PIN PACKAGE		SELECTION/TEMPERATURE RANGE				
		INDUSTRIAL			MILITARY	
		STD 5V	HI SPEED 5V	STD 10V	STD 5V	STD 10V
CERDIP (FRIT SEAL)	JG	IJG	-1I JG	AIJG	MJG	AMJG

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... +8.0V
- $V_{CC} = V_{DD}$ ..... +8.0V

Input or Output Voltage Supplied ..... GND – 0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... – 65°C to + 150°C
Operating Range
- Temperature
  - Industrial ..... – 40°C to + 85°C
  - Military ..... – 55°C to + 125°C
- Voltage
  - 6653/54 I, – 1I ..... 4.5 – 5.5
  - 6653/54 M ..... 4.5 – 5.5

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 10\%$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54I, -1I,M		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1, \overline{S}$	$V_{DD} - 2.0$		V
	V_{IH}	Address Pins	2.7		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \leq V_{IN} \leq V_{DD}$	– 1.0	1.0	μA
Logical "1" Output Voltage	$V_{OH}2$	$I_{OUT} = 0$	$V_{CC} - 0.01$		V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2mA$	2.4		
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$		GND + 0.01	
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 2.0mA$		0.45	
Output Leakage	I_{OLK}	$GND \leq V_O \leq V_{CC}$	– 1.0	1.0	μA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100	
	I_{CC}	$V_{IN} = V_{DD}$		40	
Operating Supply Current	I_{DDOP}	f = 1 MHz		6	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 10\%$, $C_L = 50pf$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6653/54-1I		IM6653/54 I		IIM6653/54 M		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		450		550		600	ns
Output Enable Time	TSLQV		110		140		150	
Output Disable Time	TE_1HQZ		110		140		150	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	130		150		150		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	450		550		600		
Address Setup Time	$TAVE_1L$	0		0		0		
Address Hold Time	TE_1LAX	80		100		100		
Chip Enable Setup Time (6654)	TE_2VE_1L	0		0		0		
Chip Enable Hold Time (6654)	TE_1LE_2X	80		100		100		

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... +11.0V
- $V_{CC} = V_{DD}$ ..... +11.0V

Input or Output Voltage Supplied ..... GND − 0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
- Temperature
  - Industrial ..... −40°C to +85°C
  - Military ..... −55°C to +125°C
- Voltage
  - 6653/54 AI, AM ..... 4.5 to 10.5V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 4.5V$ to 10.5V, T_A = Operational Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54AI, AM		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1, \overline{S}$	$V_{DD} - 2.0$		V
	V_{IH}	Address Pins	$V_{DD} - 2.0$		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \le V_{IN} \le V_{DD}$	-1.0	1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	$V_{CC} - 0.01$		V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$		GND + 0.01	
Output Leakage	I_{OLK}	$GND \le V_O \le V_{CC}$	−1.0	1.0	μA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100	
	I_{CC}	$V_{IN} = V_{DD}$		40	
Operating Supply Current	I_{DDOP}	f = 1 MHz		12	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 10V \pm 5\%$, $C_L = 50pf$, T_A = Operating Temperature Range

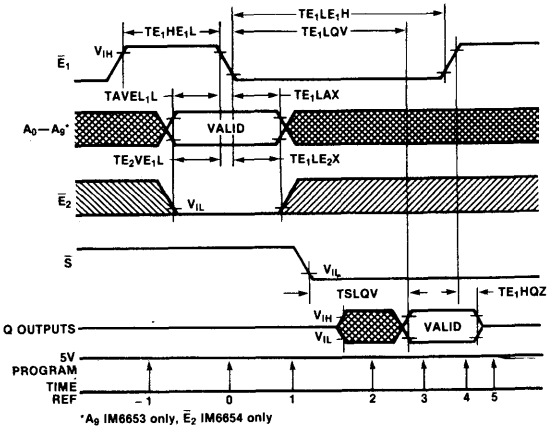
PARAMETER	SYMBOL	IM6653/54 AI		IM6653/54 AM		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		300		350	ns
Output Enable Time	TSLQV		60		70	
Output Disable Time	TE_1HQZ		60		70	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	125		125		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	300		350		
Address Setup Time	$TAVE_1L$	0		0		
Address Hold Time	TE_1LAX	60		60		
Chip Enable Setup Time (6654)	TE_2VE_1L	0		0		
Chip Enable Hold Time (6654)	TE_1LE_2X	60		60		

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	—	Address Lines
9-11,13-17	Q_0-Q_7	—	Data Out lines, 6654
	Q_0-Q_3	—	Data Out lines, 6653
12	GND	—	
18	Program	—	Programming pulse input
19	V_{DD}	—	Chip V+ supply, normally tied to V_{CC}
20	$\overline{E}_1$	L	Strobe line, latches both address lines and, for 6654, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
22	A_9	—	Additional address line for 6653
	$\overline{E}_2$	L	Chip enable line, latched by Chip enable $\overline{E}_1$ on 6654
24	V_{CC}	—	Output buffer + V Supply

2

READ CYCLE TIMING



*A_9 IM6653 only, $\overline{E}_2$ IM6654 only

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T = 0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T = 3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

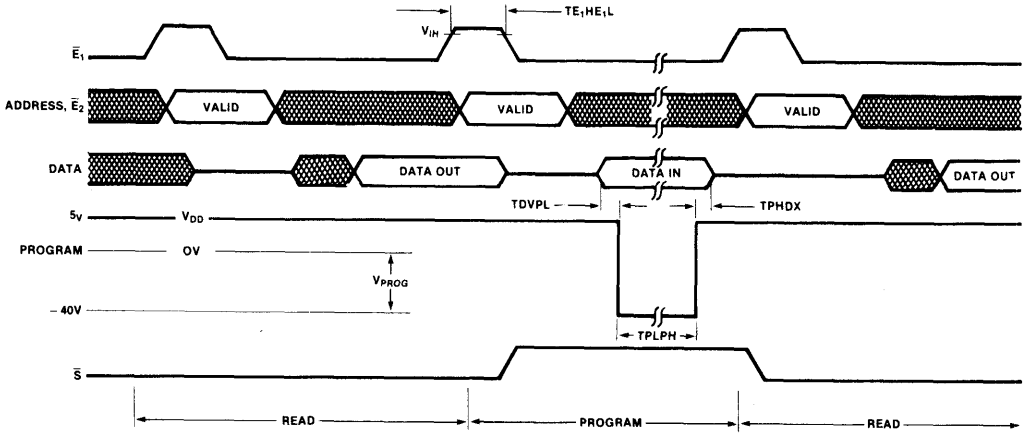
The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

FUNCTION TABLE

TIME REF	INPUTS $\overline{E1}$	INPUTS $\overline{E2}$*	INPUTS $\overline{S}$	INPUTS A	OUTPUTS Q	NOTES
-1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS -1)

READ AND PROGRAM CYCLES



DC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pin Load Current	I_{PROG}			80	100	mA
Programming Pulse Amplitude	V_{PROG}		38	40	42	V
V_{CC} Current	I_{CC}			0.1	5	mA
V_{DD} Current	I_{DD}			40	100	
Address Input High Voltage	V_{IHA}		$V_{DD} - 2.0$			V
Address Input Low Voltage	V_{ILA}				0.8	
Data Input High Voltage	V_{IH}		$V_{DD} - 2.0$			
Data Input Low Voltage	V_{IL}				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pulse Width	TPLPH	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
Program Pulse Duty Cycle					75%	
Data Setup Time	TDVPL		9			μs
Data Hold Time	TPHDX		9			
Strobe Pulse Width	TE_1HE_1L		150			ns
Address Setup Time	$TAVE_1L$		0			
Address Hold Time	TE_1LE_1X		100			
Access Time	TE_1LQV				1000	

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V_{CC} and V_{DD} are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at $V_{DD} - 2V$ minimum. Low logic levels must be set at GND + .8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to −40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences, such as the Intersil 6920 CMOS EPROM programmer, is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

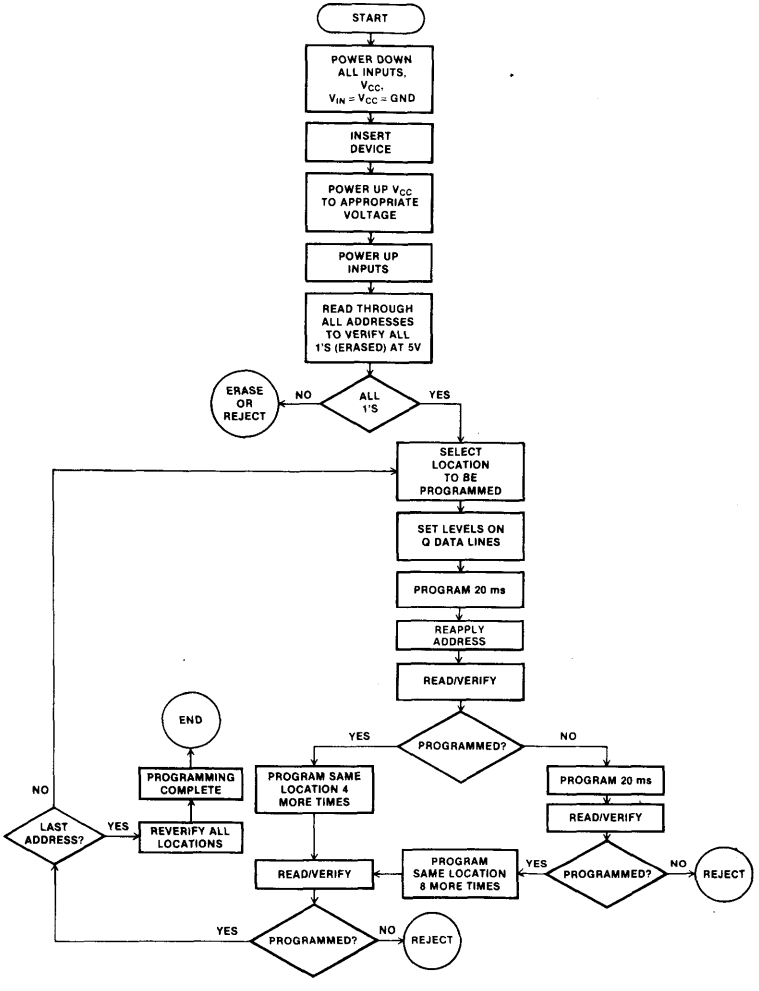
1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to -40 volts ($\pm 2V$) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V_{CC}, V_{DD} of 5V $\pm 5\%$.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

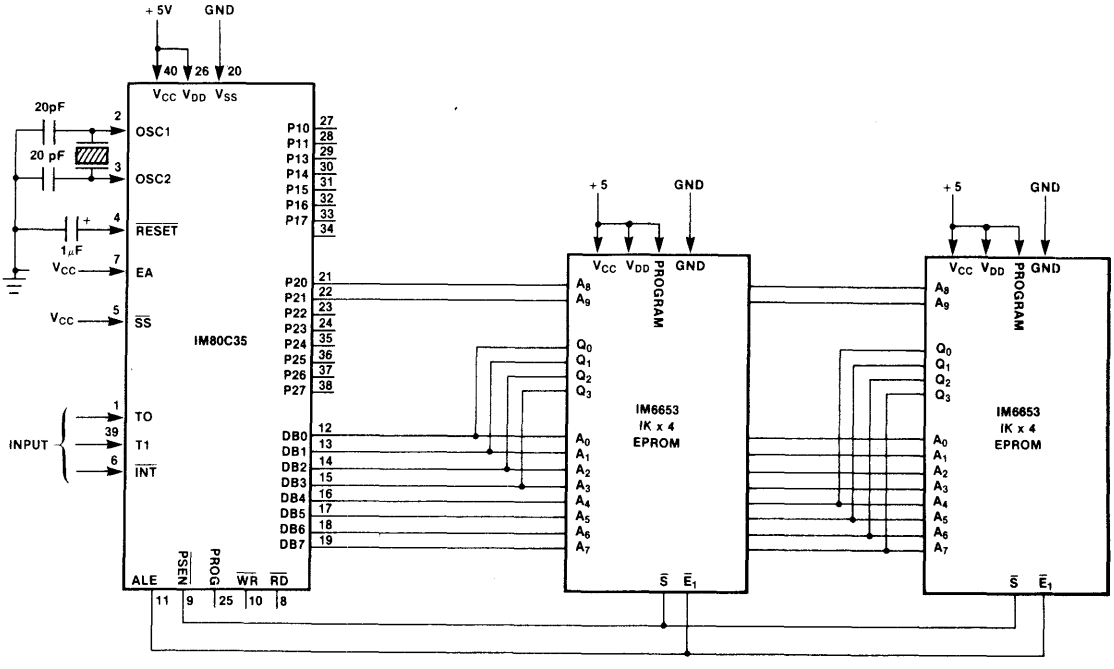
The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 Å. The recommended integrated dose (i.e.,UV intensity x exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cummulative. Care should be taken to protect EPROMs from exposure to direct sunlight or florescent lamps radiating UV light in the 2000Å to 4000Å range.

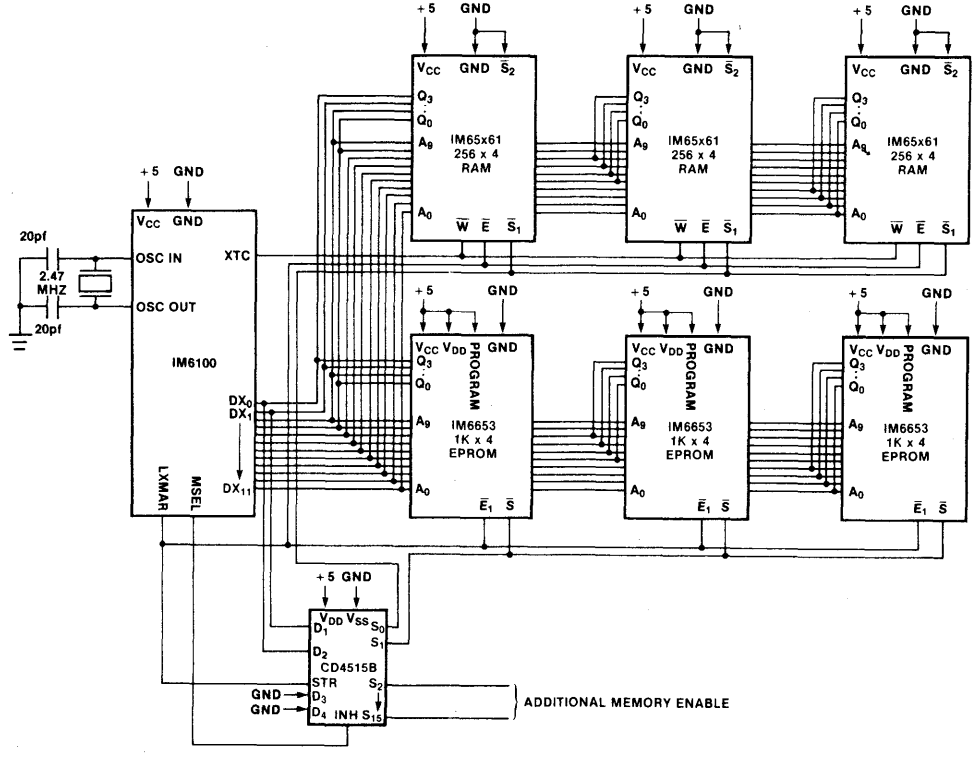
PROGRAMMING FLOW CHART



IM6653 CMOS EPROMS AS EXTERNAL PROGRAM MEMORY WITH THE IM80C35



IM6653 CMOS EPROMS AS PROGRAM MEMORY WITH THE IM6100



IM7332
32,768 BIT
(4096 x 8) HMOS ROM

FEATURES

- **High Speed — 300ns Maximum access time**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL Compatible**
- **Two programmable Chip Selects**
- **Three-state outputs**
- **Industry standard 24 lead pinout**

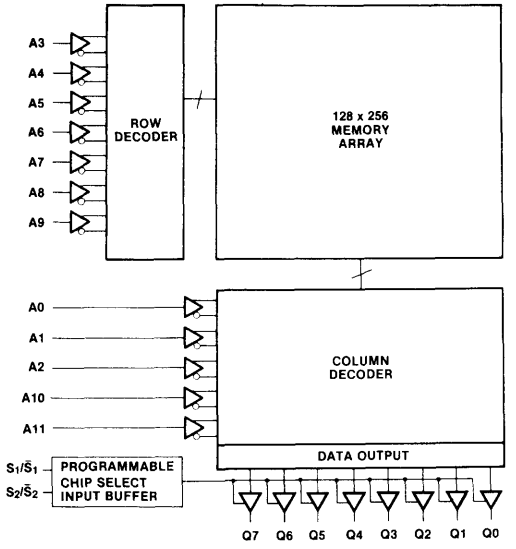
GENERAL DESCRIPTION

The IM7332 is a 32,768 bit read-only memory (ROM) organized 4096 words by 8 bits. The device is fabricated using Intersil's HMOS technology to minimize cell area and optimize circuit performance.

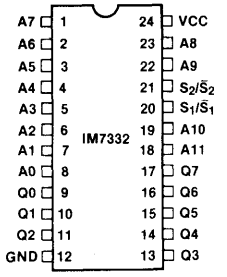
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Two chip select inputs which are programmable to either active high or active low, facilitate ease of memory expansion.

The IM7332 operates over 5V ±5% at 75mA with an access time of 300ns.

LOGICAL BLOCK DIAGRAM

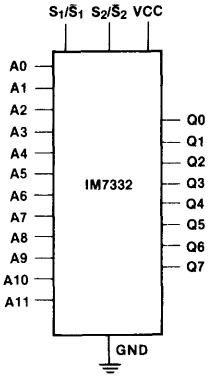


PIN CONFIGURATION



(outline dwgs JG, PG)

LOGIC SYMBOL



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM7332CPG	24 Pin PLASTIC	0°C to +70°C
IM7332 CJG	24 Pin CERDIP	0°C to +70°C

PIN NAMES

$A_0 - A_{11}$	ADDRESS INPUTS
$Q_0 - Q_7$	DATA OUTPUTS
$S_1/\bar{S}_1$, $S_2/\bar{S}_2$	PROGRAMMABLE CHIP SELECTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Voltage on Any Pin Relative to GND ..... −0.5V to +7.0V
Commercial Operating Temperature Range ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation 1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

TEST CONDITIONS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C

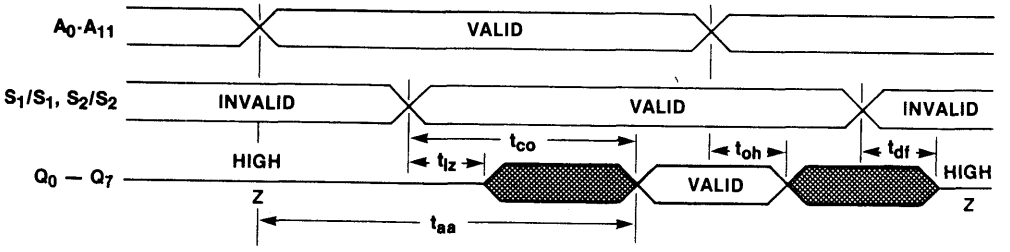
DESCRIPTION	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−0.5		0.8	V
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−10		10	μA
Output High Voltage	V_{OH}	I_{OUT} = -400μA $S_1/\bar{S}_1 = S_2/\bar{S}_2$ = 2.0V/0.8V	2.4			V
Output Low Voltage	V_{OL}	I_{OUT} = 2.1mA $S_1/\bar{S}_1 = S_2/\bar{S}_2$ = 2.0V/0.8V			0.4	V
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V $S_1/\bar{S}_1 = S_2/\bar{S}_2$ = 0.8V/2.0V	−10		10	μA
Operating Supply Current	I_{CC}	T_A = 0°C, Data Out Open V_{IN} = 5.25V, $S_1/\bar{S}_1 = S_2/\bar{S}_2$ = 2.0V/0.8V			75	mA
Input Capacitance	C_{IN}	V_{CC} = 5.0V, V_{IN} = 2.0V			7	pF
Output Capacitance	C_{OUT}	V_{CC} = 5.0V, V_{OUT} = 2.0V			10	pF

NOTE: 1. Typical values are measured at V_{CC} = 5.0V and T_A = +25°C.
2. Capacitance values are sampled, not 100% tested.

AC CHARACTERISTICS

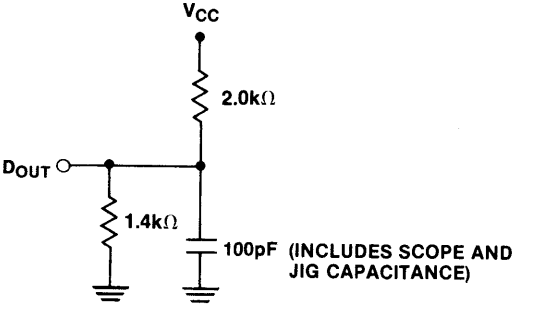
DESCRIPTION	SYMBOL	JEDEC SYMBOL	MIN	TYP	MAX	UNIT
Address Access Time 7332-45	t_{aa}	TAVQV			450	ns
Address Access Time 7332					300	
Chip Select to Low Impedance	t_{lz}	TSVQX	20			
Chip Select Delay	t_{co}	TSVQV			100	
Chip Deselect Delay	t_{df}	TSXQZ			100	
Output Hold Time	t_{oh}	TAXQX	20			

READ CYCLE TIMING



AC TEST CONDITIONS

V_{CC} ..... 5V ± 5%
T_A ..... 0°C to 70°C
Input rise and fall times ..... 20ns (10% to 90%)
Input and output reference level 1.5V



OUTPUT LOAD CIRCUIT

IM7364
65,536 BIT
(8192 x 8) HMOS ROM

FEATURES

- **High Speed — 350ns Maximum access time**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL Compatible**
- **Two Programmable Chip Select**
- **Three-state outputs**
- **Industry standard 24 lead pinout**

GENERAL DESCRIPTION

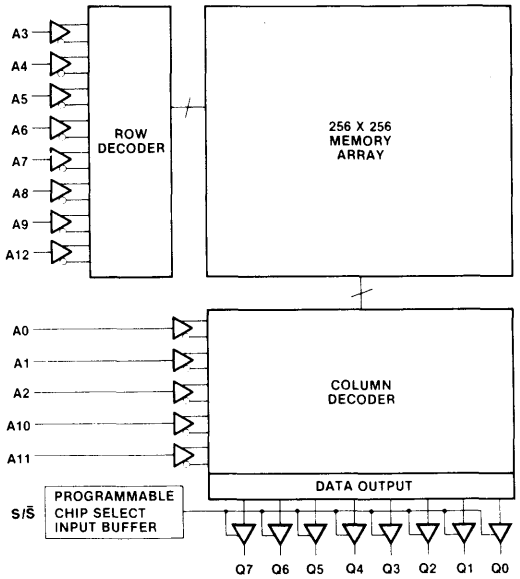
The IM7364 is a 65,536 bit read-only memory (ROM) organized 8192 words by 8 bits. The device is fabricated using Intersil's HMOS technology to minimize cell area and optimize circuit performance.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. A chip select input, which is programmable to either active high or active low, facilitates ease of memory expansion.

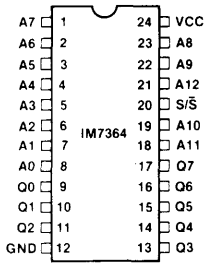
The IM7364 operates over 5V ± 5% at 90mA with an access time of 350ns.

2

LOGICAL BLOCK DIAGRAM

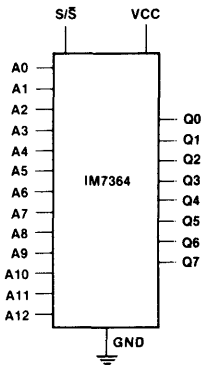


PIN CONFIGURATION



(outline dwgs JG, PG)

LOGIC SYMBOL



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM7364CPG	24 Pin PLASTIC	0°C to +70°C
IM7364 CJG	24 Pin CERDIP	0°C to +70°C

PIN NAMES

$A_0 - A_{12}$	ADDRESS INPUTS
$Q_0 - Q_7$	DATA OUTPUTS
S/S̄	PROGRAMMABLE CHIP SELECT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage on Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C

DESCRIPTION	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−0.5		0.8	V
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−10		10	μA
Output High Voltage	V_{OH}	I_{OUT} = −400μA S/$\overline{S}$ = 2.0V/0.8V	2.4			V
Output Low Voltage	V_{OL}	I_{OUT} = 2.1mA S/$\overline{S}$ = 2.0V/0.8V			0.4	V
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V S/$\overline{S}$ = 0.8V/2.0V	−10		10	μA
Operating Supply Current	I_{CC}	T_A = 0°C, Data Out Open V_{IN} = 5.25V, S/$\overline{S}$ = 2.0V/0.8V			90	mA
Input Capacitance	C_{IN}	V_{CC} = 5.0V, V_{IN} = 2.0V			7	pF
Output Capacitance	C_{OUT}	V_{CC} = 5.0V, V_{OUT} = 2.0V			10	pF

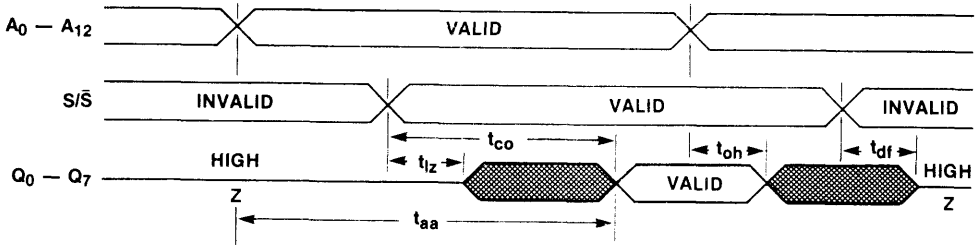
NOTE: 1. Typical values are measured at V_{CC} = 5.0V and T_A = +25°C.
2. Capacitance values are sampled, not 100% tested.

AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	MIN	TYP	MAX	UNIT
Address Access Time 7364-45					450	ns
Address Access Time 7364	t_{aa}	TAVQV			350	
Chip Select to Low Impedance	t_{lz}	TSVQX	20			
Chip Select Delay	t_{co}	TSVQV			120	
Chip Deselect Delay	t_{df}	TSXQZ			120	
Output Hold Time	t_{oh}	TAXQX	20			

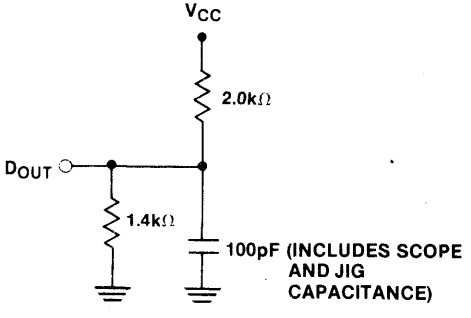
2

READ CYCLE TIMING



AC TEST CONDITIONS

V_{CC} ..... 5V ± 5%
T_A ..... 0°C to 70°C
Input rise and fall times ..... 20ns (10% to 90%)
Input and output reference level 1.5V



OUTPUT LOAD CIRCUIT

IM82C43
CMOS Input/Output Expander

FEATURES

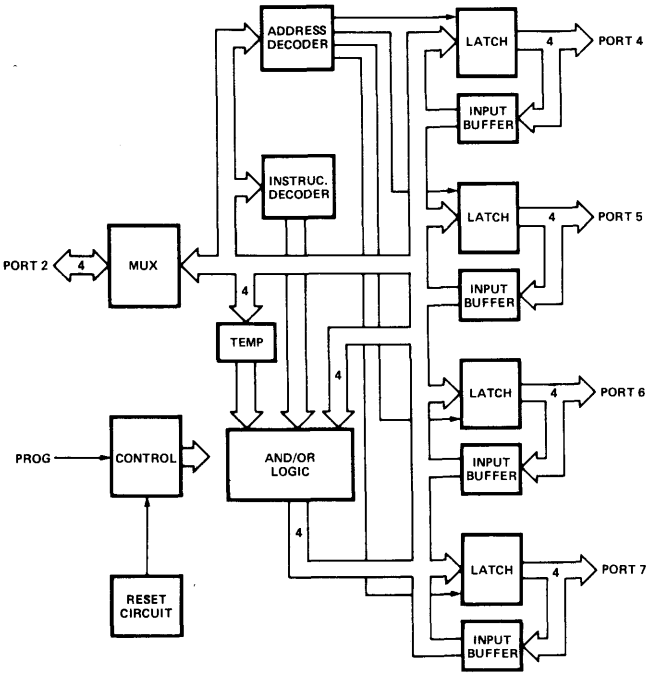
- **8048/41 compatible I/O expander**
- **CMOS pin-for-pin replacement for standard NMOS 8243**
- **Low power dissipation — maximum 25mW active**
- **Four 4-bit I/O ports in 24-pin DIP**
- **Logical AND/OR directly to ports**
- **High output drive**
- **Single +5V supply**

DESCRIPTION

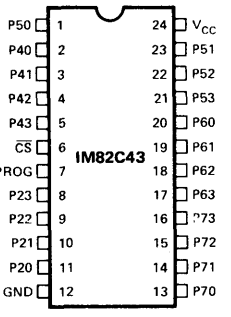
The Intersil IM82C43 is a CMOS input/output expander equivalent to the NMOS 8243. It is designed to provide I/O expansion for the CMOS IM80C48 and NMOS 8048 families of single-chip microcomputers.

The 24-pin IM82C43 provides four 4-bit bidirectional I/O ports: 8048/41 instructions control bidirectional transfers between the 82C43 and the 8048 family microcomputers, and can execute logical AND/OR operations directly on the data contained in the 82C43 ports.

LOGICAL BLOCK DIAGRAM



PIN CONFIGURATION



(outline drawings JG, PG)

ORDERING INFORMATION

PART NO.	PACKAGE
IM82C43CJG	24 PIN CERDIP
IM82C43CPG	24 PIN PLASTIC

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground..Ground -0.5V to V_{CC} +0.5V
Power Dissipation ..... 1 W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Low Voltage	V_{IL}		-0.5		0.8	V
Input High Voltage	V_{IH}	V_{CC} = 4.5	2.0		V_{CC}+0.5	
		V_{CC} = 5.5	2.4		V_{CC}+0.5	
Output Low Voltage Ports 4-7	V_{OL}	I_{OL} = 10mA			0.4	
		I_{OL} = 20mA			0.8	
Output Low Voltage Port 2		I_{OL} = 1.6mA			0.4	
Output High Voltage Ports 4-7	V_{OH}	I_{OH} = 3.2mA	2.8			
Output Voltage Port 2	V_{OH2}	I_{OH} = 1.6mA	2.8			mA
Input Leakage Ports 4-7, Port 2, $\overline{CS}$, PROG	I_{ILK}	V_{IN} = V_{CC} to 0V	-10		10	µA
Supply Current	I_{CC}	WRITE mode, All outputs open, t_k = 700ns		1.6	5.0	mA
Standby Current	I_{CCSB}	V_{IN} = 0 or V_{CC}, $\overline{CS}$ = V_{CC}, All outputs open			100	µA
Sum of all I_{CL} from 16 Outputs	ΣI_{OL}	5 mA each pin average			80	mA

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Code Valid Before PROG	t_a	80 pF Load	100		ns
Code Valid After PROG	t_b	20 pF Load	60		
Data Valid Before PROG	t_c	80 pF Load	140		
Data Valid After PROG	t_d	20 pF Load	20		
Floating After PROG	t_h	20 pF Load	0	150	
PROG Negative Pulse Width	t_k		700		
$\overline{CS}$ Valid Before/After PROG	t_{cs}		50		
Ports 4-7 Valid After PROG	t_{po}	100 pF Load		700	
Ports 4-7 Valid Before/After PROG	t_{ip}		0		
Port 2 Valid After PROG	t_{acc}	80 pF Load		650	

FUNCTIONAL PIN DESCRIPTION

Designator	Pin Number	Function
PROG	7	**Strobe input.** The falling edge of PROG implies valid address and control information on P20-P23, while the rising edge implies valid data on P20-P23.
$\overline{CS}$	6	**Chip select input.** When HIGH, it disables PROG, thus inhibiting change in output or internal status.
P20-P23	8-11	**Four bit bidirectional port** carrying address and control bits on the falling edge of PROG and I/O data on the rising edge of PROG.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1,21-23 17-20 13-16	**Four bit bidirectional I/O ports.** May be configured for input, tri-state output (READ mode) or latched output. Data on pins P20-23 may be directly written, ANDed, or ORed with previous data.
GND	12	**Circuit ground potential**
V_{CC}	24	**+5 volt supply.**

FUNCTIONAL DESCRIPTION

The IM82C43 has four 4-bit I/O ports, which are addressed as Ports 4 thru 7 by the processor. The following operations may be performed on these ports:

- Transfer accumulator to port (write)
- Transfer port to accumulator (read)
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer and the 82C43 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each data transfer consists of two 4-bit nibbles:

- The first contains the port address and command to the 82C43. This is latched from Port 2 during the high-to-low transition of PROG and is encoded as shown in the table on page 3.
- The second contains the four bits of data associated with the instruction. The low-to-high transition of PROG indicates the presence of data.

Port Address And Command Format

P23	P22	INSTRUCTION CODE	P21	P20	ADDRESS CODE
0	0	Read	0	0	Port 4
0	1	Write	0	1	Port 5
1	0	ORLD	1	0	Port 6
1	1	ANLD	1	1	Port 7

Write Modes

The device has three write modes. MOVD P,A directly writes new data into the selected port with old data being lost; ORLD P,A ORs the new data with the old data and writes it to the port; and ANLD P,A ANDs new data with old data and writes it to the selected port.

After the designated operation is performed, the data is latched and directed to the port. The old data remains latched until the new data is written by the rising edge of PROG.

Read Mode

The device has one read mode. The command and port address are latched from port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the designated port output buffers are disabled and the input buffers enabled. The read operation is terminated by the low-to-high transition of the PROG pin. The port selected is switched to the high impedance state while port 2 is returned to the input mode.

Normally a port will be in an output mode (write) or input mode (read). The first read of a port, following a mode change from write to read should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 82C43 output. A read of any port will leave that port in a high impedance state.

I/O Expansion

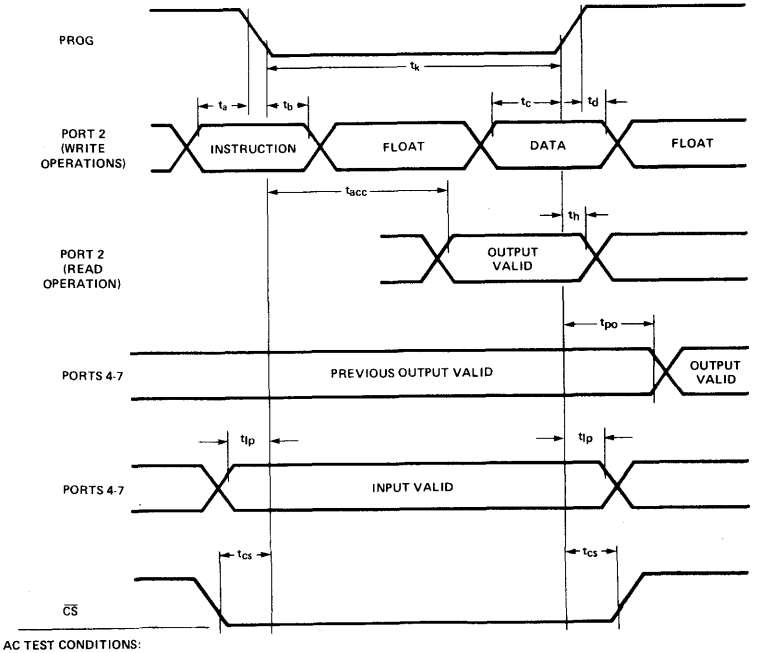
The use of a single 82C43 with an 8048 or 8021 is shown in figure 1. If more ports are required, more 82C43s can be added as shown in figure 2. Here, the upper nibble of port 2 is used to select one of the 82C43s. Two lines could have been decoded but that would require additional hardware. Assuming that the leftmost 82C43 chip select is connected to P24, the instructions to select and de-select would be:

```
MOV A, #0EFH      P24 = 0
OUTL P2, A        Enable 82C43
.
.
.
MOV A, #0FFH      Disable All
OUTL P2, A        Send It
```

Power On Initialization

Initial applicaiton of power to the device forces ports 4, 5, 6, and 7 to the high impedance state. Port 2 will be in an input state if PROG or $\overline{CS}$ are high when power is applied. The first high-to-low transition of PROG causes the device to exit the power-on mode. The power-on sequence is initiated if V_{CC} drops below one volt.

WAVEFORMS



AC TEST CONDITIONS:
V_{IH} = 2.8V

INPUT RISE AND FALL TIMES: 5ns (10 TO 90%)
INPUT AND OUTPUT TIMING VOLTAGE REFERENCE LEVELS: 0.8V AND 2.0V

TYPICAL APPLICATIONS

EXPANDER INTERFACE

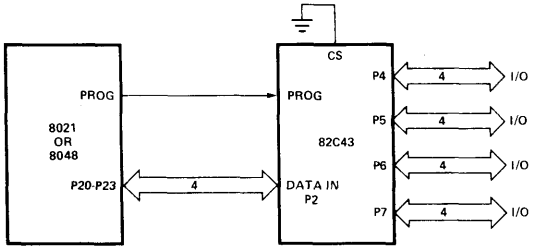
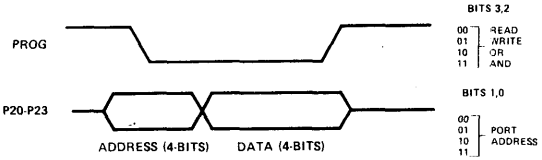


Figure 1

OUTPUT EXPANDER TIMING



Note:
The 82C43 does not have the same quasi-bidirectional port structure as P1/P2 of the 8048. When a "1" is written to P4-7 of the 82C43 it is a "hard 1" (low impedance to +5V) which cannot be pulled low by an external device. All 4 bits of any port can be switched from output mode to input mode by executing a dummy read which leaves the port in a high impedance (no pullup or pulldown) state.

2

USING MULTIPLE 82C43s

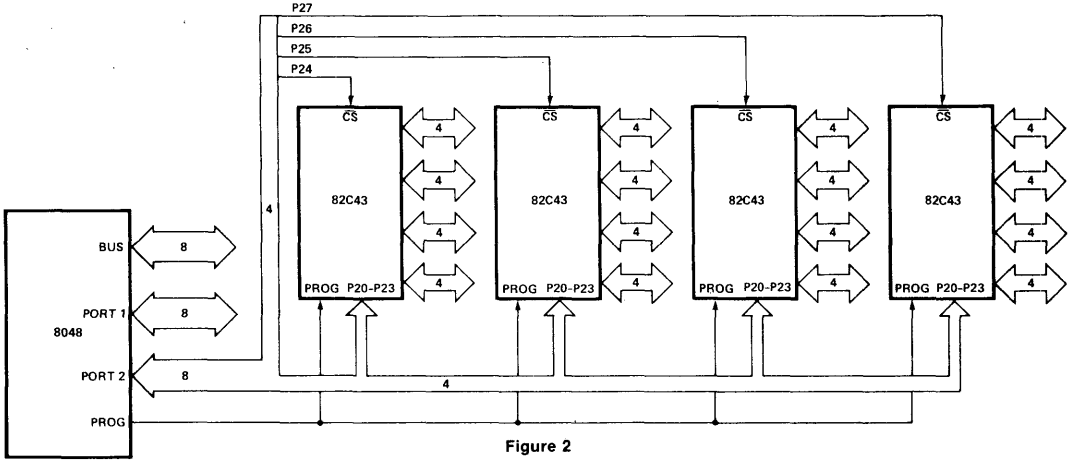


Figure 2

The IGC10000 Series CMOS Gate Arrays

FEATURES

- **Complexity from 408 to 1500 Equivalent 2-input Gates**
- **Mature Silicon Gate CMOS Technology**
  - **—Low development cost**
  - **—3.3 to 9V nominal power supply range ± 10%**
  - **—Full CMOS temperature range: − 55 °C to + 125 °C**
  - **—Resistance to latch-up and electrostatic discharge**
- **Extensive Macro Cell Library**
  - **—Numerous combinational and sequential macros**
  - **—Facilitates 7400 and 4000-based designs**
  - **—TTL or CMOS compatible I/O**
  - **—Analog capability**
- **Fully Integrated CAD Software Support**
  - **—Highly efficient auto-routing capability**
  - **—Layout fully verified against input logic**
  - **—Accurate post-layout simulation with calculated RC delays**
  - **—Automatic test code conversion**

GENERAL DESCRIPTION

An IGC10000 Gate Array is a matrix of identical cells, each containing 3 uncommitted N-P transistor pairs. Large numbers of identical arrays are prefabricated and stockpiled. A particular circuit is constructed from a prefabricated array by specifying the interconnections among the transistors within and between cells on the final metal layer. Because all except the final metal layer are prefabricated, the cost advantages of mass production can be realized even for low-volume applications. In addition, prefabrication provides a saving in both design and manufacturing time; in some cases customers can receive prototype chips in as few as 6 weeks after initiation of the project.

In most cases IGC10000 gate arrays are processed with one mask step (a customized metal mask along with a standardized contact mask). For some analog applications or where more routing flexibility is needed, users have the option of programming the contact mask in addition to the metal mask.

THE IGC10000 FAMILY OF GATE ARRAYS

Figure 1 shows a structural representation of an IGC10000 Gate Array. Each rectangle in the body of the matrix represents an array cell; the rectangles

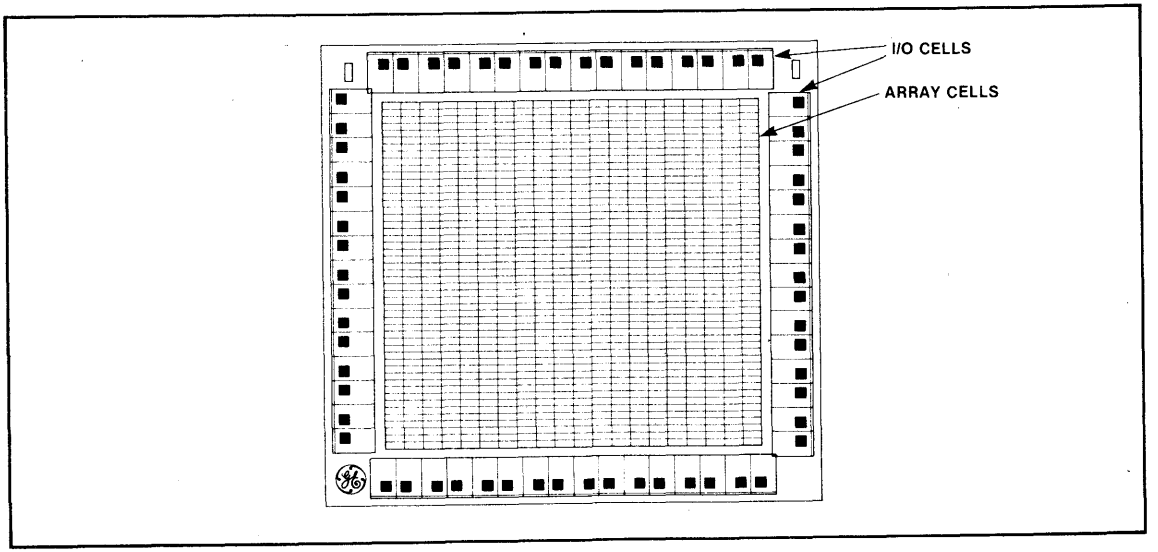


Figure 1. Gate Array Configuration

INTERSIL, INC., 10710 N. TANTAU AVE., CUPERTINO, CA 95014 (408) 996-5000 TWX: 910-338-0171

along each of the four sides of the chip represent I/O cells. Table 1 lists the members of the IGC10000 Gate Array family with their capacities and cell counts.

Table 1. The IGC10000 Gate Array Family

Part No.	Equivalent 2-Input Gates	Number of Array Cells	Bonding Pads and I/O Cells
IGC10408	408	272	34
IGC10756	756	504	44
IGC11500	1500	1000	62

TECHNOLOGY

IGC10000 gate arrays are fabricated using Intersil's high performance selectively oxidized 4-micron silicon gate CMOS process with single-layer metal interconnect. Wafers are processed using state-of-the-art processing technology with these features:

- Positive photoresist
- 1-1 scanning projection lithography
- Polysilicon, nitride and silicon dioxide plasma etching
- Ion implantation for source/drain doping and threshold adjustment
- Sputter metal deposition
- Industry standard oxidation and diffusion techniques
- Nitride and polysilicon Low Pressure Chemical Vapor Deposition (LPCVD)

ARRAY CELLS

An array cell, shown in topographical form in Figure 2, consists of three complementary transistor pairs and five strips of polysilicon (called crossunder strips) for making horizontal interconnections among array cells. Power (V_{DD}) and ground (V_{SS}) buses run vertically as shown. Metal strips (not shown) on top of the crossunder strips make the vertical interconnections within the array. The top and bottom polysilicon strips (called feed-throughs) are used for feeding horizontal connections through the array cell beneath the power and ground buses.

Figure 3 shows the circuit diagram for the array cell. Small hollow circles represent possible connection points; V_{SS} and V_{DD} metal strips are shown as dotted lines.

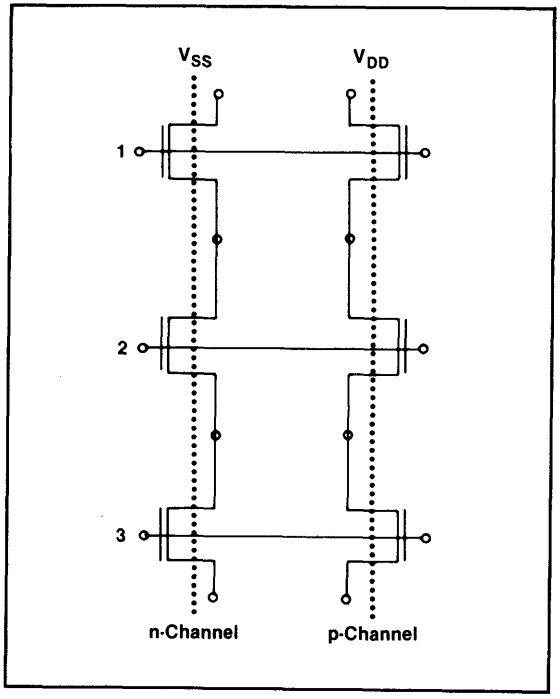


Figure 3. Schematic Diagram of the Array Cell

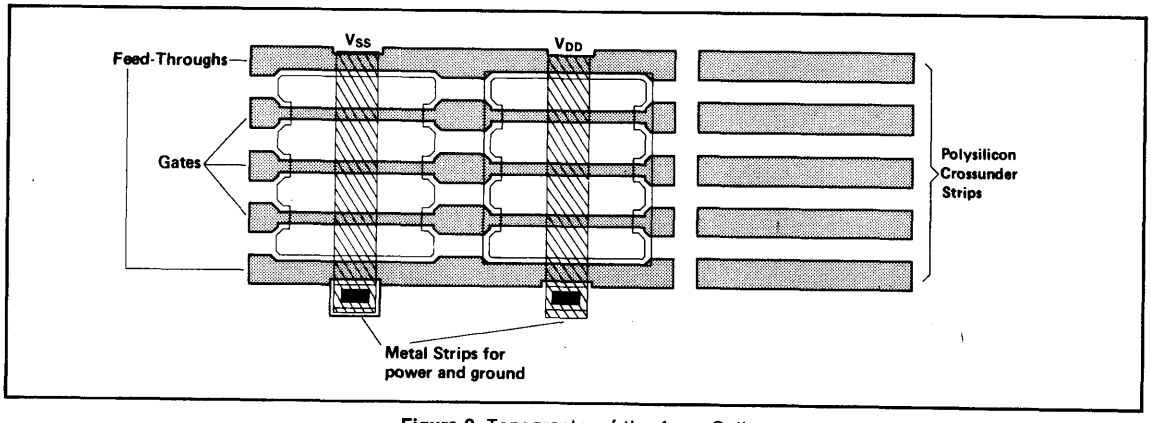


Figure 2. Topography of the Array Cell

I/O CELLS

I/O cells are used to interface the array with external circuitry. Each I/O cell consists of an array of transistors of varying sizes, and allows construction of normal digital I/O interface circuits as well as analog circuitry of simple to moderate complexity.

I/O cells have these features:

- Protection against electrostatic discharge (ESD)
- Logic level translation (CMOS-to-TTL and TTL-to-CMOS)
- Bonding pad for connecting the cell to its corresponding package pin
- Ratioed transistors for analog implementation

The output drive capability of a single output buffer is one TTL load. Applications that require additional drive capability can be handled by using multiple I/O cells in parallel. (In a typical application, not all available I/O cells are needed for external connections; unused cells will thus usually be available to provide added drive capability where needed.)

MACROS

A macro is a physical implementation of a functional block and is realized by interconnections among transistors in one or more array cells. For example, the NOR function is constructed by connecting two p-channel transistors in series to V_{DD} and two n-channel transistors in parallel to V_{SS}, as shown in the topographical and schematic diagrams, Figures 4 and 5.

Designers implement their circuits by selecting and interconnecting the macros in the Macro Library, listed in Table 2.

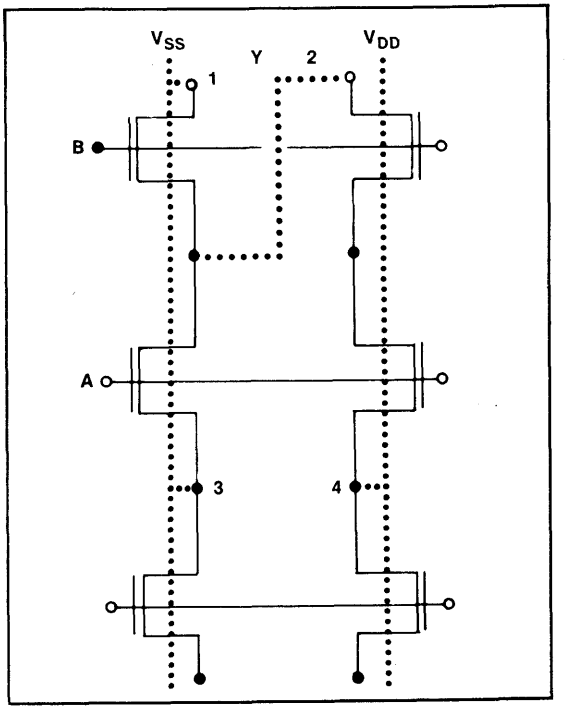


Figure 5. Schematic Diagram for the 2-Input NOR

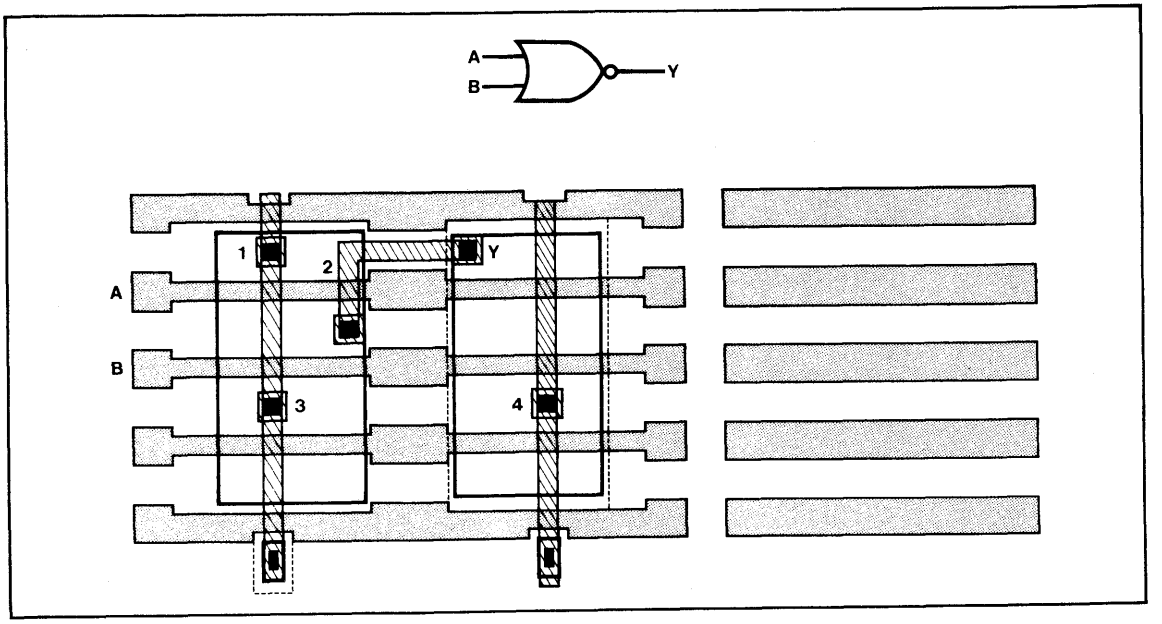


Figure 4. Interconnect Pattern for the 2-Input NOR

Table 2. IGC10000 MACRO Library

IGC10000 Combinational Macros	
Type	**Description**
NOR/NAND	2-input NAND 3-input NAND 4-input NAND 2-input NOR 3-input NOR 4-input NOR
XOR/XNOR	2-input XOR 2-input XNOR
Adder	One-bit full adder
Buffers and Inverters	1X inverter 2X inverter 3X inverter 4X inverter
Multifunction	2-1 AND-OR invert 2-2-2 AND-OR invert 3-2 AND-OR invert 2-1 OR-AND invert
Multiplexer	2 to 1 multiplexer
Schmitt Trigger	Schmitt Trigger
Transmission Gate	Buffered transmission gate Unbuffered transmission gate
Tristate Control	Tristate control

IGC10000 Sequential Macros		Set	Reset	Jam Load
D Flip-Flops	D flip-flop with reset	—	Yes	—
	D flip-flop with set	Yes	—	—
	D flip-flop with set and reset	Yes	Yes	—
	Divide by 2 flip-flop w/jam load and reset	—	Yes	Yes
	Divide by 2 flip-flop w/reset	—	Yes	—
	D flip-flop w/jam load and reset	—	Yes	Yes
	D flip-flop shift register with reset	—	Yes	—
JK Flip-Flops	JK flip-flop with reset	—	Yes	—
	JK flip-flop with set	Yes	—	—
T Flip-Flops	T flip-flop with reset	—	Yes	—
Latches	D latch	—	—	—
	D latch w/single input control	—	—	—
	D latch with reset	—	Yes	—
	D latch w/reset and single input control	—	Yes	—
	D latch w/transmission gate on output	—	—	—
Counters	Down counter with reset	—	Yes	—
	Down counter w/jam load and reset	—	Yes	Yes
	Up counter with reset	—	Yes	—
	Up counter w/jam load and reset	—	Yes	Yes
	Up/down counter with reset	—	Yes	—
	Up/down counter w/jam load and reset	—	Yes	Yes

Table 2. IGC10000 MACRO Library (continued)

IGC10000 Digital I/O Cell Macros	
Type	**Description**
Bidirectional	Tristate output/unbuffered input Tristate output/inverting TTL input buffer
Feedthrough	Input feedthrough
Internal Buffer	Inverting internal buffer Internal tristate buffer
Input Buffer	Non-inverting TTL input buffer Non-inverting CMOS input buffer with pull-up options
Output Buffer	Open drain output buffer Non-inverting TTL output buffer Inverting TTL output buffer Tristate output buffer Symmetrical drive output buffer

IGC10000 Analog I/O Cell Macros

The list below represents a sample of custom macros developed for specific analog applications. Consult your Intersil Representative for suitability to your design.

Analog Transmission Gate
Auto Null Comparator
Comparator
Compensated Op Amp
Crystal Oscillator
Current Multiplier
Current Reference
Op Amp
Power-on Reset
RC Oscillator
Schmitt Trigger

COMPUTER AIDED DESIGN SOFTWARE TOOLS

The IGC10000 family is supported by a proprietary computer aided design (CAD) system developed at the General Electric Microelectronics Center. The system provides CAD tools for logic simulation, accurate prediction of circuit speed performance, automated design of interconnect circuitry, electrical and design rule checking, post-layout simulation using RC delays extracted from the layout, and automatic conversion of simulation test pattern files into tester format.

The CAD tools are integrated under a supervisory program called the CADEXEC (for CAD Executive) that runs on a Digital Equipment Corporation VAX computer. Once the user has entered the circuit's interconnect information into the computer, this information is converted into a common database accessed by all other parts of the software through the CADEXEC.

Logic Simulation: Users have access to the TEGAS logic simulator. For pre-layout logic (functional) verification, customers may perform TEGAS simulation using our Unit Delay Macro Library database; for design verification (pre-layout timing analysis), calculated delays based on fanout are used in conjunction with Best, Typical, and Worst Case libraries, whose parameters are described in Table 3.

Table 3. Best, Typical, and Worst Case Parameters

Parameter	Best	Typical	Worst
Voltage (V)	5.5	5.0	4.5
Temperature (°C)	0	27	70
Process	Best	Typical	Worst

Routing: The SILICA layout system uses a proprietary automatic router developed at the General Electric Microelectronics Center. The SILICA router has consistently performed with higher completion rate and lower CPU time than other commercially available routers; in addition, the router improves the overall performance of the circuit by selecting paths that produce the smallest delay. Like many routers, the SILICA router has a Critical Net feature that minimizes polysilicon and total net length by routing the critical net first. Unique to the SILICA router is the Super Critical Net feature, which prohibits the use of polysilicon gates in a specified net.

Electrical and Design Rule Checking: SILICA DRC (Design Rule Checker) performs electrical and design rule checking in minutes instead of hours and extracts geometric data from the layout for input into the RC delay extraction software.

Manual editing: In rare instances manual layout editing may be done on one of our CALMA workstations. CALMA output is fed into SILICA DRC for convenient verification of electrical integrity.

Post-layout simulation: A specialized circuit simulator has been developed at the General Electric Microelectronics Center to compute the delays of the RC-interconnect nets from the topology of the network after performing layout. The RC Delay extraction software uses a full transient analysis for each net; delays are based on resistance as well as capacitance of the interconnection nets. The software calculates delays as a function both of load switching voltage and driver output impedance and handles loops, bidirectional drivers, and multiple drivers on the net.

After the RC delay information is extracted, the CADEXEC system inserts the delays into the network database for post-layout TEGAS simulation and critical path analysis, thus providing an additional opportunity for refining the layout prior to PG tape generation.

Tester Tape Generation: Test program conversion software automatically translates the customer's final TEGAS simulation output file into a test vector pattern file to be used in testing the finished device.

PACKAGING

Five types of packages are available for the IGC10000 gate arrays. Dual inline packages are available in plastic (Plastic DIP), ceramic (CerDIP) and multilayer ceramic (Side Brazed DIP); leadless chip carriers and pin grid arrays are provided in multilayer ceramic. Table 4 presents recommended package types for each pin count and array size.

Table 4. Recommended Package Types

Number of Pins	Plastic DIP	CerDIP	Side Brazed DIP	Leadless Chip Carrier	Pin Grid Array
8	408		408		
14	408	408	408		
16	408	408	408		
18	408	408	408		
20		408	408		
24	408	408	408		
	756	756	756		
	1500	1500	1500		
28	408	408	408		
	756	756	756		
	1500	1500	1500		
40	408	408	408		
	756	756	756		
	1500	1500	1500		
44				756	
				1500	
48			756		
			1500		
52				1500	
68				1500	1500

DEVELOPMENT

An overview of the gate array development process is shown in the flow chart of Figure 6. During Phase 1 (Design Translation), most of the responsibility lies with the customer; during Phase 3 (Fabrication), with Intersil. In Phase 2 (Design Implementation), most of the activities are performed by Intersil, but require customer interaction and approval. Figure 6 delineates the responsibilities of the customer and of Intersil. For more information, contact either your local Intersil representative, or Semicustom Marketing at the General Electric Microelectronics Center, Research Triangle Park, NC, telephone 919-549-3607.

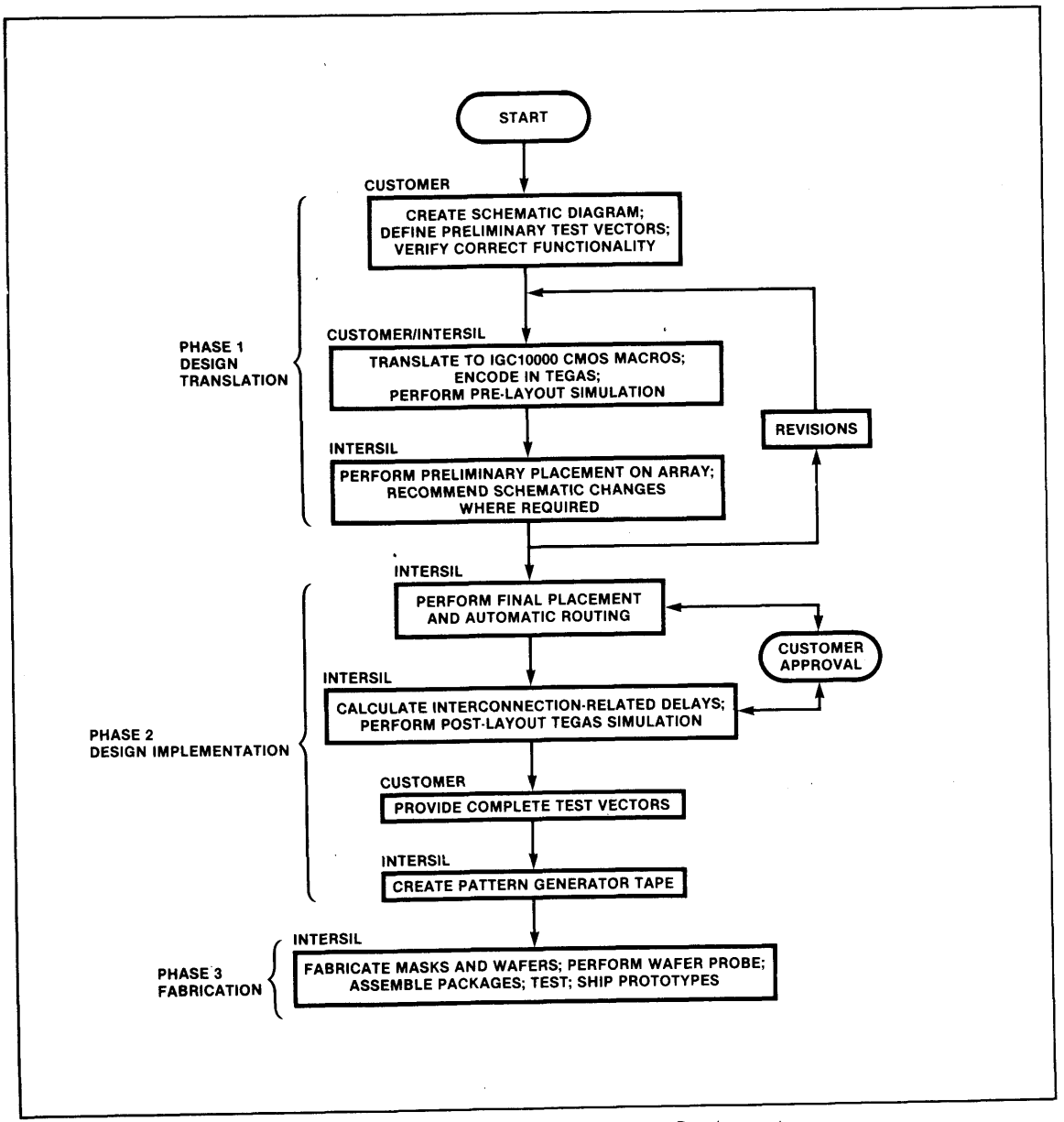


Figure 6. Simplified Flowchart for Gate Array Development

OPERATING CHARACTERISTICS[1]

Absolute Maximum Ratings[2] (Referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	− 0.5 to + 10.0	V
Input Voltage	V_I	− 0.5 to V_{DD} + 0.5	V
DC Input Current	I_I	± 10	mA
Operating Ambient Temperature Range	T_A	− 55 to + 125	°C
Storage Temperature Range (Ceramic)	T_{STG}	− 65 to + 150	°C
Storage Temperature Range (Plastic)	T_{STG}	− 40 to + 125	°C

NOTE 1: Stress ratings only. Functional operation of the device at these or any conditions beyond those indicated as Recommended Operating Conditions is not implied.

NOTE 2: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	3.3 ± 0.3V to 9.0 ± 0.9V	V
Typical Operating Frequency	f_{CK}	8.0	MHz
Operating Ambient Temperature Range[1]	T_A	− 55 to + 125	°C

NOTE 1: IGC10000 gate array macros are currently characterized between 0 and 70°C.

AC CHARACTERISTICS

Specified for nominal processing = 5V, 27°C.
Calculated for a fanout of 1.

	Parameter	Typical Delay (ns)
Array Cell Macros		
2-input NAND	D to Output	6
2-input NOR	D to Output	6
4-input NAND	D to Output	8
4-input NOR	D to Output	18
1X inverter	D to Output	5
4X inverter	D to Output	4
2-1 AND-OR invert	D to Output	9
D flip-flop with reset	CK to Output	9
Schmitt trigger	Input to Output	18
Up counter with reset	CK to Output	11
I/O Cell Macros		
Input feedthrough	Pad to Output	1
Non-inverting Input Buffer	Pad to Output	9
Non-inverting Output Buffer	D to Pad	10 (15 pF) 19 (50 pF)

DC CHARACTERISTICS

V_{DD} = 5V ± 10%

Symbol	Parameter	Condition	Limits[1]							
			0°C		25°C			70°C		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Units
I_{DD}[2]	Quiescent Device Current	$V_I = V_{DD}$ or V_{SS}				0.3			100	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$	V_{DD} − 0.05		V_{DD} − 0.05			V_{DD} − 0.05		V
V_{IL}	Low Level Input Voltage	CMOS I/O Macro		1.5			1.5		1.5	V
V_{IH}	High Level Input Voltage	CMOS I/O Macro	3.5		3.5			3.5		V
V_{IL}	Low Level Input Voltage	TTL I/O Macro		0.8			0.8		0.8	V
V_{IH}	High Level Input Voltage	TTL I/O Macro	2.0		2.0			2.0		V
I_{OL}[3]	Output Low[4] (Sink Current)	$V_O = 0.4V$	1.8		1.8	3.6		1.6		mA
		$V_O = 2.5V$	3.8		3.8	7.6		3.4		mA
I_{OH}[3]	Output High (Source Current)	$V_O = 4.6V$	0.3		0.3	0.6		0.25		mA
		$V_O = 2.5V$	1.8		1.8	3.6		1.6		mA
I_{IN}	Input Leakage Current	$V_{IN} = 0$ or V_{DD}		± 0.1		± .001	± 0.1		± 1.0	μA
I_{OZ}	Tristate Output Leakage Current	$V_O = 0$ or V_{DD}		± 1.0		± .001	± 1.0		± 10	μA
C_{IN}	Input Capacitance	Any Input				5.0				pF

NOTES:

1. IGC10000 gate arrays are designed to perform under conditions up to 125°C. Limits reflect temperature range at which the macro library is characterized.
2. Any internal oscillators disabled.
3. Results depend on specific output macro used.
4. There may be limitations on maximum current when many outputs are simultaneously low.

Analog Switches and Multiplexers

Multiplexers

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Analog Switches with Drivers

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Video/RF Switch

IH5341	3-87

Analog Switch

Low Leakage and Low Quiescent Current

DG200/201, IH5200/5201 Monolithic CMOS driver-gate combination

Features
1. DG200/201 industry standard
2. IH5200/5201 have far superior specs
3. IH520/DG201 have 4 individually controllable SPST switches
4. IH5200/DG200 have 2 individually controllable SPST switches

Notes
1. TTL, DTL, CMOS and PMOS compatible
2. IH 5200 / DG200 — Dual SPST
   IH5201 / DG201 — Quad SPST

IH5040 Family Monolithic CMOS driver gate combination

Features
1. Very low quiescent current resulting in very low power consumption
2. Low cost
3. Good speed with moderate $r_{DS(on)}$ and leakage
4. Over voltage protection to ±25V
5. Can switch up to ±13V signals with ±15V supplies

Notes
1. TTL, DTL, CMOS, and PMOS compatible
2. 5040 through 5047 have 75Ω $r_{DS(on)}$ max @25°C
3. IH5048 thru IH5051 have 35Ω $r_{DS(on)}$ max @25°C

IH5040	SPST
IH5041/5048	Dual SPST
IH5042/5050	SPDT
IH5043/5051	Dual SPDT
IH5044	DPST
IH5045/5049	Dual DPST
IH5046	DPDT
IH5047	4PST
IH5052/5053	Quad SPST
IH200	Dual SPST
IH201/202	Quad SPST

IH5140 Family Monolithic CMOS driver gate combination

Features
1. High speed switching
2. Low quiescent current resulting in low power consumption
3. Low leakage resulting in low error term
4. Lower cost than the comparable speed DG180 family
5. Can switch signals almost to the supply rails

Notes
1. TTL and CMOS compatible
2. Pin compatible with the more popular members of the DG180 family

IH5140	SPST
IH5141	Dual SPST
IH5142	SPDT
IH5143	Dual SPDT
IH5144	DPST
IH5145	Dual DPST

High Speed

DGM181 Family Monolithic CMOS replacement for DG180 Family

Features
1. Drops into DG180 family sockets. Meets or exceeds all specs
2. Lower cost than DG180
3. Lower leakages and power consumption than DG180

Notes
1. TTL, DTL, RTL and CMOS compatible
2. DGM181, 184, 187, and 190 have 30Ω max $r_{DS(on)}$
3. DGM182, 185, 188, and 191 have 75Ω max $r_{DS(on)}$

DGM181/2	Dual SPST
DGM184/5	Dual DPST
DGM187/8	SPDT
DGM190/1	Dual SPDT

Low $r_{DS(on)}$

DG180 Family Bipolar/MOS driver with N-JFET gate

Features
1. Low $r_{DS(on)}$
2. As fast as the IH5140 Family
3. Moderate leakage
4. Draw high quiescent currents

Notes
1. DTL, TTL, RTL compatible
2. DG180, 183, 185 and 189 have 10Ω max on resistance but have higher leakage than others in the family
3. DG181, 184, 187 and 190 have 30Ω max $r_{DS(on)}$
4. DG182, 185, 188 and 191 have 75Ω max $r_{DS(on)}$

DG180/1/2, Dual SPST
DG183/4/5, Dual DPST
DG186/7/8, SPDT
DG189/90/1, Dual SPDT

DG126 Family Bipolar driver with N-JFET gate

Features
1. Low $r_{DS(on)}$
2. Only switch with true chip enable pin
3. Moderate leakage
4. Draw high quiescent currents

Notes

DG133, 134, 141, 151, 152	Dual SPST
DG126, 129, 140, 153, 154	Dual DPST
DG143, 144, 146, 161, 162	Differential input, SPDT
DG139, 142, 145, 163, 164	Differential input, DPDT
IH5001/2	SPST
IH5003-7	Dual SPST

Selector Guide

Low Charge Injection	Video/RF Switch	For switches whose outputs go into the inverting input of an Op Amp	For switching positive signals only
IH181 Family CMOS driver and Varafet gate	IH5341 Family series shunt video/RF switch	IH5009 Virtual ground switch	IH5025 Positive signal switch
Features 1. Lowest charge injection 2. Almost as fast as IH5140 and DG180 Families 3. Very low quiescent current resulting in low power consumption 4. Ultra low leakage	**Features** 1. $r_{DS(on)}$ < 75Ω, flat from DC to 100 MHz (< 3dB) 2. "OFF" isolation > 60dB @ 10 MHz 3. Cross coupling isolation > 60dB @ 10MHz 4. +/−5V to +/−15V power supply range 5. High speed switching	Output of a switch must go into the virtual ground point of an Op Amp (unless signal is <0.2V) **Features** 1. Very low quiescent current 2. Does not need driver; can be driven directly by CMOS gates 3. Low cost	Can switch positive signals only unless a translator driver is used **Features** 1. Very low quiescent current 2. Does not need driver; can be driven directly by TTL 3. Low cost
Notes 1. TTL, HTL, CMOS and PMOS compatible 2. *Pin for pin compatible* with DG180 family IH181/182 Dual SPST IH184/185 Dual DPST IH187/188 SPDT IH190/191 Dual SPDT	**Notes** 1. TTL, DTL, RTL and CMOS compatible 2. IH5341 Dual SPST	**Notes** 1. All switches in IH5009 family are SPST 2. Odd numbered devices are driven by 15V logic 3. Even numbered devices are driven by 5V logic IH5009/5010 quad, compensated IH5011/5012 quad uncompensated IH5013/5014 triple compensated IH5015/5016 triple uncompensated IH5017/5018 dual compensated IH5019/5020 dual uncompensated IH5021/5022 single compensated IH5023/5024 single uncompensated	**Notes** 1. All switches in IH5025 family are SPST 2. All devices can be driven by 15V logic. All devices can be driven by 5V logic if input signal is less than 1V IH5025/5026 quad, common drain IH5027/5028 quad IH5029/5030 triple, common drain IH5031/5032 triple IH5033/5034 dual, common drain IH5035/5036 dual IH5037/5038 single

Analog Switches with Driver

Type	No. of Channels	Intersil Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic input: Logic Level	Logic input: Input Type(2)	Power Consumption mW
		IH5021	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5022	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
SPST	1	IH5023	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5024	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5037	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5038	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5040	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5140	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
		DG180	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	lo	120
		DG181	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	lo	120
		DG182	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	lo	120
		DGM182	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	lo	.035
		DG200	CMOS	70	1.0	0.7	0.5	DTL, TTL, RTL, CMOS, TTL High Level	lo	3.0
		IH5017	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5018	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5019	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
SPST	2	IH5020	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5033	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5034	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5035	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5036	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5041	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5048	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5141	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
		IH5341	CMOS	75	0.1	0.3	0.15	TTL, CMOS	hi	.035
		IH5013	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5014	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5015	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5016	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
SPST	3	IH5029	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5030	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5031	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5032	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		DG118	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG201	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	lo	.350
		IH5009	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
SPST	4	IH5010	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5011	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5011	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5025	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5026	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5027	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5028	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5052	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	lo	.350
		IH5053	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		DG123	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	hi	133
		DG125	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG143A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG144A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
SPST	5	DG146A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG161A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG162A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		DG186	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	73
		DG187	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	73
		DG188	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	73
		DGM188	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	035
SPDT	1	IH5042	CMOS	75	1.0	0.05	0.025	DTL, TTL, RTL PMOS, CMOS	(3)	035
		IH5050	CMOS	35	1.0	0.25	0.15	DTL TTL, RTL PMOS, CMOS	(3)	035
		IH5142	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	035

Analog Switches with Driver continued

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic input: Logic Level	Logic input: Input Type(2)	Power Consumption mW
		DG189	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	120
		DG190	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	120
		DG191	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	120
		DGM191	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	035
SPDT	2	IH5043	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	(3)	035
		IH5051	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	(3)	035
		IH5143	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	035
DPST	1	IH5044	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	035
		IH5144	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	035
		DG183	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	hi	84
		DG184	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	hi	84
		DG185	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	hi	84
DPST	2	DGM185	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	hi	.035
		IH5045	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5049	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5145	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
		DG139A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG142A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
DPDT	1	DG145A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG163A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG164A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		IH5046	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	(3)	.035
4PST	1	IH5047	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035

3

Multiplexers

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic input: Logic Level	Logic input: Input Type(2)	Power Consumption mW
CMOS	1 of 8	IH6108	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	1 of 16	IH6116	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	2 of 8	IH6208	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	2 of 16	IH6216	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS Fault Protected	1 of 8	IH5108	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
	2 of 8	IH5208	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5

Drivers for FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

No. of Channels	Device No.	V_{OUT} Positive Volts	V_{OUT} Negative Volts	t_{on} ns max	t_{off} ns max	I_{INL} µA (max)	I_{INH} mA (max)	Logic Input Level	Power Consumption (mW)
2	IH6201	+14.0	-14.0	200	300	1.0	1.0	TTL	350
4	D129	V_{supply}	-19.3	250	1000	200	0.25µA	TTL/DTL	55
6	D123	V_{supply}	-19.7	250	600	1.0	1.0µA	TTL/DTL	20
	D125	V_{supply}	-19.7	250	600	1.0	1.5µA	TTL	50

RF/VIDEO SWITCH

Type	No. of Channels	Device No.	$r_{DS\ (ON)}$ Ω Max.	Off Isolation	Logic Input	Power Consumption (mW)
CMOS	2	IH5341	75.	>60dB @ 10 MHz	TTL, CMOS	0.030

Notes:
1. Switch Resistance under worst case analog voltage.
2. Positive logic LO ("0") or HI ("1") voltage at driver input necessary to turn switch on.
3. Logic "0" or "1" can be arbitrarily assigned for double-throw switches.
4. Switch resistance under best case analog voltage.

DG118/123/125
4 and 5-Channel Driver-MOS-FET Switch Combinations

FEATURES

- Available With and Without Programmable Constant Current pull-up
- Zener Protection on All Gates
- P-Channel Enhancement-Type MOS-FET Switches
- Each Switch Summed to One Common Point

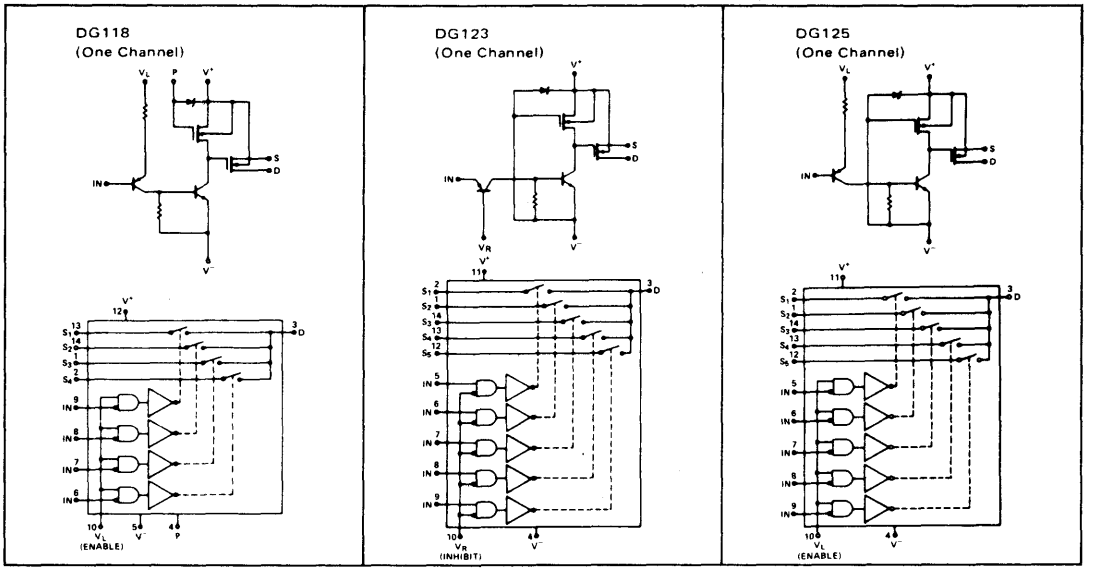
GENERAL DESCRIPTION

This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOS-FET switch. Two driver versions are supplied for inverting and noninverting applications. A MOS-FET, used as a current source provides an active pull-up for faster switching.

An external biasing connection is brought out for biasing the current source for optimization of speed and power.

3

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

DG118 A K

- Package
  - K — 14-pin CERDIP
  - L — 14-pin Flat Package
  - P — 14-Pin Ceramic DIP (Special Order Only)
- Temperature Range
  - A — Military (−55°C to +125°C)
  - B — Industrial (−20°C to +85°C)
- Device Chip Type

TRUTH TABLE

DG123		DG118, DG125		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V^+ - V^-$) 33V
Collector to Pull-up ($V^+ - V_P$) 33V
Drain to Emitter ($V_D - V^-$) 32V
Source to Emitter ($V_S - V^-$) 32V
Drain to Source ($V_D - V_S$) 28V
Source to Drain ($V_S - V_D$) 28V
Logic to Emitter ($V_L - V^-$) 33V
Reference to Emitter ($V_R - V^-$) 31V
Reference to Input ($V_R - V_{IN}$) 6V
Logic to Input ($V_L - V_{IN}$) . . . . . ±6V

Input to Emitter ($V_{IN} - V^-$) 33V
Current (any terminal) 30mA
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -55°C to +125°C
Dissipation (Note) 750mW
Lead Temperature (soldering, 10 sec.) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

ELECTRICAL CHARACTERISTICS

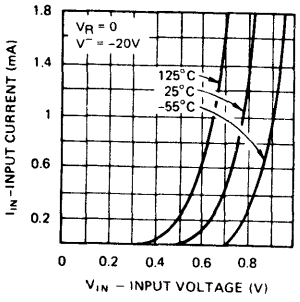
Test conditions unless specified otherwise are as follows: V_L = 4.5V, V_R = 0, V^- = -20V, and P = -20V. Input ON and OFF test conditions used for output and power supply specifications.

		PARAMETER (NOTE)	MAX LIMITS				CONDITIONS
			-55°C	+25°C	+125°C	UNITS	
INPUT	DG123	$I_{IN(OFF)}$	1	1	100	µA	V_{IN} = 0.4V
		$V_{IN(ON)}$	1.3	1.0	0.8	V	I_{IN} = 1 mA
	DG118 DG125	$I_{IN(OFF)}$	1	1	20	µA	V_{IN} = 4.1V
		$I_{IN(ON)}$	-0.7	-0.7	-0.7	mA	V_{IN} = 0.5V
OUTPUT	All circuits	$r_{DS(ON)}$	100	100	125	Ω	V_D = 10V, I_S = -1mA
			200	200	250	Ω	V_D = 0, I_S = -100 µA
			450	450	600	Ω	V_D = -10V, I_S = -100 µA
		$I_{D(ON)}$		4	4000	nA	V_D = 10V, $I_{S(all)}$ = 0
		$I_{D(OFF)}$		-4	-4000	nA	$V_{S(all)}$ = 10V, V_D = -10V
		$I_{S(OFF)}$		-1	-1000	nA	V_D = 10V, V_S = -10V
POWER SUPPLY	All circuits	$I_{CC(ON)}$		3		mA	One Channel (ON)
		$I_{L(ON)}$		3		mA	
		$I_{R(ON)}$		-0.5		mA	
		$I_{EE(ON)}$		-6		mA	
	All circuits	$I_{CC(OFF)}$		10		µA	All Channels (OFF)
		$I_{L(OFF)}$		10		µA	
		$I_{R(OFF)}$		-15		µA	
		$I_{EE(OFF)}$		-20		µA	
SWITCHING TIMES	All circuits	$t_{(ON)}$		0.3		µs	See Switching Times
		$t_{(OFF)}$		1		µs	

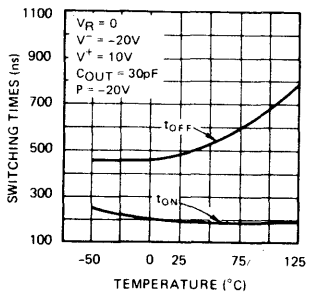
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOS-FET switch for the given test condition.

TYPICAL CHARACTERISTICS

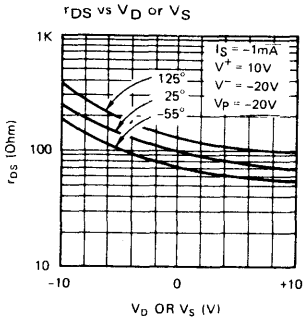
I_{IN} vs V_{IN} DG123



SWITCHING TIMES vs TEMPERATURE



r_{DS} vs V_D or V_S



APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and T^2L Logic are shown in Figures 1 and 2.

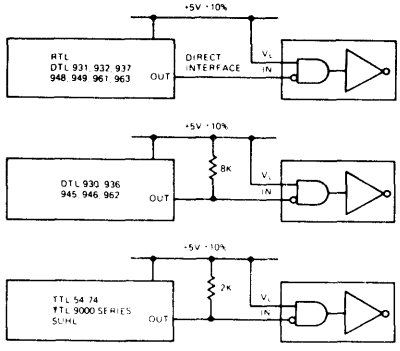


Figure 1. DG118 and DG125 Interface

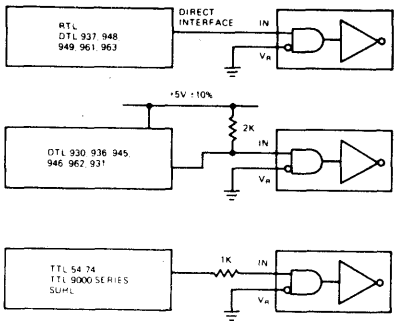
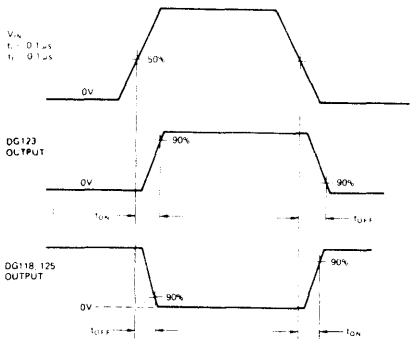


Figure 2. DG123 Interface

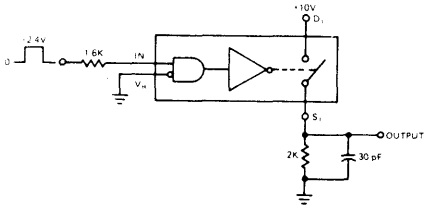
Enable Control

The V_R and V_L terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG118 and DG125, and $I_{R(ON)}$ x No. of channels used, for the DG123 devices. The voltage at V_L must be greater than the voltage at V_{IN} by at least + 4V.

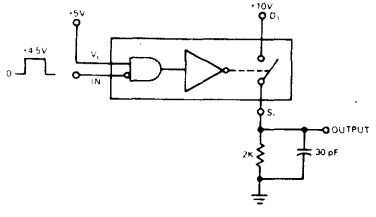
SWITCHING TIMES



DG123



DG118, 125



D123/D125
6-Channel FET Switch Drivers

FEATURES

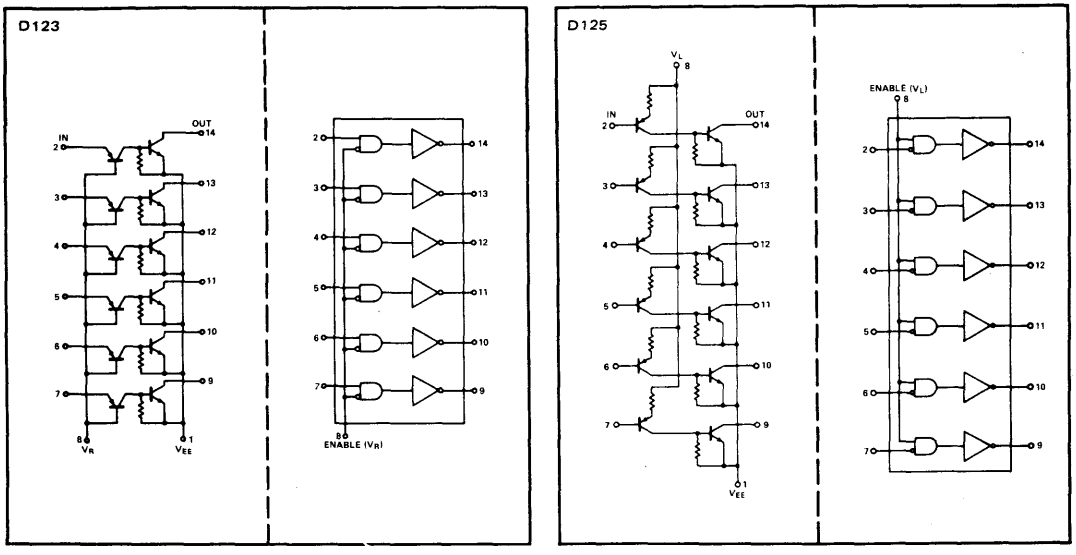
- Provides DC level shifting between low-level Logic and MOS-FET or J-FET switches
- External Collector Pull-ups required
- Direct interface with G116, G117, G119, G115, and G123 MOS-FET switches

GENERAL DESCRIPTION

The D123 and D125 monolithic bi-polar drivers convert low-level positive signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

3

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

D123 A K

Package
K – 14-Pin CERDIP
L – 14-Pin Flat Pack
P – 14-Pin Hermetic DIP (Special Order Only)

Temperature Range
A – Military (–55°C to +125°C)
B – Industrial (–20°C to +85°C)

Device Chip Type

ABSOLUTE MAXIMUM RATINGS

Input-to-Emitter Voltage ($V_{IN} - V_{EE}$)	33V
Output-to-Emitter Voltage ($V_O - V_{EE}$)	33V
Logic Supply-to-Emitter Voltage ($V_L - V_{EE}$)	27V
Input-to-Reference Voltage ($V_{IN} - V_R$)	2V
Input-to-Logic Supply Voltage ($V_{IN} - V_L$)	+6V
Reference-to-Emitter Voltage ($V_R - V_{EE}$)	31V
Maximum Dissipation (Note)	750 mW
Current (any pin)	30 mA

Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10 mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

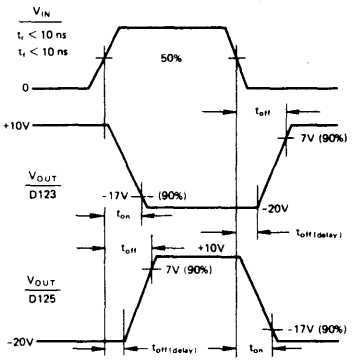
ELECTRICAL CHARACTERISTICS

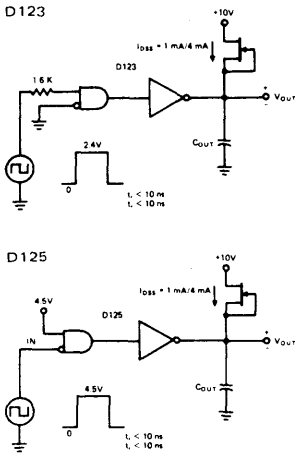
Test conditions unless otherwise specified are as follows: V_{EE} = -20V, V_L = 4.5V, I_{OUT} = 0, V_R = 0. Output and power supply measurements based on specified input conditions.

		PARAMETER	MAX LIMIT -55°C	MAX LIMIT 25°C	MAX LIMIT 125°C	UNITS	CONDITIONS
INPUT	D123	$I_{IN(OFF)}$	1	1	100	μA	V_{IN} = 0.4V
		$V_{IN(ON)}$	1.3	1	0.8	V	I_{IN} = 1 mA
	D125	$I_{IN(OFF)}$	1	1	20	μA	V_{IN} = 4.1V
		$I_{IN(ON)}$	−0.7	−0.7	−0.7	mA	V_{IN} = 0.5V
OUTPUT	D125 & D123	$I_{OUT(OFF)}$	0.1	0.1	10	μA	V_{OUT} = +10V
		$V_{OUT(ON)}$	-19.7	-19.7	-19.5	V	I_{OUT} = 1 mA
		$V_{OUT(ON)}$	-19.2	-19.2	-19.0	V	I_{OUT} = 4 mA
POWER SUPPLY	D123	$I_{R(ON)}$ (1)	0.5	0.5	0.5	mA	I_{OUT} = 0 for ON measurements. V_{OUT} = +10V for OFF measurements.
		$I_{R(OFF)}$ (2)	1	1	150	μA	
		$I_{EE(ON)}$ (1)	1	1	1	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	μA	
	D125	$I_{L(ON)}$ (1)	2	2	1.9	mA	
		$I_{L(OFF)}$ (2)	1	1	100	μA	
		$I_{EE(ON)}$ (1)	2	2	1.9	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	μA	
SWITCHING TIMES	D125 & D123	$t_{(on)}$		250		ns	I_{OUT} = 1 mA C_{OUT} (3) = 10 pF
		$t_{(off)}$ (4)		800		ns	(See Switching Times)
		$t_{(on)}$		250		ns	I_{OUT} = 4 mA C_{OUT} (3) = 10 pF
		$t_{(off)}$ (5)		600		ns	(See Switching Times)

NOTES: (1) One channel ON, 5 channels OFF.
(2) All channels OFF.
(3) Add 30 ns per pF for 1 mA and add 8 ns per pF for 4 mA for additional capacitive loading.
(4) For Dual-In-Line package add 120 ns to $t_{(off)}$.
(5) For Dual-In-Line package add 30 ns to $t_{(off)}$.

SWITCHING TIMES

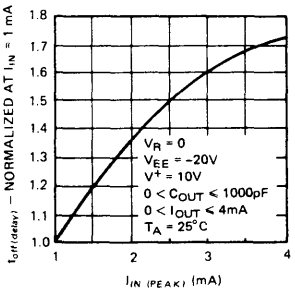




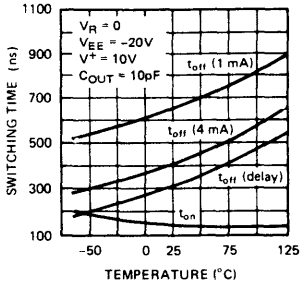
Circuit Diagrams

TYPICAL CHARACTERISTICS

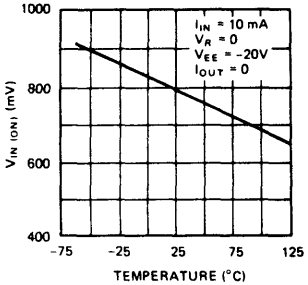
$t_{off(delay)}$ VS $I_{IN(PEAK)}$ D123



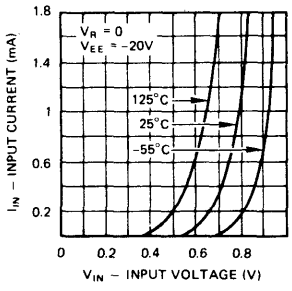
SWITCHING TIMES VS TEMPERATURE D123 AND D125 (SEE NOTES 4 AND 5)



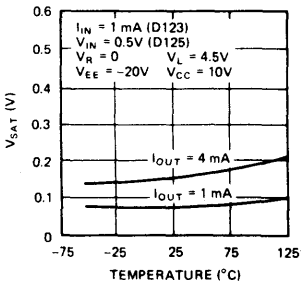
$V_{IN(ON)}$ VS TEMPERATURE D123



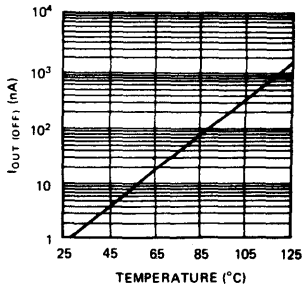
I_{IN} VS V_{IN} D123



V_{SAT} VS TEMPERATURE D123 AND D125



$I_{OUT(OFF)}$ VS TEMPERATURE D123 AND D125

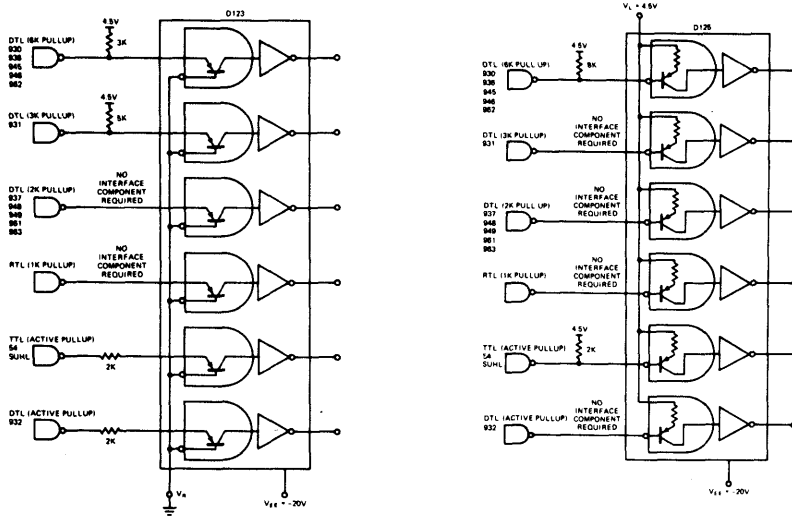


APPLICATION TIPS

Interfacing the D123 and D125

In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping $V_L - V_{IN} \leq 0.4V$ is a must to insure turn-off. To accomplish this a shunt resistor must be added to supply the leakage current (I_{CES}) for DTL devices. Since I_{CES} = 50 μA, a 0.4V/0.05 mA = 8k or less should be used. For T^2L devices using a 2k resister will insure turn-off with up to 200 μA of leakage current.

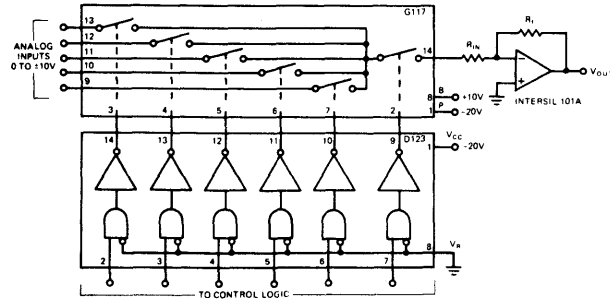


Using the ENABLE Control

Device pins V_R or V_L, can be used to enable the D123 or D125 drivers. For the D123 the enabling driver must sink $I_{R(ON)}$ X no. of channels used. For the D125, $I_{L(ON)}$ X no. of channels used must be sourced with a voltage at least +4V greater than V_{IN}.

APPLICATIONS

Using INTERSIL'S MOS-FET SWITCH G117 with either the D123 or D125 drivers provides a reliable means of providing up to 5 channels with a series block for multiplexing applications.



5-Channel Multiplexer

D129
4-Channel MOS FET Switch Driver with Decode

FEATURES

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible with Low Power TTL and DTL, I_F = 200μA Max
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required
- Compatible with G115 and G123 Series Multichannel MOS FET Switches which include Current-Limiter Pull-Up FETs

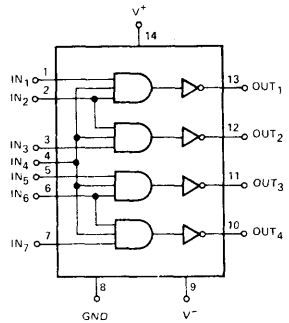
GENERAL DESCRIPTION

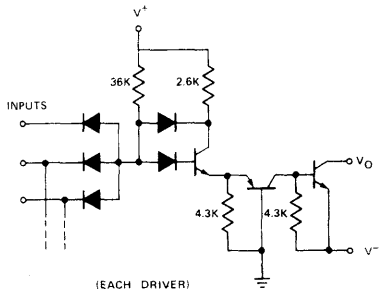
The D129 is a 4-channel driver with binary decode input. It has been designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V^- terminal can be set at any voltage between -5V and -30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V^- in the off-state.

The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)





ORDERING INFORMATION

D129 A K

- K — Package
  - K — 14-pin CERDIP
  - L — 14-pin Flat Pak
  - P — 14-pin Ceramic DIP (Special Order Only)
- A — Temperature Range
  - A — -55°C to +125°C
  - B — -20°C to +85°C
- D129 — Device Chip Type

ABSOLUTE MAXIMUM RATINGS

$V_O - V^-$	50V
GND – V^-	33V
V^+ – GND	8V
V_{IN} – GND	±6V
Current (any terminal)	30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation (note)	750mW
Lead Temperature (Soldering, 10 sec)	300°C

Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient termperatures.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

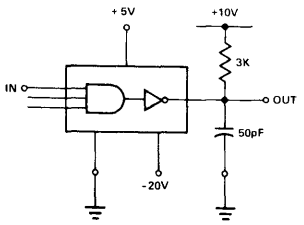
3

ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified V^- = −20V, V^+ = 5V

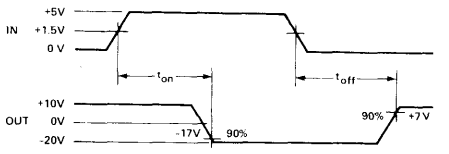
	PARAMETER		CONDITIONS		MAX LIMITS D129M −55°C	D129M 25°C	D129M 125°C	D129I −20°C	D129I 25°C	D129I 85°C	UNIT
OUT	V_{OL}	Output Voltage, Low	I_O = 10mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.3	-19.3	-19	-19.25	-19.25	-19	V
OUT	V_{OL}	Output Voltage, Low	I_O = 1mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.8	-19.8	-19.75				V
OUT	I_{OH}	Output Current, High	V_O= 10V, V_{IN} = 0.7V		0.1	0.1	20	0.2	0.2	10	µA
IN	I_{INH}*	Input Current Input Voltage High	V_{IN}= 5V Input Under Test, V_{IN}= 0 All Other Inputs		0.25	0.25	5	1	1	5	µA
IN	I_{INL}*	Input Current, Input Voltage Low	V_{IN} = 0, V^+ = 5.5V		-250	-200	-160	-250	-225	-200	µA
TIME	t_{on}	Turn-ON Time	See Switching Time Test Circuit			0.25			0.3		µs
TIME	t_{off}	Turn-OFF Time	See Switching Time Test Circuit			1.0			1.5		µs
SUPPLY	I_{EE}	Negative Supply Current	V^- = −20V, V^+ = 5.5V	One Channel "ON"		- 2			- 2.25		mA
SUPPLY	I_L	Logic Supply Current	V^- = −20V, V^+ = 5.5V	One Channel "ON"		3			3.3		mA
SUPPLY	I_{EE}	Negative Supply Current	V^- = −20V, V^+ = 5.5V	All V_{IN} = 0, All Channels "OFF"		-10			-25		µA
SUPPLY	I_L	Logic Supply Current	V^- = −20V, V^+ = 5.5V	All V_{IN} = 0, All Channels "OFF"		0.75			1		mA

* Per gate Input

SWITCHING TIME AND TEST CIRCUIT



t_f = 100ns
t_r = 100ns
t_{pw} = 1µs
f = 100K Hz



INTERSIL DG139, DG142 — DG146, DG161 — DG164

Drivers with Differentially Driven FET Switches

FEATURES

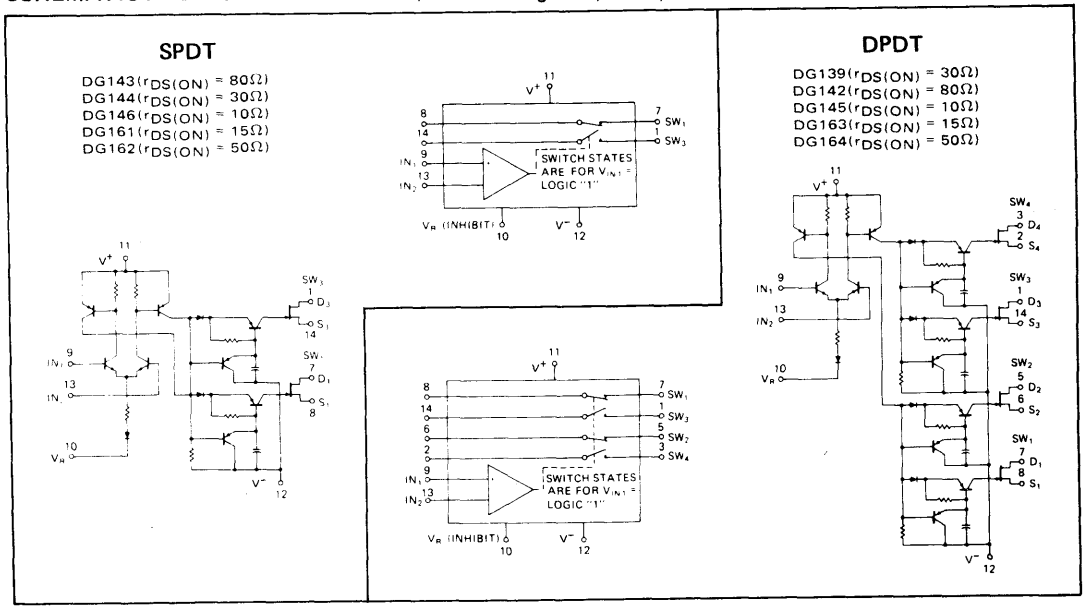
- Each channel complete-interfaces with most integrated logic
- Low OFF power dissipation, 1 mW
- Switches analog signals up to 20 volts peak-to-peak
- Low $r_{DS(ON)}$, 10 ohms max on DG145 and DG146

GENERAL DESCRIPTION

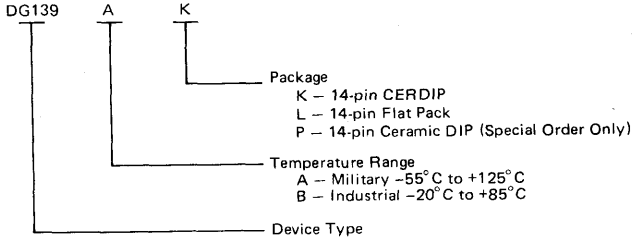
Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

3

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ 36V
$V_S - V^-$ 30V
$V^+ - V_S$ 30V
$V_S - V_D$ . . . . . ±22V
$V_R - V^-$ 21V
$V^+ - V_R$ 17V
$V^+ - V_{IN1}$ or V_{IN2} . 14V
$V_{IN1} - V_{IN2}$ . . . . . ±6V
$V_{IN1} - V_R$ . . . . . ±6V
$V_{IN2} - V_R$ . . . . . ±6V
Power Dissipation (Note) . . . . . 750 mW
Current (any terminal) . . . . . 30 mA

Storage Temperature . . . . . -65 to +150°C
Operating Temperature . . . . . -55 to +125°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG139, DG142, DG143, DG144, DG145, DG146 (V^+ = 12V, V^- = -18V, V_R = 0, V_{IN2} = 2.5V) and DG161, DG162, DG163, DG164 (V^+ = 15V, V^- = -15V, V_R = 0, V_{IN2} = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage—On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$V_{IN(OFF)}$	Input Voltage—Off		1.4	1.0	0.6	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$\|V_9 - V_{13}\|$	Differential Voltage		0.5 min	0.5 min	0.5 min	Volts	See Note 1, Pg. 4
	$I_{IN1(ON)}$	Input Current		120	60	60	µA	V_{IN1} 3.0V
	$I_{IN2(ON)}$			120	60	60	µA	V_{IN2} 2.0V
	$I_{IN1(OFF)}$	Input Leakage Current		0.1	0.1	2	µA	V_{IN1} 2.0V
	$I_{IN2(OFF)}$			0.1	0.1	2	µA	V_{IN2} 3.0V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG142, DG143	80	80	150	Ω	V_D = 10V, I_S = -10mA
			DG139, DG144	30	30	60	Ω	
			DG145, DG146	10	10	20	Ω	V_D = 10V, I_S = -10mA
			DG161, DG163	15	15	30	Ω	V_D 7.5V, I_S -10 mA
			DG162, DG164	50	50	100	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG139, DG142, DG143, DG144		2	100	nA	V_D V_S -10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S 10V, V_D -10V
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	V_D 10V, V_S -10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG145, DG146		2	100	nA	V_D V_S -10V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S 10V, V_D -10V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D 10V, V_S -10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG161, DG163		2	500	nA	V_D V_S -7.5V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S 7.5V, V_D -7.5V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D 7.5V, V_S -7.5V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG162, DG164		2	500	nA	V_D V_S -7.5V
	$I_{S(OFF)}$	Source Leakage Current			2	200	nA	V_S 7.5V, V_D -7.5V
	$I_{D(OFF)}$	Drain Leakage Current			2	200	nA	V_D 7.5V, V_S -7.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		4.0		mA	V_{IN1} 3V or V_{IN1} 2V
	$I_{2(ON)}$	Negative Power Supply Drain Current			-2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			-2.0		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		µA	V_{IN1} V_{IN2} 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			-25		µA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			-25		µA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

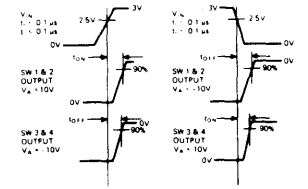
ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°C	25°	125°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164		0.8		µs	See Below
			DG139, DG142 DG143, DG144 DG162, DG164		0.4	0.7	µs	
	t_{OFF}	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164		1.6		µs	See Below
			DG139, DG142 DG143, DG144 DG162, DG164		0.8	1.2	µs	
	t_{ON}	Turn-On Time	DG145, DG146 DG161, DG163		1.0		µs	See Below
			DG145, DG146 DG161, DG163		0.5	0.8	µs	
	t_{OFF}	Turn-Off Time	DG145, DG146 DG161, DG163		2.5		µs	See Below
			DG145, DG146 DG161, DG163		1.25	1.8	µs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

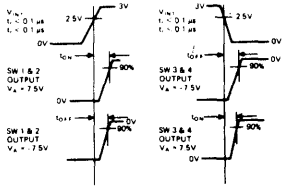
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (25°C)

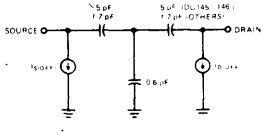
DG139, 142, 143, 144, 145, 146



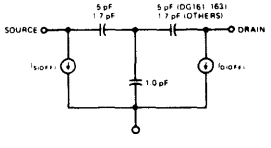
DG161, 162, 163, 164



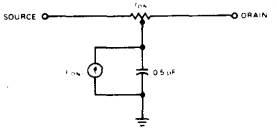
OFF MODEL



OFF MODEL



ON MODEL



ON MODEL

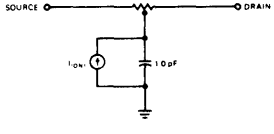


FIGURE 1

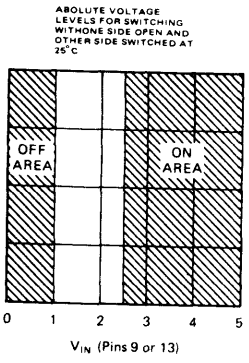
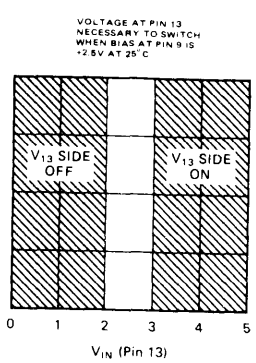


FIGURE 2

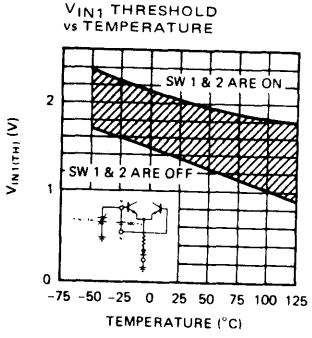


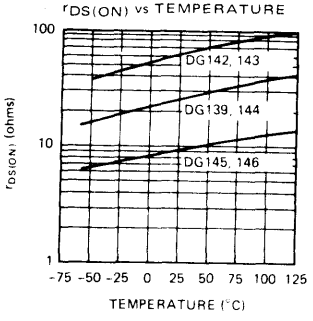
3

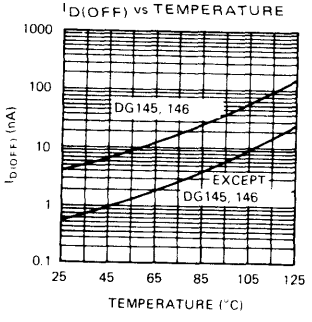
NOTE1: An example of Absolute Minimum Differential Voltage, $|V_9 - V_{13}|$, is when V_9 = 3V and V_{13} = 2.5V, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when V_9 = 2V and V_{13} = 2.5V, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

TYPICAL CHARACTERISTICS (per channel)

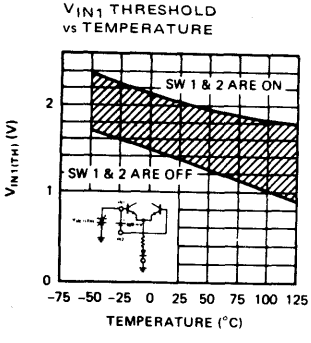
DG139, 142, 144, 145, 146

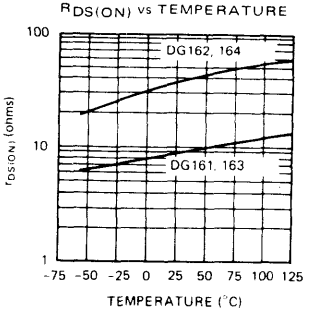


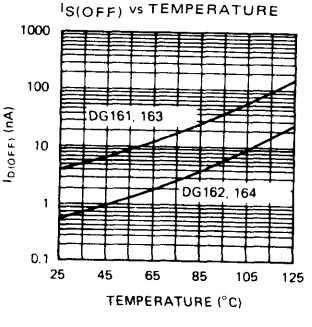




DG161, 162, 163, 164







DG180-191

High-Speed Driver With Junction FET Switches

FEATURES

- **Constant ON-resistance for signals to ±10V (DG182, 185, 188, 191), to ±7.5V (all devices)**
- **±15V power supplies**
- **<2nA leakage from signal channel in both ON and OFF states**
- **TTL, DTL, RTL direct drive compatibility**
- **t_{on}, t_{off} <150ns, break-before-make action**
- **Cross-talk and open switch isolation >50dB at 10MHz (75Ω load)**

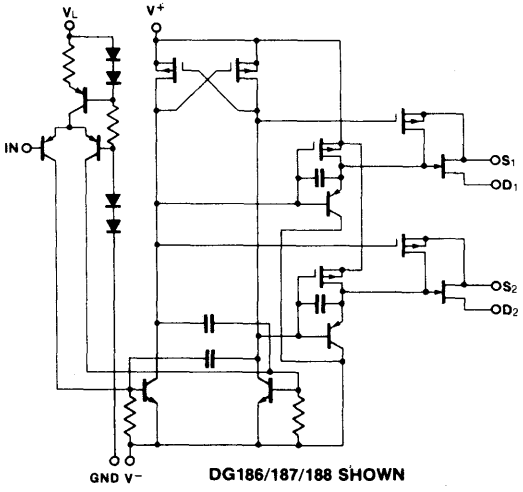
GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consists of 2 or 4 N-channel junction-type field-effect transistors (J-FET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output feedthrough is >50dB down at 10MHz, because of the low output impedance of the FET-gate driving circuit.

3

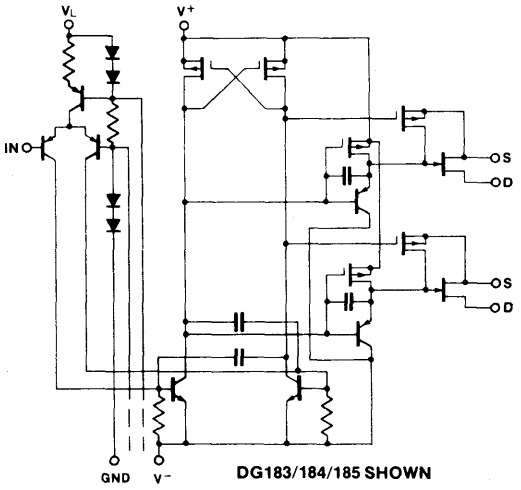
SCHEMATIC DIAGRAM (Typical Channel)

ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION



DG186/187/188 SHOWN

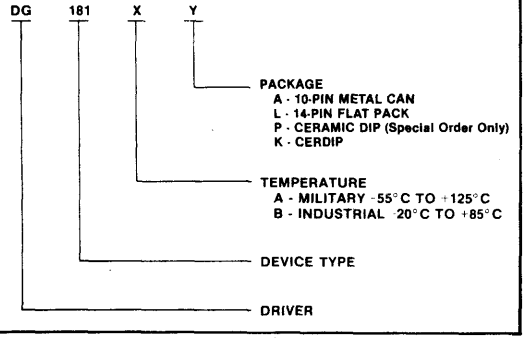
TWO CHANNEL DPST CIRCUIT CONFIGURATION



DG183/184/185 SHOWN

ORDERING INFORMATION

PART NUMBER	TYPE	$r_{DS(on)}$ (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75



MAXIMUM RATINGS

V^+-V^- 36V
V^+-V_D 33V
V_D-V^- 33V
V_D-V_S ..... ±22V
V_L-V^- 36V
V_L-V_{IN} 8V
V_L-GND 8V
V_{IN}-GND 8V
GND-V^- 27V
GND-V_{IN} 20V
Lead Temperature (Soldering, 10 sec) ..... 300°C
Current (S or D) See Note 3 ..... 200mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation* ..... 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, Unless Noted)

	PARAMETER	DEVICE	A SERIES −55°C	A SERIES +25°C	A SERIES +125°C	B SERIES −20°C	B SERIES +25°C	B SERIES +85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	$I_{S(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, V_{IN} = "OFF"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DG182, 185, 188, 191		1	100		5	100	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, V_{IN} = "OFF"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DG182, 185, 188, 191		1	100		5	100	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(on)} + I_{S(on)}$	DG180, 181, 183, 184 186, 187, 189, 190		−2	−200		−10	−200	nA	$V_D = V_S = -7.5V$, V_{IN} = "ON"
		DG182, 185, 188, 191		−2	−200		−10	−200	nA	$V_D = V_S = -10V$, V_{IN} = "ON"
INPUT	I_{INL}	ALL	−250	−250	−250	−250	−250	−250	µA	$V_{IN} = 0V$
	I_{INH}	ALL		10	20		10	20	µA	$V_{IN} = 5V$
DYNAMIC	t_{on}	10Ω Switches		300			350		ns	See switching time test circuit
		30Ω Switches		150			180			
		75Ω Switches		250			300			
	t_{off}	10Ω Switches		250			300			
		30Ω and 75Ω Switches		130			150			
	$C_{S(off)}$	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186, 189)	9 typical (21 typical)						pF	$V_S = -5V$, $I_D = 0$, f = 1MHz
	$C_{D(off)}$		6 typical (17 typical)							$V_D = +5V$, $I_S = 0$, f = 1MHz
	$C_{D(on)} + C_{S(on)}$		14 typical (17 typical)							$V_D = V_S = 0$, f = 1MHz
	OFF Isolation		Typically >50dB at 10MHz (See Note 2)							$R_L = 75Ω$, $C_L = 3pF$
SUPPLY	I^+	DG180, 181, 182, 189 190, 191		1.5			1.5		mA	$V_{IN} = 5V$
		DG183, 184, 185		0.1			0.1			
		DG186, 187, 188		0.8			0.8			
	I^-	DG180, 181, 182, 189, 190, 191		−5.0			−5.0			
		DG183, 184, 185		−4.0			−4.0			
		DG186, 187, 188		−3.0			−3.0			
	I_L	DG180, 181, 182, 183, 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_{GND}	ALL		−2.0			−2.0			
	I^+	DG180, 181, 182, 189, 190, 191		1.5			1.5			$V_{IN} = 0V$
		DG183, 184, 185		3.0			3.0			
		DG186, 187, 188		0.8			0.8			
	I^-	DG180, 181, 182, 189, 190, 191		−5.0			−5.0			
		DG183, 184, 185		−5.5			−5.5			
		DG186, 187, 188		−3.0			−3.0			
	I_L	DG180, 181, 182, 183, 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_{GND}	ALL		−2.0			−2.0			

Note 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.
Note 2: Off Isolation typically >55dB at 1MHz for DG180, 183, 186, 189.
Note 3: Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2msec Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

ELECTRICAL CHARACTERISTICS (CONT'D)

MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

DEVICE NUMBER	MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNITS	CONDITIONS (Note 1) $V^+ = 15V$, $V^- = -15V$, $V_L = 5V$	
	−55°C	+25°C	+125°C	−20°C	+25°C	+85°C			
DG180	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG181	30	30	60	50	50	75	Ω	$V_D = -7.5V$	
DG182	75	75	100	100	100	150	Ω	$V_D = -10V$	
DG183	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG184	30	30	60	50	50	75	Ω	$V_D = -7.5V$	
DG185	75	75	150	100	100	150	Ω	$V_D = -10V$	$I_S = -10mA$
DG186	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG187	30	30	60	50	50	75	Ω	$V_D = -7.5V$	V_{IN} = "ON"
DG188	75	75	150	100	100	150	Ω	$V_D = -10V$	
DG189	10	10	20	15	15	25	Ω	$V_D = -7.5V$	
DG190	30	30	60	50	50	50	Ω	$V_D = -7.5V$	
DG191	75	75	150	100	100	150	Ω	$V_D = -10V$	

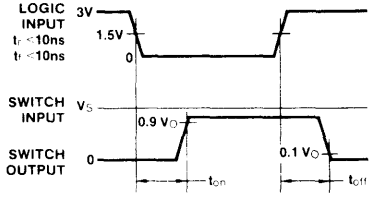
APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω switches (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V^- \leq V_{ANALOG}(peak) - V_p$ where $V_p = 7.5V$ for the 10Ω and 30Ω switches and $V_p = 5.0V$ for 75Ω switches e.g., −10V minimum (−peak) analog signal and a 75Ω switch ($V_p = 5V$), requires that $V^- \leq -10V - 5V = -15V$.

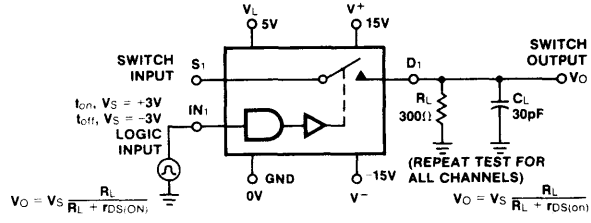
3

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. *Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.*

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)





DUAL SPST
DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

DUAL DPST
DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

SPDT
DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

DUAL SPDT
DG189/190/191

TEST CONDITIONS

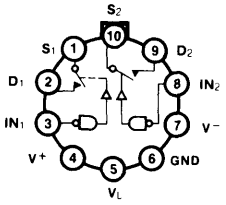
DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

PIN CONFIGURATIONS AND SWITCHING STATE DIAGRAM (See previous page for logic input)

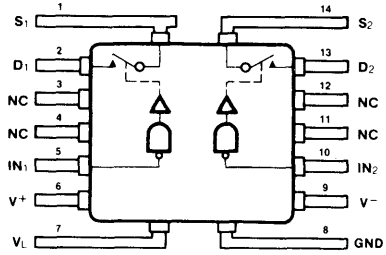
DUAL SPST (DG180, 181, 182)

Metal Can Package



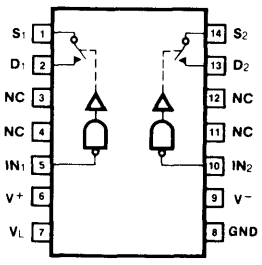
(OUTLINE DWG TO-100)

Flat Package



(OUTLINE DWG FD-2)

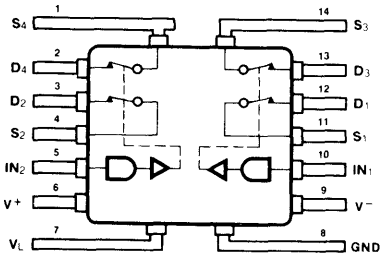
CERDIP*



(OUTLINE DWG JD)

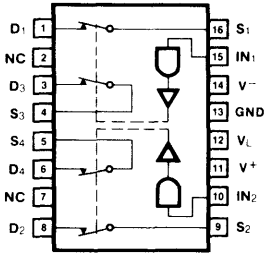
DUAL DPST (DG183, 184, 185)

Flat Package



(OUTLINE DWG FD-2)

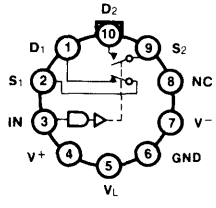
CERDIP*



(OUTLINE DWG JE)

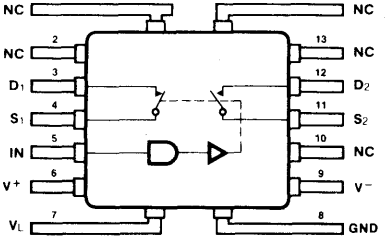
SPDT (DG186, 187, 188)

Metal Can Package



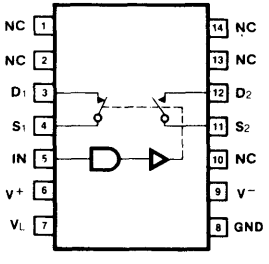
(OUTLINE DWG TO-100)

Flat Package



(OUTLINE DWG FD-2)

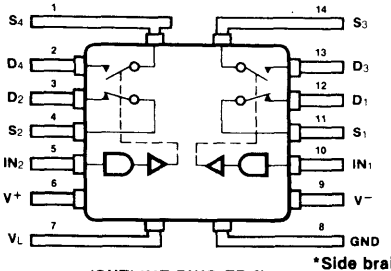
CERDIP*



(OUTLINE DWG JD)

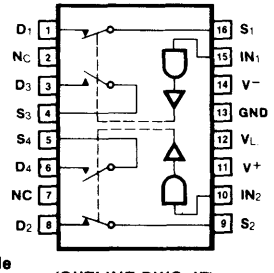
DUAL SPDT (DG189, 190, 191)

Flat Package



(OUTLINE DWG FD-2)

CERDIP*



(OUTLINE DWG JE)

*Side braize ceramic package available as special order only. Consult factory.

DGM181-191
High-Speed CMOS Analog Switches

FEATURES
- **Pin and Function Replacement for DG181 Family**
- **Meets or exceeds all DG181 family specifications with monolithic reliability**
- **Low power consumption**
- **1nA leakage from signal channel in both ON and OFF states**
- **TTL, DTL, RTL direct drive capability**
- **t_{on}, t_{off} < 150ns, break-before-make action**
- **Crosstalk and open load switch isolation > 50dB at 10MHz (75Ω load)**

GENERAL DESCRIPTION
The DGM181 family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to combine the speed of the hybrid DG181 family with the reliability and low power consumption of a monolithic CMOS construction. These devices, therefore, are an ideal replacement for the DG181 family.

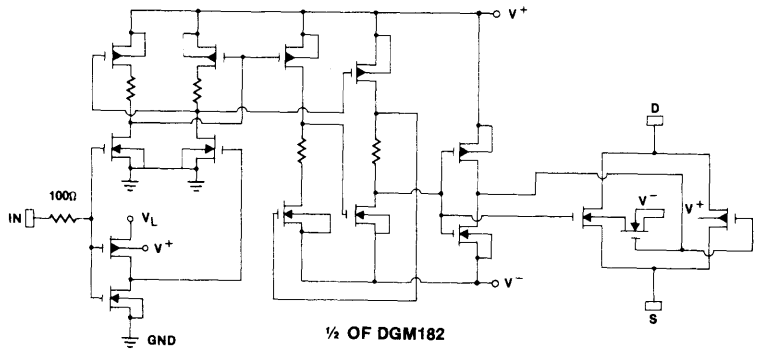
The DGM181 family has a high state threshold of 2.4V; devices which have a threshold of 2.0V (the DG181 specification) can be selected and are available as the DGMS series — see ordering information.

Both series meet or exceed all other specifications of the DG181 family.

No quiescent power is dissipated in either the ON or OFF state of the switch. Maximum power supply current is 10μA from any supply, and typical quiescent currents are in the 10nA range. OFF leakages are guaranteed to be less than 200pA at 25°C.

3

SCHEMATIC DIAGRAM (Typical Channel)



½ OF DGM182

ORDERING INFORMATION

TYPE	STANDARD PART NUMBER	SELECTED PART NUMBER	$r_{DS(on)}$ MAX AT 25°C
Dual SPST	DGM181BX	DGMS181BX	50
	DGM182AX	DGMS182AX	50
	DGM182BX	DGMS182BX	75
Dual DPST	DGM184BX	DGMS184BX	50
	DGM185AX	DGMS185AX	50
	DGM185BX	DGMS185BX	75
SPDT	DGM187BX	DGMS187BX	50
	DGM188AX	DGMS188AX	50
	DGM188BX	DGMS188BX	75
Dual SPDT	DGM190BX	DGMS190BX	50
	DGM191AX	DGMS191AX	50
	DGM191BX	DGMS191BX	75

DGM S 181 A A

- PACKAGE
  - A · 10-PIN METAL CAN
  - L · 14-PIN FLAT PACK
  - K · CERAMIC DIP
  - J · EPOXY DIP
- TEMPERATURE RANGE
  - A · MILITARY −55°C TO +125°C
  - B · INDUSTRIAL −20°C TO +85°C
- DEVICE TYPE
- OPTION
- CMOS ANALOG DRIVER

DGM181-191

INTERSIL

MAXIMUM RATINGS

V^+-V^- 36V
V^+-V_D 33V
V_D-V^- 33V
V_D-V_S ..... ±22V
V_L-V^- 36V
Current (Any Terminal) 30mA
V_L-V_{IN} 30V
V_L-V_{GND} 20V
V_{IN}-V_{GND} 20V
GND-V^- 27V
GND-V_{IN} 20V

Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation* ..... 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, unless noted)

	PARAMETER	DEVICE	A SERIES −55°C	A SERIES +25°C	A SERIES +125°C	B SERIES −20°C	B SERIES +25°C	B SERIES +85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	$I_{S(off)}$	DGM181, 184, 187, 190					2.0	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DGM182, 185, 188, 191		0.2	50		0.5	50	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(off)}$	DGM181, 184, 187, 190					2.0	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DGM182, 185, 188, 191		0.2	50		0.5	50	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(on)} + I_{S(on)}$	DGM181, 184, 187, 190					5.0	100	nA	$V_D = V_S = -7.5V$, V_{IN} = "ON"
		DGM182, 185, 188, 191		0.5	50		2.0	50	nA	$V_D = V_S = -10V$, V_{IN} = "ON"
IN	I_{INL}	ALL		1.0	20		10	20	µA	$V_{IN} = 0V$
	I_{INH}	ALL		1.0	20		10	20	µA	$V_{IN} = 5V$
DYNAMIC	t_{on}	DGM181, 184, 187, 190					180		ns	See switching time test circuit
		DGM182, 185, 188, 191		250			300			
	t_{off}	ALL		130			150			
	$C_{S(off)}$	DGM181, 182, 184, 185, 187, 188, 190, 191	5pF typical						pF	$V_S = -5V$, $I_D = 0$, f = 1MHz
	$C_{D(off)}$		6pF typical							$V_D = +5V$, $I_S = 0$, f = 1MHz
	$C_{D(on)} + C_{S(on)}$		11pF typical							$V_D = V_S = 0$, f = 1MHz
	OFF Isolation		Typically >50dB at 10MHz							$R_L = 75\Omega$, $C_L = 3pF$
SUPPLY	I^+	ALL		10	100		100		µA	$V_{IN} = 5V$
	I^-	ALL		10	100		100			
	I_L	ALL		10	100		100			
	I_{GND}	ALL		10	100		100			
	I^+	ALL		10	100		100			$V_{IN} = 0V$
	I^-	ALL		10	100		100			
	I_L	ALL		10	100		100			
	I_{GND}	ALL		10	100		100			

NOTE 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.

ELECTRICAL CHARACTERISTICS

MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

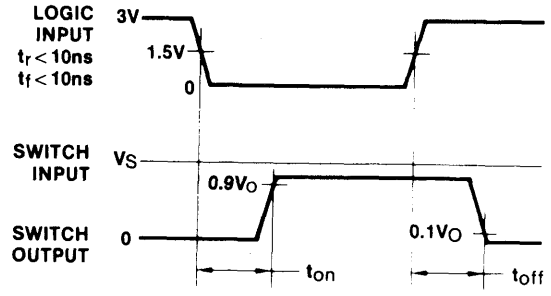
DEVICE NUMBER	MILITARY TEMPERATURE −55°C	MILITARY TEMPERATURE +25°C	MILITARY TEMPERATURE +125°C	INDUSTRIAL TEMPERATURE −20°C	INDUSTRIAL TEMPERATURE +25°C	INDUSTRIAL TEMPERATURE +85°C	UNITS	CONDITIONS (Note 1) $V^+ = 15V$, $V^- = -15V$, $V_L = 5V$	
DGM181				50	50	75	Ω	$V_D = -7.5V$	
DGM182	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM184				50	50	75	Ω	$V_D = -7.5V$	
DGM185	50	50	75	75	75	100	Ω	$V_D = -10V$	$I_S = -10mA$
DGM187				50	50	75	Ω	$V_D = -7.5V$	V_{IN} = "ON"
DGM188	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM190				50	50	75	Ω	$V_D = -7.5V$	
DGM191	50	50	75	75	75	100	Ω	$V_D = -10V$	

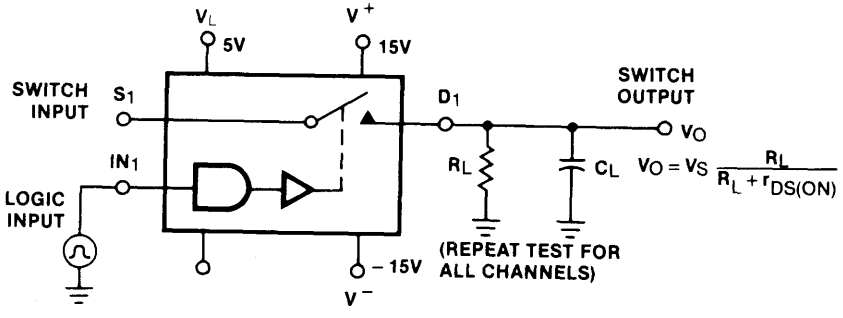
APPLICATION COMMENT: The charge injection in these switches is of opposite polarity to that of the standard DG180 family, but considerably smaller.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)





SWITCH STATES

DUAL SPST
DGM181/182

TEST CONDITIONS	
DGM181/182	
V_{IN}"ON" = 0.8V	All Channels
V_{IN}"OFF" = 2.4V+	All Channels

DUAL DPST
DGM184/185

TEST CONDITIONS	
DGM184/185	
V_{IN}"ON" = 2.4V+	All Channels
V_{IN}"OFF" = 0.8V	All Channels

SPDT
DGM187/188

TEST CONDITIONS	
DGM187/188	
V_{IN}"ON" = 2.4V+	Channel 1
V_{IN}"ON" = 0.8V	Channel 2
V_{IN}"OFF" = 2.4V+	Channel 2
V_{IN}"OFF" = 0.8V	Channel 1

DUAL SPDT
DGM190/191

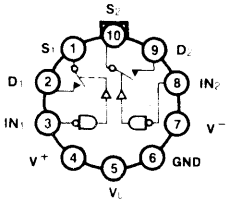
TEST CONDITIONS	
DGM190/191	
V_{IN}"ON" = 2.4V+	Channels 1 & 2
V_{IN}"ON" = 0.8V	Channels 3 & 4
V_{IN}"OFF" = 2.4V+	Channels 3 & 4
V_{IN}"OFF" = 0.8V	Channels 1 & 2

† FOR SELECTED DEVICES, LOGIC "1" INPUT = 2.0V

PIN CONFIGURATIONS & SWITCHING STATE DIAGRAM

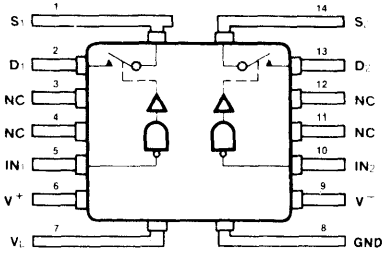
DUAL SPST (DGM181, 182)

Metal Can Package



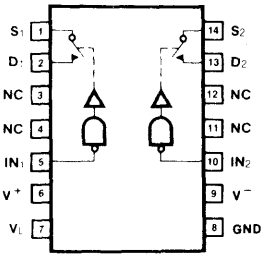
(OUTLINE DWG TO-100)

Flat Package (FD-2)



SWITCH STATES ARE FOR LOGIC "1" INPUT

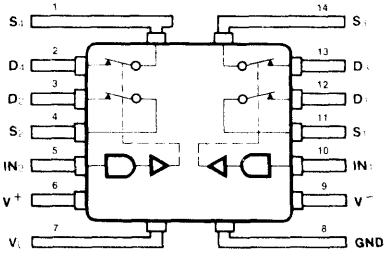
Dual-In-Line Package



(OUTLINE DWGS DD, PD)

DUAL DPST (DGM184, 185)

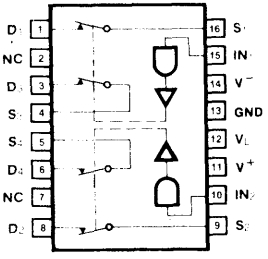
Flat Package



(OUTLINE DWG FD-2)

SWITCH STATES ARE FOR LOGIC "1" INPUT

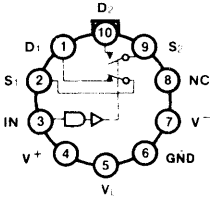
Dual-In-Line Package



(OUTLINE DWGS DE, PE)

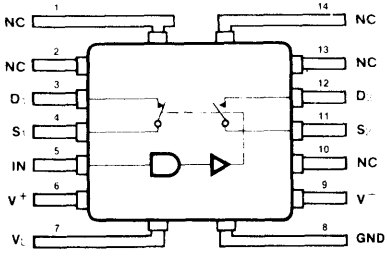
SPDT (DGM187, 188)

Metal Can Package



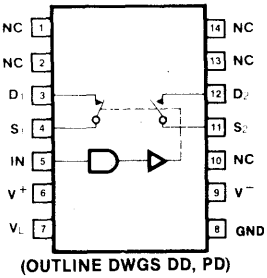
(OUTLINE DWG TO-100)

Flat Package (FD-2)



SWITCH STATES ARE FOR LOGIC "1" INPUT

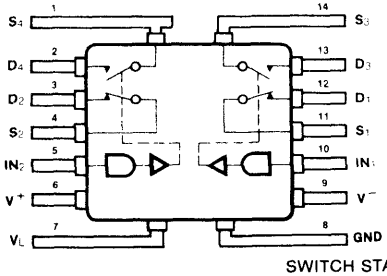
Dual-In-Line Package



(OUTLINE DWGS DD, PD)

DUAL SPDT (DGM190, 191)

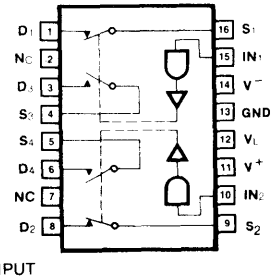
Flat Package



(OUTLINE DWG FD-2)

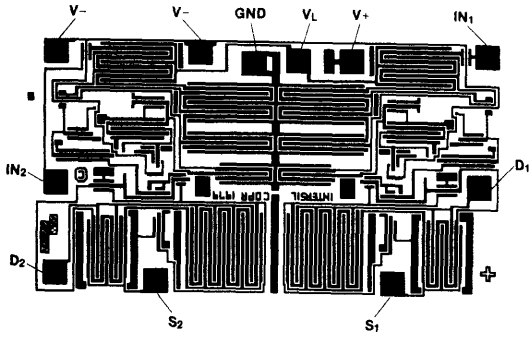
SWITCH STATES ARE FOR LOGIC "1" INPUT

Dual-In-Line Package



(OUTLINE DWGS DE, PE)

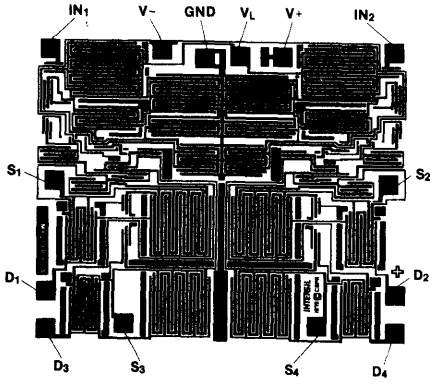
CHIP TOPOGRAPHIES



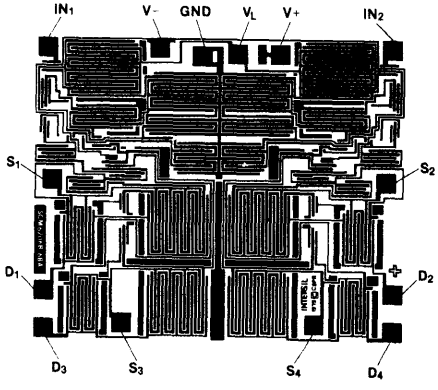
DGM181/182
91x53

CONSULT FACTORY

DGM188



DGM185
91x76



DGM191
91x76

NOTE: BACKSIDE OF CHIP IS COMMON TO V+.

DG200/IH5200
CMOS Dual SPST Analog Switches

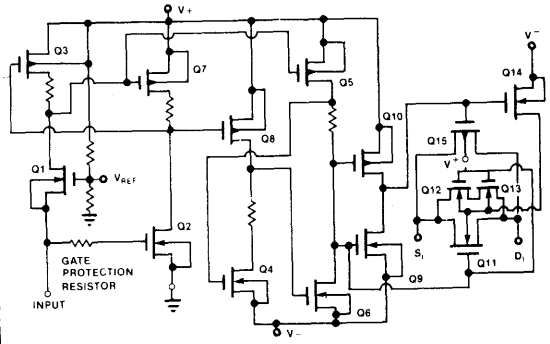
FEATURES
- **Switches Greater Than 28Vpp Signals With ± 15V Supplies**
- **Break-Before-Make Switching t_{off} 250 nsec, t_{on} 700nsec Typical**
- **T^2L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG200)**
- **Improved Performance Version (IH5200)**

3

GENERAL DESCRIPTION
The DG200/IH5200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG200 is completely spec and pin-out compatible with the industry standard device, while the IH5200 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (½ DG200/IH5200)

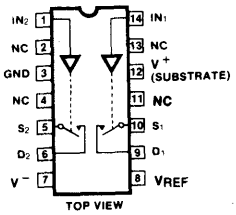


ORDERING INFORMATION

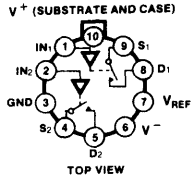
INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG200AA	IH5200MTW	10-Pin Metal Can	−55 to +125°C
DG200AK	IH5200MJD	14-Pin CERDIP	−55 to +125°C
DG200AL	IH5200MFD	14-Pin Flat Pak	−55 to +125°C
DG200BA	IH5200ITW	10-Pin Metal Can	−25 to +85°C
DG200BK	IH5200IJD	14-Pin CERDIP	−25 to +85°C
DG200BL	IH5200IFD	14-Pin Flat Pak	−25 to +85°C
DG200CJ	IH5200CPD	14-Pin Epoxy DIP	0 to +70°C

PIN CONFIGURATIONS

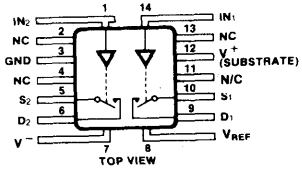
CERDIP & EPOXY DUAL-IN-LINE PACKAGE
(outline dwgs JD, PD)



METAL CAN PACKAGE
(outline dwg TO-100)



FLAT PACKAGE
(outline dwg FD-2)



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

INTERSIL

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... >30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board.) Derate 6mW/°C Above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DG200

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL/INDUSTRIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(on)}$	Drain-Source On Resistance	70	70	100	80	80	100	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(on)}$	Channel-to-Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±15			±15		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	2	2	100	5	5	100	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{S(OFF)}$	Switch OFF Leakage Current	2	2	100	5	5	100	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	2	2	200	10	10	200	nA	$V_D = V_S = -14V$ to $+14V$
t_{on}	Switch "ON" Time		1.0			1.0		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_{V1}	+ Power Supply Quiescent Current	1000	1000	2000	1000	1000	2000	μA	$V_{IN} = 0V$ or $V_{IN} = 5V$
I_{V2}	− Power Supply Quiescent Current	1000	1000	2000	1000	1000	2000	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

Note 1: These parameters are not tested in production.

TEST CIRCUITS

Figure A

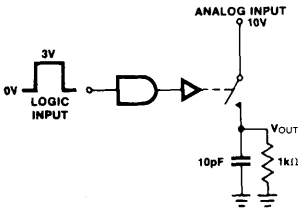


Figure B

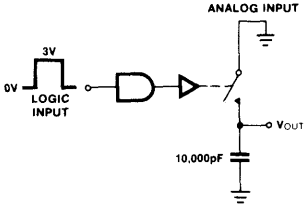
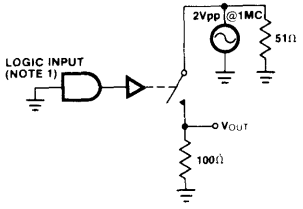


Figure C



3

IH5200

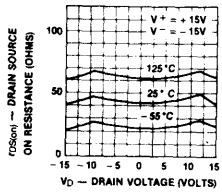
ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, V_{REF} open)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL/INDUSTRIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(on)}$	Drain-Source On Resistance	70	70	100	80	80	100	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(on)}$	Channel-to-Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±15			±15		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = -14V$ to $+14V$
t_{on}	Switch "ON" Time		0.7			0.8		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.4		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_{V1}	+ Power Supply Quiescent Current	250	200	150	300	250	200	μA	$V_{IN} = 0V$ or $V_{IN} = 5V$
I_{V2}	− Power Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

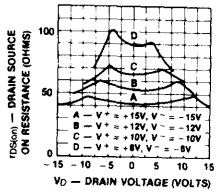
Note 1: These parameters are not tested in production.

TYPICAL CHARACTERISTICS

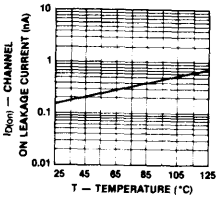
$r_{DS(on)}$ vs V_D and Temperature



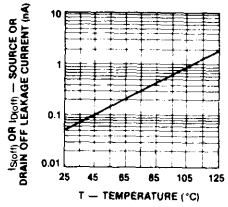
$r_{DS(on)}$ vs V_D and Power Supply Voltage



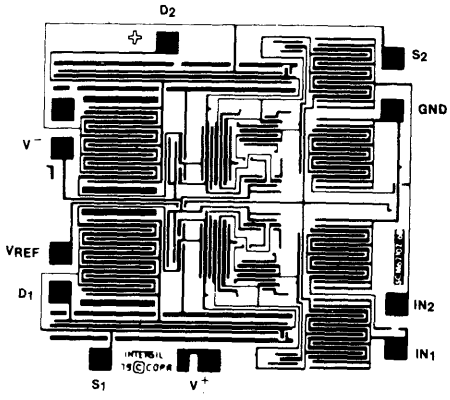
$I_{D(on)}$ vs Temperature*



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



CHIP TOPOGRAPHY



NOTE: Backside of chip of common to V+.

3

APPLICATIONS

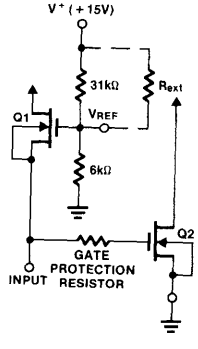
Using the V_{REF} Terminal

The DG200 has an internal voltage divider setting the TTL threshold on the input control lines for +15V on V^+. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be < 0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds > 1.5V, allowing the user to define the "low" as < 1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to > 4.1V. An external resistor of 27kΩ between V^+ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	—	—
+12	100	—
+10	51	—
+9	(34)	34
+8	(27)	27
+7	18	18



DG201/IH5201
Quad SPST CMOS Analog Switches

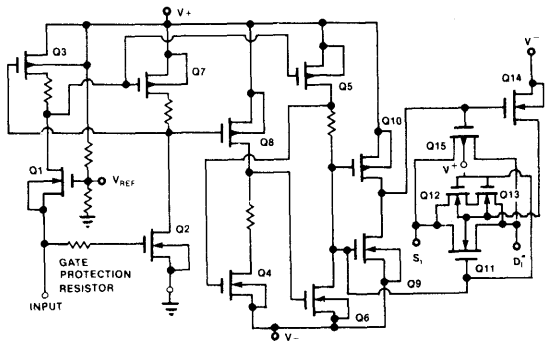
FEATURES
- **Switches Greater Than 28V_{p-p} Signals With ± 15V Supplies**
- **Break-Before-Make Switching t_{off} = 250nsec, t_{on} = Typically 500nsec**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG201)**
- **Improved Performance Version IH5201**

3

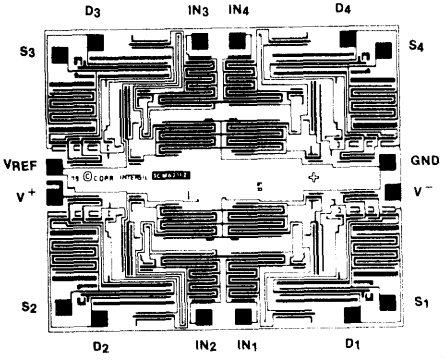
GENERAL DESCRIPTION
The DG201/IH5201 solid-state analog gates are designed using an improved, high-voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG201 is completely spec and pin-out compatible with the industry standard device, while the IH5201 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (¼ DG201/IH5201)



CHIP TOPOGRAPHY



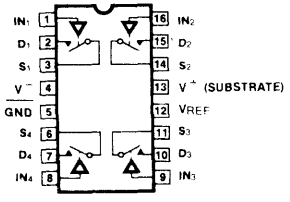
NOTE: Backside of chip common to V+.

ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG201AK	IH5201MJE	16-Pin CERDIP	−55°C to +125°C
DG201BK	IH5201IJE	16-Pin CERDIP	−20°C to +85°C
DG201CJ	IH5201CPE	16-Pin Plastic DIP	0°C to +70°C

PIN CONFIGURATION (outline dwgs JE, PE)

DUAL-IN-LINE PACKAGE



SWITCH OPEN FOR LOGIC "1" INPUT

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_{REF} - V^-$ ..... <33V
$V_{REF} - V_{IN}$ ..... <30V
V_{REF}-GND ..... <20V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DG201

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	80	80	125	100	100	125	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Analog Signal Handling Capability		± 15			± 15		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{S(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	2	2	200	5	5	200	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		1.0			1.0		μs	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		μs	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1MHz, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_Q^+	+ Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	μA	$V_{IN} = 0V$ or 5V
I_Q^-	− Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

Note 1: These parameters not tested in production.

TEST CIRCUITS

Figure A

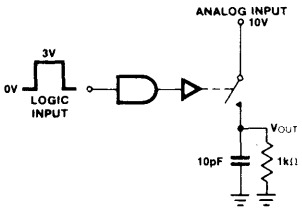


Figure B

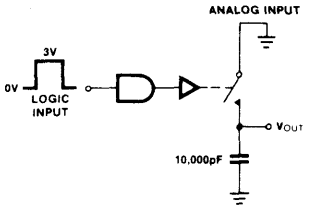
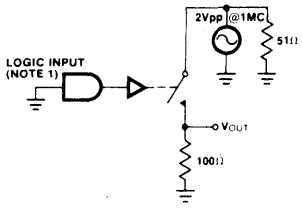


Figure C



3

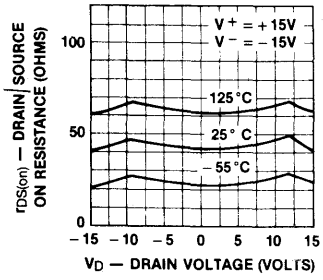
IH5201

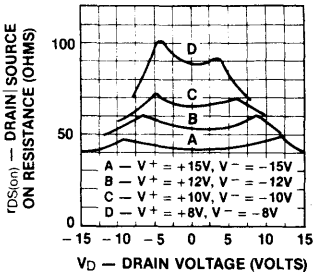
ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

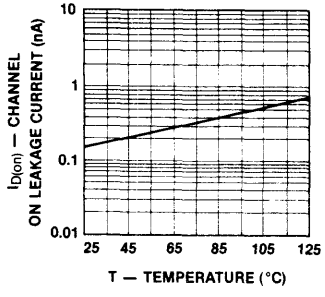
PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	100	100	125	Ω	$I_S = 10mA$ $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Analog Signal Handling Capability		± 15			± 15		V	
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		0.5			0.75		μs	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.3		μs	$R_L = 1k\Omega$, V_{ANALOG} $= -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C, (Note 1)
I_Q^+	+ Power Supply Quiescent Current	1000	750	600	1500	1000	1000	μA	$V_{IN} = 0V$ to $5V$
I_Q^-	− Power Supply Quiescent Current	10	10	100	20	20	200	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off (Note 1)

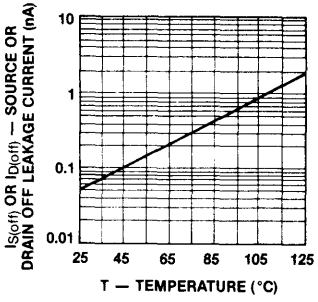
Note 1: These parameters not tested in production.

TYPICAL CHARACTERISTICS









APPLICATIONS

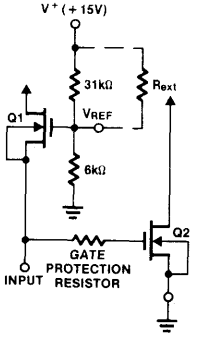
Using the V_{REF} Terminal

The DG201 has an internal voltage divider setting the TTL threshold on the input control lines for +15V on V^+. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds >1.5V, allowing the user to define the "low" as <1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27kΩ between V^+ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	—	—
+12	100	—
+10	51	—
+9	(34)	34
+8	(27)	27
+7	18	18



IH5009 — IH5024
Virtual Ground
Analog Switches

FEATURES

- **Switches Analog Signals up to 20 Volts Peak-to-Peak**
- **Each Channel Complete — Interfaces with Most Integrated Logic**
- **Switching Speeds Less than 0.5μs**
- **$I_{D(OFF)}$ Less than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ — 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

3

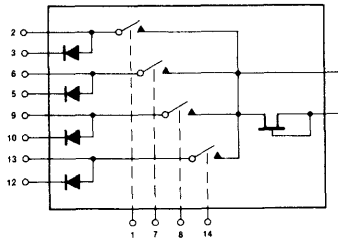
GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

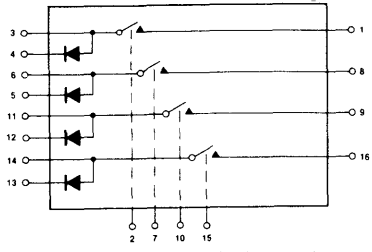
Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from T^2L open collector logic (15 volts) while the even numbered devices are driven directly from low level T^2L logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

PIN CONNECTIONS

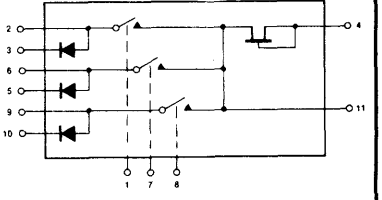
IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PD, JD)



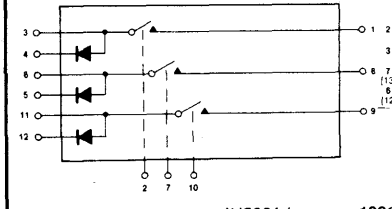
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)



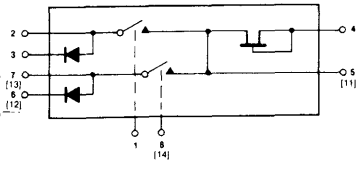
IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PE, JE)



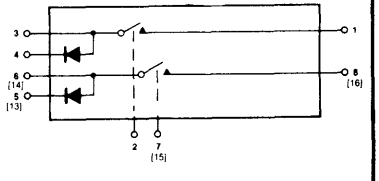
IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)



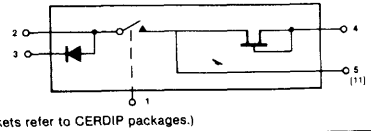
IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)



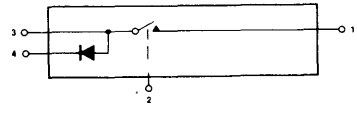
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA, JE)



IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA)



(Note: Numbers in brackets refer to CERDIP packages.)

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage ..... −15V
Diode Current 10mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Operating Temperature
5009C Series ..... 0°C to +70°C
5009M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT −55°C (M) 0°C (C) MIN/MAX	SPECIFICATION LIMIT 25°C TYP.	SPECIFICATION LIMIT 25°C MIN/MAX	SPECIFICATION LIMIT +125°C (M) +70°C (C) MIN/MAX	UNITS
$I_{IN(ON)}$	Input Current-ON	All	V_{IN} = 0V, I_D = 2mA	0.1	.01	0.1	100	µA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	V_{IN} = +4.5V, V_A = ±10V	0.2	.04	0.1	10	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	V_{IN} = +11V, V_A = ±10V	0.2	.04	0.2	10	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 5, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 6, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 5, Note 3	4.5		4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 6, Note 3	11.0		11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	V_{IN} = +4.5V, V_A = ±10V	0.2	.02	0.2	10	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	V_{IN} = +11V, V_A = ±10V	0.2	.02	0.2	10	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN} = 0V, I_S = 1mA	1.0	0.30	1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN} = 0V, I_S = 1mA	0.5	0.10	0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	V_{IN} = 0V, I_S = 2mA	1.0		1.0	10	µA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	V_{IN} = 0V, I_S = 2mA	2.0		2.0	1000	nA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	I_D = 2mA, V_{IN} = 0.5V	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	I_D = 2mA, V_{IN} = 1.5V	100	60	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 3 & 4		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 3 & 4		300	500		ns
CT	Cross Talk	All	f = 100Hz		120			dB

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

NOTE 2: Refer to Figure 2 for definition of terms.

NOTE 3: *$V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of respectively $r_{DS(ON)}$ and $I_{D(OFF)}$.*

NOTE 4: "5V Logic CKTS" applies to even-numbered devices.
"15V Logic CKTS" applies to odd-numbered devices.

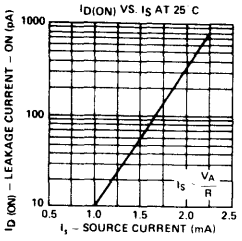
ORDERING INFORMATION

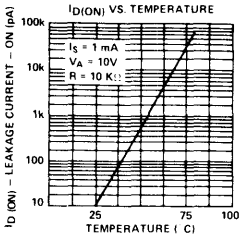
IH50XX — BASIC PART NUMBER
M — TEMPERATURE RANGE
M = MILITARY (−55°C to +125°C)
C = COMMERCIAL (0°C to +70°C)
DE — PACKAGE
PA — 8-PIN PLASTIC DIP
PD — 14-PIN PLASTIC DIP
PE — 16-PIN PLASTIC DIP
DD — 14-PIN CERAMIC DIP (Special Order Only)
DE — 16-PIN CERAMIC DIP (Special Order Only)
JD — 14-PIN CERDIP
JE — 16-PIN CERDIP

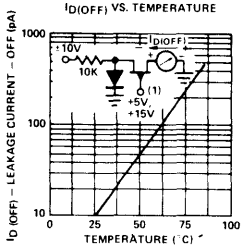
BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5009	4	+15	JD,DD,PD
IH5010	4	+ 5	JD,DD,PD
IH5011	4	+15	JE,DE,PE
IH5012	4	+ 5	JE,DE,PE
IH5013	3	+15	JD,DD,PD
IH5014	3	+ 5	JD,DD,PD
IH5015	3	+15	JE,DE,PE
IH5016	3	+ 5	JE,DE,PE
IH5017	2	+15	JD,DD,PA
IH5018	2	+ 5	JD,DD,PA
IH5019	2	+15	JE,DE,PA
IH5020	2	+ 5	JE,DE,PA
IH5021	1	+15	JD,DD,PA
IH5022	1	+ 5	JD,DD,PA
IH5023	1	+15	JE,DE,PA
IH5024	1	+ 5	JE,DE,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available ceramic packages only.

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)







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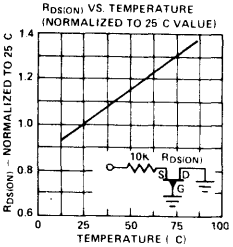
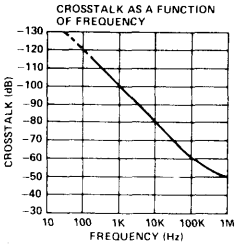
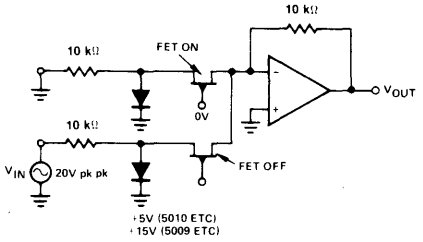




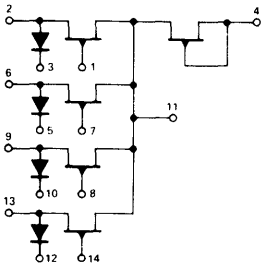
CROSSTALK MEASUREMENT CIRCUIT



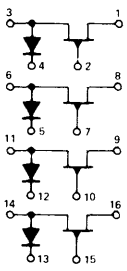
DEVICE SCHEMATICS AND PIN CONNECTIONS

FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

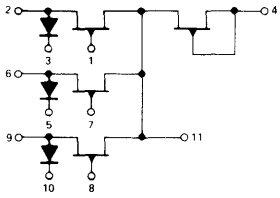


IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

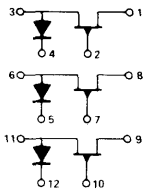


THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

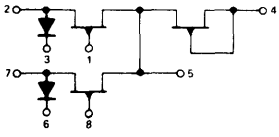


IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

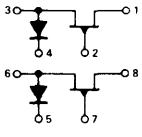


TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

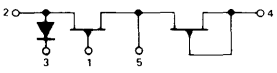


IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

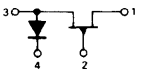


SINGLE CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



THEORY OF OPERATION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 1) the gain is given by

$$\text{GAIN} = \frac{10k\Omega + r_{DS(ON)}\ (\text{compensator})}{10k\Omega + r_{DS}\ (\text{switch})}$$

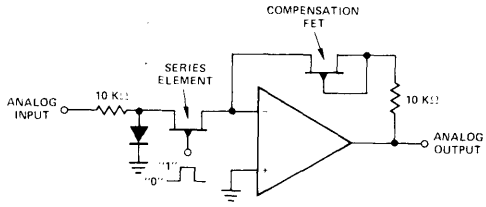


Figure 1. Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

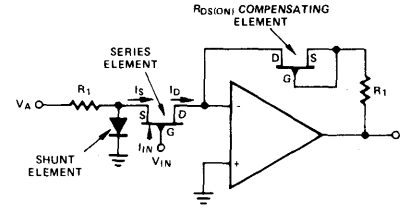


Figure 2.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by T²L open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

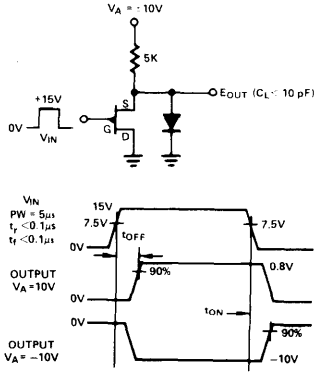


Figure 3. High Level Logic

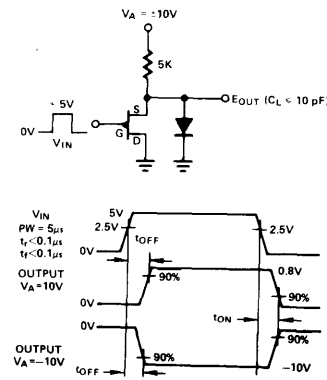


Figure 4. Standard DTL, TTL, RTL

LOGIC INTERFACE CIRCUITS

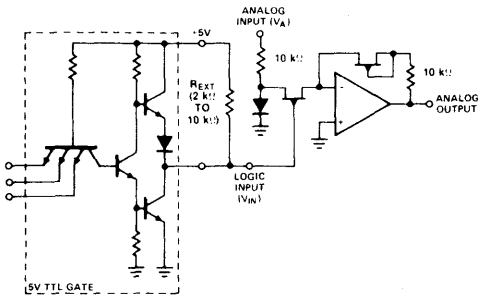


Figure 5. Interfacing with +5V Logic

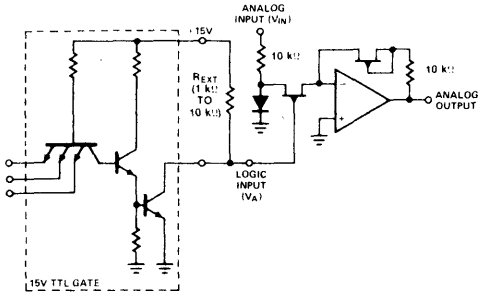
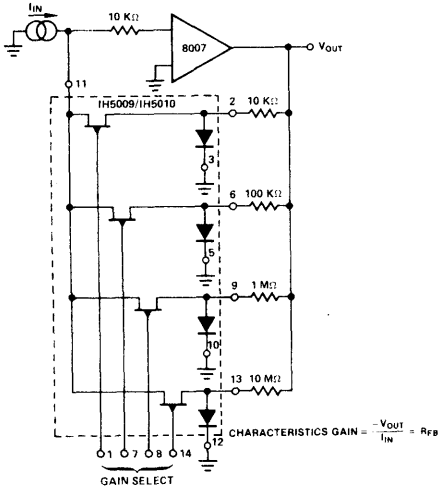
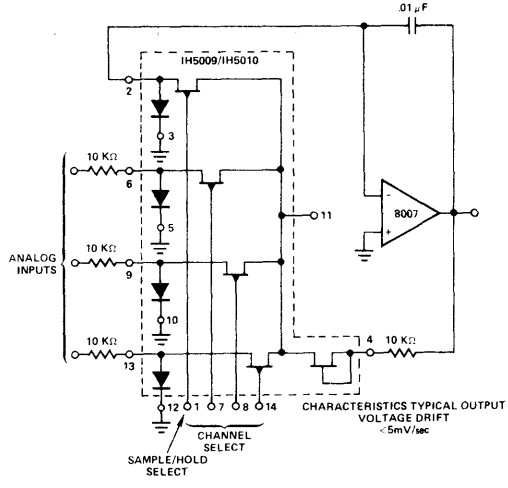


Figure 6. Interfacing with +15V Open Collector Logic

3

APPLICATIONS (Note)





NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches". See also September '79 issue of Product Engineering "Analog Switching" by Paresh Maniar.

IH5025 — IH5038
Positive Signal Analog Switches

FEATURES

- **Switches up to +20V into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)**
- **Driven from TTL Open Collector Logic**
- **$I_{D(OFF)} < 50pA$**
- **$r_{DS(ON)} < 150\Omega$**
- **$r_{DS(ON)}$ Match $< 50\Omega$ Channel to Channel**
- **Switching Speeds < 100ns**

GENERAL DESCRIPTION

The IH5025 series of analog switches was designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

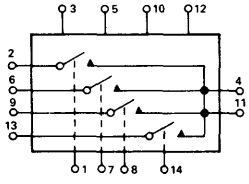
Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

3

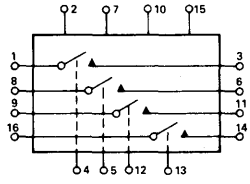
The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 11) or by capacitor isolation (Figure 10). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

PIN CONNECTIONS

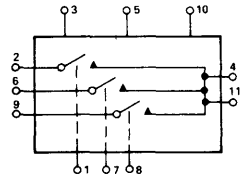
IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



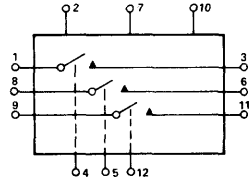
IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



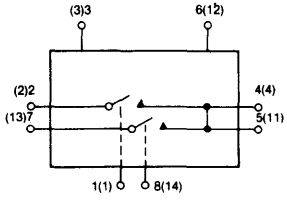
IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



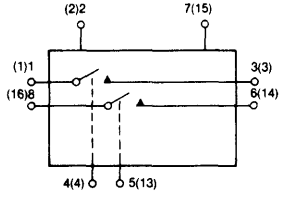
IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



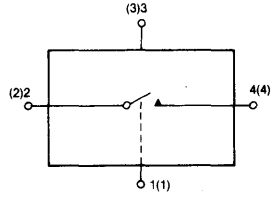
IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



NUMBERS IN PARENTHESES INDICATE CERAMIC PACKAGE PIN-OUT

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 25V
Negative Analog Signal Voltage ..... −0.5VDC
Drain Current 25mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C

Operating Temperature
5025C Series ..... 0°C to +70°C
5025M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

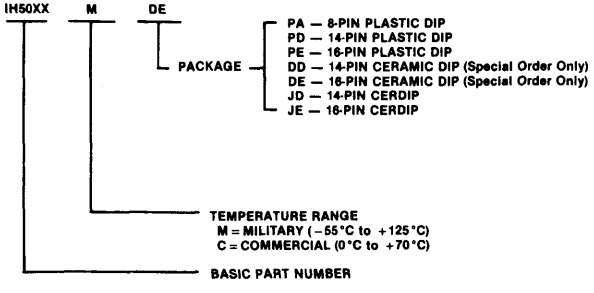
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	TEST CONDITIONS	SPECIFICATION LIMIT				UNITS MIN/MAX
				−55°C (M) 0°C (C)	25°C		+125°C (M) +70°C (C)	
					TYP.	MIN/MAX		
$I_{IN(ON)}$	Input Current-ON	All	V_{IN} = 0V		0.30	1.0	100 (M) 25 (C)	nA (max)
$I_{IN(OFF)}$	Input Current-OFF	All	V_{IN} = 15V		0.20	1.0	50 (M) 10 (C)	nA (max)
$V_{IN(ON)}$	Channel Control Voltage-ON	All	See Figure 1	1.5		1.5	1.5	V (max)
$V_{IN(OFF)}$	Channel Control Voltage-OFF	All	See Figure 1	14.0		14.0	14.0	V (min)
$I_{D(OFF)}$	Leakage Current-OFF	All	V_{IN} = 15V		0.06	0.5	100 (M) 10 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Odd Nos.	V_{IN} = 0V		1.00	10.0	5000 (M) 250 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Even Nos.	V_{IN} = 0V		0.10	1.0	500 (M) 25 (C)	nA (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 0.5V, I_D = 1mA		60.00	100.0	250 (M) 150 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 0.5V, I_D = 1mA		90.00	150.0	385 (M) 240 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 1.0V, I_D = 1mA		85.00	160.0	420 (M) 250 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 1.0V, I_D = 1mA		110.00	200.0	400 (M) 250 (C)	Ω (max)
$t_{(on)}$	Turn-ON Time	All	See Figure 2		0.10	0.2	0.4	μs (max)
$t_{(off)}$	Turn-OFF Time	All	See Figure 2		0.10	0.2	0.4	μs (max)
$Q_{(INJ)}$	Charge Injection	All	See Figure 3		7.00	20.0		mV_{p-p} (max)
$V_{A(OFF)}$	Cross Coupling Rejection	All	See Figure 4		0.10	1.0		mV_{p-p} (max)
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	All	V_{IN} = 0.5V, I_D = 1mA		25.00	50.0	50	Ω (max)

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

ORDERING INFORMATION

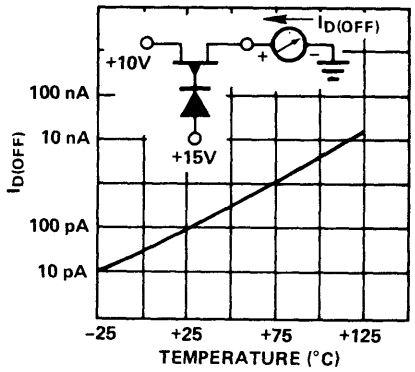


BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5025	4	+15	JD,DD,PD
IH5026	4	+ 5	JD,DD,PD
IH5027	4	+15	JE,DE,PE
IH5028	4	+ 5	JE,DE,PE
IH5029	3	+15	JD,DD,PD
IH5030	3	+ 5	JD,DD,PD
IH5031	3	+15	JE,DE,PE
IH5032	3	+ 5	JE,DE,PE
IH5033	2	+15	JD,DD,PA
IH5034	2	+ 5	JD,DD,PA
IH5035	2	+15	JE,DE,PA
IH5036	2	+ 5	JE,DE,PA
IH5037	1	+15	JD,DD,PA
IH5038	1	+ 5	JD,DD,PA

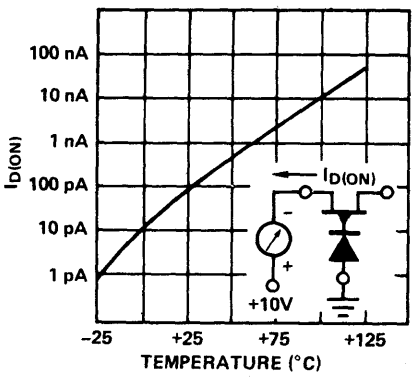
NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)

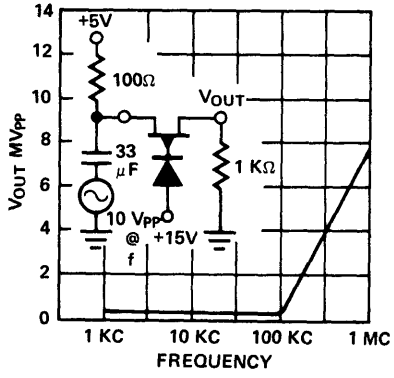
$I_{D(OFF)}$ VS. TEMPERATURE



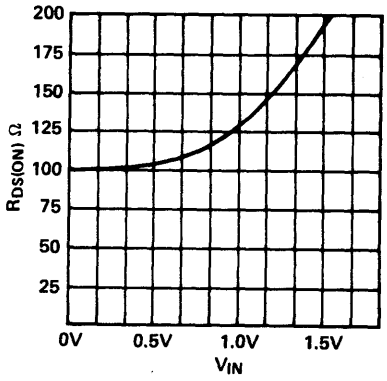
$I_{D(ON)}$ VS. TEMPERATURE



CROSS COUPLING REJECTION VS. FREQUENCY



$R_{DS(ON)}$ VS. V_{IN}



TEST CIRCUITS

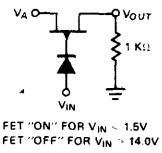


Figure 1

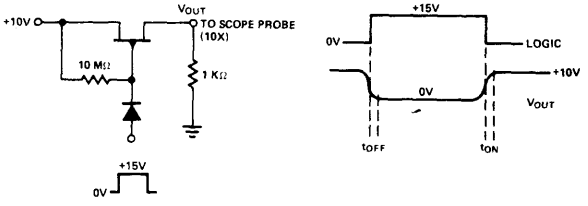


Figure 2

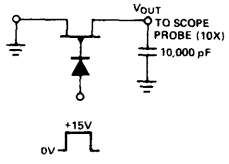


Figure 3

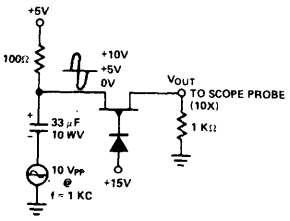
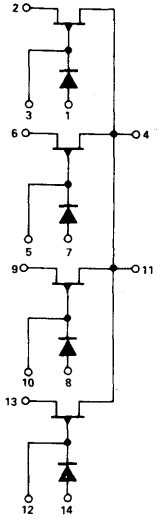


Figure 4

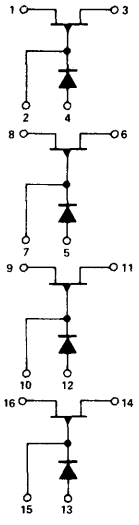
DEVICE SCHEMATICS

FOUR CHANNEL

IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

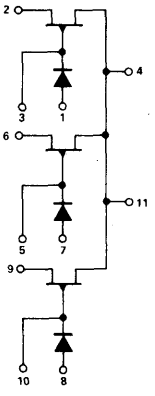


IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

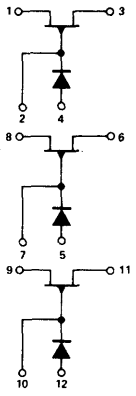


THREE CHANNEL

IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

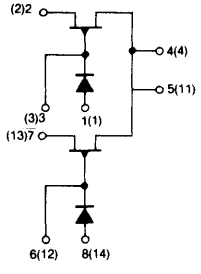


IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

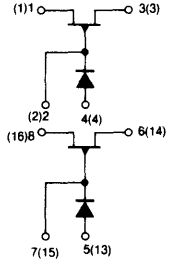


TWO CHANNEL

IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

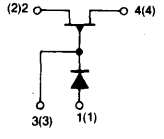


IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



SINGLE CHANNEL

IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



Numbers in parentheses indicate CERAMIC PACKAGE LAYOUT

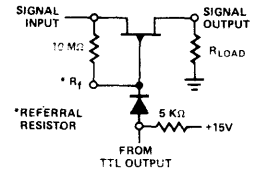
THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that they may be driven by floating outputs. This family is generally used when operating into the non-inverting input of an operational amplifier, while the IH5009 series is used in operations where the output feeds into the inverting (virtual ground) input.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacity vs. voltage relationship for the diode junctions. This C vs. V, when integrated, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched.

The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:



For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

3

LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pull-up resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.

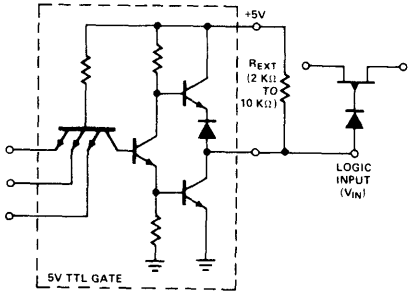


Figure 5. Interfacing with +5V Logic

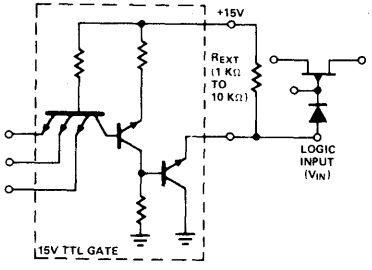


Figure 6. Interfacing with +15V Open Collector Logic

APPLICATIONS

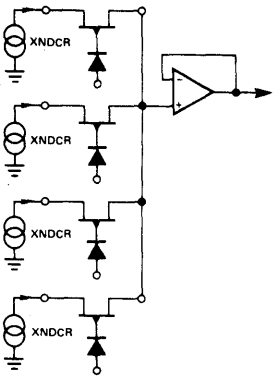


Figure 7. Multiplexer from Positive Output Transducers

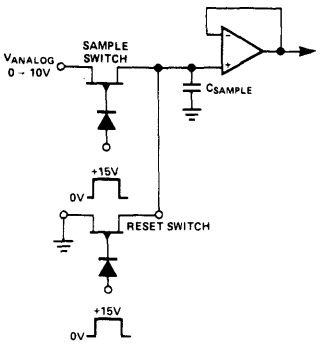


Figure 8. Sample and Hold Switch

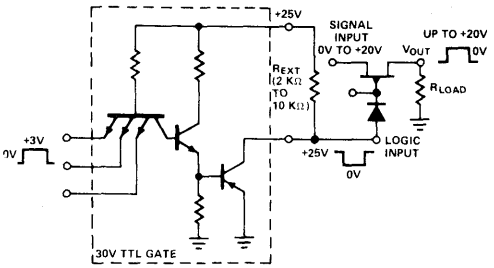
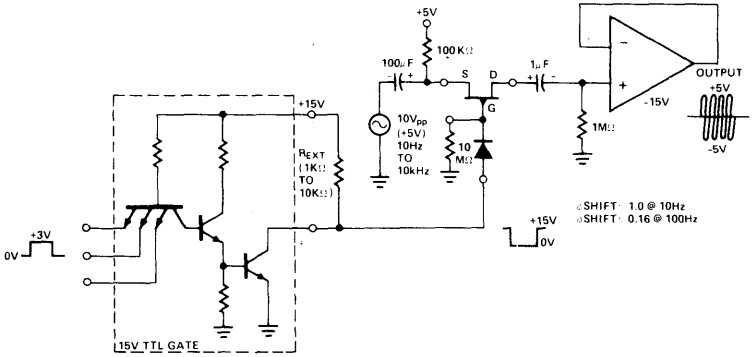
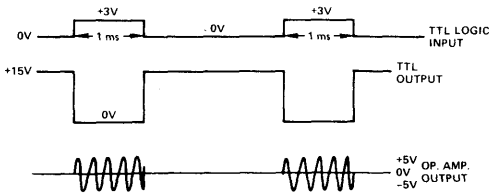


Figure 9. Switching up to +20V Signals with T²L Logic

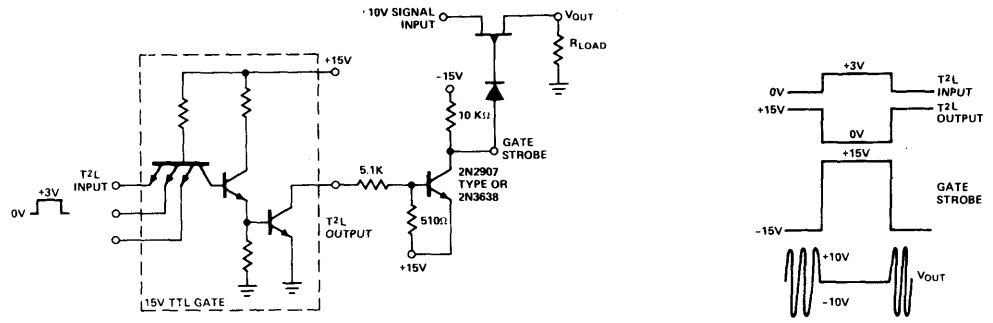




NOTE: TO SWITCH -10 VAC (20Vpp): (1) INCREASE -5V SUPPLY TO +10V. (2) INCREASE TTL SUPPLY FROM +15V TO +25V.

Figure 10. Switching Bipolar Signals with T²L Logic

APPLICATIONS (Cont.)



ADVANTAGES OVER FIGURE NO. 10 METHOD
A. DC LEVELS OF UP TO ±10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100 KC; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10 Hz TO 10 kHz.
B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES:
A. PNP CKT DRAWS 3 mA, WHEN ON; THUS ADDS 3 mA X 30V = 90 mW POWER DISS.
B. t_{ON} TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100 ns (BEFORE IN FIGURE NO. 10) TO 1 ± 2 µs NOW.

Figure 11. Switching Bipolar Signals with T²L Logic (Alternate Method)

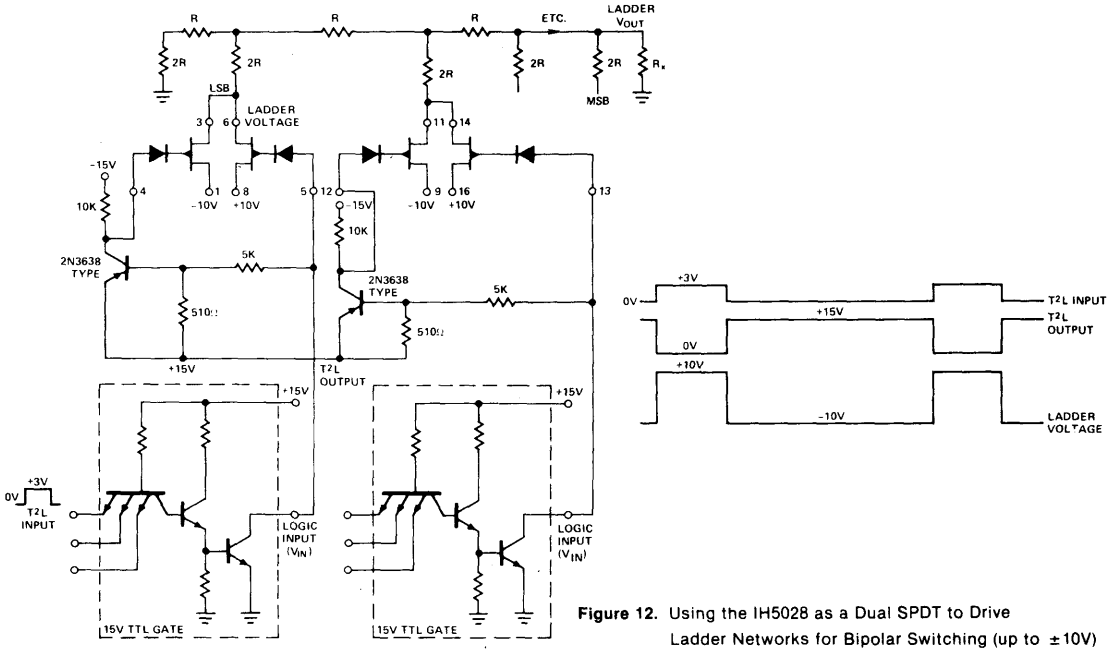
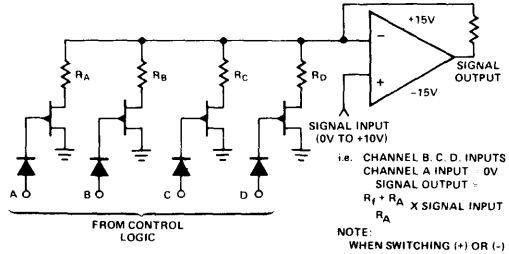


Figure 12. Using the IH5028 as a Dual SPDT to Drive Ladder Networks for Bipolar Switching (up to ±10V)



i.e. CHANNEL B, C, D, INPUTS = +15V;
CHANNEL A INPUT 0V
SIGNAL OUTPUT =
$\frac{R_f + R_A}{R_A}$ X SIGNAL INPUT

NOTE:
WHEN SWITCHING (+) OR (-) SIGNAL INPUTS, A SCHEME SIMILAR TO FIGURES 10 OR 11 SHOULD BE USED.

Figure 13. Gain Control with High Input Impedance

IH5040-IH5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{off} 200 nsec, t_{on} 300 nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low $r_{DS(on)}$ – 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction IH5040 through IH5047

FUNCTIONAL DIAGRAM

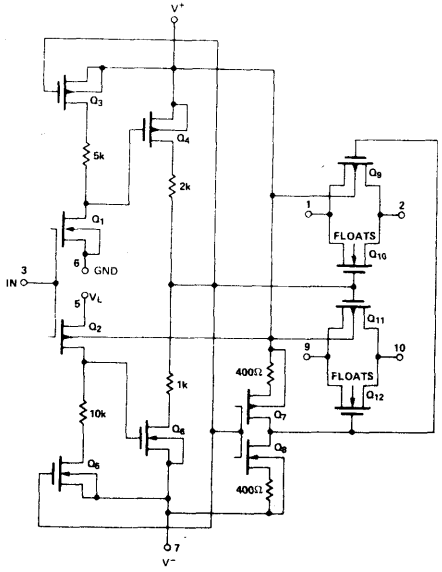


FIGURE 1. TYPICAL DRIVER, GATE – IH5042

ORDERING INFORMATION

IH5040 M JE

Package
DE – 16-Pin Ceramic DIP (Special Order Only)
FD-2 – 14-Pin Flatpak
JE – 16-Pin CERDIP
PE – 16-Pin Plastic DIP
TW – TO-100 Metal Can (IH5041/2, IH5044, IH5048, IH5050 Only)

Temperature Range
M – Military -55°C to +125°C
C – Commercial 0°C to +70°C

Basic Part Number

GENERAL DESCRIPTION

The IH5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{on} time (300 nsec TYP.) so that it exceeds t_{off} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$	PIN/FUNCTIONAL EQUIVALENT (Note 1)
IH5040	SPST	75Ω	
IH5041	Dual SPST	75Ω	
IH5042	SPDT	75Ω	DG 188AA/BA
IH5043	Dual SPDT	75Ω	DG 191AP/BP
IH5044	DPST	75Ω	
IH5045	Dual DPST	75Ω	DG 185AP/BP
IH5046	DPDT	75Ω	
IH5047	4PST	75Ω	
IH5048 Dual	SPST	35Ω	
IH5049 Dual	DPST	35Ω	DG 184AP/BP
IH5050	SPDT	35Ω	DG 187AA/BA
IH5051 Dual	SPDT	35Ω	DG 190AP/BP

NOTE 1. See Switching State diagrams for applicable package equivalency.

Pin and functional equivalent monolithic versions of the DG181, DG182, DG187 and DG188 are available. See data sheet for this and also IH181 to IH191.

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) . . . . . < 30mA

Storage Temperature . . . . . -65°C to +150°C

Operating Temperature . . . . . -55°C to +125°C

Power Dissipation 450mW

(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

Lead Temperature (Soldering, 10 sec) . . . . . 300°C

$V^+ - V^-$	< 33V
$V^+ - V_D$	< 30V
$V_D - V^-$	< 30V
$V_D - V_S$	< ±22V
$V_L - V^-$	< 33V
$V_L - V_{IN}$	< 30V
V_L-GND	< 20V
V_{IN}-GND	< 20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15 V, V^- = -15 V, V_L = +5 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain–Source On Resistance	75(35)	75(35)	150(60)	80(45)	80(45)	130(45)	Ω	(IH5048 Thru IH5051) I_S = 10 mA V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (15) (typ)			30(15) (typ)		Ω	(IH5048 thru IH5051)
V_{ANALOG}	Min. Analog Signal Handling Capability		±11(±10)			±10(±10)		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} = -10 V to +10 V (IH5048 thru IH5051
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10(10)	10(10)	100(200)	nA	V_D = V_S = -10 V to + 10 V (IH5048 thru IH5051)
t_{on}	Switch "ON" Time		500(250)			500(300)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A
t_{off}	Switch "OFF" Time		250(150)			250(150)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A (IH5048 thru IH5051)
$Q_{(INJ.)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (IH5048 thru IH5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L = 5 pF See Fig. C, (Note 1)
I^+_Q	+ Power Supply Quiescent Current	1	1	10	10	10	100	µA	
I^-_Q	– Power Supply Quiescent Current	1	1	10	10	10	100	µA	V^+ = +15 V, V^- = -15 V, V_L = +5 V
I^-_{LQ}	+5 V Supply Quiescent Current	1	1	10	10	10	100	µA	V_L = +5 V
I_{GND}	Gnd Supply Quiescent Current	1	1	10	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off, Any Other Channel Switches as per Fig. E (Note 1)

Note 1: Not tested in production.

TEST CIRCUITS

FIG. A

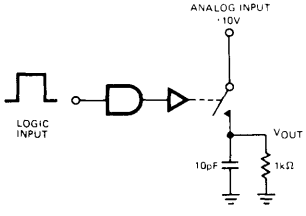


FIG. B

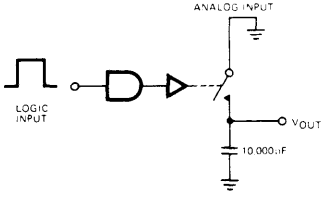
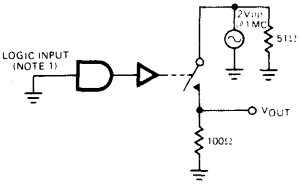
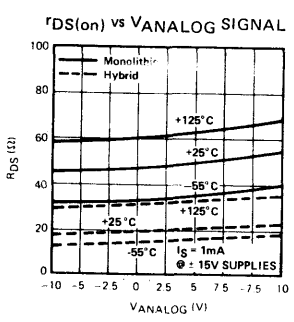


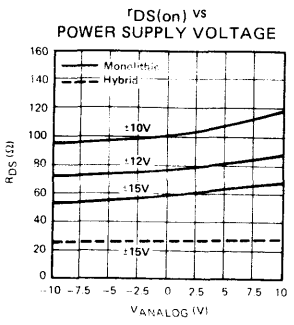
FIG. C



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)





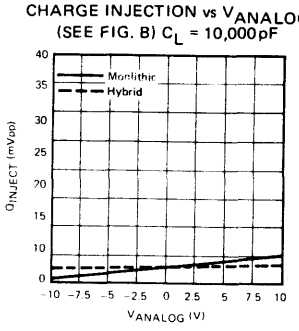
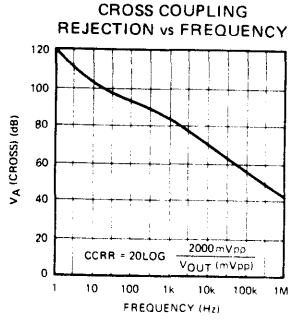


FIGURE D



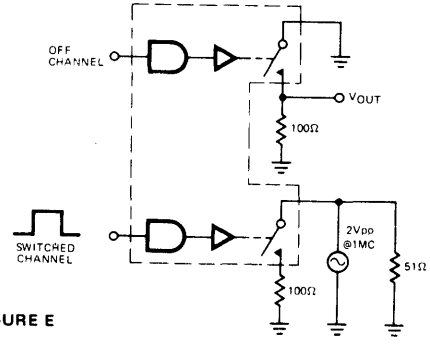
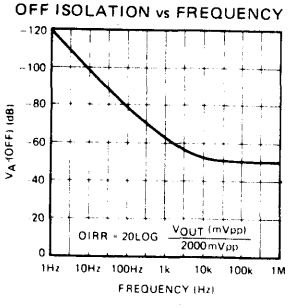


FIGURE E



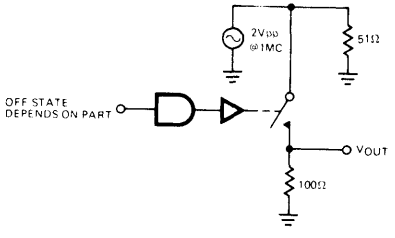
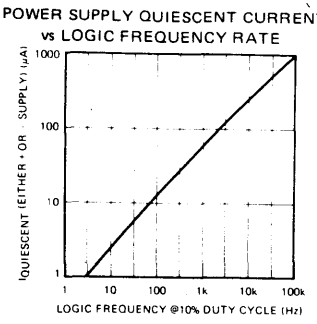


FIGURE F



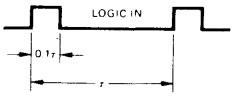
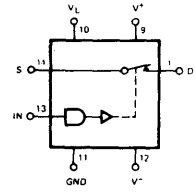
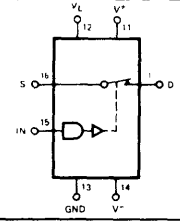
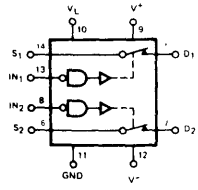
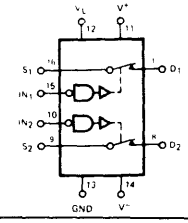
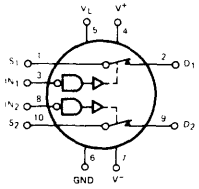
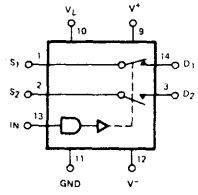
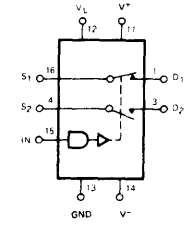
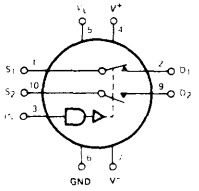
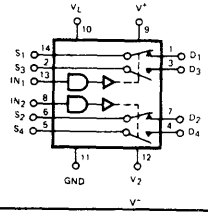
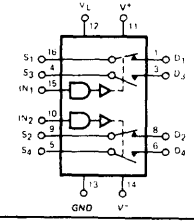
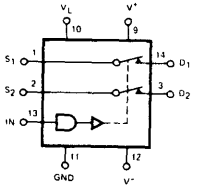
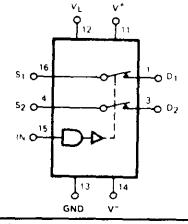
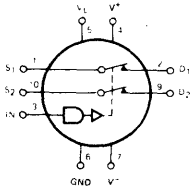
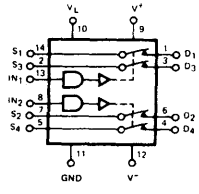
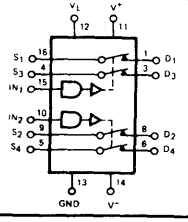


FIGURE G

SWITCHING STATE DIAGRAMS

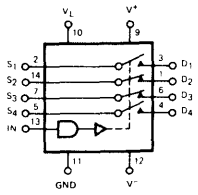
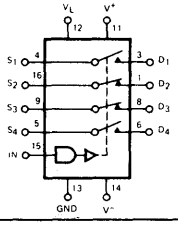
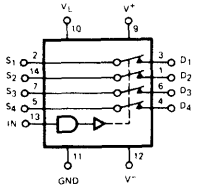
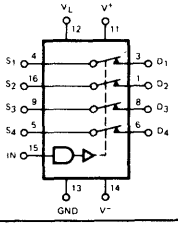
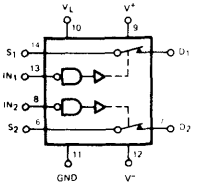
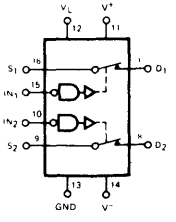
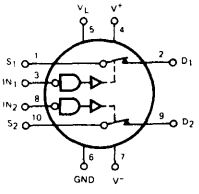
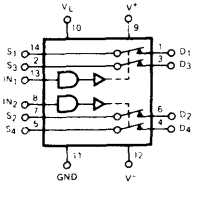
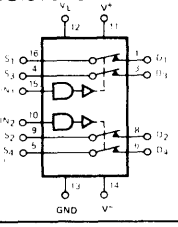
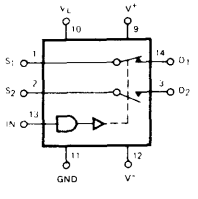
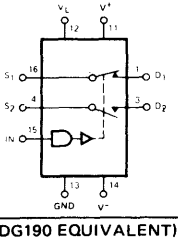
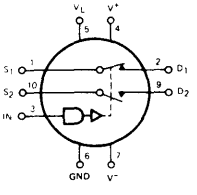
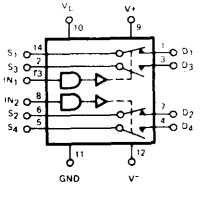
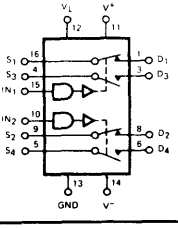
SWITCH STATES ARE FOR LOGIC "1" INPUT

	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE, PE)	(OUTLINE DWG TO-100)
SPST **IH5040 ($r_{DS(on)}$ < 75Ω)**			
DUAL SPST **IH5041 ($r_{DS(on)}$ < 75Ω)**			
SPDT **IH5042 ($r_{DS(on)}$ < 75Ω)**			(DG188 EQUIVALENT) 
DUAL SPDT **IH5043 ($r_{DS(on)}$ < 75Ω)**		(DG191 EQUIVALENT) 	
DPST **IH5044 ($r_{DS(on)}$ < 75Ω)**			
DUAL DPST **IH5045 ($r_{DS(on)}$ < 75Ω)**		(DG185 EQUIVALENT) 	

3

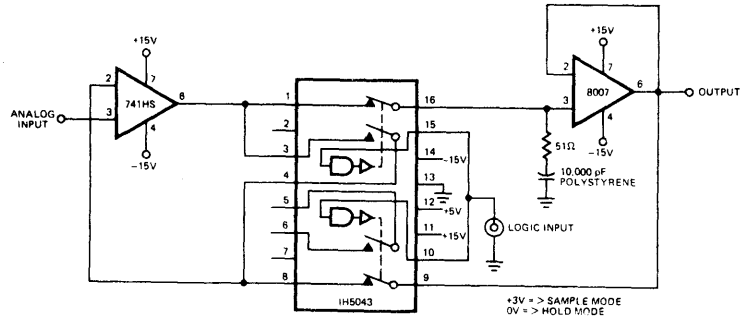
SWITCHING STATE DIAGRAMS (Cont.)

SWITCH STATES ARE FOR LOGIC "1" INPUT

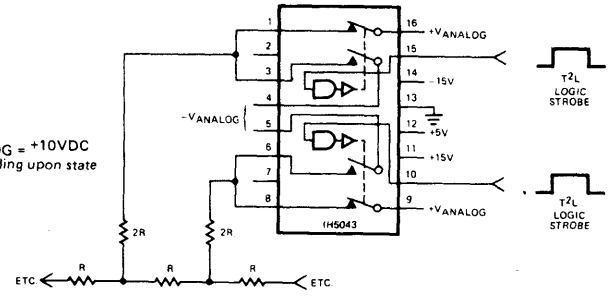
	FLAT PACKAGE (FD-2)	DIP (DE) PACKAGE	TO-100
DPDT **IH5046 (r_{DS} (ON) <75Ω)**			
4PST **IH5047 (r_{DS} (ON) <75Ω)**			
DUAL SPST **IH5048 (r_{DS} (ON) <35Ω)**			
DUAL DPST **IH5049 (r_{DS} (ON) <35Ω)**	(DG184 EQUIVALENT) 		
SPDT **IH5050 (r_{DS} (ON) <35Ω)**			(DG187 EQUIVALENT) 
DUAL SPDT **IH5051 (r_{DS} (ON) <35Ω)**	(DG190 EQUIVALENT) 		

APPLICATIONS

IMPROVED SAMPLE & HOLD
USING IH5043

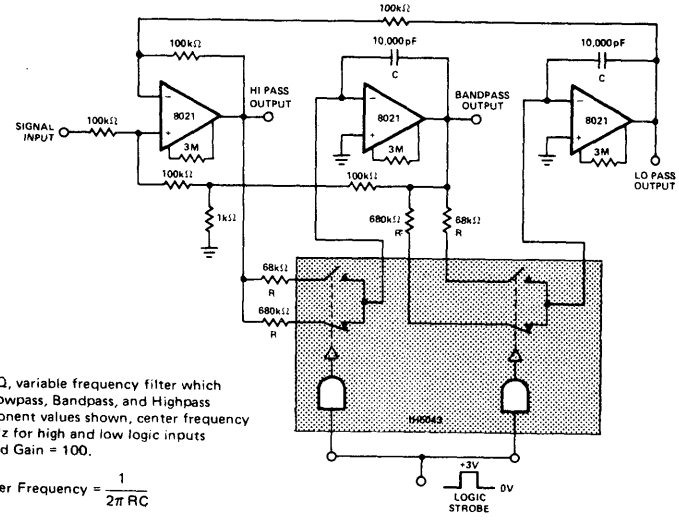


USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

DIGITALLY TUNED
LOW POWER ACTIVE FILTER



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

THEORY OF OPERATION

A. FLOATING BODY CMOS STRUCTURE

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. J). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. K). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

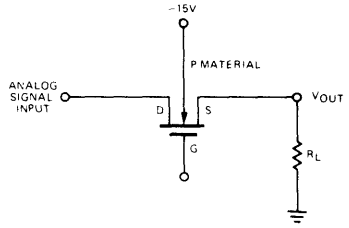


FIGURE J

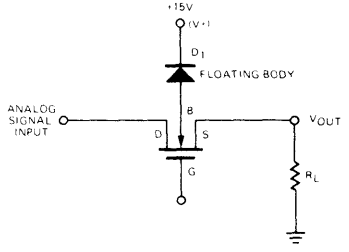


FIGURE K

B. OVERVOLTAGE PROTECTION

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i. e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. J if the analog signal input is more negative than -15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of -25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. L. Fig. L describes an output stage showing the paralleling of an N and P channel to linearize the $r_{DS(ON)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides over voltage protection to a maximum of ±25V.

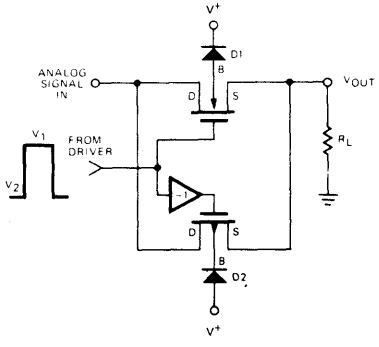
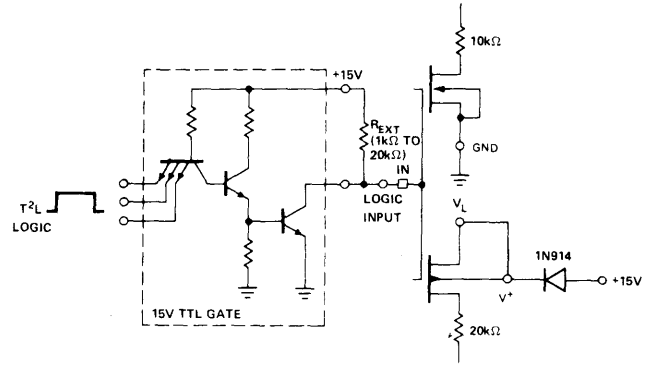


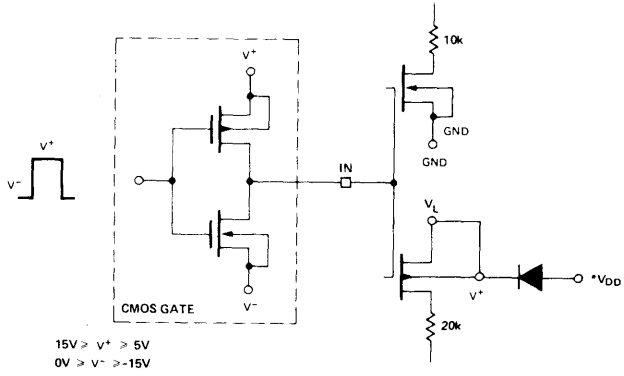
FIGURE L

FOR INTERFACING WITH T²L OPEN COLLECTOR LOGIC.



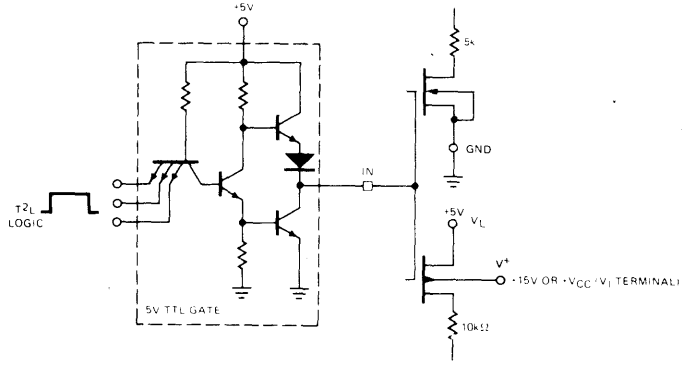
TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.



15V ≥ V^+ ≥ 5V
0V ≥ V^- ≥ -15V

LOGIC INTERFACING



IH5052/IH5053
CMOS Analog Gates

FEATURES

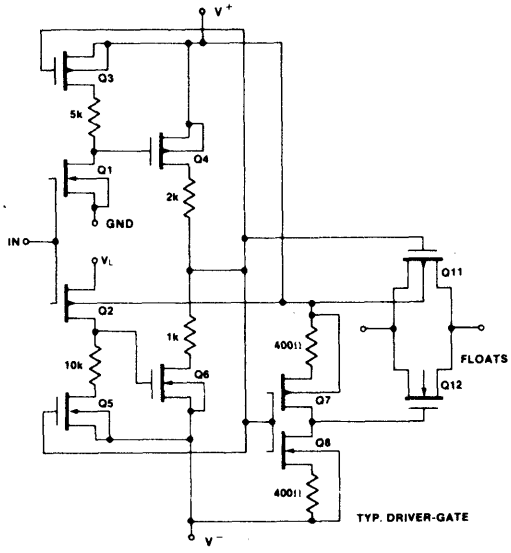
- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ± 25V**
- **Break-Before-Make Switching t_{off} 100nsec, t_{on} 250nsec Typical**
- **T²L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **IH5052 4 Normally Closed Switches**
- **IH5053 4 Normally Open Switches**

3

GENERAL DESCRIPTION

The IH5052/3 solid state analog gates are designed using an improved, high voltage CMOS technology. This provides ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ± 25 volts without damage to the device, and the destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem. Key performance advantages are TTL compatible and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH5052/3 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400nsec TYP.) such that it exceeds t_{OFF} time (200nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON and eliminates the need for external logic required to avoid channel shorting during switching. The IH5052 is designed to have switch closure with Logic "0" (0.8V or less) and the IH5053 is designed to close switches with a Logical "1" (2.4V or more).

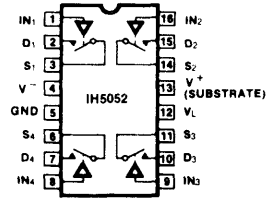
FUNCTIONAL DIAGRAM



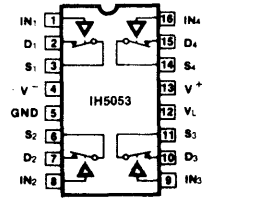
PIN CONFIGURATIONS

OUTLINE DWGS
DE, JE

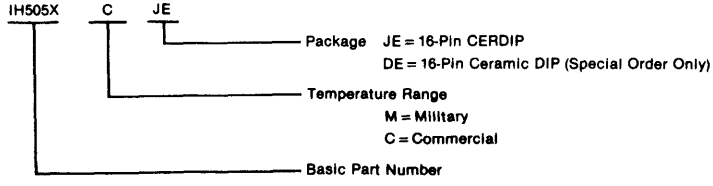
DUAL-IN-LINE PACKAGE



SWITCH STATES ARE
FOR LOGIC "1" INPUT



ORDERING INFORMATION



MAXIMUM RATINGS

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... <33V
$V_L - V_{IN}$ ..... <30V
V_L-GND ..... <20V
V_{IN}-GND ..... <20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, GND = 0V)

PER CHANNEL		MIN./MAX. LIMITS							TEST CONDITIONS
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	80	80	100	Ω	I_S = 10mA, V_{analog} = 10V to +10V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±11			±10		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	V_{ANALOG} = −10V to +10V
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2	2	200	10	10	100	nA	$V_D = V_S$ = −10V to +10V
t_{ON}	Switch "ON" Time		500			500		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
t_{OFF}	Switch "OFF" Time		250			250		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, $C_L \leq$ 5pF See Fig. C (Note 1)
I^+	+ Power Supply Quiescent Curent	10	10	100	10	10	100	µA	
I^-	− Power Supply Quiescent Current	10	10	100	10	10	100	µA	V^+ = +15 V, V^- = −15 V, V_L = +5 V with GND
I_{VL}	+5V Supply Quiescent Current	10	10	100	10	10	100	µA	
I_{GND}	Gnd Supply Quiescent Current	10	10	100	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E (Note 1)

Note 1: Not tested in production.

TEST CIRCUITS

FIG. A

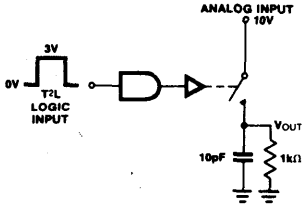


FIG. B

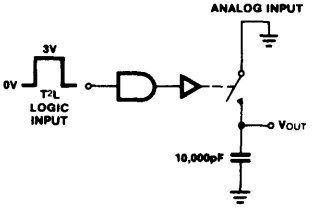
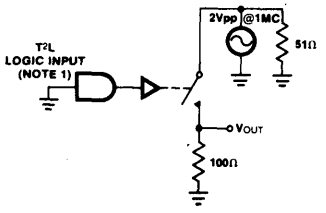
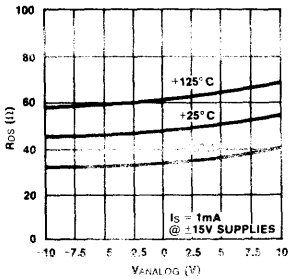


FIG. C

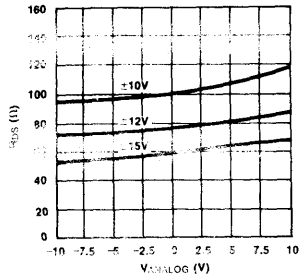


TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

$r_{DS}(ON)$ vs V_{ANALOG} SIGNAL



$r_{DS}(ON)$ vs POWER SUPPLY VOLTAGE



CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF

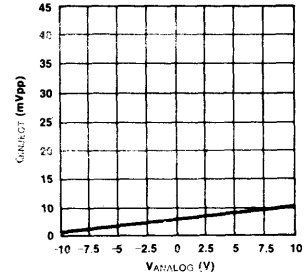
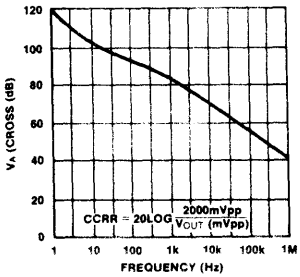


FIGURE D

3

CROSS COUPLING REJECTION vs FREQUENCY



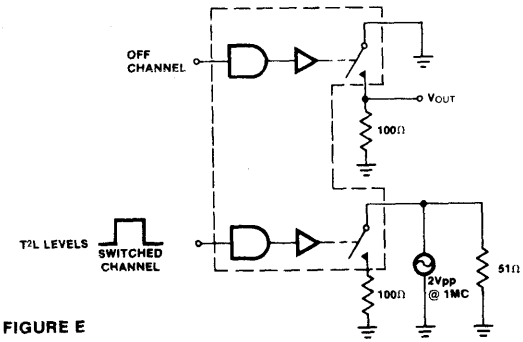
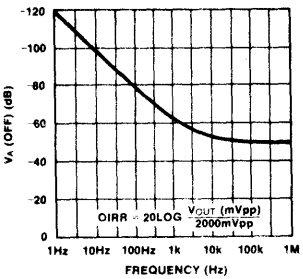


FIGURE E

OFF ISOLATION vs FREQUENCY



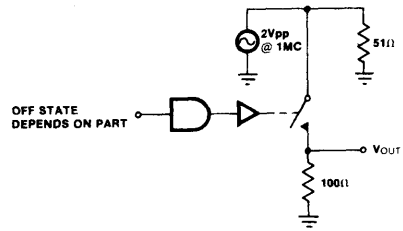
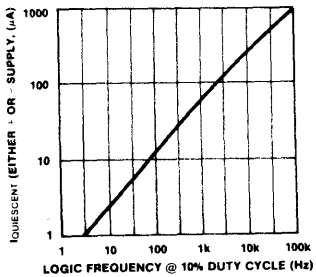


FIGURE F

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



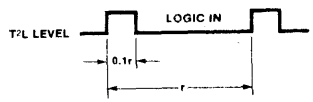


FIGURE G

THEORY OF OPERATION

A. Floating Body CMOS Structure

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. H). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. I). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

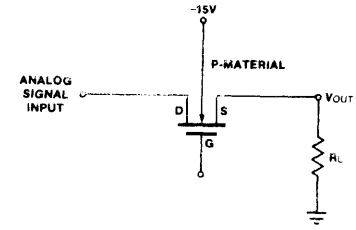


FIGURE H

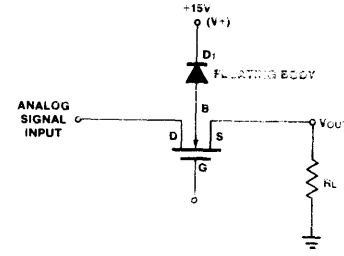


FIGURE I

B. Overvoltage Protection

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i.e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. H if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of −25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. J. Fig. J describes an output stage showing the paralleling of an N and P-channel to linearize the $r_{DS(on)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides overvoltage protection to a maximum of ±25V.

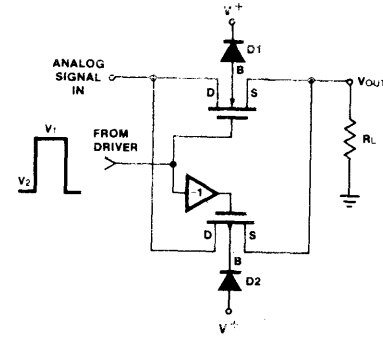
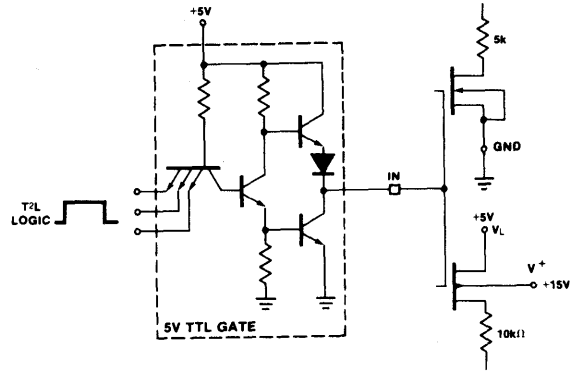
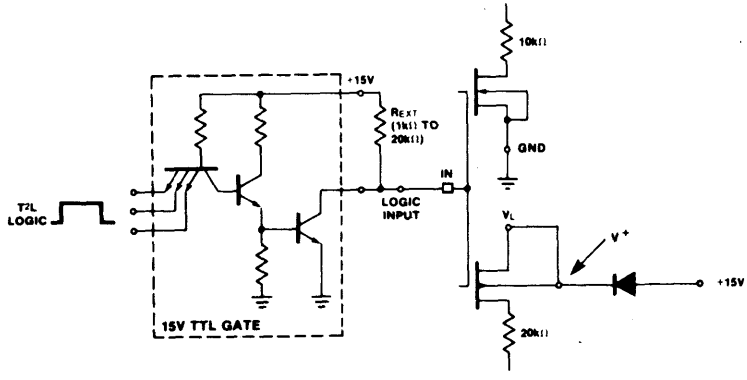


FIGURE J

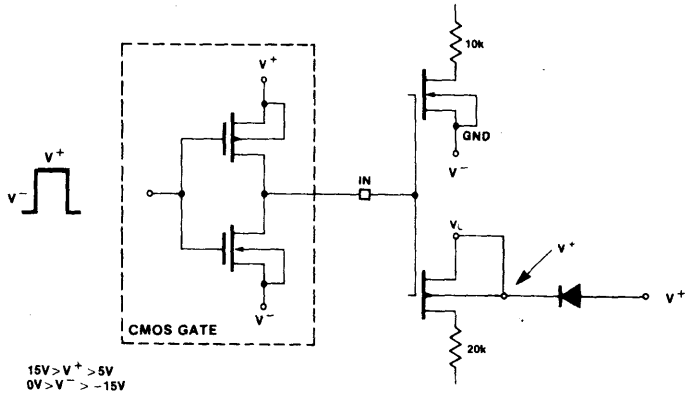


FOR INTERFACING WITH T²L OPEN COLLECTOR LOGIC.



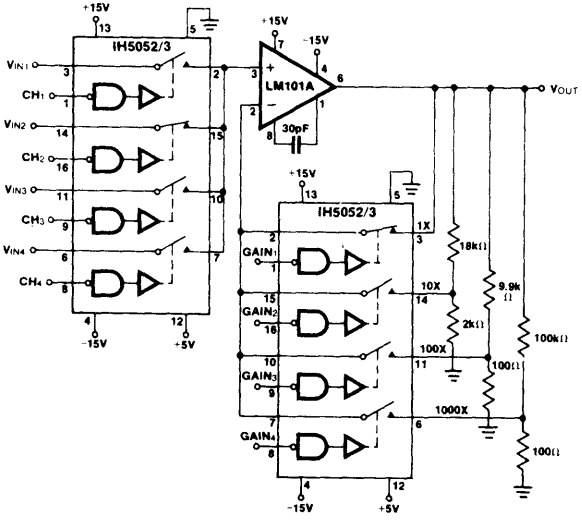
TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.



APPLICATIONS

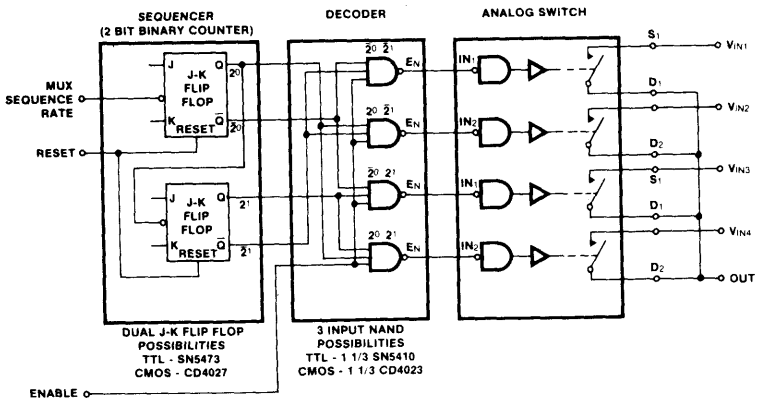
PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS



ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

APPLICATIONS (Continued)

4-CHANNEL SEQUENCING MUX

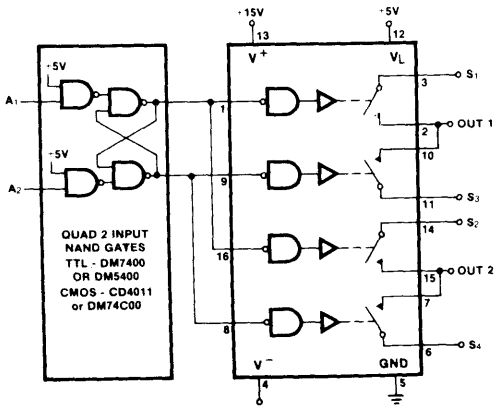


Truth Table (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT		SWITCH STATES (– DENOTES OFF)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

A Latching DPDT

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



Truth Table (IH5052)

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

IH5108

8-Channel Fault Protected CMOS Analog Multiplexer

FEATURES

- **Ultra low leakage—$I_{D(off)} \leq 100pA$**
- **Power supply quiescent current less than 1mA**
- **± 13V analog signal range**
- **No SCR latchup**
- **Break-before-make switching**
- **Pin compatible with DG508, HI508 and AD7508**
- **All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ± 25V**
- **Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput always < ± 14V (± 15V supplies)**
- **TTL and CMOS compatible binary Address and ENable inputs**

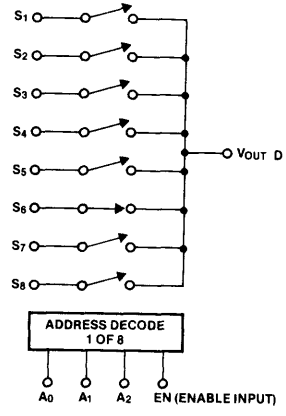
GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG508 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ± 25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any one channel or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

3

FUNCTIONAL DIAGRAM



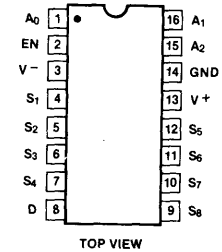
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN HI
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	− 55°C to + 125°C	16 pin CERDIP
IH5108IJE	− 20°C to + 85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

IH5108

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) 20mA

Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipaton (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

3

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	I/C SUFFIX −20°C/ 0°C	I/C SUFFIX 25°C	I/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(on)}$		S to D	8	700	900	900	1200	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
				8	500	900	900	1200	1200	1200	1800		$V_D = -10V$ $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$				5		10			10		%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$		S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
				8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$		D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	
				1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$		D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF		S	8	1		100	1000	50	50	5000	nA	$V^+ = V^- = 0V$, $V_S = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$ or 5V	
	$I_{S(off)}$ with Overvoltage (Note 1)		S	8	1		2000	5000		5000	5000		$V_S = \pm 25V$, $V_D = \mp 10V$	Sequence each switch
IN	$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$		A_0, A_1, EN	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
				4	.01		10	30		10	30		$V_A = 15V$ or 0V	
DYNAMIC	$t_{transition}$		D		0.3		1					μs	See Figure 1	
	t_{open}		D		0.2								See Figure 2	
	$t_{on(EN)}$		D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$		D		0.4		1							
	t_{on}-t_{off} Break-Before-Make Delay Settling Time		D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 KHz	
	$C_{S(off)}$		S		5							pF	$V_S = 0$	$V_{EN} = 0V$, f = 140 KHz to 1 MHz
	$C_{D(off)}$		D		25								$V_D = 0$	
	$C_{DS(off)}$		D to S		1								$V_S = 0$, $V_D = 0$	
SUP	Supply Current	+	V^+	1	500	900	750	600		1000		μA	All V_A, $V_{EN} = 0$ or 5V	
		−	V^-	1	500	900	750	600		1000				

Note 1. Readings taken 400ms after the overvoltage occurs.

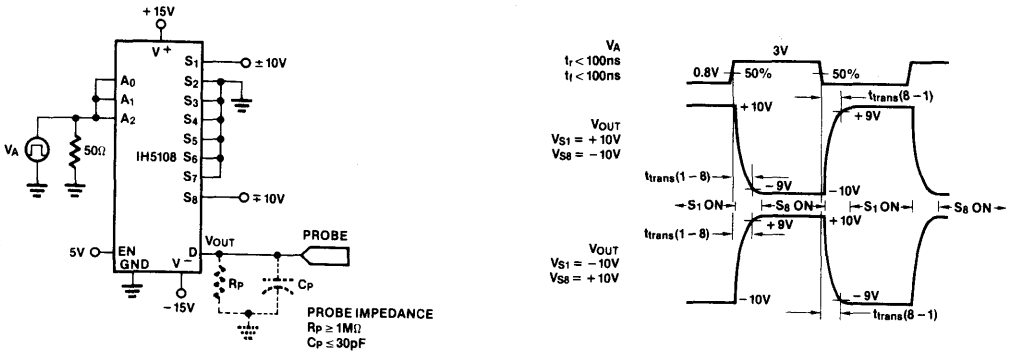


Figure 1. $t_{transition}$ Switching Test

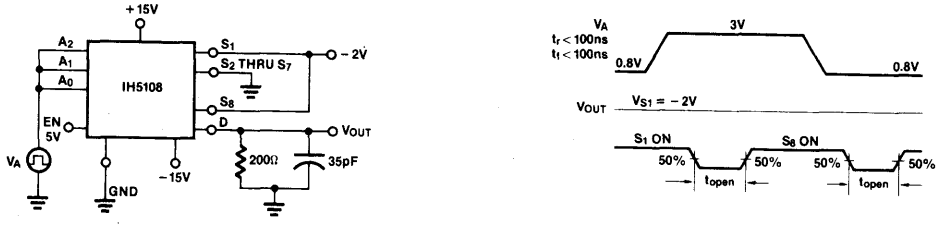


Figure 2. t_{open} (Break-Before-Make) Switching Test

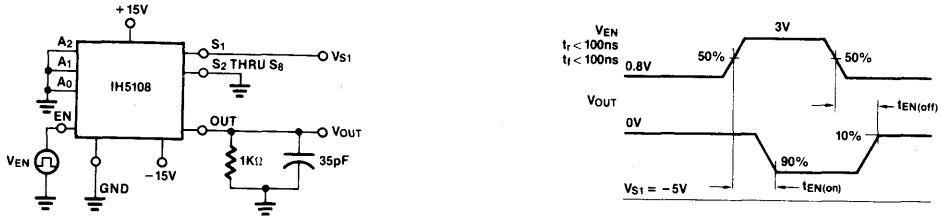


Figure 3. t_{on} and t_{off} Switching Test

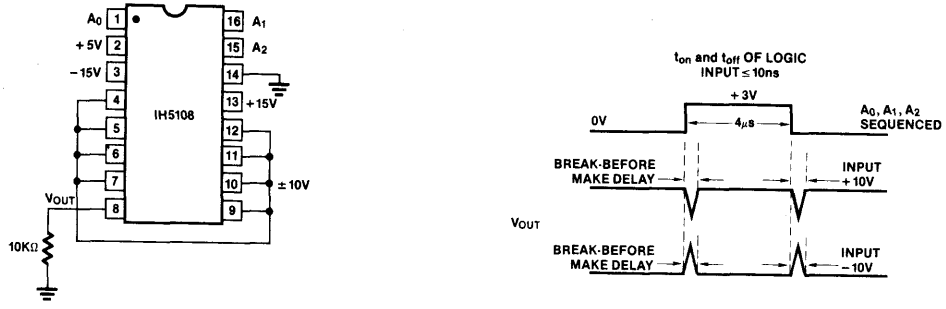


Figure 4. Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5108, like all Intersil's multiplexers, contains a set of CMOS switches forming the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special treatment that many multiplexer enable inputs require for proper logic swings. This identical circuit treatment of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important, difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches, and while this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 5) combined with a dielectrically isolated process to obviate these problems.

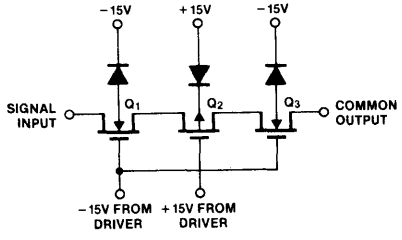


Figure 5. Series Connection of Channel Switches

Within the normal analog signal band, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 6). Thus protection is provided to any input or output channel against overvoltage on any (or several) input or output channels even in the absence of multiplexer supply voltages, and applies up to the breakdown voltage of the respective switches, drawing only leakage currents. Figure 7 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 8).

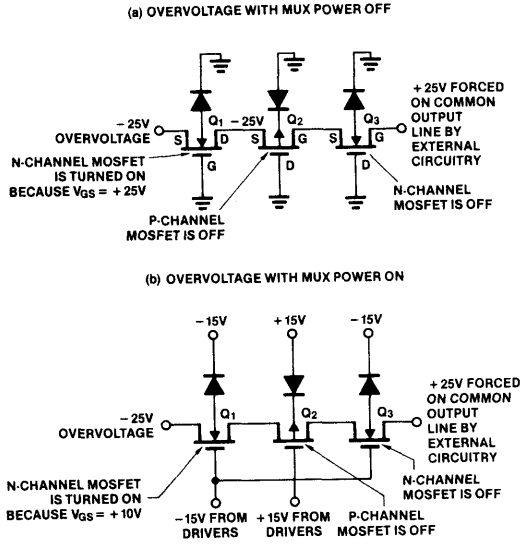


Figure 6. Overvoltage Protection

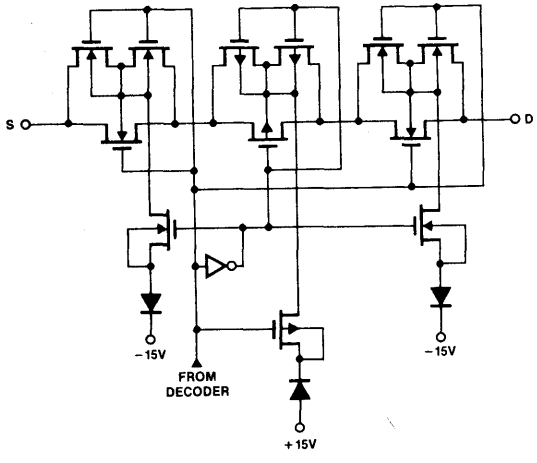


Figure 7. Detailed Channel Switch Schematic

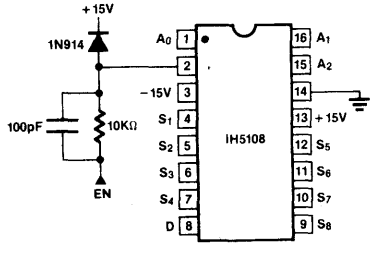


Figure 8. Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the ± 10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ± 13V, however, $r_{DS(on)}$ will increase to about 1.8K. Beyond ± 13V the device approaches an open circuit, and thus ± 12V is about the practical limit, see Figure 9.

Figure 10 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 11 gives the ON resistance variation with temperature.

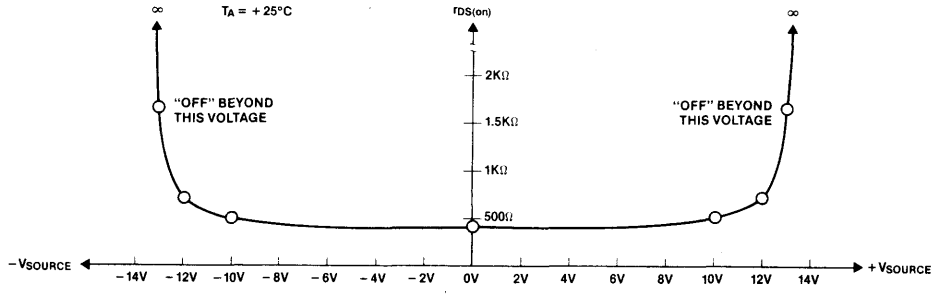


Figure 9. $r_{DS(on)}$ vs Signal Output Voltage @ T_A = + 25 °C

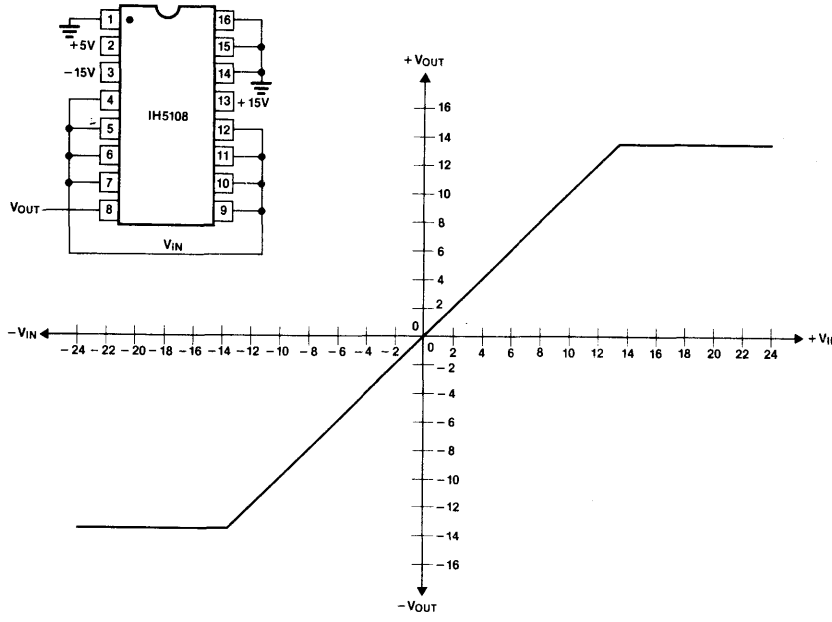


Figure 10. MUX Output Voltage vs Input Voltage
Channel 1 Shown; All Channels Similar

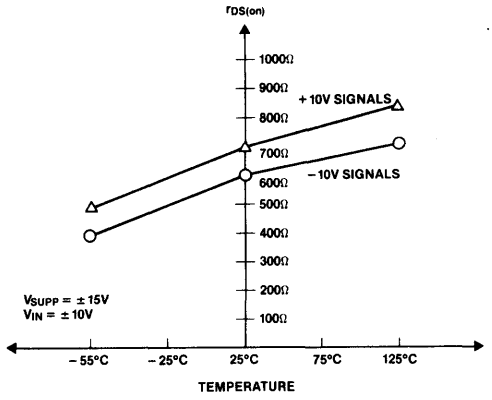


Figure 11. Typical $r_{DS(on)}$ vs Temperature

3

USING THE IH5108 WITH SUPPLIES OTHER THAN ±15V

The IH5108 will operate successfully with supply voltages from ±5V to ±15V; $r_{DS(on)}$ increases as supply voltage decreases, see Figure 12. Leakage currents, however, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels will remain TTL compatible.

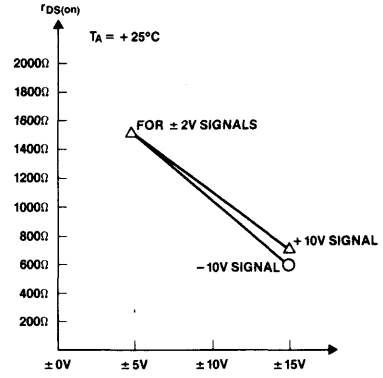
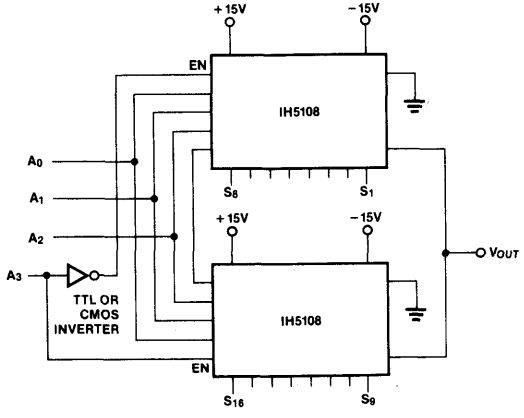


Figure 12. $r_{DS(on)}$ vs Supply Voltages

IH5108 APPLICATIONS INFORMATION

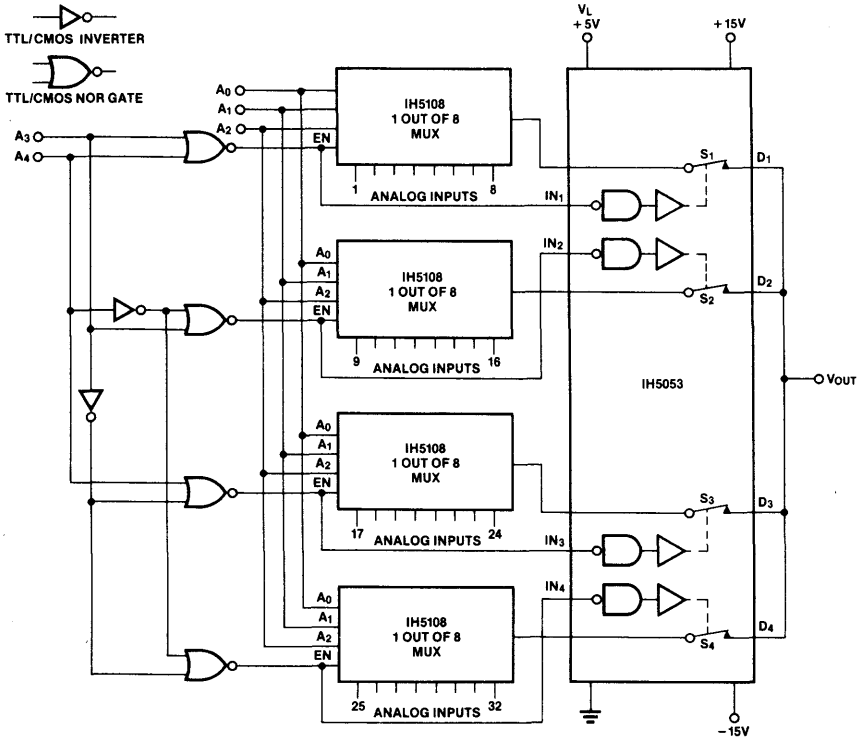


DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 13. 1 of 16 channel multiplexer using two IH5108s. Overvoltage protection is maintained between all channels, as is break-before-make switching.

IH5108 APPLICATIONS INFORMATION (Continued)



DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 14. 1 of 32 multiplexer using 4 IH5108s and an IH5053 as a submultiplexer. Note that the IH5053 is protected against overvoltages by the IH5108s. Submultiplexing reduces output leakage and capacitance.

APPLICATION NOTES

Further information may be found in:

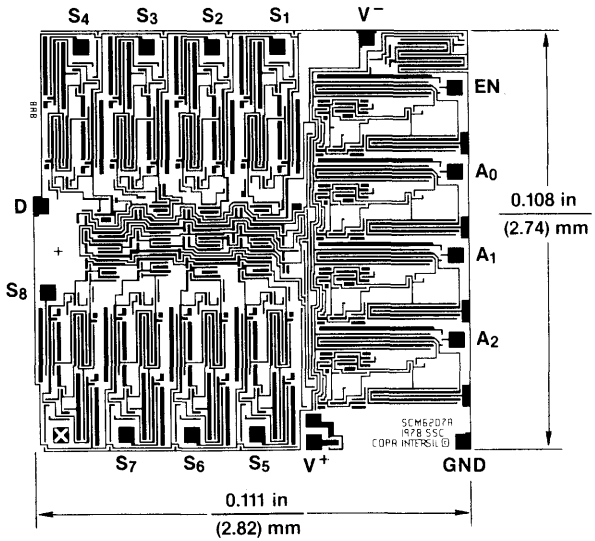
A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

CHIP TOPOGRAPHY



IH5140 Family High Level CMOS Analog Gates

FEATURES

- **Super fast break before make switching t_{on} 80ns typ, t_{off} 50ns typ (SPST switches)**
- **Power supply currents less than 1μA**
- **OFF leakages less than 100pA @ 25°C guaranteed**
- **Non-latching with supply turn-off**
- **Single monolithic CMOS chip**
- **Plug-in replacements for IH5040 family and part of the DG180 family to upgrade speed and leakage**
- **Greater than 1MHz toggle rate**
- **Switches greater than 20Vp-p signals with ±15V supplies**
- **T^2L, CMOS direct compatibility**

GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches now available. These switches can be toggled at a rate of greater than 1 MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches therefore combines the speed of the hybrid FET DG 180 Family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 100pA at 25°C. No quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic gates. It is pin compatible with Intersil's IH5040 Family and part of the DG180/190 Family as shown in the switching state diagrams.

3

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	Dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

Note:
1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

FUNCTIONAL DIAGRAM

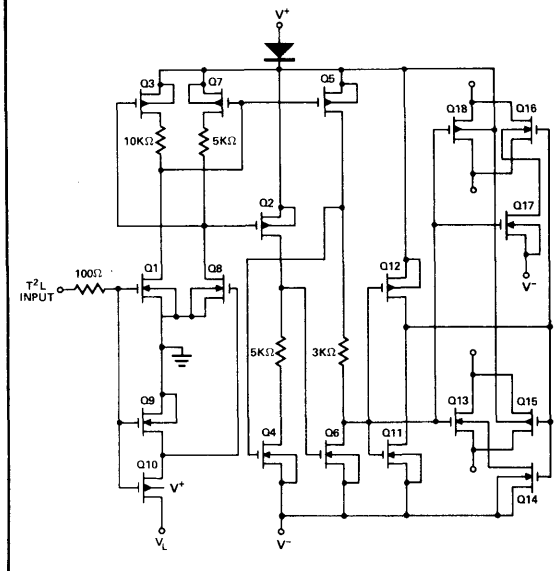


FIGURE 1. Typical Driver/Gate — IH5142

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) ..... < 30 mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Power Dissipation ..... 450 mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering 10 sec.) .. 300°C

$V^+ - V^-$	<33V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	<±22V
$V_L - V^-$	<33V
$V_L - V_{IN}$	<30V
V_L	<20V
V_{IN}	<20V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = -15V, V_L = +5V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
I_{INH}	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4 V Note 1
I_{INL}	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain—Source On Resistance	50	50	75	75	75	100	Ω	I_S = -10 mA V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±11			±10		V	
$I_{D(off)}$+	Switch OFF Leakage	0.1	0.1	20	0.5	0.5	20	nA	V_D = +10 V, V_S = -10 V
$I_{S(off)}$	Current	0.1	0.1	20	0.5	0.5	20		V_D = -10V, V_S = +10 V
$I_{D(on)}$+	Switch On Leakage	0.2	0.2	40	1	1	40	nA	V_D = V_S = -10 V to +10 V
$I_{S(on)}$	Current								
t_{on}	Switch "ON" Time	See switching time specifications and timing diagrams.							
t_{off}	Switch "OFF" Time								
$Q_{(INJ.)}$	Charge Injection		100			150		pC	See Fig. 4, Note 2
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, $C_L \leq$ 5 pF See Fig. 5, Note 2
I^+	+ Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	V^+ = +15 V, V^- = -15 V, V_L = +5 V See Fig. 6
I^-	- Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	
I_L	+5 V Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	
I_{GND}	Gnd Supply Quiescent Current	1.0	1.0	10.0	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches See Fig. 7, Note 2

Note: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.

2. Charge injection, OFF isolation, and Channel to Channel isolation are only sample tested in production.

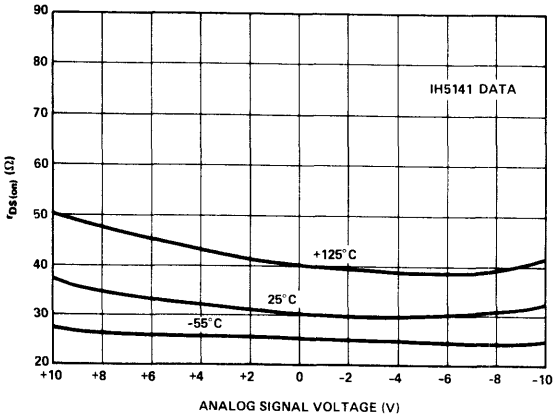


FIGURE 2. $r_{DS(on)}$ vs. Temp., @ ±15V, +5V Supplies.

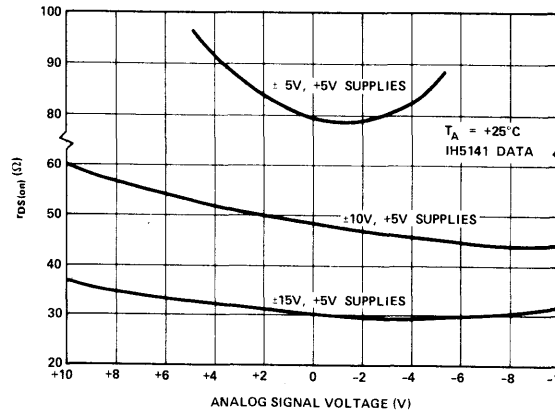


FIGURE 3. $r_{DS(on)}$ vs. Power Supplies.

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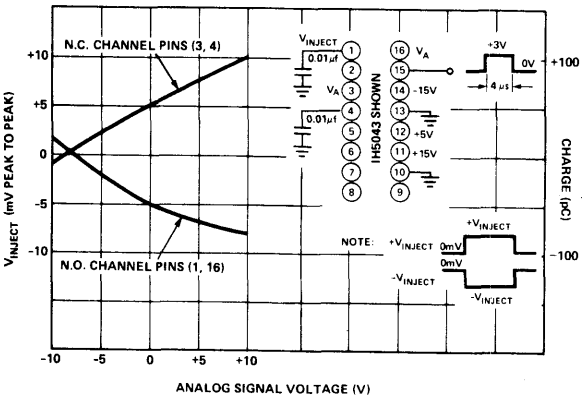


FIGURE 4. Charge Injection vs. Analog Signal.

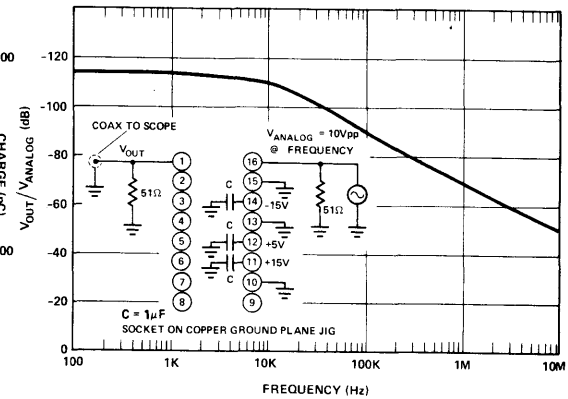


FIGURE 5. "OFF" Isolation vs. Frequency.

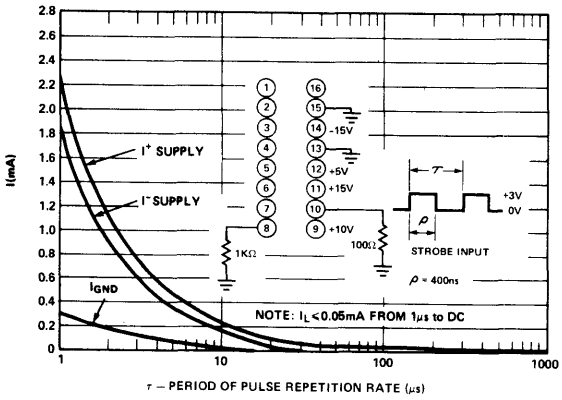


FIGURE 6. Power Supply Currents vs. Logic Strobe Rate.

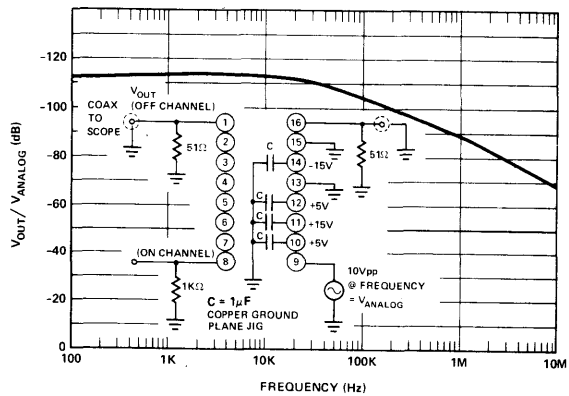


FIGURE 7. Channel to Channel Cross Coupling Rejection vs. Frequency.

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

Part Number	Symbol	Characteristics	MILITARY -55°C	MILITARY +25°C	MILITARY +125°C	COMMERCIAL 0°C	COMMERCIAL +25°C	COMMERCIAL +70°C	Units	Test Conditions
IH5140-5141	t_{on}	Switch "ON" time		100			150		ns	Figure 8
	t_{off}	Switch "OFF" time		75			125			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		150			175		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
IH5142-5143	t_{on}	Switch "ON" time		175			250		ns	Figure 8
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		175			250		ns	Figure 10
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 11
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
IH5144-5145	t_{on}	Switch "ON" time		175			250		ns	Figure 8
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			

3

NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS.

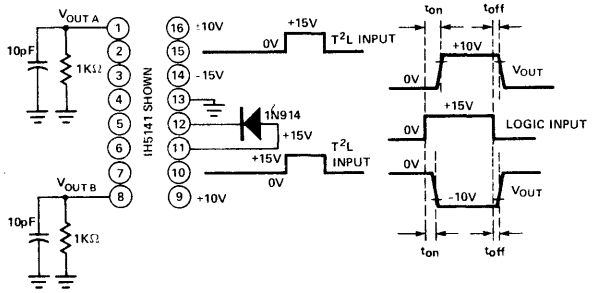


FIGURE 8.

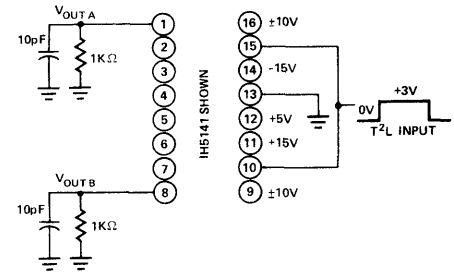


FIGURE 9.

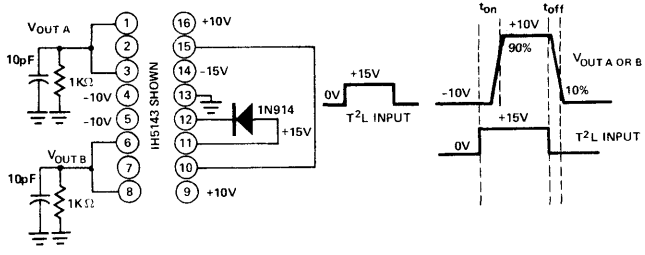


FIGURE 10.

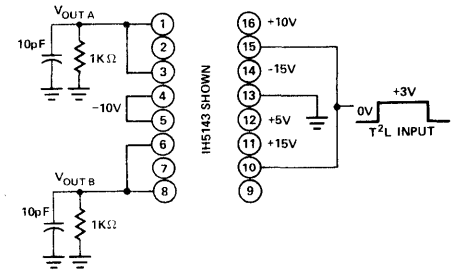
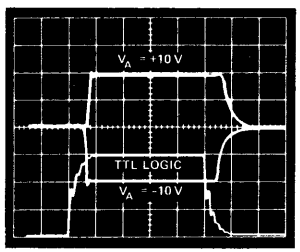


FIGURE 11.

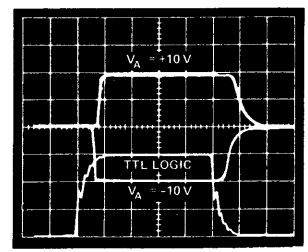
TYPICAL SWITCHING WAVEFORMS

SCALE: VERT. = 5V/DIV.
HORIZ. = 100ns/DIV.

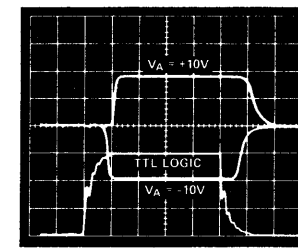
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



-55°C

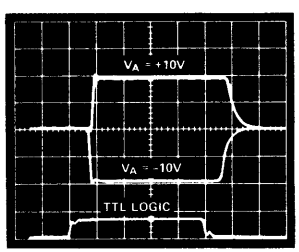


+25°C

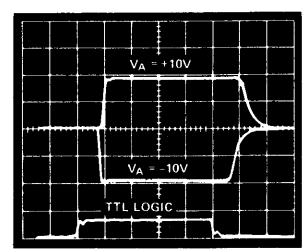


+125°C

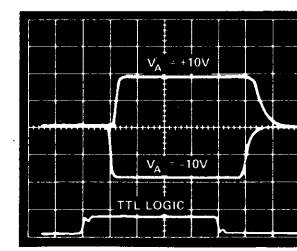
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



-55°C

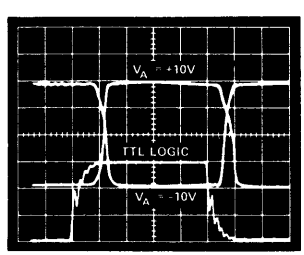


+25°C



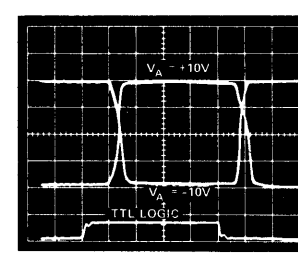
+125°C

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 10)



+25°C

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 11)



+25°C

APPLICATION NOTE

To maximize switching speed on the IH5140 family use TTL open collector logic (15V with a 1kΩ or less collector resistor). This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V→+3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 12.

The typical channel of the IH5140 family consists of both P and N-channel MOS-FETs. The N-channel MOS-FET uses a "Body Puller" FET to drive the body to -15V(±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 13). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS(ON)}$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 14.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 15. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

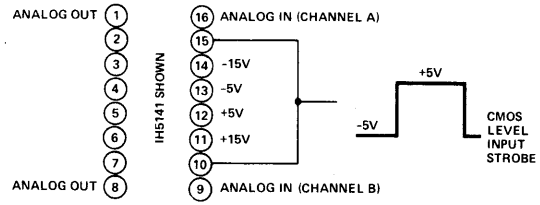


FIGURE 12.

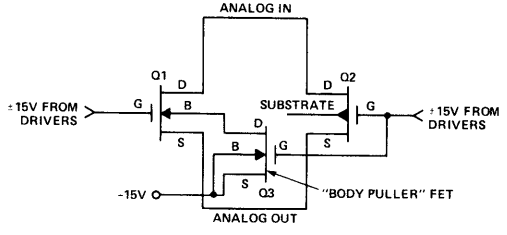


FIGURE 13.

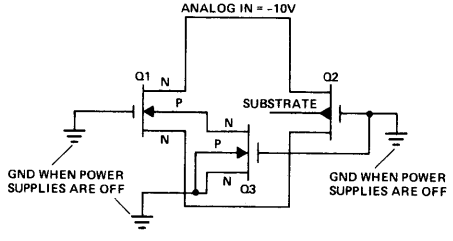


FIGURE 14.

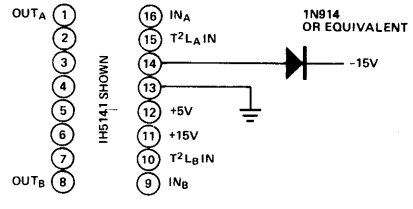


FIGURE 15.

APPLICATIONS

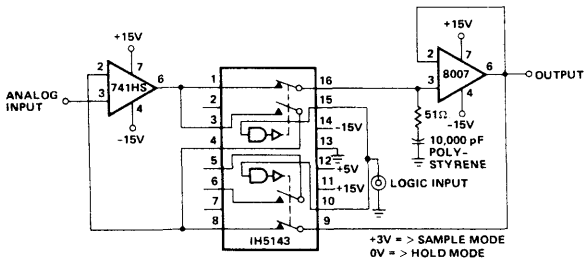
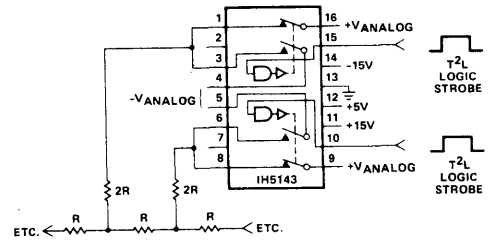
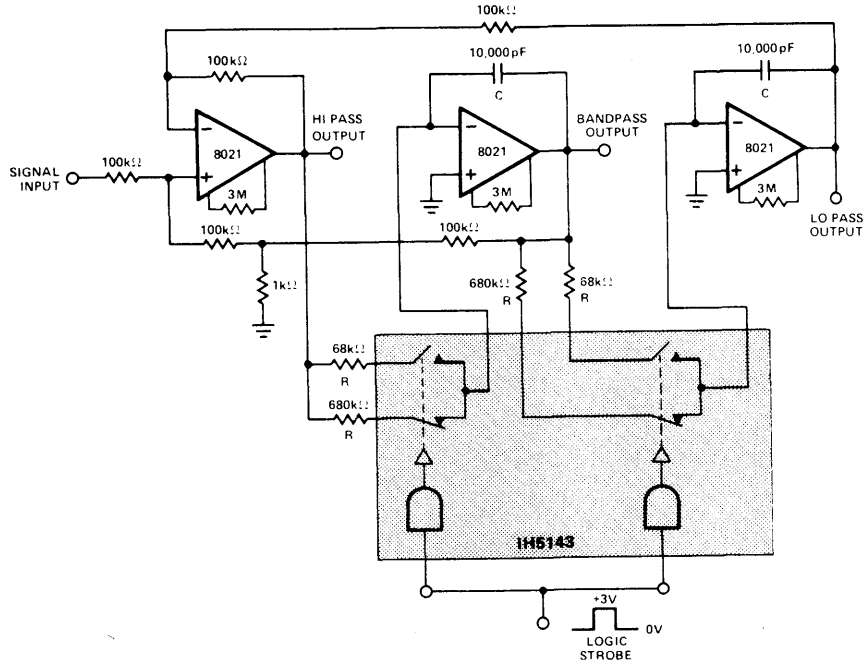


FIGURE 16. Improved Sample and Hold Using IH5143



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

FIGURE 17. Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)



CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

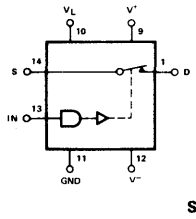
$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

FIGURE 18. Digitally Tuned Low Power Active Filter.

SWITCHING STATE DIAGRAMS

SWITCH STATES ARE FOR LOGIC "1" INPUT

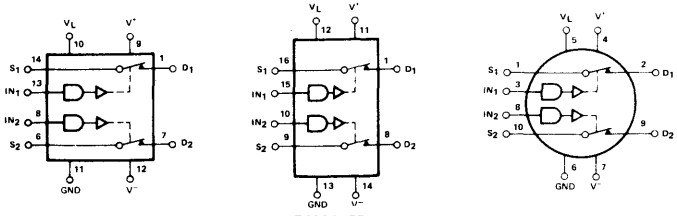
FLATPACK (FD-2) DIP (JE, PE)



SPST

IH5140 ($r_{DS(on)}$ < 75Ω)

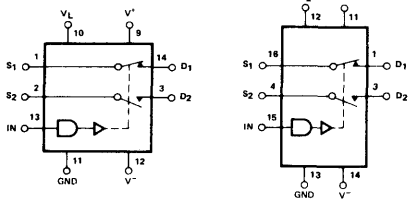
FLATPACK (FD-2) DIP (JE, PE) TO-100



DUAL SPST

IH5141 ($r_{DS(on)}$ < 75Ω)

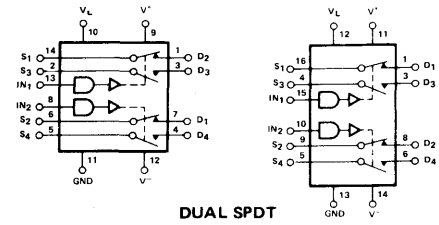
FLATPACK (FD-2) DIP (JE, PE) TO-100 (DG188 EQUIVALENT)



SPDT

IH5142 ($r_{DS(on)}$ < 75 Ω)

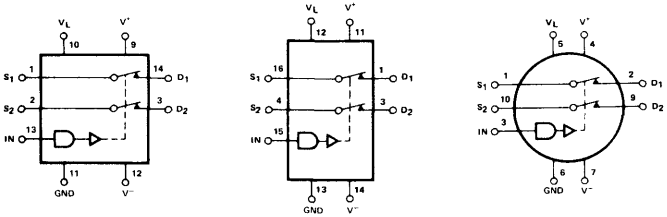
FLATPACK (FD-2) DIP (JE, PE) (DG191 EQUIVALENT)



DUAL SPDT

IH5143 ($r_{DS(on)}$ < 75Ω)

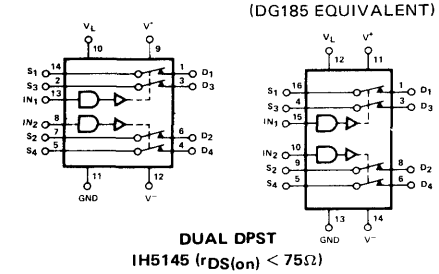
FLATPACK (FD-2) DIP (JE, PE) TO-100



DPST

IH5144 ($r_{DS(on)}$ < 75Ω)

FLATPACK (FD-2) DIP (JE, PE) (DG185 EQUIVALENT)



DUAL DPST

IH5145 ($r_{DS(on)}$ < 75Ω)

IH5208

4-Channel Differential Fault Protected CMOS Analog Multiplexer

FEATURES

- Ultra low leakage — $I_{D(off)} \leq 100pA$
- Power supply quiescent current less than $1\mu A$
- ± 13V analog signal range
- No SCR latchup
- Break-before-make switching
- TTL and CMOS compatible strobe control
- Pin compatible with HI509, DG509 and AD7509
- All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ± 25V
- Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ± 25V. Throughput always < ± 14V (± 15V supplies)
- TTL and CMOS compatible binary Address and ENable inputs

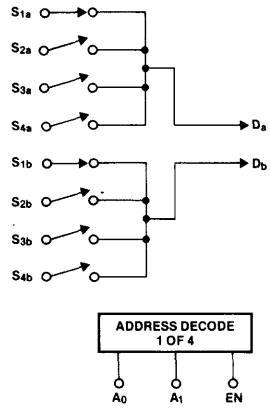
GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG509 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ± 25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

3

FUNCTIONAL DIAGRAM



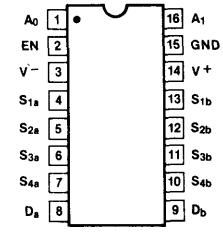
2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 1
ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5208MJE	− 55°C to + 125°C	16 pin CERDIP
IH5208IJE	− 20°C to + 85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, +15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) 20mA

Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipaton (Package)* 1200mW

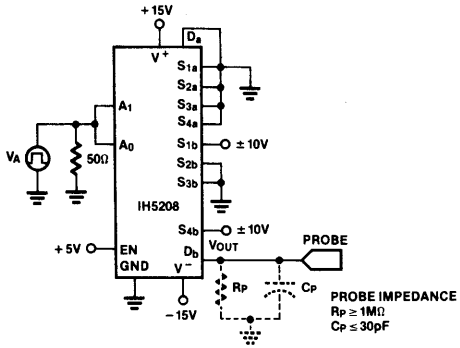
*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	MAX LIMITS M SUFFIX 25°C	MAX LIMITS M SUFFIX 125°C	MAX LIMITS I/C SUFFIX −20°C/0°C	MAX LIMITS I/C SUFFIX 25°C	MAX LIMITS I/C SUFFIX 85°C/70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(on)}$		S to D	8	700	900	900	1200	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
				8	500	900	900	1200	1200	1200	1800		$V_D = -10V$ $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$				5		10			10		%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$		S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	
				8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$		D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0$
				1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$		D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
				8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF		S	8	1		100	1000	50	50	5000	nA	$V^+ = V^- = 0V$, $V_S = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$ or $5V$	
	$I_{S(off)}$ with Overvoltage (Note 1)		S	8	1		2000	5000		5000	5000		$V_S = \pm 25V$, $V_D = \mp 10V$	Sequence each switch
IN	$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$		A_0, A_1, A_2, or EN	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or $0V$	
				4	.01		10	30		10	30		$V_A = 15V$ or $0V$	
DYNAMIC	$t_{transition}$		D		0.3		1					μs	See Figure 1	
	t_{open}		D		0.2								See Figure 2	
	$t_{on(EN)}$		D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$		D		0.4		1							
	t_{on}-t_{off} Break-Before-Make Delay Settling Time		D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation		D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, $f = 500$ KHz	
	$C_{S(off)}$		S		5							pF	$V_S = 0$	$V_{EN} = 0V$, $f = 140$ KHz to 1 MHz
	$C_{D(off)}$		D		25								$V_D = 0$	
	$C_{DS(off)}$		D to S		1								$V_S = 0$, $V_D = 0$	
SUP	Supply Current	+	V^+	1	500	900	750	600		1000		μA	All V_A, $V_{EN} = 0$ or $5V$	
		−	V^-	1	500	900	750	600		1000				

Note 1. Readings taken 400ms after the overvoltage occurs.



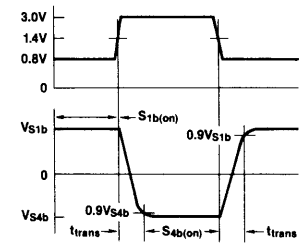
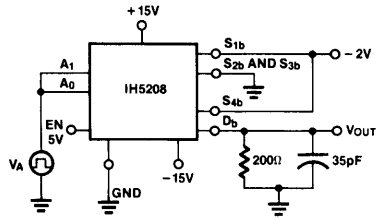


Figure 1. t_{trans} Switching Test



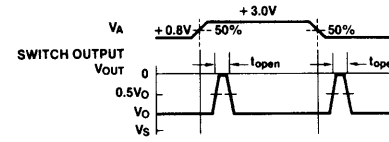
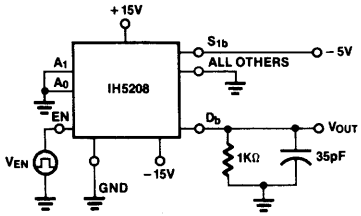


Figure 2. t_{open} (Break-Before-Make) Switching Test



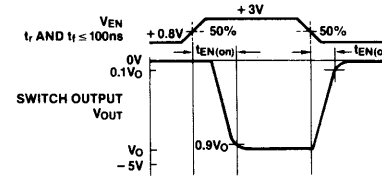
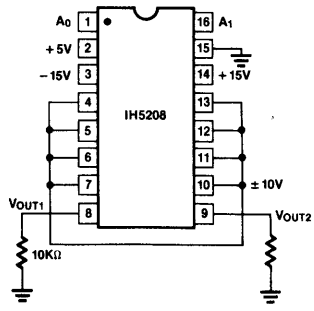


Figure 3. t_{on} and t_{off} Switching Test



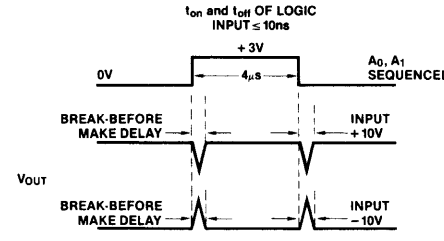


Figure 4. Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5208, like all Intersil's multiplexers, contains a set of CMOS switches forming the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special treatments that many multiplexer enable inputs require for proper logic swings. This identical circuit treatment of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important, difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches, and while this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the inpout goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 5) combined with the dielectrically isolated process to obviate these problems.

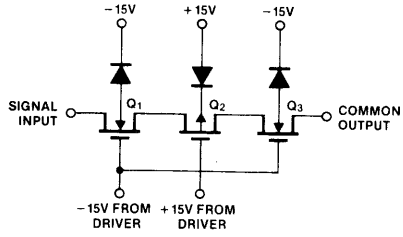


Figure 5. Series Connection of Channel Switches

Within the normal analog signal band, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 6). Thus protection is provided to any input or output channel against overvoltage on any (or several) input or output channels even in the absence of multiplexer supply voltages, and applies up to the breakdown voltage of the respective switches, drawing only leakage currents. Figure 7 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 8).

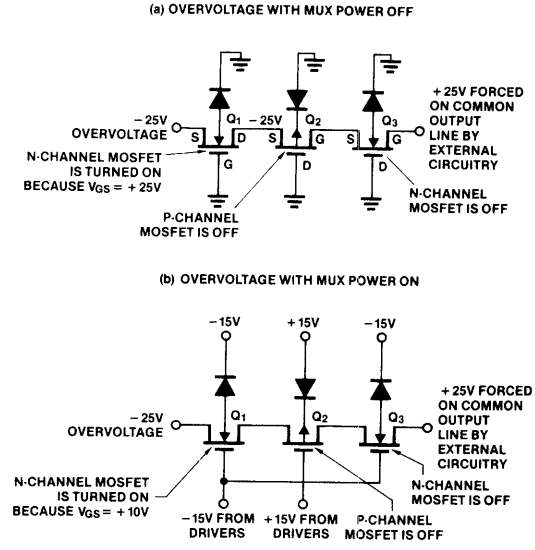


Figure 6. Overvoltage Protection

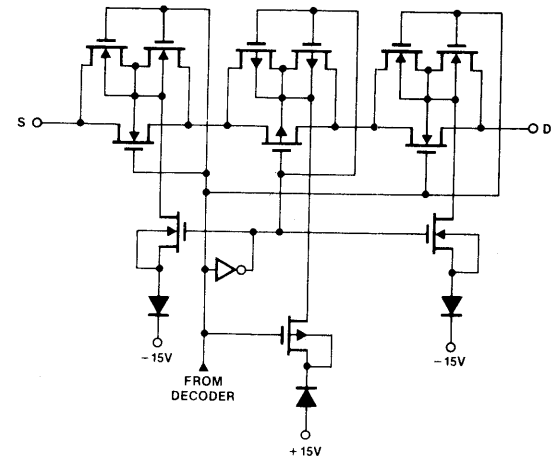


Figure 7. Detailed Channel Switch Schematic

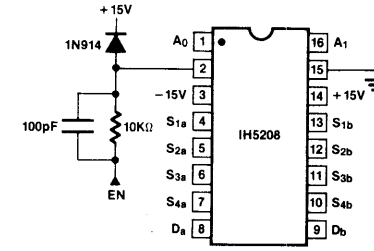


Figure 8. Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the ± 10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ± 13V, however, $r_{DS(on)}$ will increase to about 1.8K. Beyond ± 13V the device approaches an open circuit, and thus ± 12V is about the practical limit, see Figure 9.

Figure 10 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 11 gives the ON resistance variation with temperature.

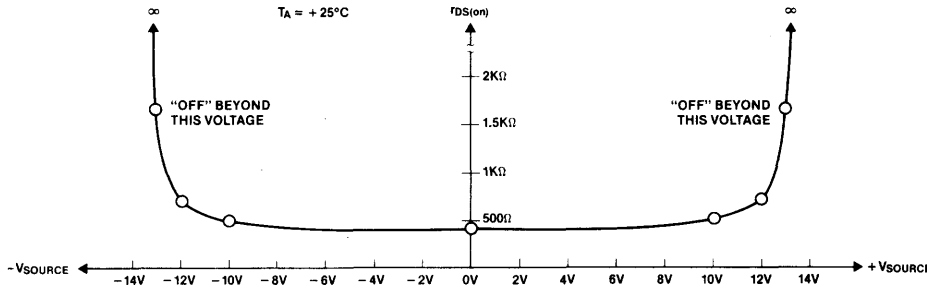


Figure 9. $r_{DS(on)}$ vs Signal Input Voltage @ T_A = + 25°C

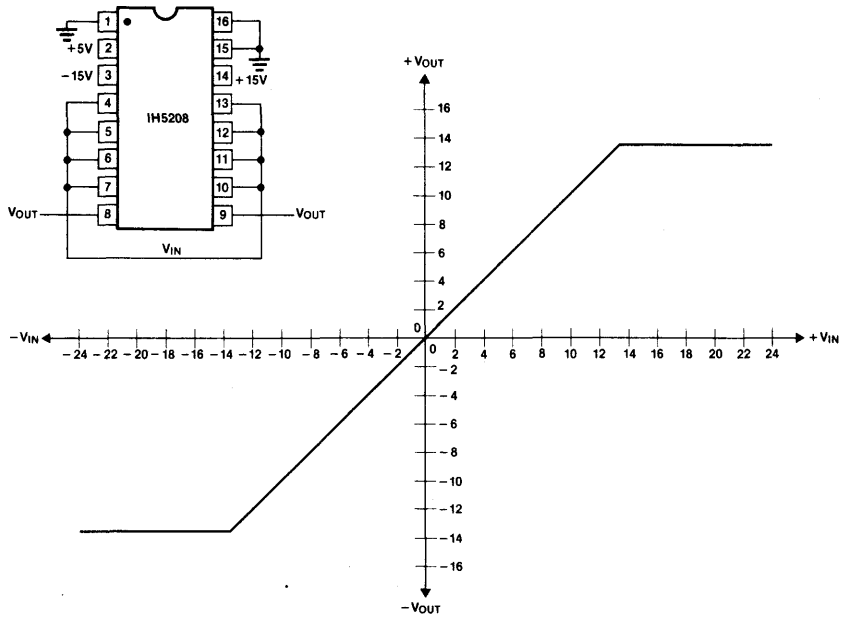


Figure 10. MUX Output Voltage vs Input Voltage
Channel 1 Shown; All Channels Similar

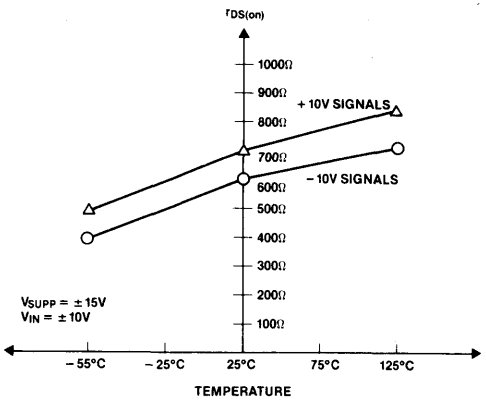


Figure 11. Typical $r_{DS(on)}$ vs Temperature

USING THE IH5208 WITH SUPPLIES OTHER THAN ± 15V

The IH5208 will operate successfully with supply voltages from ± 5V to ± 15V; $r_{DS(on)}$ increases as supply voltage decreases, see Figure 12. Leakage currents, however, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds will remain TTL compatible.

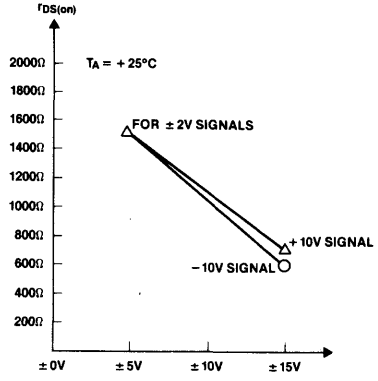
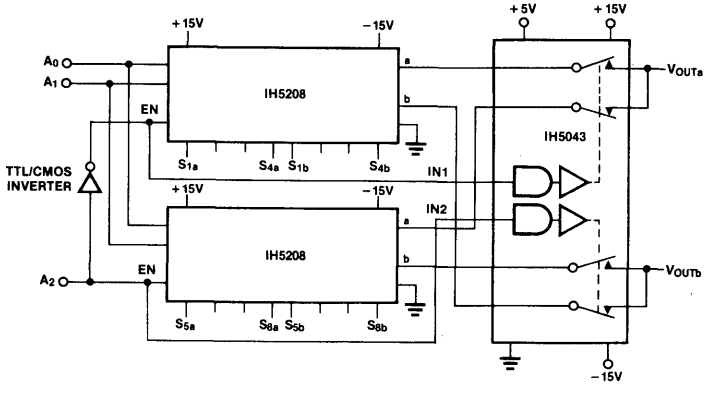


Figure 12. $r_{DS(on)}$ vs Supply Voltages

IH5208 APPLICATIONS INFORMATION

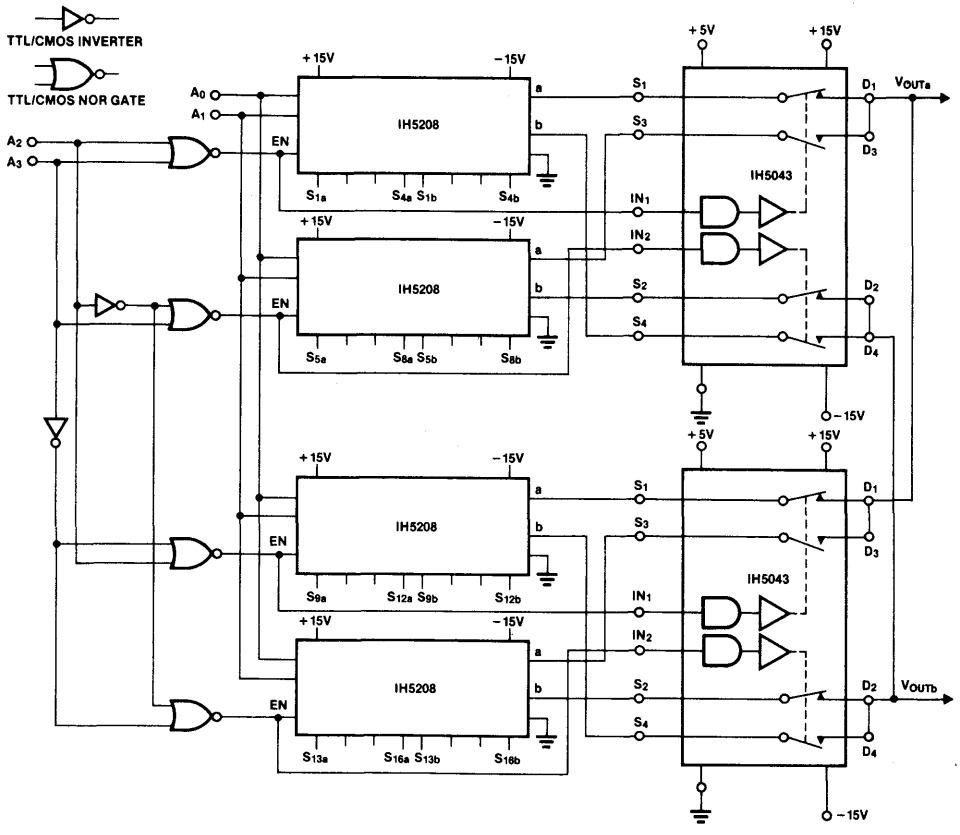


DECODE TRUTH TABLE

A_2	A_1	A_0	ON SWITCH PAIR
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Figure 13. 2 of 16 channel multiplexer using two IH5208s. Overvoltage protection and break-before-make switching are extended to all channels.

IH5208 APPLICATIONS INFORMATION (Continued)



DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH		ON SWITCH	
0	0	0	0	S1a		S1b	
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a	V_{OUTa}	S8b	V_{OUTb}
1	0	0	0	S9a		S9b	
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

Figure 14. Submultiplexed 2 of 32 system. The two IH5043s are overvoltage protected by the IH5208s. Submultiplexing reduces output capacitance and leakage currents.

APPLICATION NOTES

Further information may be found in:

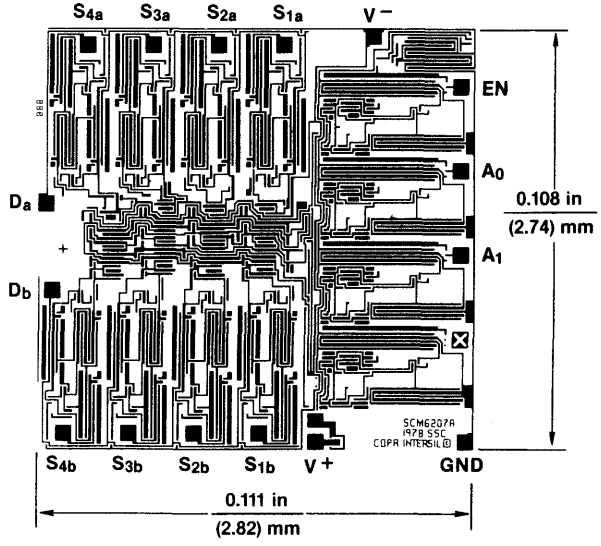
A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

CHIP TOPOGRAPHY



IH5341

CMOS Monolithic RF/Video Switch

FEATURES

- $r_{ds(on)} < 75\Omega$, flat from DC to 100MHz (< 3dB)
- "OFF" isolation > 60dB @ 10MHz
- Cross coupling isolation > 60dB @ 10MHz
- Directly compatible with TTL, CMOS
- Wide operating power supply range
- Power supply current < 1μA
- "Break-before-Make" switching
- Fast switching (80ns/150ns typ)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0 to +70°C	14-Pin DIP
IH5341ITW	−20°C to +85°C	TO-100
IH5341MTW	−55°C to +125°C	TO-100

GENERAL DESCRIPTION

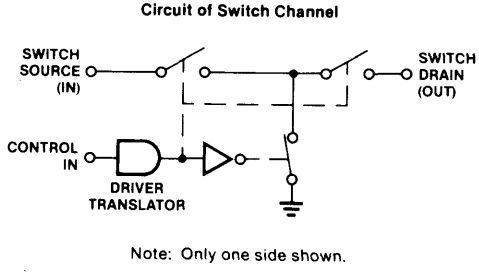
The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typical $t_{on} = 150ns$ and $t_{off} = 80ns$, and guaranteed "Break-before-Make" switching.

Switch "ON" resistance is typically 40Ω-50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

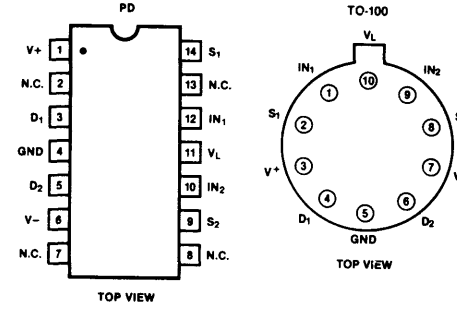
3

FUNCTIONAL DIAGRAM



Note: Only one side shown.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltages V^+ and V^- ..... ±17V
Current in any Terminal 50mA
Analog Input Voltage ..... V^+ to V^-
Operating Temperature
(M Version) ..... −55°C to +125°C
(I Version) ..... −20°C to +85°C
(C Version) ..... 0 to +70°C

Storage Temperature ..... −65°C to +160°C
Power Dissipation 250mW
Derate above 25°C @ ..... 7.5mW/°C
Logic Control Voltage ..... V^+ to V^-
Voltage on Pin 10 ..... V^+ to V^-
Lead Temperature (soldering, 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS $V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified.

3

PARAMETER	SYMBOL	CONDITIONS	TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				−55°C	+25°C	+125°C	−20/0°C	+25°C	+85/ +70°C	
Supply Voltage Ranges										
Positive Supply	V^+		4.5>16		5 to 15			5 to 15		
Logic Supply	V_L	(Note 3)	4.5>V^+		5 to V^+			5 to V^+		V
Negative Supply	V^-		−4> −16		−5 to −15			−5 to −15		
Switch "ON" Resistance	$r_{ds(on)}$	V_D = −5V to +5V, I_S = 10mA, V_{IN} = 2.4V		75	75	100	75	75	100	
(Note 4)		V_D = −15V to +15V		125	125	175	150	150	175	Ω
Switch "ON" Resistance	$r_{ds(on)}$	$V^+ = V_L = 5V$, V_{IN} = 3V, $V^- = 5V$, $V_D = \pm 5V$		250	250	350	300	300	350	
On Resistance Match		I_S = 10mA, $V_D = \pm 5V$	5							
Switch "OFF" Leakage	$I_{D(off)}$ or	$V_{S/D}$ = +5V to −5V, V_{IN} = 0.8V		0.1	0.1	20	0.5	0.5	20	
(Notes 2 and 4)	$I_{S(off)}$	$V_{S/D}$ = +14V to −14V		0.2	0.2	50	1.0	1.0	100	nA
Switch "ON" Leakage	$I_{D(on)}$ +	V_D = +5V or −5V, V_{IN} = 2.4V		0.3	0.3	50	1.0	1.0	40	
	$I_{S(on)}$	V_D = +14V to −14V		0.5	0.5	100	1.0	1.0	100	
Input Logic Current	I_{IN}	V_{IN} > 2.4V or < 0		1	1	10	1	1	10	
Positive Supply Quiescent Current	I^+	V_{IN} = 0V or +5V		1	1	10	1	1	10	μA
Negative Supply Quiescent Current	I^-	V_{IN} = 0V or +5V		1	1	10	1	1	10	
Logic Supply Quiescent Current	I_L	V_{IN} = 0V or +5V		1	1	10	1	1	10	

Note 1: Typical values are not tested in production. They are given as a design aid only.
Note 2: Positive and negative voltages applied to opposite sides of switch, in both directions successively.
Note 3: These are the operating voltages at which the other parameters are tested, and are not directly tested.
Note 4: The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

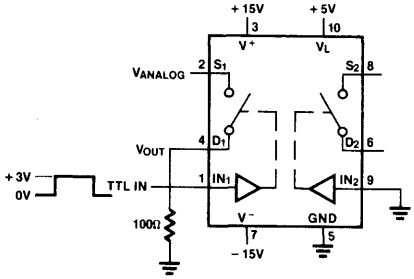
AC ELECTRICAL CHARACTERISTICS $V^+ = +15V$, $V_L = +5V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified (Note 5).

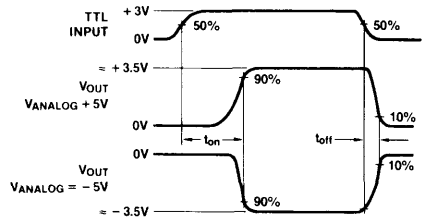
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch "ON" Time	t_{on}	See Figure 1			300	ns
Switch "OFF" Time	t_{off}	See Figure 1			150	
"OFF" Isolation Rejection Ratio	OIRR	See Figure 2 (Note 6)	60			dB
Cross Coupling Rejection Ratio	CCRR	See Figure 3 (Note 6)	60			
Frequency where $r_{ds(on)} = 0.7 \times DC$		See Figure 4 (Note 6)	100			MHz

Note 5: All AC parameters are sample tested only.

Note 6: Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

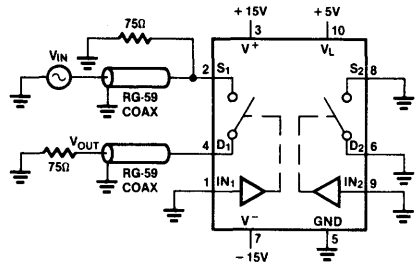
TEST CIRCUITS





Note: Only one side shown. Other acts identically.

Figure 1. Switching Time Test Circuit and Waveforms

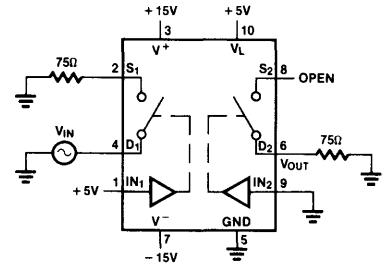


$V_{IN} = \pm 5V$ (10Vp-p) @ f = 10MHz

$OIRR = 20 \log \frac{V_{IN}}{V_{OUT}}$

Note: Only one side shown. Other acts identically.

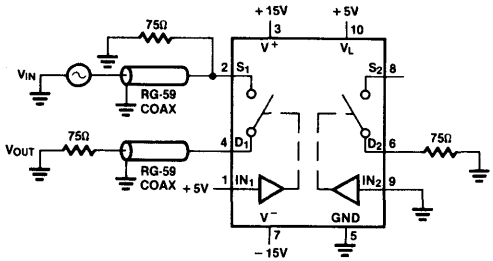
Figure 2. OFF Isolation Test Circuit



$V_{IN} = 225mVrms$ @ f = 10MHz

$CCRR = 20 \log \frac{V_{IN}}{V_{OUT}}$

Figure 3. Cross-Coupling Rejection Test Circuit



Note: Only one side shown. Other acts identically.

$r_{ds(on)3dB} =$ > frequency where $20 \log \frac{V_{OUT}}{V_{IN}}$ changes by +3dB

i.e., from DC to f = 40MHz, $20 \log \frac{V_{OUT}}{V_{IN}} \cong -4dB$;

when this ratio reaches −1dB, the frequency causing this is $r_{ds(on)3dB}$ frequency.

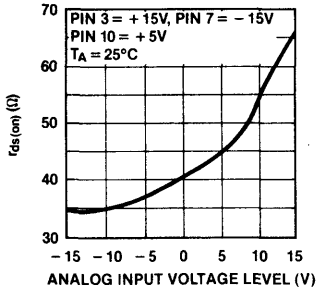
$V_{IN} = 225mVrms$ @ f = 10MHz -100MHz

$\frac{V_{OUT}}{V_{IN}} = \frac{75\Omega \text{ (load)}}{75\Omega + r_{ds(on)}} = \frac{141mVrms}{225mVrms}$ typically @ f = 10MHz

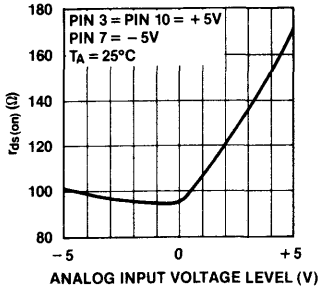
Figure 4. $r_{ds(AC)}$ Pole Frequency Test Circuit

TYPICAL CHARACTERISTICS

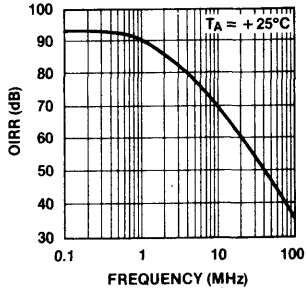
$r_{ds(on)}$ vs Analog Input Voltage with ±15V Power Supplies



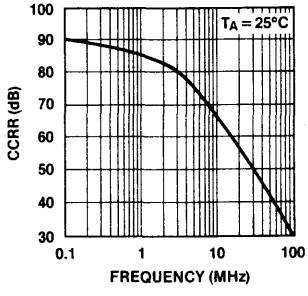
$r_{ds(on)}$ vs Analog Input Level with ±5V Power Supplies



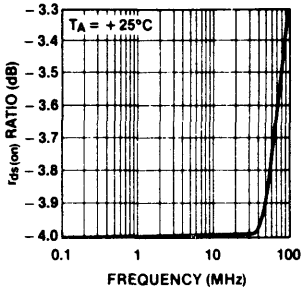
OIRR (OFF Isolation Rejection) vs Frequency (See Figure 2)



CCRR (Cross Coupling Rejection) vs Frequency (See Figure 3)



Switch $r_{ds(on)}$ Change with Frequency (Expressed in Voltage Divider Terms with a 75Ω Load (See Figure 4)



DETAILED DESCRIPTION

As can be seen in the Functional Diagram, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much better isolation between the input and the output than does the single series switch, especially at high frequencies, and the result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, and gives very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility.

APPLICATIONS

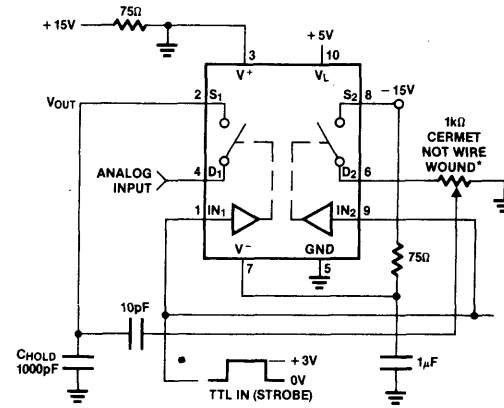
Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 5 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1k potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the −5V to +5V range.

Since the individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 6. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to −5V as shown in the figure. The choice of −5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.



*Adjust pot for 0mVp-p step @ V_{OUT} with no analog (AC) signal present

Figure 5. Charge Injection Compensation

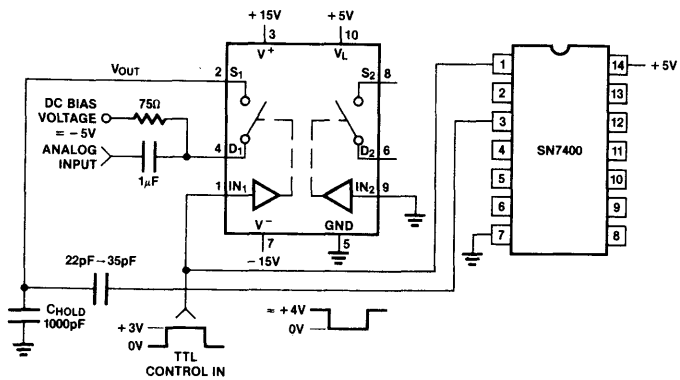


Figure 6. Alternative Compensation Circuit

Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 7.

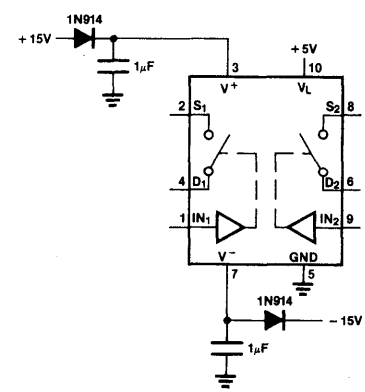
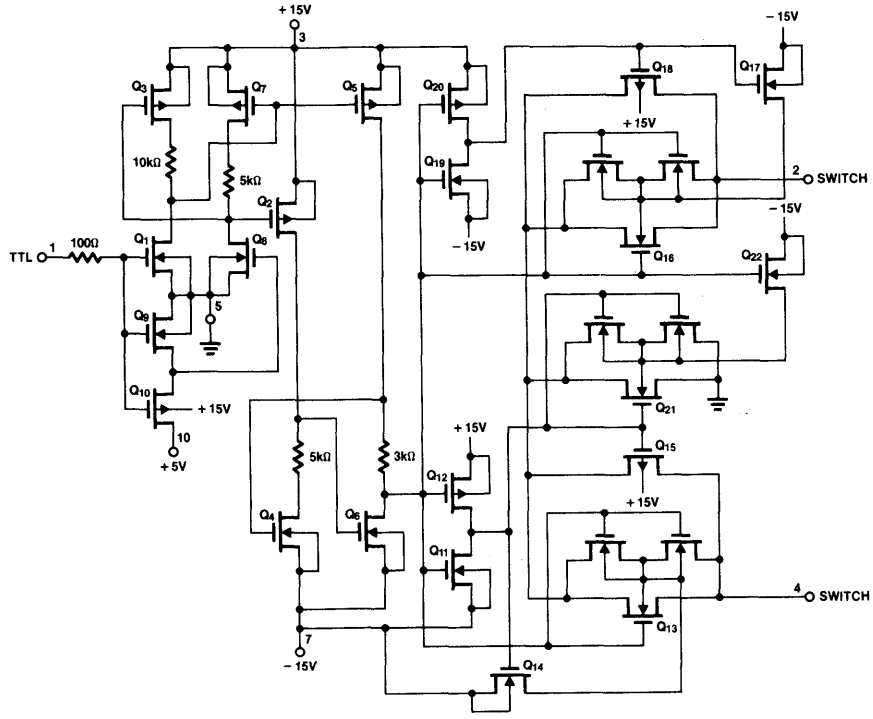
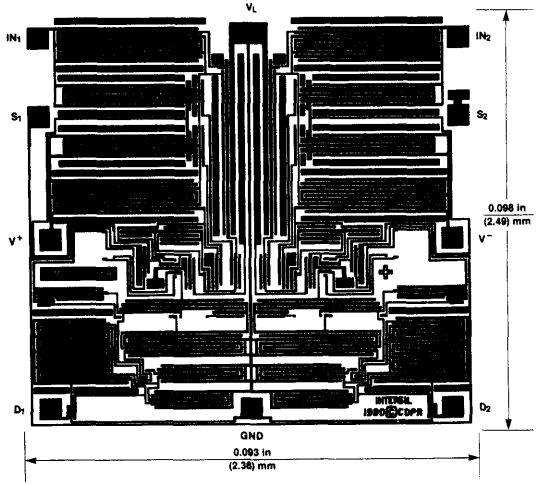


Figure 7. Overvoltage Protection Circuit

EQUIVALENT SCHEMATIC DIAGRAM (1/2 of actual circuit on chip shown)



CHIP TOPOGRAPHY



IH6108

8-Channel CMOS Analog Multiplexer

FEATURES

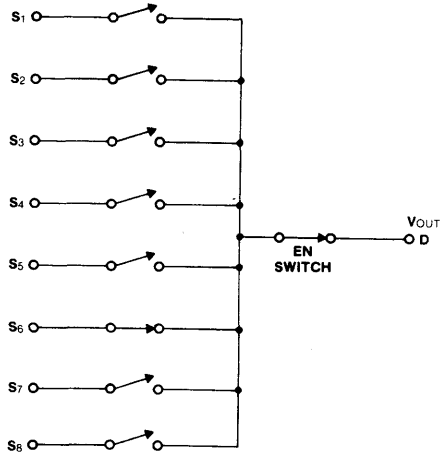
- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)} < 400$ ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **$\pm$14V analog signal range**
- **No SCR latchup**
- **Break-before-make switching**
- **Binary Address control (3 Address inputs control 8 channels)**
- **TTL and CMOS compatible strobe control**
- **Pin compatible with DG508, HI-508 & AD7508**

GENERAL DESCRIPTION

The IH6108 is a CMOS monolithic, one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line binary decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line Address inputs, and when low (0V) all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements, a "0" corresponding to any voltage greater than 2.4V. Note that the ENable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM



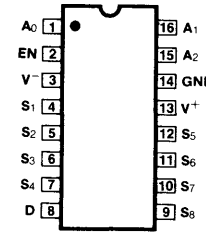
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6108MDE/CDE)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MJE	-55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temp (Soldering, 10 sec) ..... 300°C
Power Dissipation (Package)* ..... 1200 mW

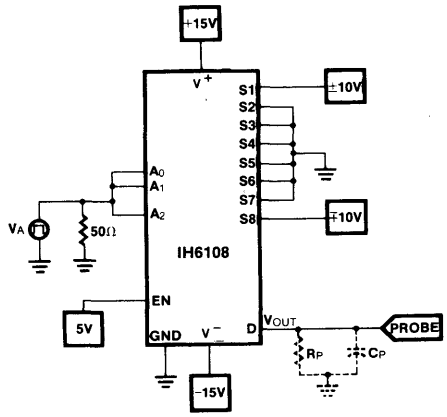
*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	MAX LIMITS M SUFFIX 25°C	MAX LIMITS M SUFFIX 125°C	MAX LIMITS C SUFFIX 0°C	MAX LIMITS C SUFFIX 25°C	MAX LIMITS C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
			8	150	300	300	400	350	350	450		$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$	$V_S = \pm 10V$
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0$
			1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
INPUT	$I_{AN(ON)}$ or $I_{A(on)}$	A_0, A_1 or A_2	3	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	$I_{AN(OFF)}$ $I_{A(off)}$	Inputs	3	.01		10	30		10	30		$V_A = 15V$ or 0V	
	I_A	A_0 A_1											
		A_2	3			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$ (Address pins)
		EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(EN)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(EN)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 kHz	
	$C_{S(off)}$	S		5							pF	$V_S = 0$	
	$C_{d(off)}$	D		25								$V_D = 0$	$V_{EN} = 0V$, f = 140 kHz to 1 MHz
	$C_{DS(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	V^+	1	40		200			1000		μA	$V_{EN} = 5V$	All $V_A = 0$ or 5V
	Supply Current −	V^-	1	2		100			1000				
	Standby Current +	V^+	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	V^-	1	1		100			1000				

NOTE 1: See Enable Input Strobing Levels, Section 1.



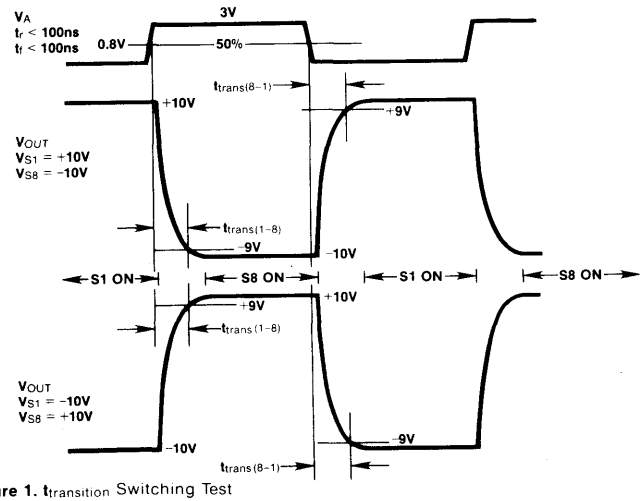


Figure 1. $t_{transition}$ Switching Test

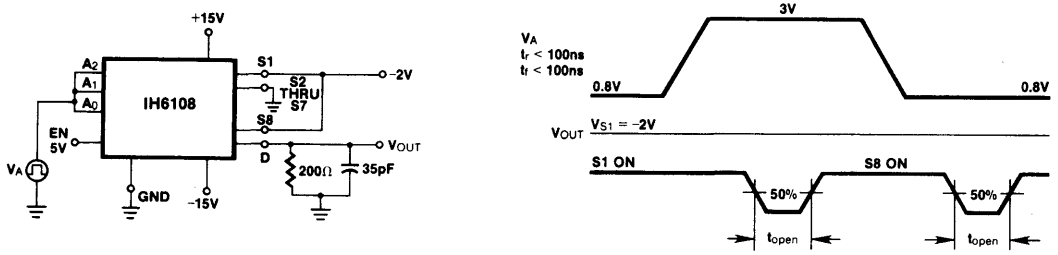


Figure 2. t_{open} (Break-Before-Make) Switching Test

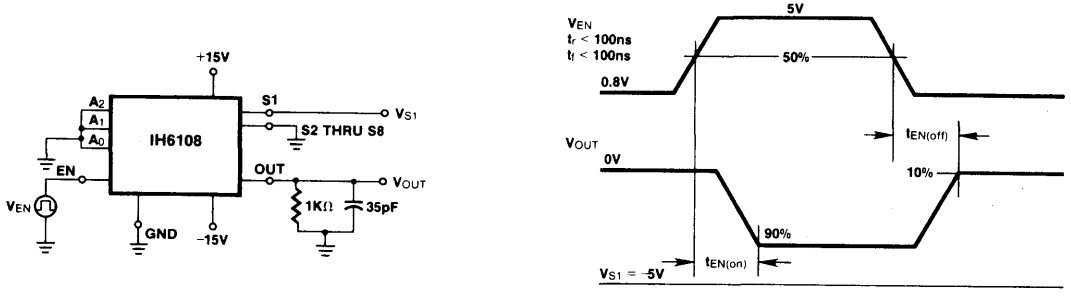


Figure 3. t_{on} and t_{off} Switching Test

IH6108 APPLICATION INFORMATION

I. ENable Input Strobing Levels

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 4)

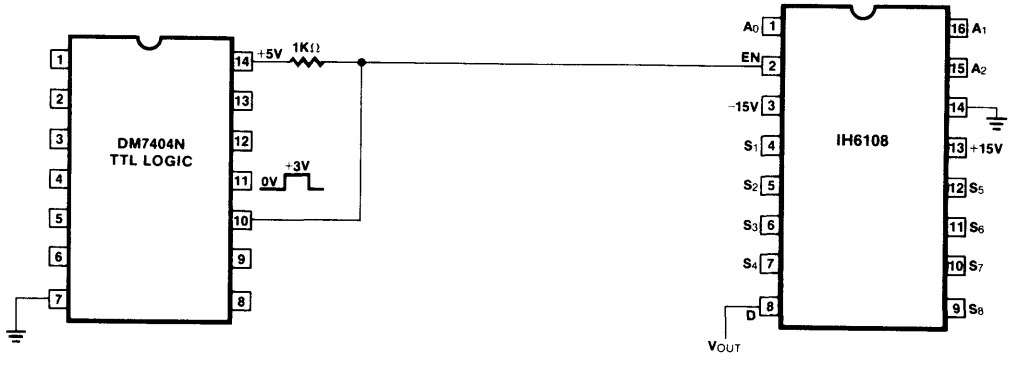


Figure 4. ENable Input Strobing from TTL Logic

IH6108 APPLICATION INFORMATION (Continued)

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 5.

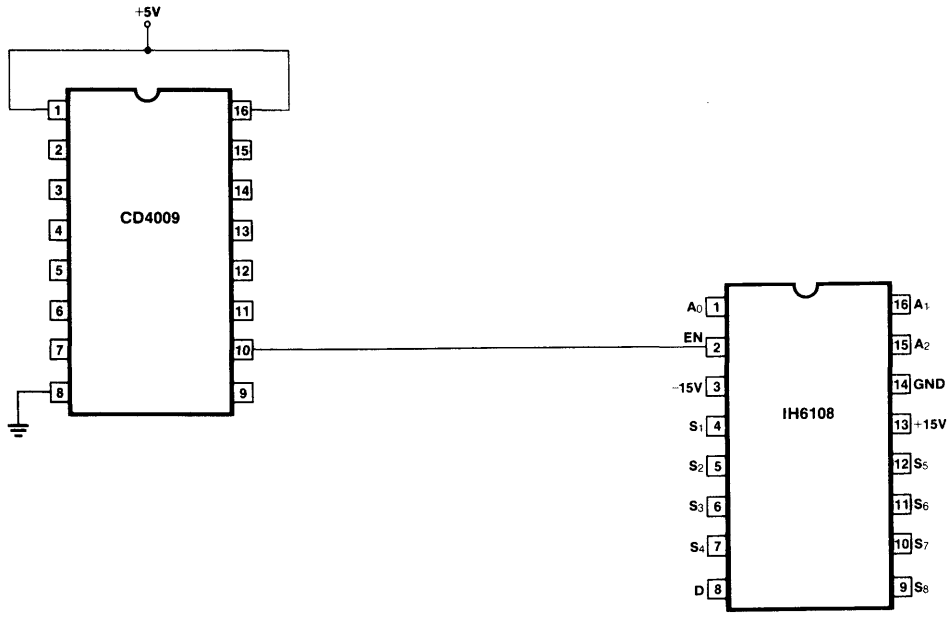


Figure 5. ENable Input Driven from CMOS Logic

The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The chart below shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 4 and 5 deal with ENable strobing when expansion to more than eight channels is required; in these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

IH6108 APPLICATION INFORMATION (Continued)

II. Using the IH6108 with supplies other than ±15V

The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V+ at all times. If this is not done the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V+ (pin 13) via a silicon diode as shown in Figure 6. When using this type of configuration, a further requirement must be met- the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V+ and EN. (See Figure 7) A 1μF capacitor can be placed across the diode to minimize switching glitches.

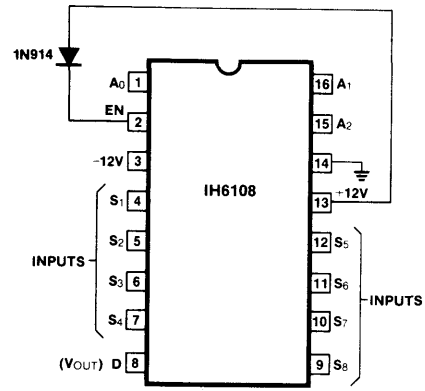


Figure 6. IH6108 Connection Diagram for less than ±15V Supply Operation.

IH6108 APPLICATION INFORMATION (Continued)

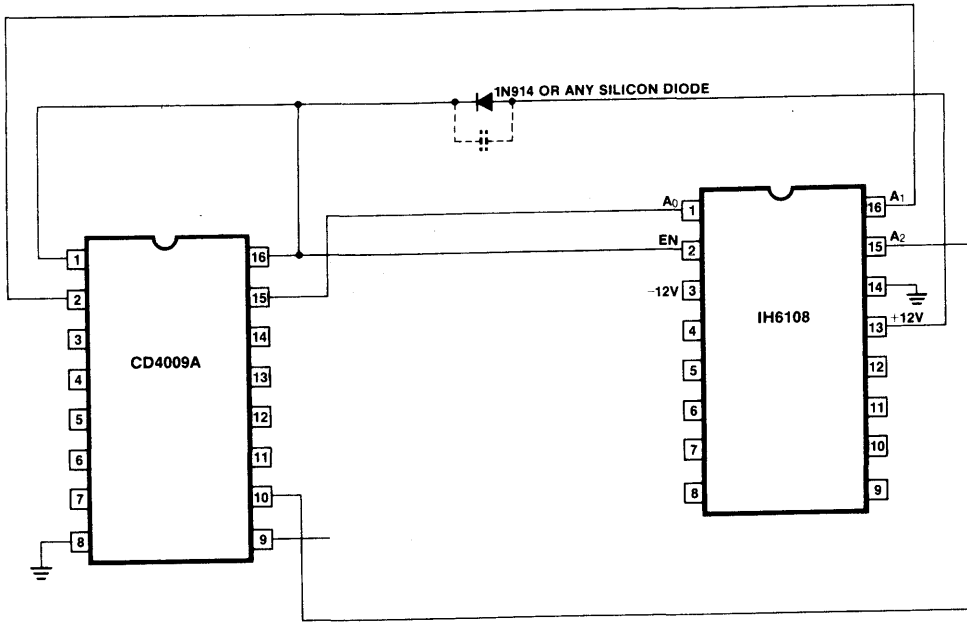


Figure 7. IH6108 Connection Diagram with ENable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6108 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

IH6116

16-Channel CMOS Analog Multiplexer

FEATURES

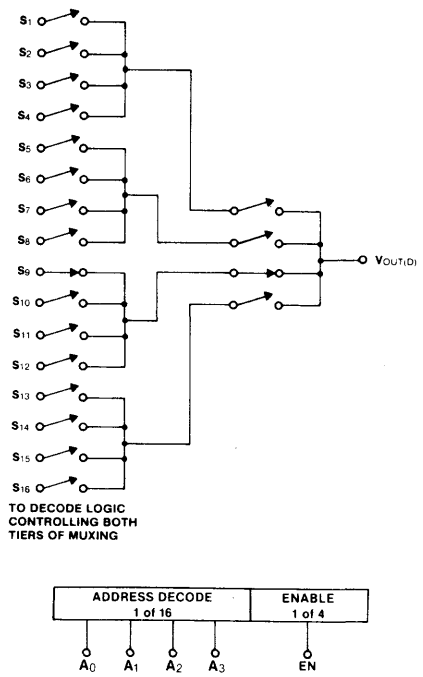
- **Pin compatible with DG506, HI-506 & AD7506**
- **Ultra Low Leakage — $I_{D(off)} \leq$ 100pA**
- **±11 analog signal range**
- **$r_{DS(on)}$ <700 ohms over full signal and temperature range**
- **Break-before-make switching**
- **TTL and CMOS compatible Address control**
- **Binary Address control (4 Address inputs control 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latchup**

GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to use as system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM

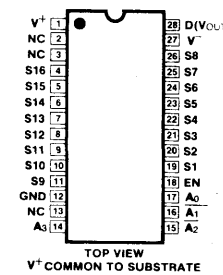


DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
x	x	x	x	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq$ 3.0V $V_{ENH} \geq$ 4.5V
Logic "0" = $V_{AL} \leq$ 0.8V

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6116MDI/CDI)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MJI	−55°C to +125°C	28 pin CERDIP
IH6116CJI	0°C to 70°C	28 pin CERDIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16v
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Lead Temperature (Soldering, 10 secs) ..... 300°C
Power Dissipation (Package)* ..... 1200 mW

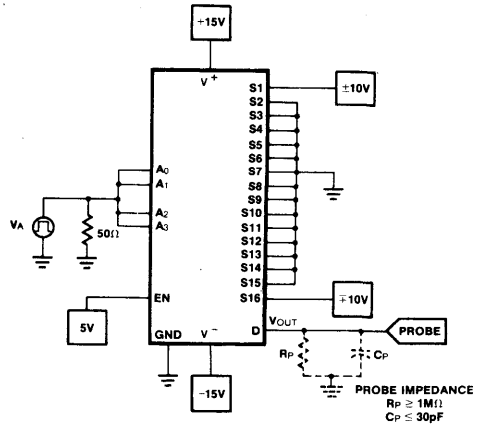
*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	16	480	600	600	700	650	650	750	Ω	V_D = 10V, I_S = −10mA	Sequence each switch on
				16	300	600	600	700	650	650	750		V_D = −10V, I_S = 10mA	V_{AL} = 0.8V, V_{AH} = 3V
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$	$V_S = \pm 10V$
	$I_{S(OFF)}$		S	16	0.01		0.1	50		0.2	50	nA	V_S = 10V, V_D = −10V	V_{EN} = 0
				16	0.01		0.1	50		0.2	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$		D	1	0.1		0.2	100		0.4	100		V_D = 10V, V_S = −10V	
				1	0.1		0.2	100		0.4	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$		D	16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
				16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 3V
INPUT	$I_{A(on)}$ or $I_{A(off)}$		A_0 A_1 A_2 A_3	4	.01		−10	−30		−10	−30	μA	V_A = 3.0V	
				4	.01		10	30		10	30		V_A = 15V	
	I_A			4			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
			EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	t_{trans}		D		0.6		1					μs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{EN(on)}$		D		0.8		1.5						See Fig. 3	
	$t_{EN(off)}$		D		0.3		1							
	"OFF" Isolation		D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$		S		5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	$C_{D(OFF)}$		D		40								V_D = 0	
	$C_{DS(OFF)}$		D to S		1								V_S = 0, V_D = 0	
SUPPLY	Supply Current	+	V^+	1	55		200			1000		μA	V_{EN} = 5V	All V_A = 0 or 3V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			V_{EN} = 0	
		−	V^-	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.



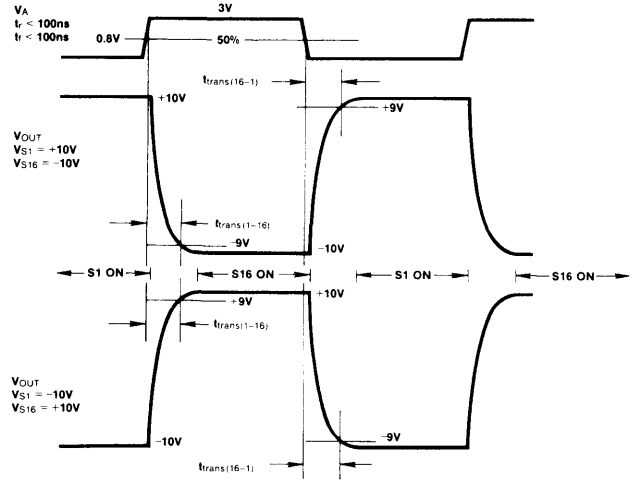
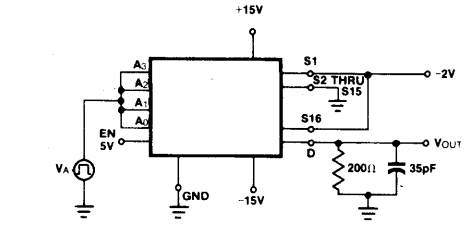


Figure 1



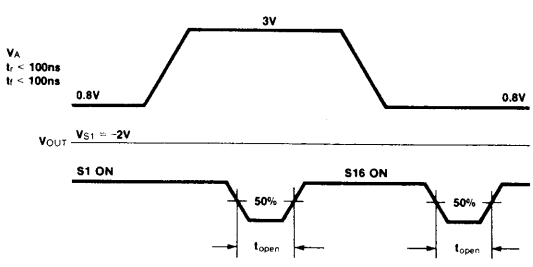
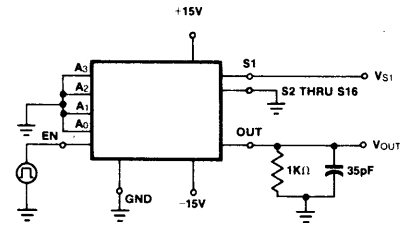


Figure 2



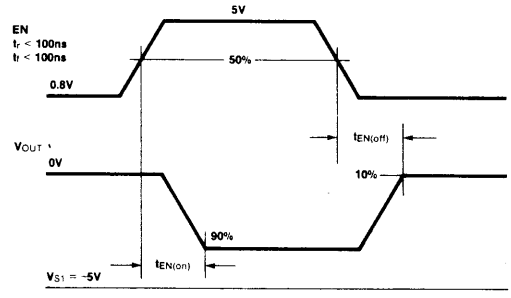
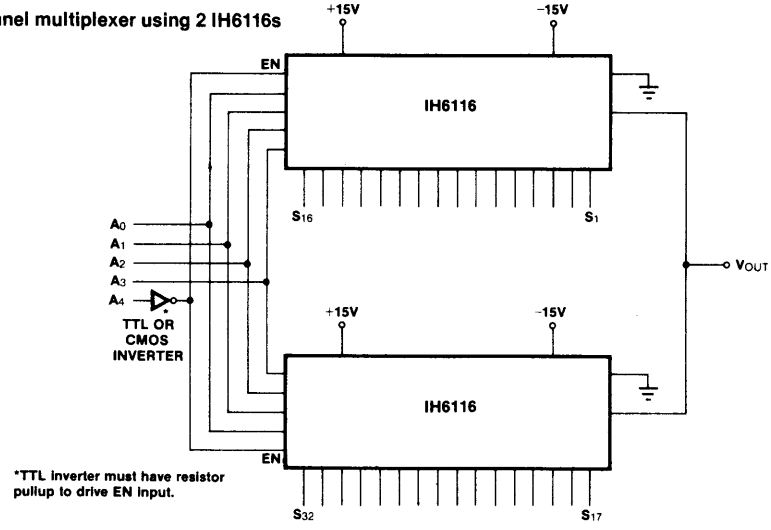


Figure 3

IH6116 APPLICATIONS

I. 1 out of 32 channel multiplexer using 2 IH6116s



*TTL inverter must have resistor pullup to drive EN input.

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

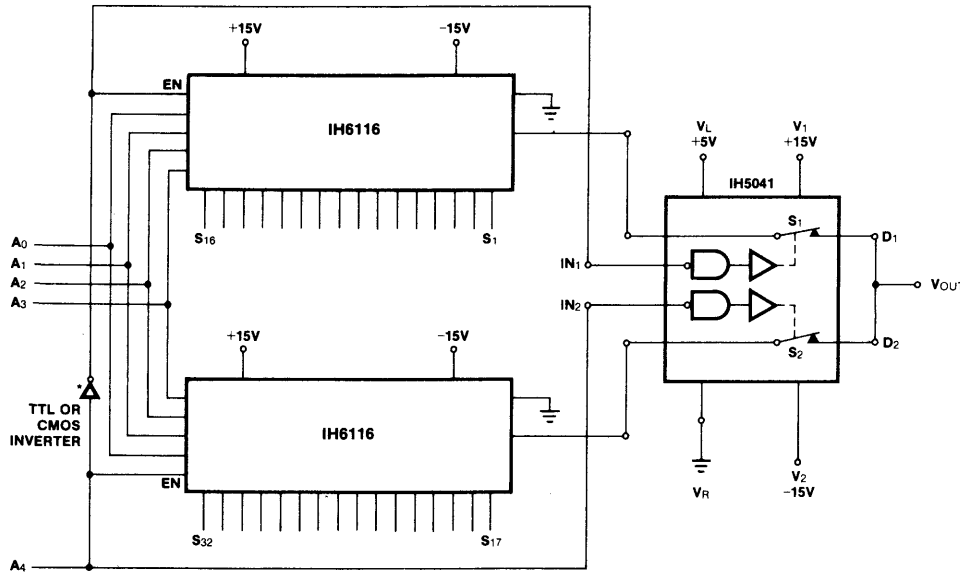
DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 4

IH6116 APPLICATIONS (Continued)

II. 1 out of 32 channel multiplexer using 2 IH6116s; using an IH5041 for submultiplexing



*TTL gate must have
pullup resistor to +5V to drive EN inputs

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 5

IH6116 APPLICATIONS (Continued)

III. 1 out of 64 multiplexer using 4 1/16s and IH5053 as submultiplexer

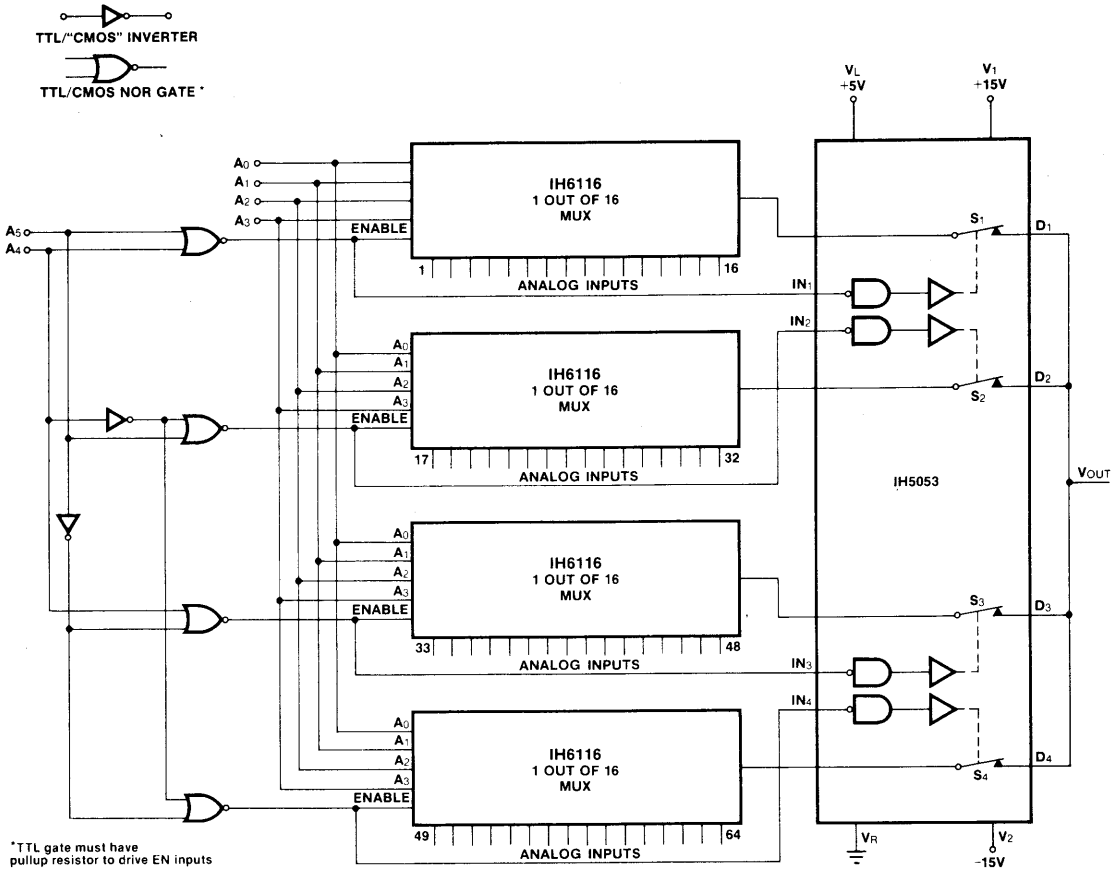


Figure 6

IV. General note on expandability of IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacity and leakage that would be possible using a system with all 16 channels tied to one common output. Also the expandability into 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6116 is expanded.

Figure 4 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each 6116 are tied together so that 8 channels are tied to the V_{OUT} common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$, or about 1.0 nA of typical leakage at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500Ω area.

Figure 5 shows the 1 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2 nA.

3

Figure 6 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5053 is used to get the third tier of MUXing. The V_{OUT} point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550 ohm area with thruput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of 1-2μA so that no excessive system power is generated. Note that the logic of the 5053 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

V. Enable input strobing levels

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX. However, when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V $\pm$5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor of 1kΩ or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6108 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

IH6201
Dual CMOS Driver/ Voltage Translator

FEATURES

- **Driven direct from TTL or CMOS logic**
- **Translates logic levels up to 30V levels**
- **Switches 20V_{ACPP} signals when used in conjunction with Intersil IH401A Varafet (as an analog gate)**
- **$t_{ON} \leq$ 300nS & $t_{OFF} \leq$ 200nS for 30V level shifts**
- **Quiescent supply current $\leq 100\mu a$ for any state (d.c.)**
- **Provides both normal & inverted outputs**

GENERAL DESCRIPTION

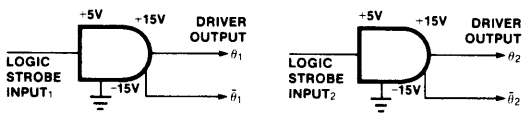
The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes the low level TTL or CMOS logic level and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

When used in conjunction with the Intersil IH401 family Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time < t_{on} time). The combination has typical t_{off} ≈ 80nS and typ. t_{on} ≈ 200nS for signals up to 20Vpp in amplitude.

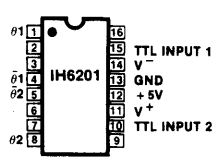
A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\bar{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\bar{\theta}$ goes to V^+; thus θ and $\bar{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive an N and P channel Mosfet, to make a complete Mosfet analog gate.

The driver typically uses +5V and ±15V power supplies; however a wide range of V^+ and V^- is possible, however $V^+ > 5V$ is necessary for the driver to work properly.

BLOCK DIAGRAM



PIN CONFIGURATION



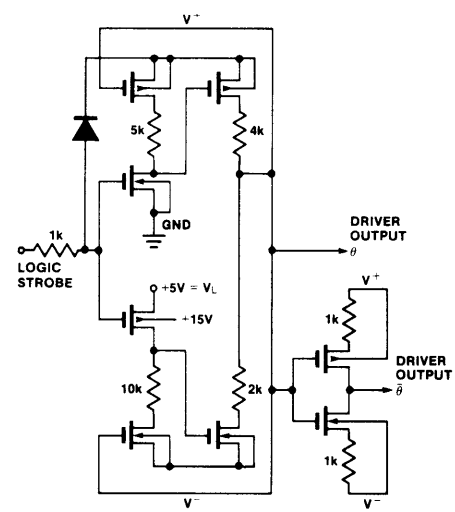
OUTLINE DWGS
DE, JE, PE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE
*IH6201CDE	0°C to 70°C
*IH6201MDE	−55°C → +125°C
IH6201CJE	0°C to 70°C
IH6201MJE	−55°C to 125°C
IH6201CPE	0°C to 70°C

*Special Order Only

SCHEMATIC DIAGRAM (ONE CHANNEL)



ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V

Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$

ITEM	CONDITIONS	IH6201CDE			IH6201MDE			UNITS
		−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	
θ or $\bar{\theta}$ driver output swing	V_{IN} = 0V ⊓ +3V fig. 2B	28	28	28	28	28	28	Vpp
V_{IN} strobe level ("1") for proper translation	$\theta \geq 14V$ $\bar{\theta} \geq -14V$	3.0	3.0	3.0	2.4	2.4	2.4	$V_{D.C.}$
V_{IN} strobe level ("0") for proper translation	$\theta \geq -14V$ $\bar{\theta} \geq 14V$	0.4	0.4	0.4	0.8	0.8	0.8	$V_{D.C.}$
I_{IN} input strobe current draw (for 0V → 5V range)	V_{IN} = 0V or +5V	1	1	1	1	1	1	μA
t_{on} time	V_{IN} = 0V ⊓ 3V, 4μS C_L = 30pf switching turn-on time fig. 2B	400	400	400	300	300	300	nS
t_{off} time	V_{IN} = 0V ⊓ +3V, 4μS C_L = 30pf switching turn-off time fig. 2B	300	300	300	200	200	200	nS
I^+ (V^+) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I^- (V^-) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I_L (V_L) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA

APPLICATIONS

I. INPUT DRIVE CAPABILITY

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V → 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to −15V) circuit is unaffected as long as V^+ to V_{IN} does not exceed absolute maximum rating.

II. OUTPUT DRIVE CAPABILITY

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel J-FETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents forward biasing between the signal input and the $+V_{CC}$ supply. The IH6201 will drive any J-FET provided some sort of isolation is added i.e.

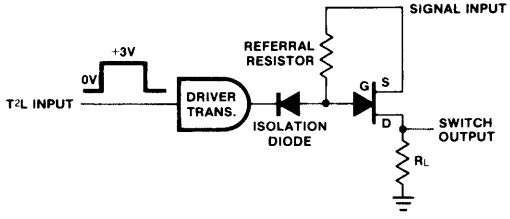


Figure 1

You will notice in Figure 1 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for inadequate charge area curve for isolation diode (i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output J-FET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100kΩ to 1MΩ range and is not too critical.

III. MAKING A COMPLETE SOLID STATE SWITCH THAT CAN HANDLE 20Vpp SIGNALS

The limitation on signal handling capability comes from the output gating device. When a J-FET is used, it's the pinch-off of the J-FET acting with the V^- supply that does the

APPLICATIONS, CONTINUED

limiting. In fact max. signal handling capability = 2 (Vp + (V^-)) Vpp where Vp = pinch-off voltage of J-FET chosen. i.e. Vp = 7V, V^- = −15V ∴ max. signal handling = 2 (7V + (−15V)) Vpp = 2(7V−15)pp=2(−8Vpp)=16Vpp. Obviously to get ≥ 20Vpp, Vp ≥ 5V with V^- = −15V. Another simple way to get 20Vpp with Vp = 7V, is to increase V^- to −17V. In fact using V^+ = +12V or +15V and setting V^- = −18V allows one to switch 20Vpp with any member of IH401 family. The advantage of using the Vp = 7V pinch-off (along with unsymmetrical supplies) over the Vp = 5V pinch-off (and ±15V supplies) is that you will have a much lower $R_{DS(ON)}$ resistance for the Vp = 7V fet.(i.e. for the 2N4391 fet $r_{DS(ON)} \approx 22\Omega$, $r_{DS(ON)} \approx 35\Omega$)
$V_p = 7V$ $V_p = 5V$

The IH6201 is a dual translator, each containing 4 CMOS FETs. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 2A.

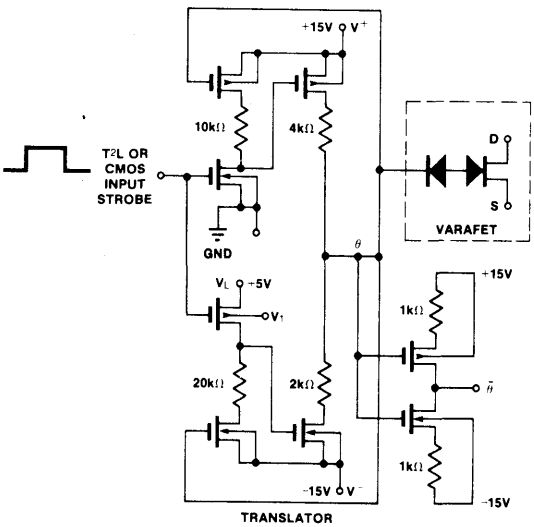
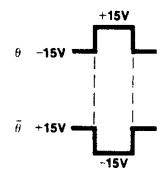


Figure 2A



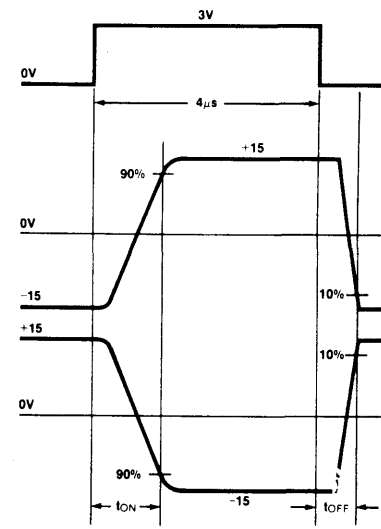
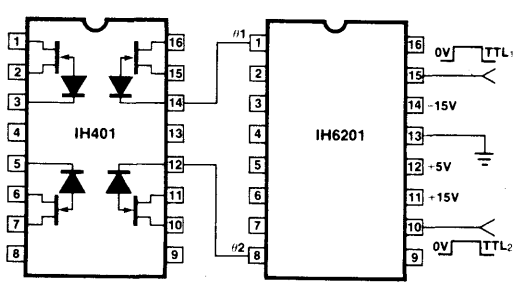


Figure 2B

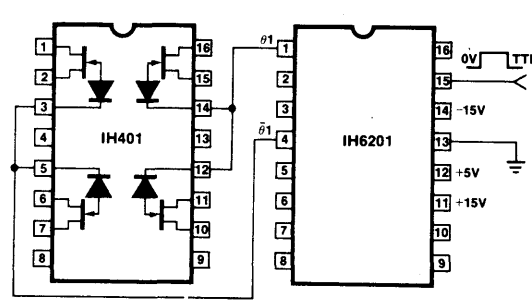
NOTE: Each translator output has a θ and $\bar{\theta}$ output. θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See III.)

I. Dual SPST Analog Switch



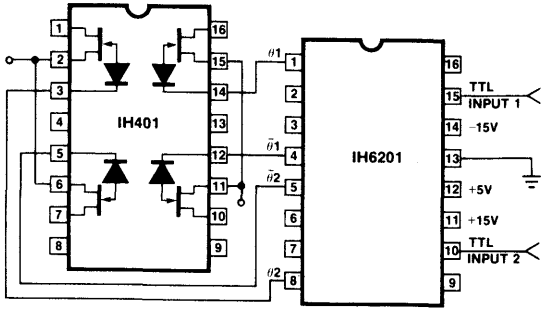
II. DPDT Analog Switch



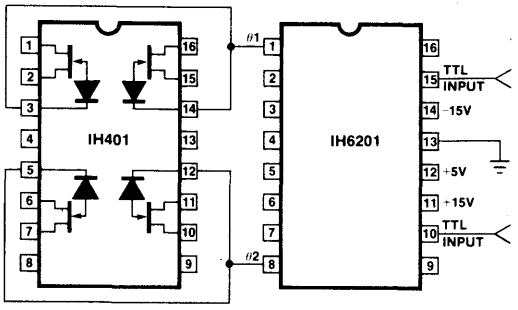
NOTE: Either switch is turned on when strobe input goes high.

APPLICATIONS, CONTINUED

III. Dual SPDT



IV. Dual DPST



3

IH6208

4-Channel Differential CMOS Analog Multiplexer

FEATURES

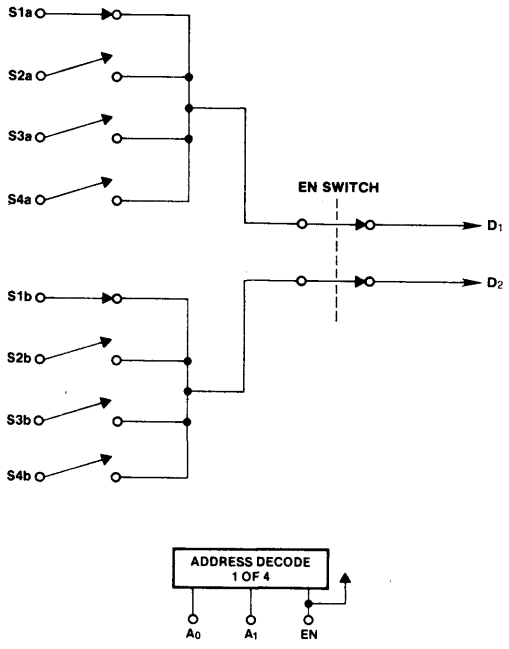
- **Ultra low leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)} < 400$ ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **$\pm$14V analog signal range**
- **No SCR latch up**
- **Break-before-make switching**
- **Binary Address control (2 Address inputs control 2 out of 8 channels)**
- **TTL and CMOS compatible Address control**
- **Pin compatible with HI509, DG509 & AD7509**

GENERAL DESCRIPTION

The IH6208 is a monolithic 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM



2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 5V (EN = "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

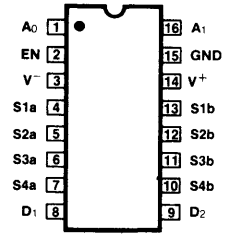
DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1

LOGIC "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
LOGIC "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6208MDE/CDE)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MJE	–55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temp (Soldering, 10 sec) ..... 300°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

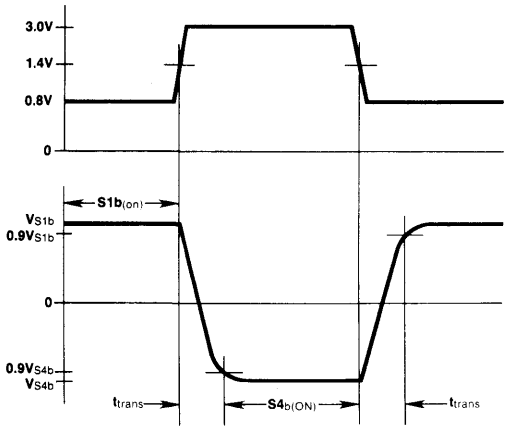
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

CHARACTERISTIC			MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	8	180	300	300	400	350	350	450	Ω	V_D = 10V, I_S = −1.0 mA	Sequence each switch on
				8	150	300	300	400	350	350	450		V_D = −10V, I_S = −1.0 mA	V_{AL} =0.8V, V_{AH} =2.4V
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$	$V_S = \pm 10V$
	$I_{S(OFF)}$		S	8	0.002		0.05	50		0.1	50	nA	V_S = 10V, V_D = −10V	V_{EN} = 0
				8	0.002		0.05	50		0.1	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$		D	2	0.03		0.1	50		0.2	100		V_D = 10V, V_S = −10V	
				2	0.03		0.1	50		0.2	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$		D	8	0.1		0.2	50		0.4	100		$V_{S(All)}$= V_D = 10V	Sequence each switch on
				8	0.1		0.2	50		0.4	100		$V_{S(All)}$ = V_D = −10V	V_{AL} =0.8V, V_{AH} =2.4V
INPUT	$I_{A(on)}$			2	.01		−10	−30		−10	−30	μA	V_A = 2.4V or 0V	
	$I_{A(off)}$			2	.01		10	30		10	30		V_A = 15V or 0V	
	I_A		A0, A1	2			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
			EN	1			−10	−30		−10	−30		V_{EN} = 0	(Address Pins)
DYNAMIC	t_{trans}		D		0.3		1					μs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{EN(on)}$		D		0.6		1.5						See Fig. 3	
	$t_{EN(off)}$		D		0.4		1							
	"OFF" Isolation		D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{s(off)}$		S		5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	$C_{d(off)}$		D		12								V_D = 0	
	$C_{ds(off)}$		D to S		1								V_S = 0, V_D = 0	
SUPPLY	Supply Current	+	V^+	1	40		200			1000		μA	V_{EN} = 5V	All V_A = 0 or 5V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			V_{EN} = 0	
		−	V^-	1	1		100			1000				

NOTE 1: See Section I Enable Input Strobing Levels.

SWITCHING INFORMATION



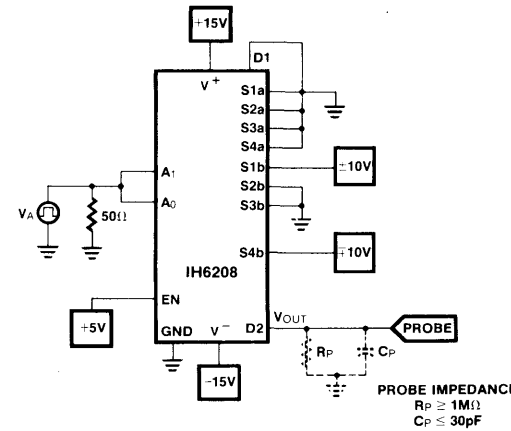


Figure 1. t_{trans} Switching Test

SWITCHING INFORMATION (Continued)

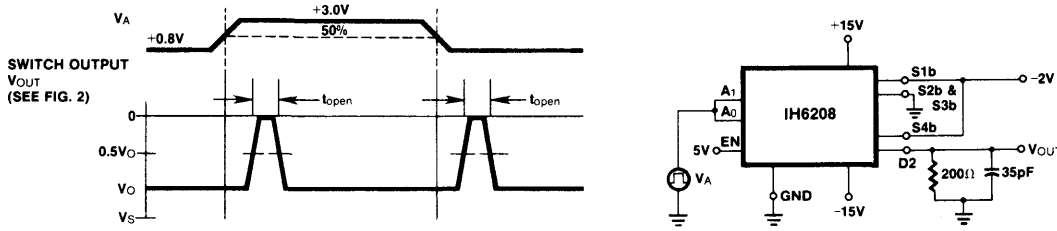


Figure 2. t_{open} Break-Before-Make Switching Test

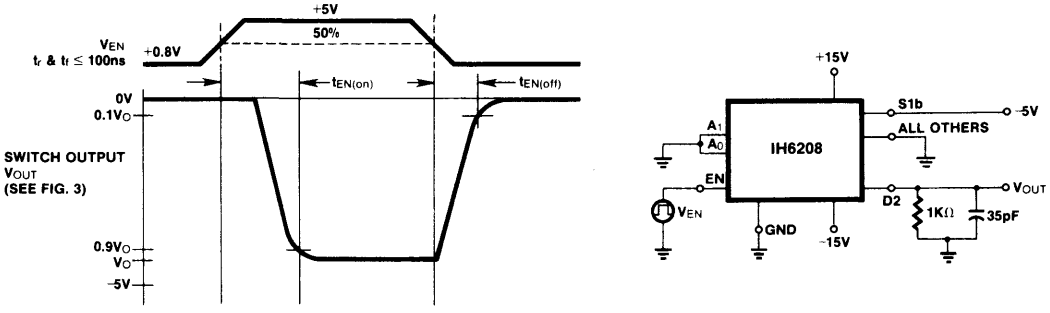


Figure 3. t_{on} and t_{off} Switching Test

IH6208 APPLICATION INFORMATION

I. ENable Input Strobing Levels

The ENable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 4).

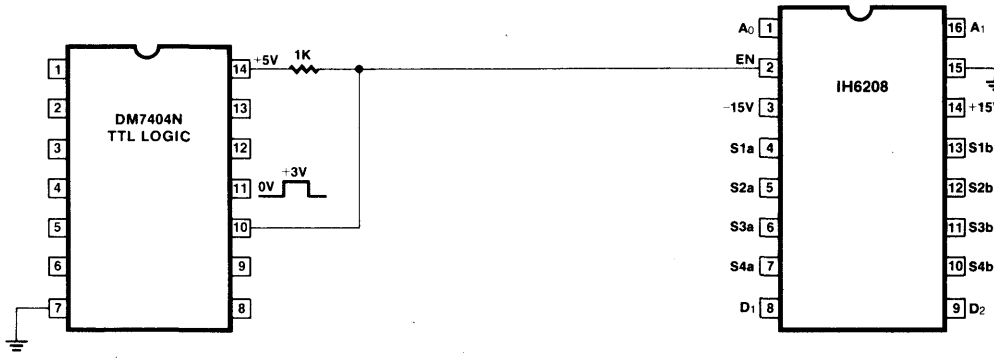


Figure 4. ENable Input Strobing from TTL Logic

IH6208 APPLICATION INFORMATION (Continued)

When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 5)

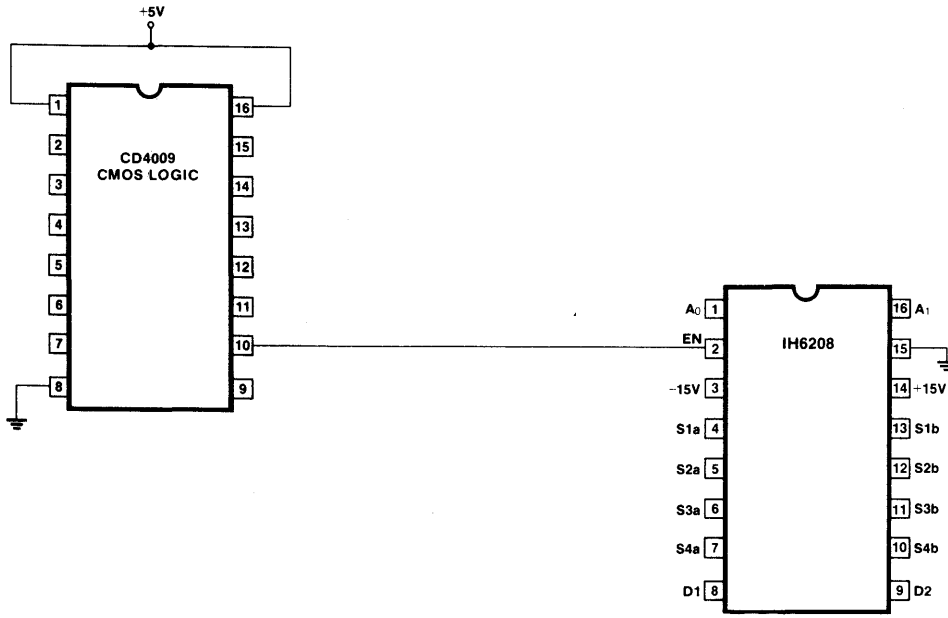


Figure 5. CMOS Logic Driving ENable Pin.

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 4 and 5 deal with ENable strobing when expansion to more than four differential channels is required; in these cases the EN terminal acts as a third address input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

IH6208 APPLICATION INFORMATION (Continued)

II. Using the IH6208 with supplies other than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 14) via a silicon diode as shown in Figure 6. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V, which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN (See Figure 7). A 1μF capacitor can be placed across the diode to minimize switching glitches.

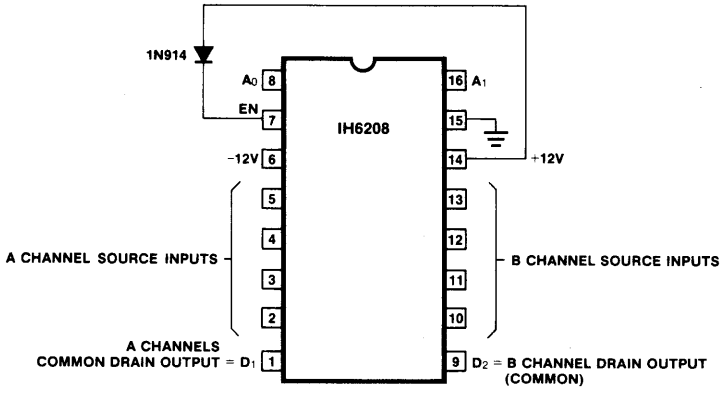


Figure 6. IH6208 Connection Diagram for less than ±15V Supply Operation.

IH6208 APPLICATION INFORMATION (Continued)

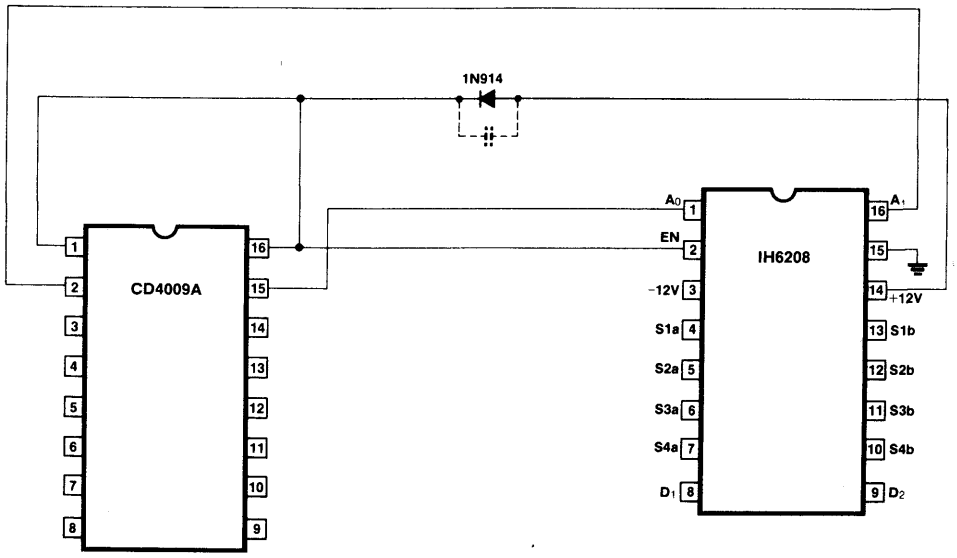


Figure 7. IH6208 Connection Diagram with ENable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

IH6216

8-Channel Differential CMOS Analog Multiplexer

FEATURES

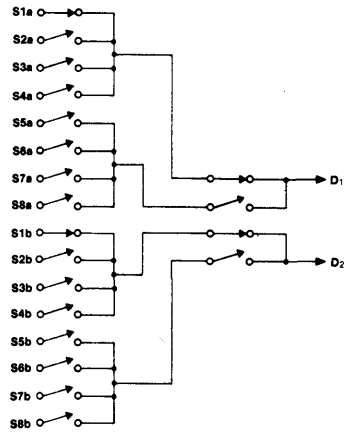
- **Pin compatible with HI507, DG507 & AD7507**
- **±11V analog signal range**
- **$r_{DS(on)}$ < 700 ohms over full signal and temperature range**
- **Break-before-make switching**
- **TTL and CMOS compatible Address control**
- **Binary Address control (3 Address inputs control 2 out of 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latch up**
- **Very low leakage $I_{D(off)} \leq$ 100pA**

GENERAL DESCRIPTION

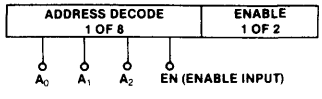
The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V) all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

3

FUNCTIONAL DIAGRAM



TO DECODE LOGIC CONTROLLING BOTH TIERS OF MUXING



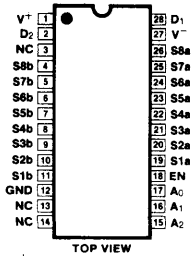
3 LINE BINARY ADDRESS INPUTS
(0 0 0) AND EN = 5V
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = V_{AH} > 3V V_{ENH} > 4.5V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION



TOP VIEW
V^+ COMMON TO SUBSTRATE

ORDERING INFORMATION

Ceramic package available as special order only (IH6216MDI/CDI)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6216MJI	−55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V^+ ..... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA

Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Power Dissipation (Package)* 1200mW
Lead Temperature (Soldering 10 sec) ..... 300 °C

*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C

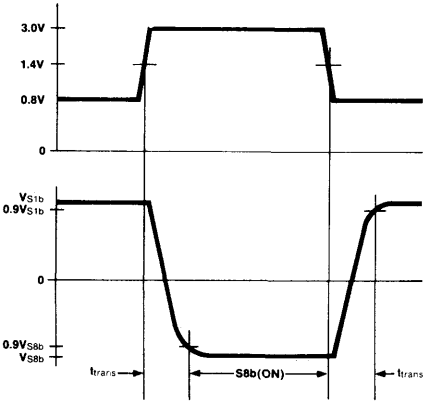
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

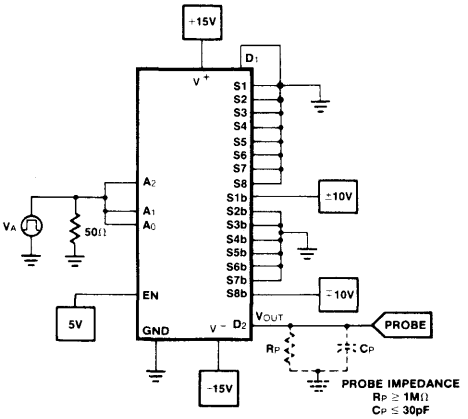
ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$		S to D	16	480	600	600	700	650	650	750	Ω	V_D = 10V, I_S = −10mA	Sequence each switch on
				16	300	600	600	700	650	650	750		V_D = −10V, I_S = 10mA	V_{AL} =0.8V, V_{AH} =3V
	$\Delta r_{DS(ON)}$				20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ V_S = ±10V	
	$I_{S(OFF)}$		S	16	0.01		0.1	50		0.2	50	nA	V_S = 10V, V_D = −10V	V_{EN} = 0
				16	0.01		0.1	50		0.2	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$		D	2	0.1		0.2	100		0.4	100		V_D = 10V, V_S = −10V	
				2	0.1		0.2	100		0.4	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$		D	16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
				16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	V_{AL} =0.8V, V_{AH} =3V
INPUT	$I_{A(on)}$ or $I_{A(off)}$			3	.01		−10	−30		−10	−30	μA	V_A = 3.0V	
				3	.01		10	30		10	30		V_A = 15V	
	I_A		A_0 A_1 A_2 A_3	3			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
			EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	t_{trans}		D		0.6		1					μs	See Fig. 1	
	t_{open}		D		0.2								See Fig. 2	
	$t_{on(EN)}$		D		0.8		1.5						See Fig. 3	
	$t_{off(EN)}$		D		0.3		1							
	"OFF" Isolation		D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	C_s		S		5							pF	V_S = 0	
	$C_{d(off)}$		D		20								V_D = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	C_{ds}		D to S		1								V_S = 0, V_D = 0	
SUPPLY	Supply Current	+	V^+	1	55		200			1000		μA	V_{EN} = 5V	All V_A = 0 or 3V
		−	V^-	1	2		100			1000				
	Standby Current	+	V^+	1	1		100			1000			V_{EN} = 0	
		−	V^-	1	1		100			1000				

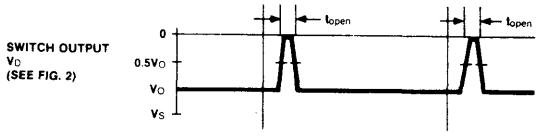
NOTE 1: See Section V. Enable Input Strobing Levels.

SWITCHING INFORMATION





SWITCHING INFORMATION (Continued)



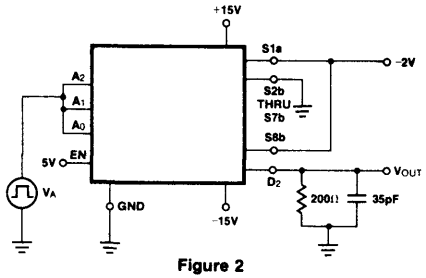
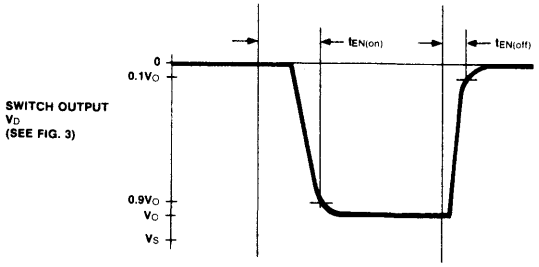


Figure 2



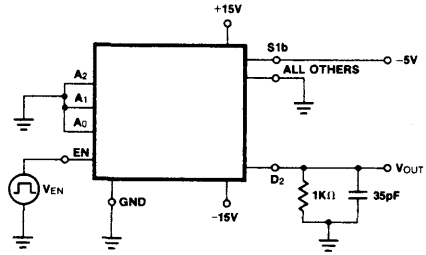
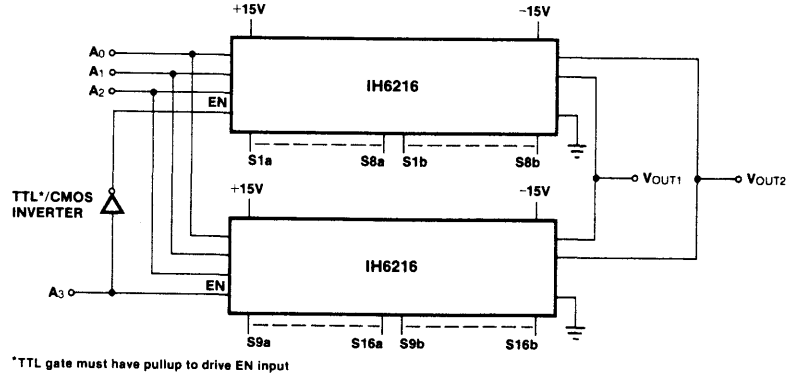


Figure 3

IH6216 APPLICATIONS

I. 2 out of 32 channel multiplexer using 2 IH6216s



*TTL gate must have pullup to drive EN input

Figure 4

DECODE TRUTH TABLE

A3	A2	A1	A0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	VOUT1
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A3	A2	A1	A0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	VOUT2
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS (Continued)

II. 2 out of 32 channel multiplexer using 2 IH6216s; with an IH5043 for submultiplexing

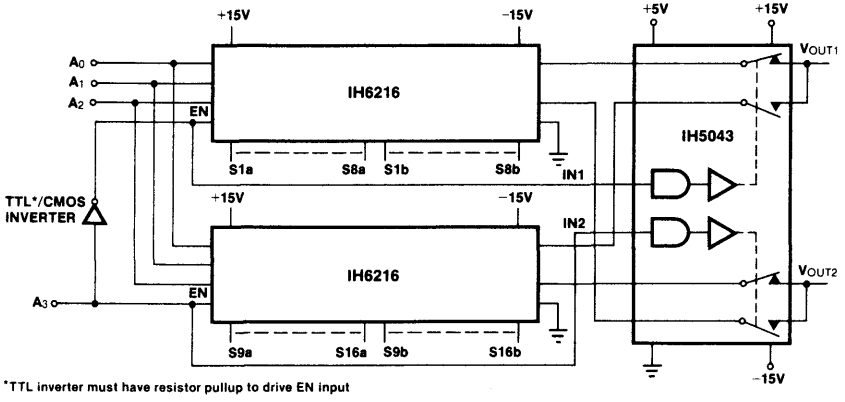


Figure 5

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS

III. 2 out of 64 multiplexer using 4 IH6216s and 2 IH5043s as submultiplexers

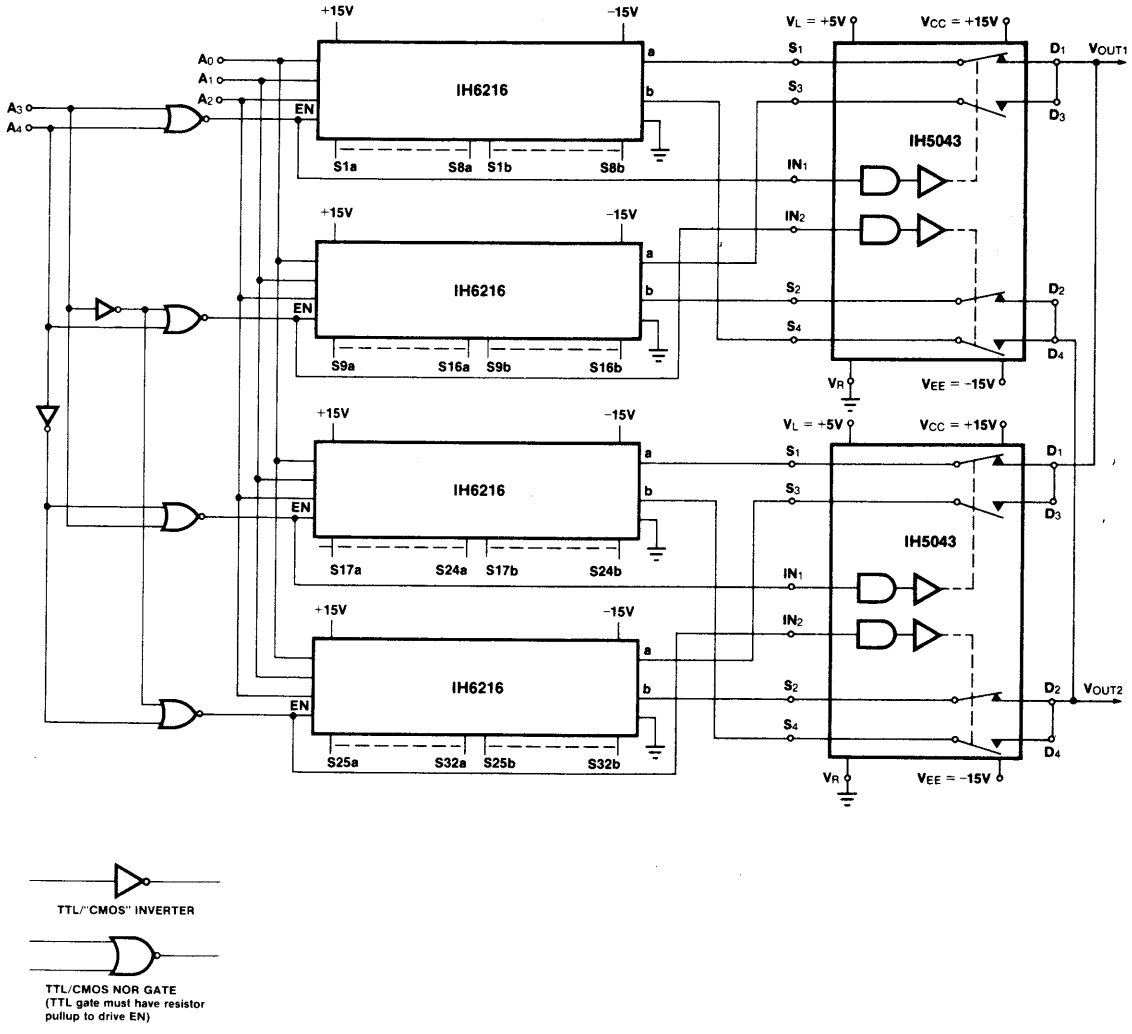


Figure 6

IV. General note on expandability of IH6216

The IH6216 is a two tier multiplexer where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacity and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6216 is expanded.

Figure 4 shows a 2 of 32 multiplexer using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the ENable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4 nA at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}, with thruput channel resistance in the 500Ω area.

Figure 5 shows the 2 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2 nA.

Figure 6 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5043 is used for the third tier of MUXing. Each V_{out} point will see 3 OFF channels and 1 ON channel at any time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550Ω area and thruput switching speeds will be about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

V. Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of 1kΩ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6208 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

Data Acquisition

A/D Converters/ DVM Circuits

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†ICL7126	4-67
ICL7129	4-75
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ICL8068/7104	4-166

D/A Converters

ICL7134	4-86
ICL7145	4-124
ICL7146	4-132
AD7520/21/30/31	4-138
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D/A Current Switches

ICL8018A/19A/20A	4-158

†The ICL7136 is recommended for all applications which currently employ the ICL7126.

Integrating Analog-to-Digital Converters for Display

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	ICL7136	ICL7137	ICL7135	ICL7129	ICL7106/ICL7116	ICL7107/ICL7117
Resolution	±3½ Digit	±3½ Digit	±4½ Digit	±4½ Digit	±3½ Digit	±3½ Digit
Accuracy						
Non-Linearity	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Zero Input Reading	±0.000	±0.000	±0.000	±0.000	±0.000	±0.000
Ratiometric Reading	±1.000	±1.000	±1.000	±0.9997	±1.000	±1.000
$V_{IN} = V_{REF}$	±1 Count	±1 Count	±1 Count	±3 Counts	±1 Count	±1 Count
Rollover Error	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Stability						
Offset vs. Temperature	1μV/°C	1μV/°C	1μV/°C	1μV/°C	1μV/°C	1μV/°C
Gain vs. Temperature	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C
Conversion Time	0.1 to 3 conv/sec	0.1 to 3 conv/sec	0.1 to 15 conv/sec	0.1 to 6 conv/sec	0.1 to 15 conv/sec	0.1 to 15 conv/sec
Analog Input						
Voltage Range	±200mV to ±2V	±200mV to ±2V	±2V	±200mV to ±2V	±200mV to ±2V	±200mV to ±2V
Impedance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$
Leakage Current	2pA	2pA	3pA	1pA	2pA	3pA
Noise (peak-to-peak)	15μV typ.	15μV typ.	15μV typ.	7μV typ.	15μV typ.	15μV typ.
Digital Input	—	—	—	Decimal Points Continuity Hold, Range Select	Display Hold (7116)	Display Hold (7117)
Digital Outputs						
Format	Direct 7 Segment LCD Display	Direct 7 Segment LCD Display	Multiplex BCD	4½ Digit Triplexed LCD Display Drive w/Decimal Points, Low Battery and Continuity Indicators	Direct 7 Segment LCD Display	Direct 7 Segment LED Display
Logic Level	AC:4.5V Down from V+	AC:4.5V Down from V+	TTL/CMOS		AC:4.5V Down from V+	Comm Anode DTL/TTL/CMOS
Power Supply						
Voltage	+9V	±5V	±5V	+9V	+9V	±5V
Current	100μA	200μA	1.8mA	1.8mA	1.8mA	1.8mA
Package	40 pin DIP	40 pin DIP	28 pin DIP	40 pin DIP	40 pin DIP	40 pin DIP

*Also available LD110/111/114 (not recommended for new designs), and ICL7126 (recommended use ICL7136).

Integrating Analog-to-Digital Converters for Data Acquisition

Type	Single Chip	Two Chip System***	
Model	**ICL7109**	**ICL8052A/8068 ICL7104-14**	**ICL8052A/8068 ICL7104-16**
Resolution	±12-Bit Binary	±14-Bit	±16-Bit
Accuracy	±1 Count	±1 Count	±1 Count
Microprocessor Compatible	Yes	Yes	Yes
Output	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 bit bytes	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 Bit Byte for ICL7104-12/14 3-8 Bit Byte for ICL7104-16	
Control Lines	Run/Hold, Busy, Byte Enables, Mode, Load, Send Enable, Out of Range		
Conversion Time	10ms	80ms	330ms
UART Compatible	Yes	Yes	Yes
Noise (Typical)	15μV	2μV (8068)	2μV (8068)
Input Current	10pA	30pA (8052)	30pA (8052)
Input Voltage Range	+400mV to +4.1V	+100mV to +10V	−200mV to −10V

***ICL8052/8068 and ICL8053 can be combined as analog portion of dual-slope A/D converter under μp control. See ICL8052/8068 and ICL 7104-16 for performance characteristics.

Digital-to-Analog Converters*

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	ICL7134U/B	7145	7146	AD7523	AD7533	AD7520 (7530)	AD7520 (7531)	AD7541
Resolution	14 bit	16 bit	12 bit	8 bit	10 bit	10 bit	12 bit	12 bit
Accuracy	J/K/L	J/K	J/K	J/K/L	J/K/L	J/K/L	J/K/L	J/K/L
Linearity	0.01/0.006/0.003%	0.006/0.003%	0.01%	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.02%/0.01%/0.05%	0.2%/0.1%/0.5%	0.02%/0.01%/0.01%
Zero Offset	10 nA	10 mV	120 μV	50 μA	200 nA	200 nA (300 nA)	200 nA (300 nA)	50 nA
Full Scale Reading	0.003%	0.04/0.02% FSR	0.04/0.02% FSR	1.5% max	1.4%	0.3% typ	0.3% typ	0.3%
Stability								
Gain vs. Temperature	5 ppm/°C	1 ppm/°C typ	5 ppm/°C typ	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C
Linearity vs. Temperature	1 ppm/°C	1 ppm/°C typ	1 ppm/°C typ	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C
Setting Time To 1/2 LSB	0.9 μs typ	3 μs	10 μ	150 ns	600 ns typ	500 ns typ	500 ns typ	~1 μs
Input Code	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS
Logic Compatibility option	Binary (U) 2's Complement (B)	2's Complement	Binary or 2's Complement	Binary Offset Binary	Binary Offset Binary	Binary Offset Binary	Binary Offset Binary	Binary Offset Binary
Power Supply								
Voltage	+3.5 to +6.0V	4.5 to 5.5V	±4.5 to 5.5V	+6 to +16V	+5 to +15V	+5 to +15V	+5 to +15V	+5 to +16V
Current	2mA	1.2mA	5mA	100 μA	2mA	2mA	2mA	2mA
Package	28 pin DIP	28 pin DIP	28 pin DIP	16 pin DIP	16 pin DIP	16 pin DIP	18 pin DIP	18 pin DIP

*R2R Ladder Multiplying Type

Successive Approximation Analog-to-Digital Converters

Model	ADC0801-4	ICL7115
Resolution	8 bit	14 bit binary
Accuracy	± ¼/½/½/1 LSB	± ½ LSB
Microprocessor Compatible	Yes	Yes
Output	Programmable: 1. Latched parallel 3' state Binary	Programmable: 1. Two latched bytes
	2. One 8 bit byte	2. 15 bit parallel
Control Lines	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, BUS
Conversion Time	100μs	40μs
UART Compatible	Yes	No
Input Voltage Range	5V span	0 - 5V

Quad Current Switches ICL8018/8019/8020

High speed precision current switches for use in current summing D/A converters. Can be purchased individually or in matched sets with accuracies of 0.01% (ICL8018), 0.1% (ICL8019), or 1.0% (ICL8020)

Sample and Hold

Type	V_{analog} (V_{p-p})	t_{acq}** (μs)	V_{inject}** (mV)	V_{os} (mV)	Drift Rate (mV/sec)
IH5110	±7.5	6	5	40	5
IH5111	±10	6	5	40	5
IH5112	±7.5	6	5	10	5
IH5113	±10	6	5	10	5
IH5114	±7.5	6	5	5	5
IH5115	±10	6	5	5	5

**C_{STO} = 0.01 μF

Monolithic Voltage Converter—The ICL7660

Converts positive voltage into negative over a range of + 1.5V through + 10V. May be cascaded for higher negative output voltages, paralleled for greater output current, used as a positive voltage multiplier, or any combination of the above. Typical supply current is 170 μA, and output source resistance is 55Ω at T_A = 25°C and I_O = 20 mA

ADC0801–ADC0804

8-Bit Microprocessor Compatible A/D Converters

FEATURES

- MCS-48 and MCS-80/85 bus compatible–no interfacing logic required
- Conversion time < 100μs
- Easy interface to all microprocessors
- Will operate "stand alone"
- Differential analog voltage inputs
- Works with bandgap voltage references
- TTL compatible inputs and outputs
- On-chip clock generator
- 0V to 5V analog voltage input range (single +5V supply)
- No zero-adjust required

4

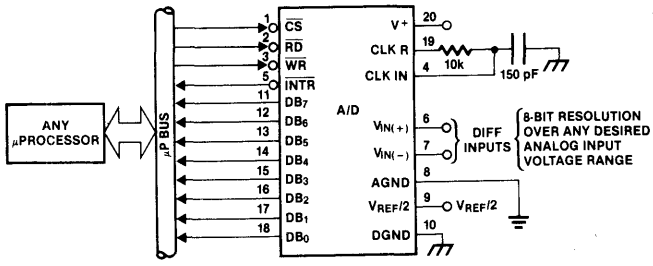
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing logic is required.

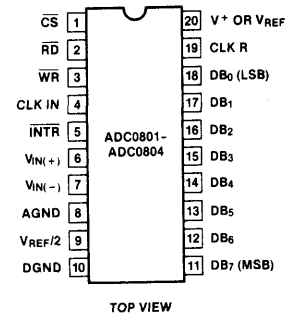
The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0801 family is available in the industry standard 20 pin CERDIP package.

TYPICAL APPLICATION



PIN CONFIGURATION



TOP VIEW

(Outline dwg. JP)

ORDERING INFORMATION

PART	ERROR	TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
ADC0801	± 1/4 bit adjusted full-scale	0°C to +70°C	20 pin CERDIP	ADC0801LCN
		−40°C to +85°C	20 pin CERDIP	ADC0801LCD
		−55°C to +125°C	20 pin CERDIP	ADC0801LD
ADC0802	± 1/2 bit no adjust	0°C to +70°C	20 pin CERDIP	ADC0802LCN
		−40°C to +85°C	20 pin CERDIP	ADC0802LCD
		−55°C to +125°C	20 pin CERDIP	ADC0802LD
ADC0803	± 1/2 bit adjusted full-scale	0°C to +70°C	20 pin CERDIP	ADC0803LCN
		−40°C to +85°C	20 pin CERDIP	ADC0803LCD
		−55°C to +125°C	20 pin CERDIP	ADC0803LD
ADC0804	± 1 bit no adjust	0°C to +70°C	20 pin CERDIP	ADC0804LCN
		−40°C to +85°C	20 pin CERDIP	ADC0804LCD

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Voltage at Any Input . . . . . −0.3V to (V+ + 0.3V)
Storage Temperature Range . . . . . −65°C to +150°C
Package Dissipation at T_A = +25°C . . . . . 875 mW
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

OPERATING RATINGS

Temperature Range
ADC0801/02/03LD . . . . . −55°C to +125°C
ADC0801/02/03/04LCD . . . . . −40°C to +85°C
ADC0801/02/03/04LCN . . . . . 0°C to +70°C
Supply Voltage Range . . . . . 4.5V to 6.3V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYSTEM ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640kHz$ unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC0801: Total Adjusted Error	With Full Scale Adjust			±1/4	LSB
ADC0802: Total Unadjusted Error	Completely Unadjusted			±1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND − 0.05		V^+ + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		±1/16	±1/8	LSB

AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25°C$ unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLK}	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100 100	640 640	1280 800	kHz kHz
Clock Periods per Conversion (Note 4)	t_{conv}		66		73	
Conversion Rate In Free-Running Mode	CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, f_{CLK} = 640kHz			8888	conv/s
Width of $\overline{WR}$ Input (Start Pulse Width)	$t_{W(\overline{WR})l}$	$\overline{CS}$ = 0V (Note 5)	100			ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	t_{acc}	C_L = 100pF (Use Bus Driver IC for Larger C_L)		135	200	ns
3-State Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	t_{1h}, t_{0h}	C_L = 10 pF, R_L = 10k (See **3-State Test Circuits**)		125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$	t_{WI}, t_{RI}			300	450	ns
Input Capacitance of Logic Control Inputs	C_{IN}			5	7.5	pF
3-State Output Capacitance (Data Buffers)	C_{OUT}			5	7.5	pF

4

DC ELECTRICAL CHARACTERISTICS

Digital Levels and DC Specifications: $V^+ = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL INPUTS (Note 6)						
Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{INH}	$V^+ = 5.25V$	2.0		V^+	V
Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{INL}	$V^+ = 4.75V$			0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage	V_{CLK}^+		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage	V_{CLK}^-		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis $(V_{CLK}^+) - (V_{CLK}^-)$	V_H		0.6	1.3	2.0	V
Logical "1" Input Current (All Inputs)	I_{INHI}	$V_{IN} = 5V$		0.005	1	μA
Logical "0" Input Current (All Inputs)	I_{INLO}	$V_{IN} = 0V$	−1	−0.005		μA
Supply Current (Includes Ladder Current)	I^+	$f_{CLK} = 640kHz$, $T_A = +25°C$ and $\overline{CS}$ = HI		1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$						
Logical "0" Output Voltage	V_{OL}	$I_O = 1.6mA$, $V^+ = 4.75V$			0.4	V
Logical "1" Output Voltage	V_{OH}	$I_O = -360\mu A$, $V^+ = 4.75V$	2.4			V
3-State Disabled Output Leakage (All Data Buffers)	I_{LO}	$V_{OUT} = 0V$	−3			μA
		$V_{OUT} = 5V$			3	μA
Output Short Circuit Current		$T_A = +25°C$				
	I_{SOURCE}	V_{OUT} Short to Gnd	4.5	6		mA
	I_{SINK}	V_{OUT} Short to V^+	9.0	16		mA

Note 1: All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

Note 2: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.

Note 3: With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.

Note 4: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

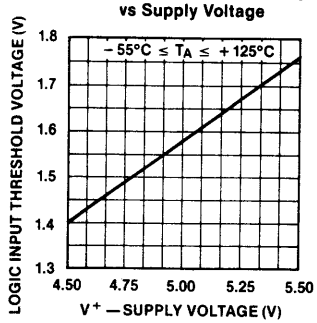
Note 5: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see **Timing Diagrams**).

Note 6: CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.

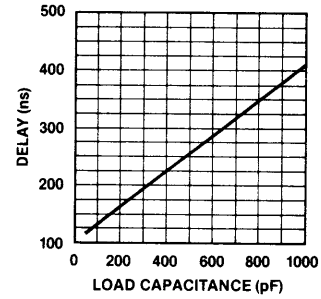
Note 7: None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See **Zero Error** below.

TYPICAL PERFORMANCE CHARACTERISTICS

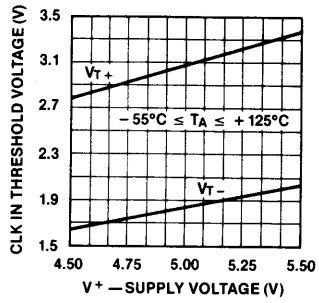
Logic Input Threshold Voltage vs Supply Voltage



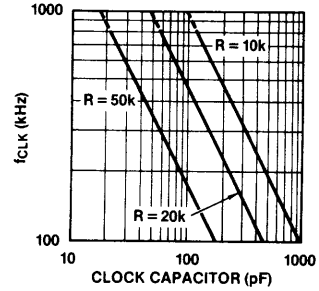
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



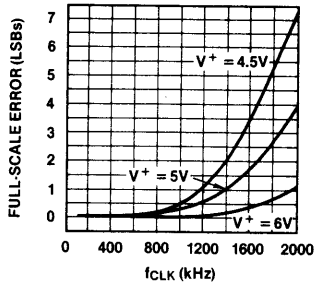
CLK IN Schmitt Trip Levels vs Supply Voltage



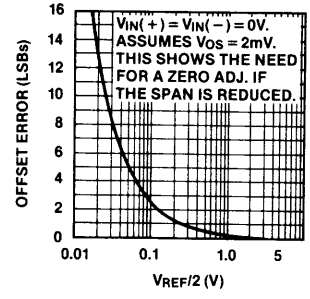
f_{CLK} vs Clock Capacitor



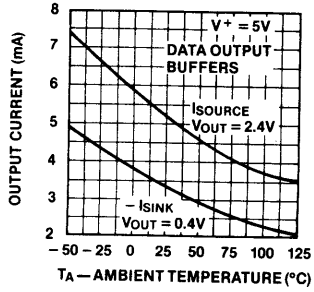
Full-Scale Error vs f_{CLK}



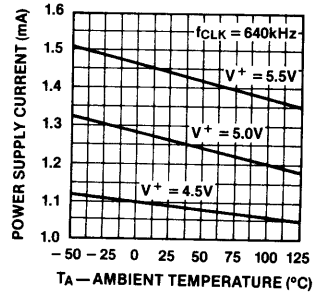
Effect of Unadjusted Offset Error



Output Current vs Temperature vs $V_{REF}/2$ Voltage

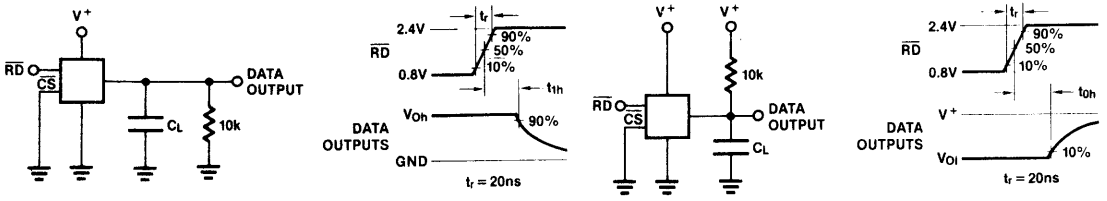


Power Supply Current vs Temperature



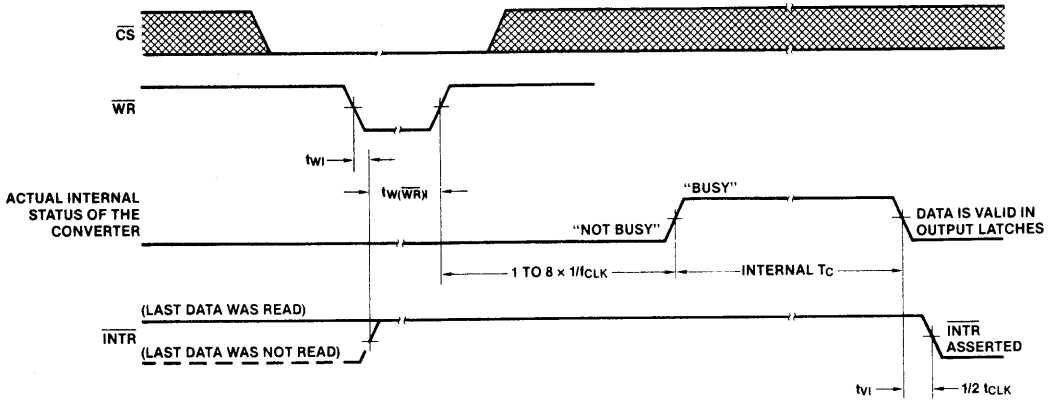
3-STATE TEST CIRCUITS AND WAVEFORMS

t_{1h} t_{1h}, $C_L = 10pF$ t_{0h} t_{0h}, $C_L = 10pF$

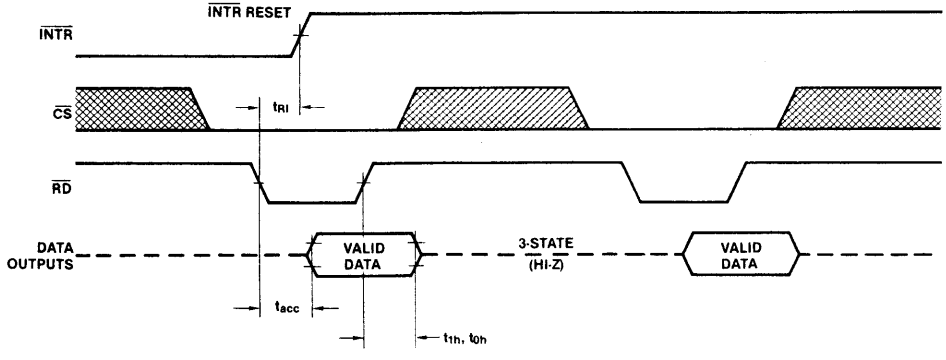


TIMING DIAGRAMS

Start Conversion



Output Enable and Reset $\overline{INTR}$



Note: All timing is measured from the 50% voltage points.

UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 1a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D – 1, D, and D + 1. For the perfect A/D, not only will center-value (A – 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows the worst case transfer function for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±1/4 LSB.

In other words, if we apply an analog input equal to the center-value ±1/4 LSB, the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

The error curve of Figure 1c shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 1a is +1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

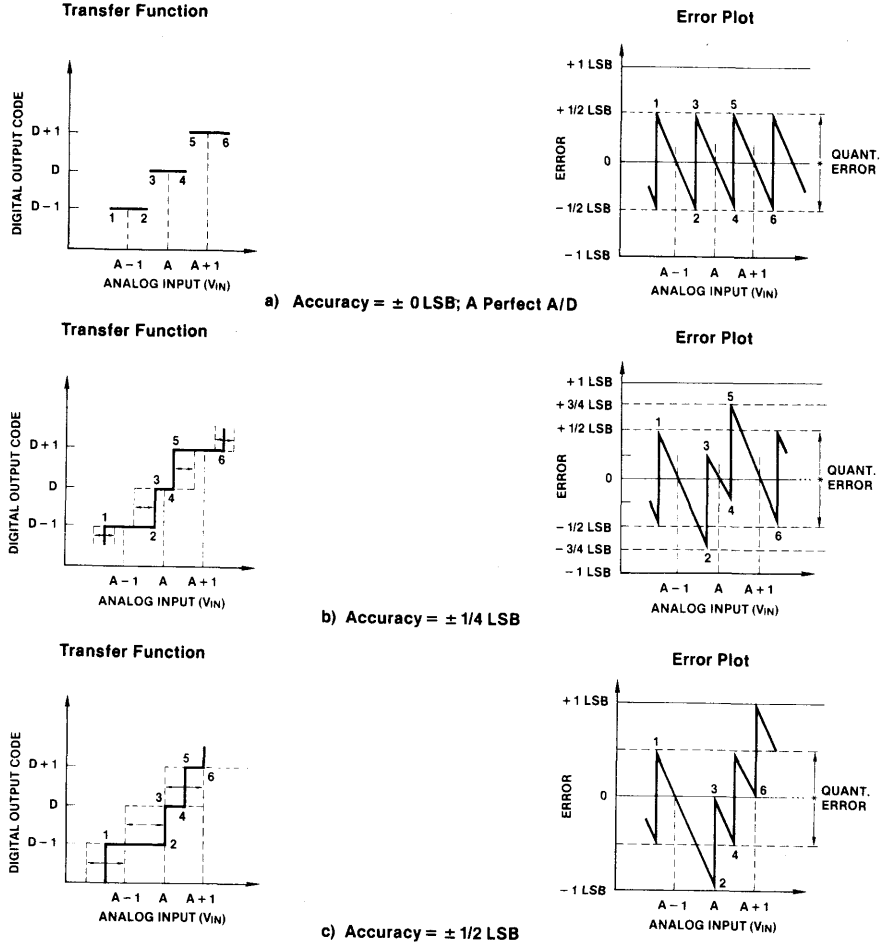


Figure 1. Clarifying the Error Specs of an A/D Converter

FUNCTIONAL DESCRIPTION

A functional diagram of the ADC0801 series of A/D converters is shown in Figure 2. All of the package pinouts are shown and the major logic control paths are drawn in heavier-weight lines. The device operates on the successive approximation principle (see A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the $\overline{WR}$ input, the internal SAR latches and the shift-register stages are reset, and the $\overline{INTR}$ output will be set high. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.* After the requisite number of clock pulses to complete the conversion, the $\overline{INTR}$ pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A $\overline{RD}$ operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line high again. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

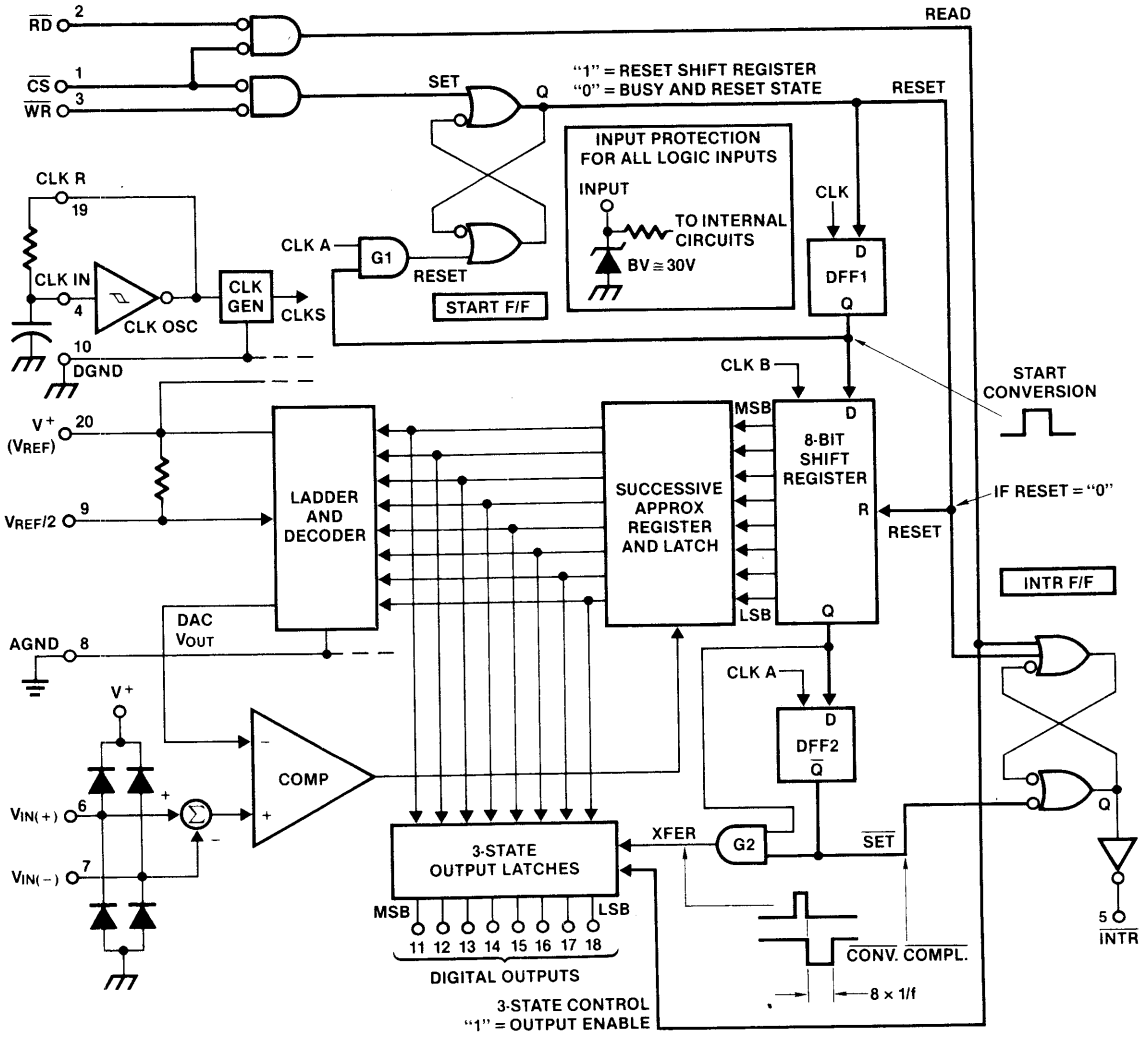


Figure 2. Block Diagram of ADC0801-ADC0804

Digital Details

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide $\overline{CS}$ and $\overline{WR}$ signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the $\overline{WR}$ input (pin 3). The Output Enable function is achieved by an active low pulse at the $\overline{RD}$ input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by 1/2 LSB (see Figure 1a).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA-20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)\ (2\pi f_{cm}) \left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 640kHz A/D clock, f_{CLK}, keeping this error to 1/4 LSB (~5mV) would allow a common-mode voltage, V_P, given by:

$$V_P = \frac{[\Delta V_e(MAX)(f_{CLK})]}{(2\pi f_{cm})\ (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\ (640 \times 10^3)}{(6.28)\ (60)\ (4.5)} \simeq 1.9V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see **Reference Voltage Span Adjust**).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not inherently cause errors* as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor ($\leq 1k\Omega$) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, ($\leq 1k\Omega$), a $0.1\mu F$ bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below $5k\Omega$. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see **Analog Input Current**). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see **Full-Scale Adjustment**) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 3.

Notice that the reference voltage for the IC is either 1/2 of the voltage which is applied to the V^+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V^+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to 1/2 of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 4. For expanded scale inputs, the circuits of Figures 5 and 6 can be used.

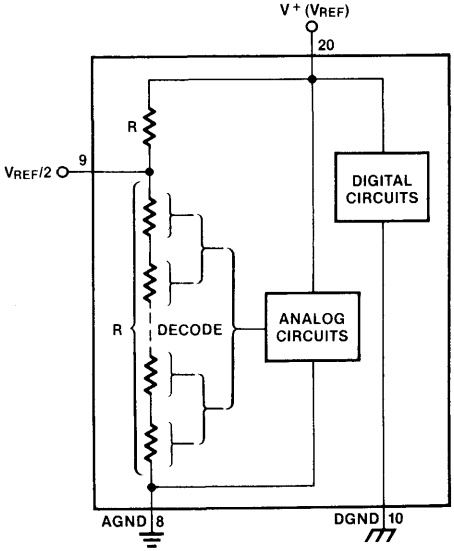


Figure 3. The $V_{REFERENCE}$ Design on the IC

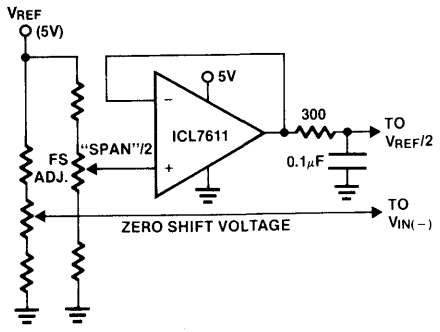


Figure 4. Offsetting the Zero of the ADC0801 and Performing an Input Range (Span) Adjustment

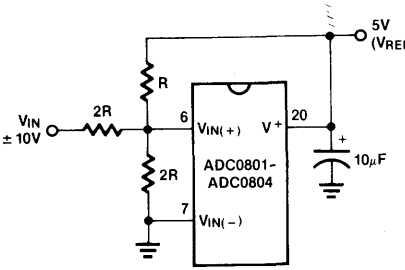


Figure 5. Handling ±10V Analog Input Range

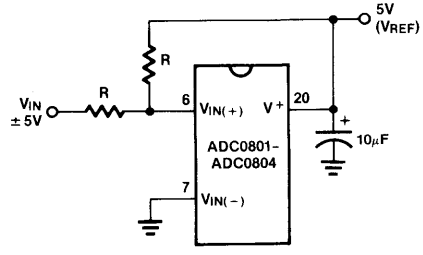


Figure 6. Handling ±5V Analog Input Range

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8mV for $V_{REF}/2 = 2.500V$).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}\,\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 7.

Heavy capacitive or DC loading of the CLocK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power T^2L buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard T^2L buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 8 for details.

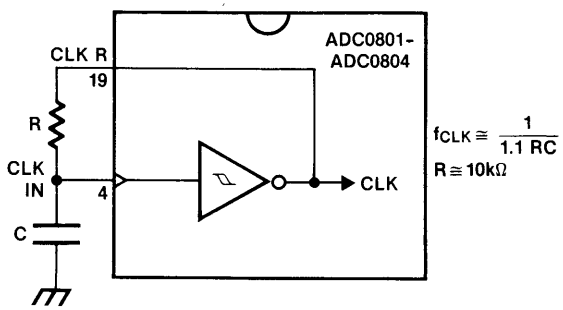


Figure 7. Self-Clocking the A/D

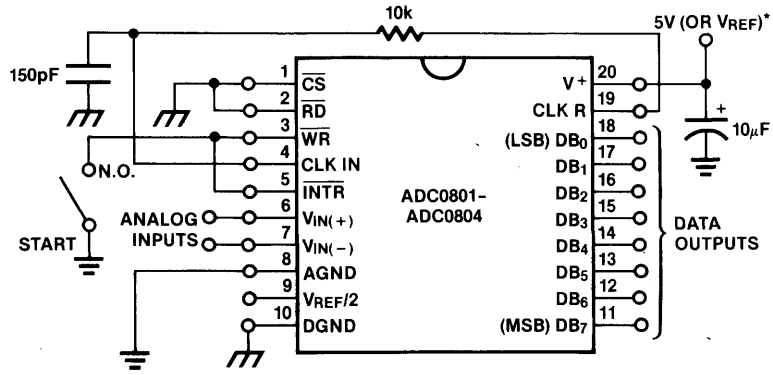


Figure 8. Free-Running Connection

4

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see **Typical Performance Characteristics**).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in A018.

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 9.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V (5.120 – 1½ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

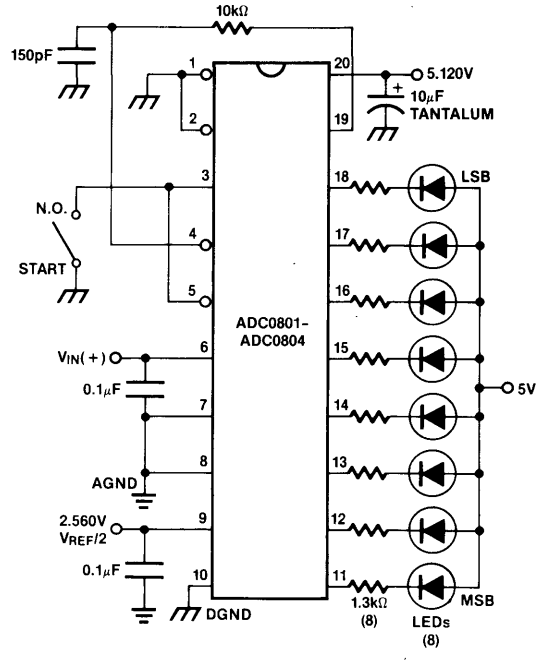


Figure 9. Basic Tester for the A/D

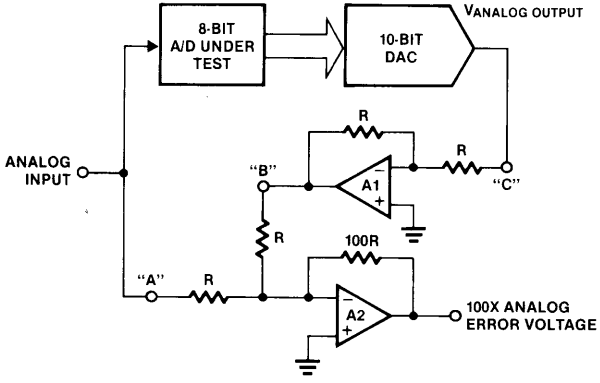


Figure 10. **A/D Tester with Analog Error Output.** This circuit can be used to generate "error plots" of Figure 1.

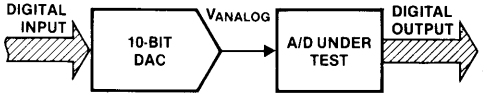


Figure 11. Basic "Digital" A/D Tester

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)\,V.$$

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

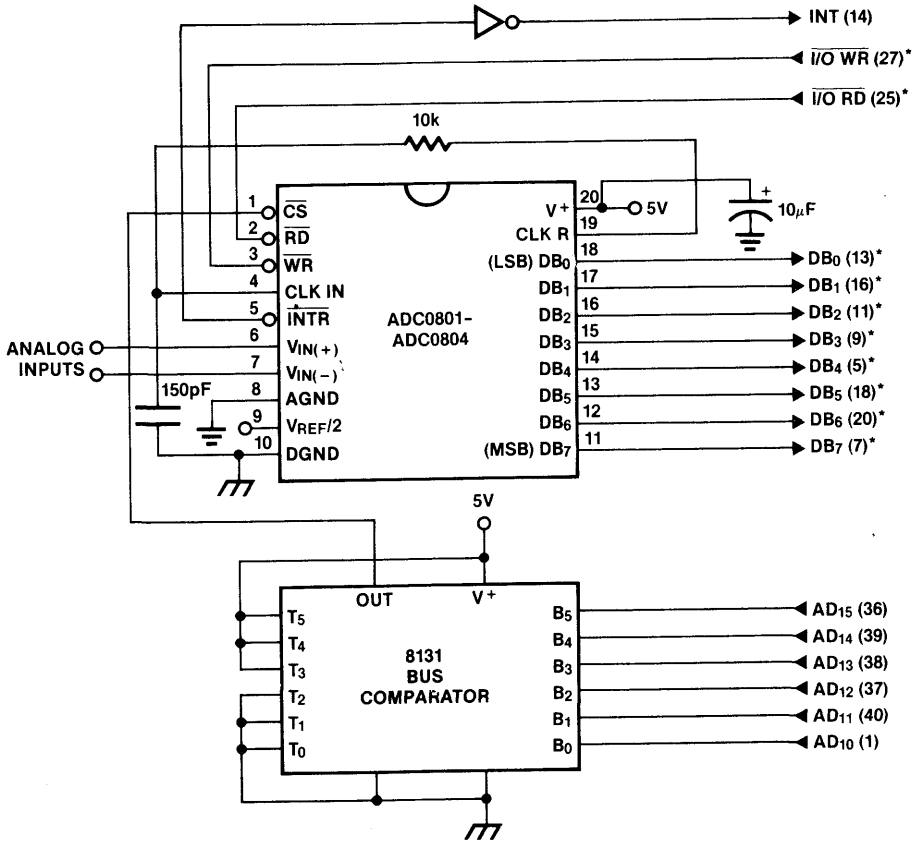
$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 10 and 11 show more sophisticated test circuits.

APPLICATIONS

Interfacing MCS-48, and MCS-80/85 Processors

This converter has been designed to directly interface with an MCS-80/85 microprocessor or system. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 12.



***Note:** Pin numbers for 8228 system controller: others are 8080A

Figure 12. ADC0801 to 8080A CPU Interface

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control busses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 13. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 13 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 14 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 15 the ADC0801 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

4

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters," by Dave Fullagar.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

A030 "The ICL7104—A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

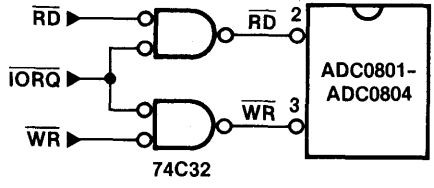
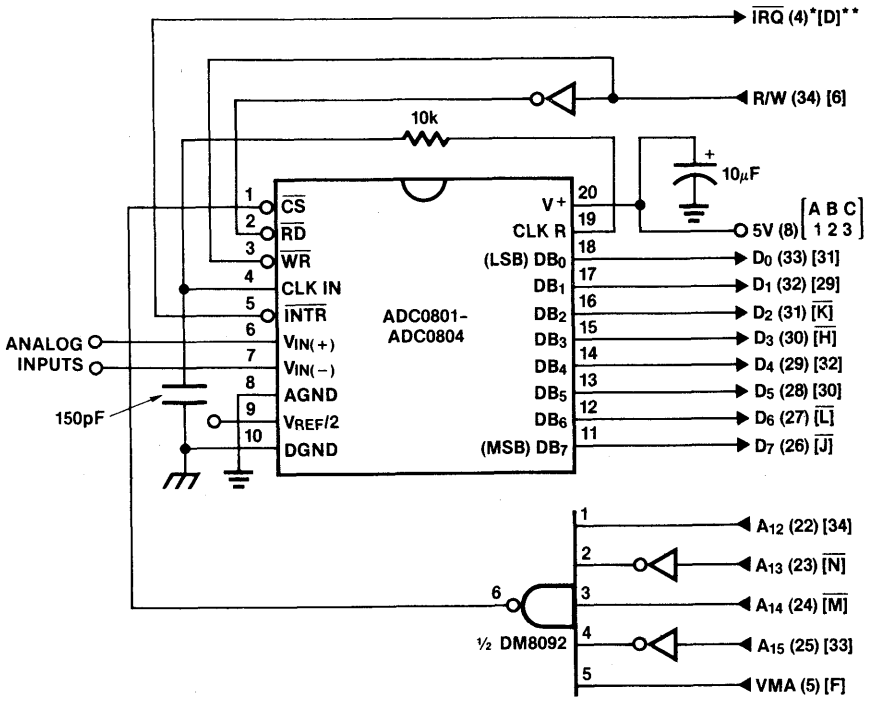


Figure 13. Mapping the A/D as an I/O device for use with the Z-80 CPU



*Note 1: Numbers in parentheses refer to MC6800 CPU pinout.
**Note 2: Numbers or letters in brackets refer to standard MC6800 system common bus code.

Figure 14. ADC0801 to MC6800 CPU Interface

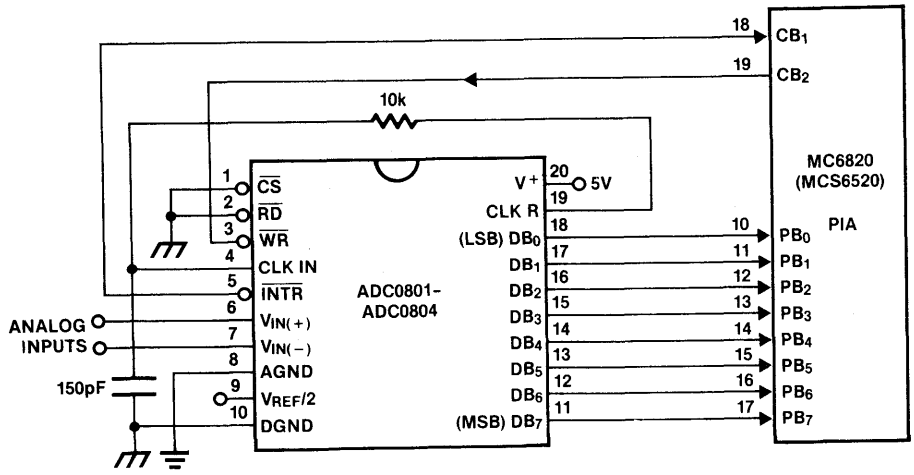
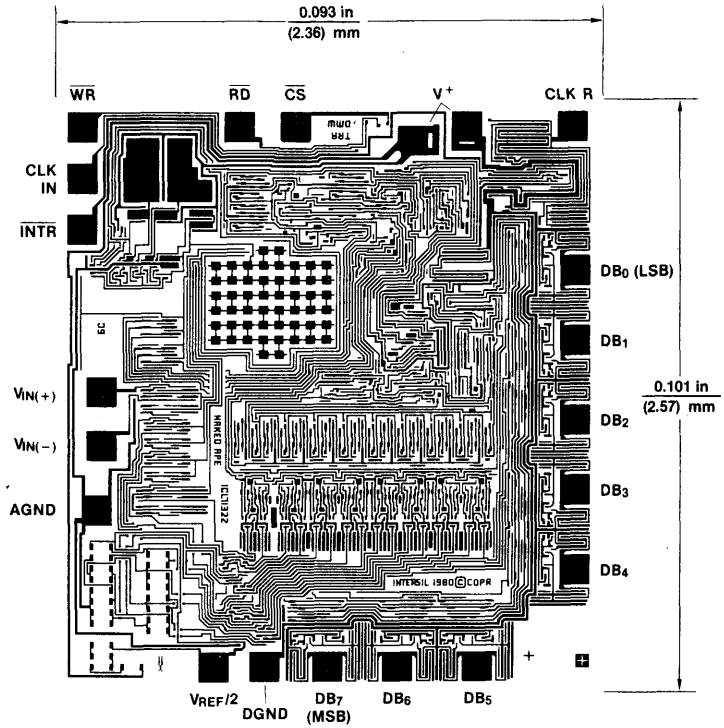


Figure 15. ADC0801 to MC6820 PIA Interface

CHIP TOPOGRAPHY



ICL7106/7107

3½-Digit Single Chip A/D Converter

FEATURES

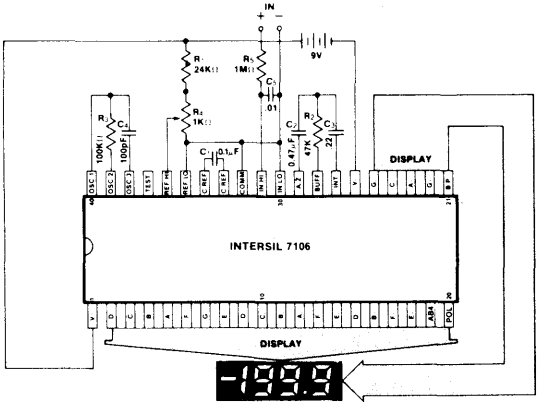
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA typical input current.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7106**
  — LED ICL7107
- **Low noise - less than 15μV p-p.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**
- **Evaluation Kit available.**

4

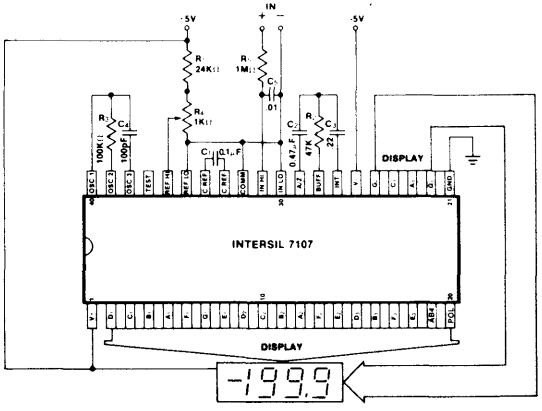
GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and roll-over error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.



ICL7106 with Liquid Crystal Display

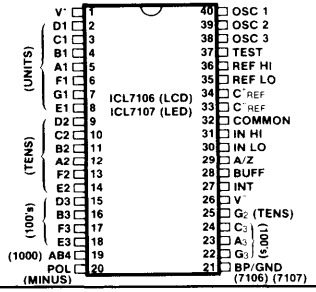


ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7106	40 pin CERDIP	0°C to +70°C	ICL7106CJL
7107	40 pin CERDIP	0°C to +70°C	ICL7107CJL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit 7107 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.		ICL7106EV/Kit ICL7107EV/Kit

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current | Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70° C		0.2	1	μV/° C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70° C (Ext. Ref. 0ppm/° C)		1	5	ppm/° C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/° C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25° C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

TEST CIRCUITS

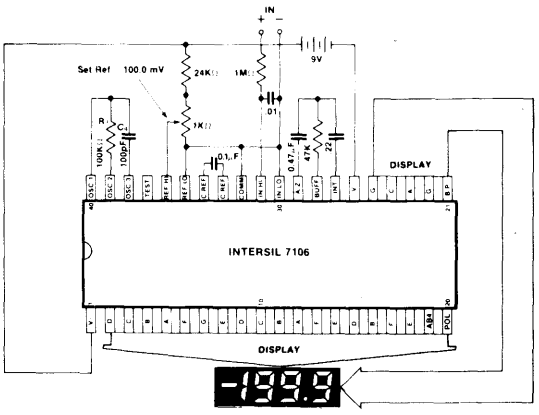


Figure 1: 7106

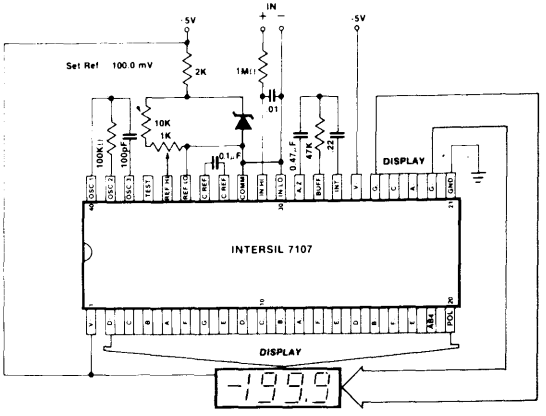


Figure 2: 7107

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

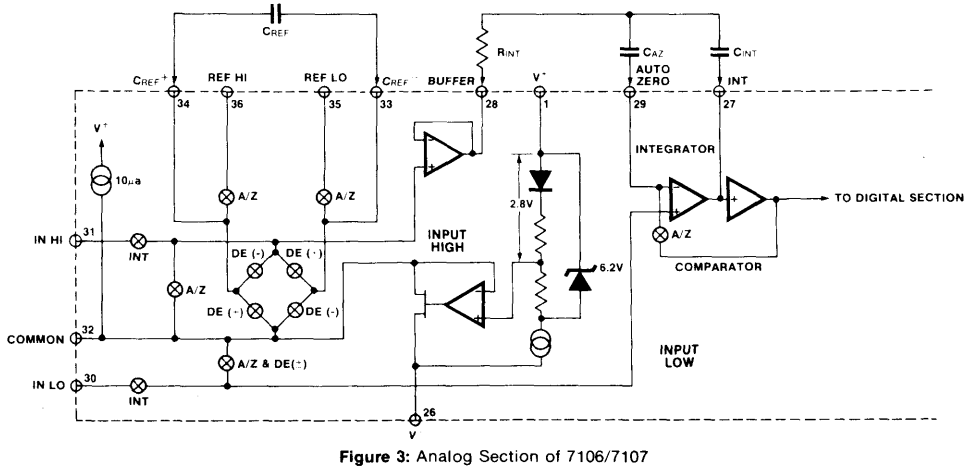


Figure 3: Analog Section of 7106/7107

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000 \left(\frac{V_{IN}}{V_{REF}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

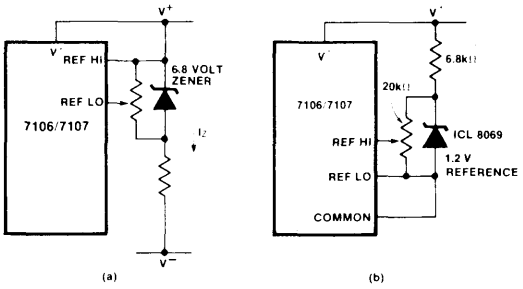


Figure 4: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

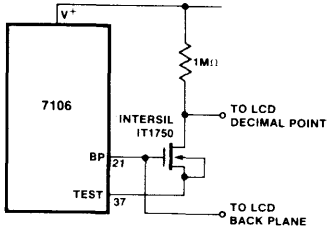


Figure 5: Simple Inverter for Fixed Decimal Point

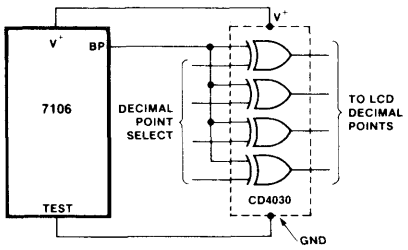


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

4

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

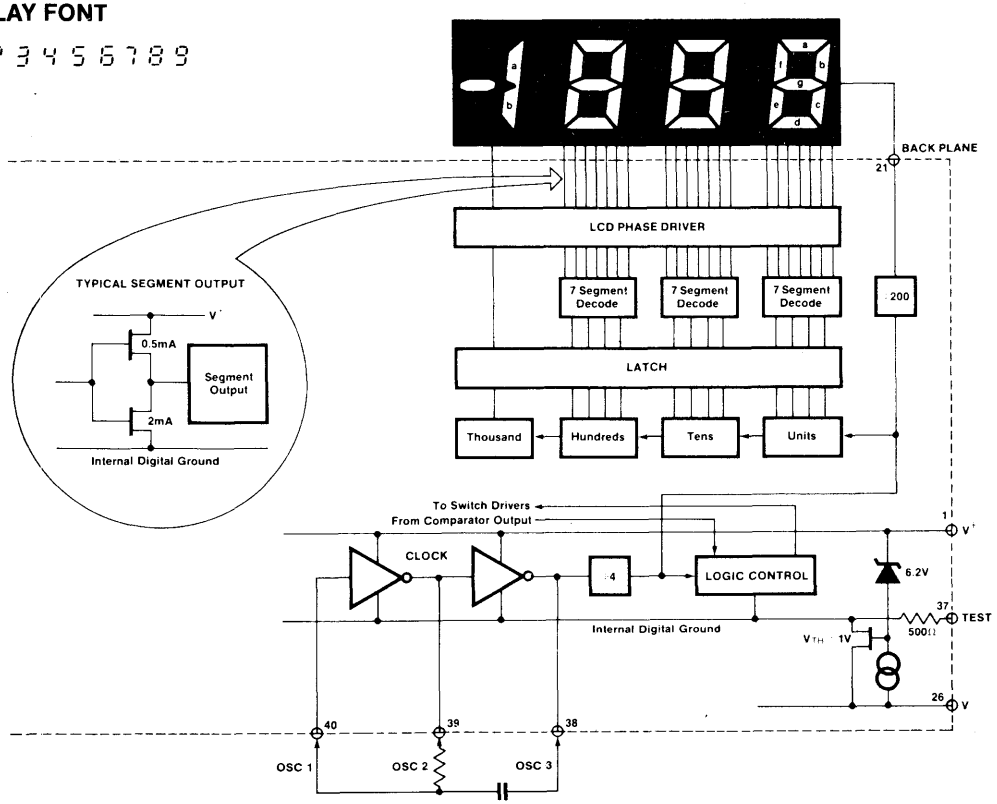


Figure 7: Digital Section 7106

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

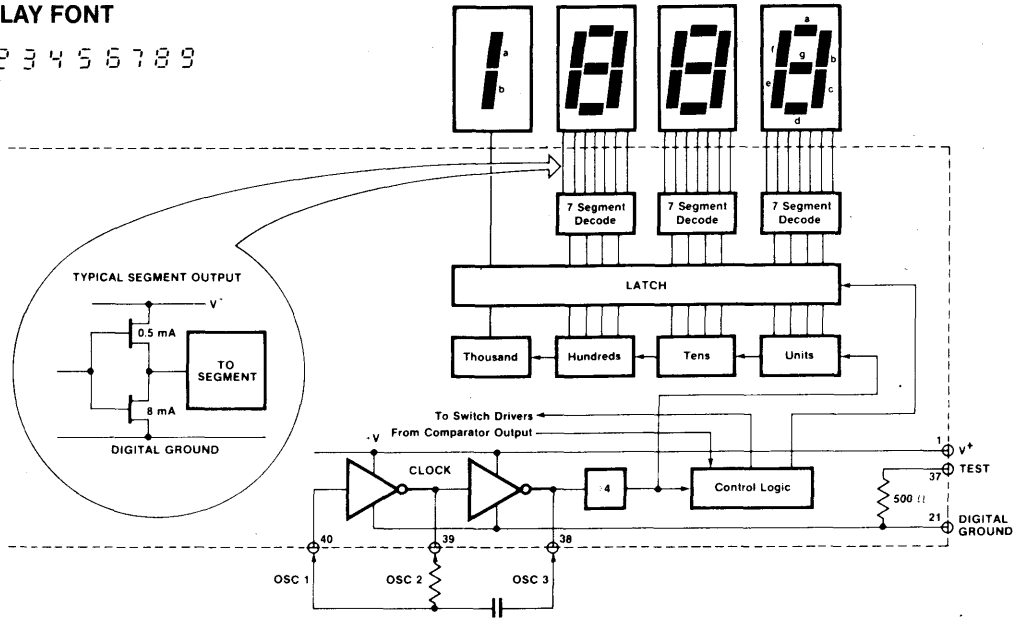


Figure 8: Digital Section 7107

4

System Timing

Figure 9 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

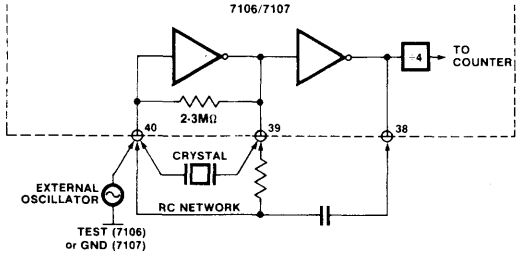


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470KΩ is near optimum and similarly a 47KΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 100KΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = .341V. Suitable values for integrating resistor and capacitor would be 120KΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this sytem occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

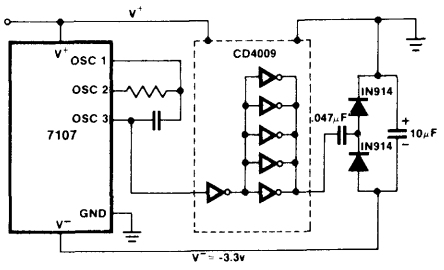


Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

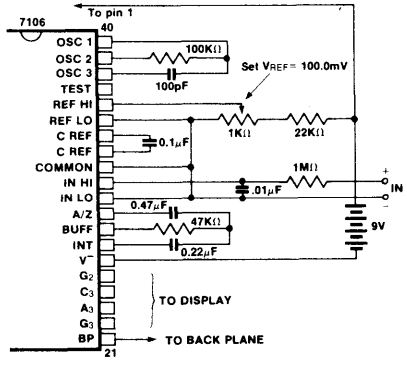


Figure 11: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

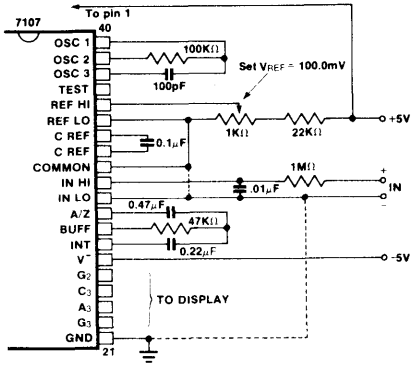


Figure 12: 7107 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

TYPICAL APPLICATIONS (Contd.)

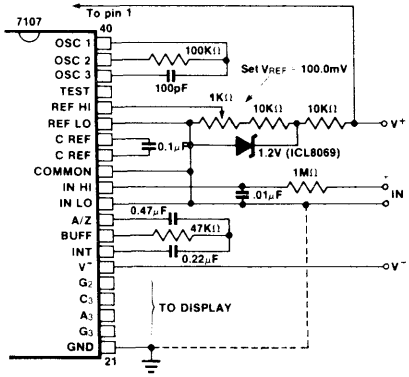


Figure 13: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

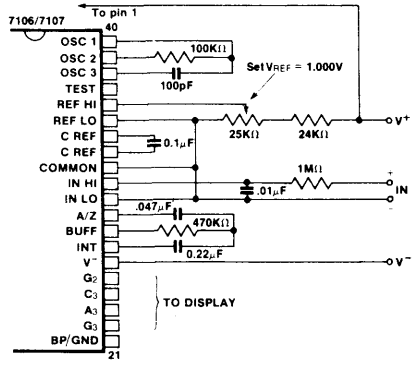


Figure 15: 7106/7107: Recommended component values for 2.000V full scale.

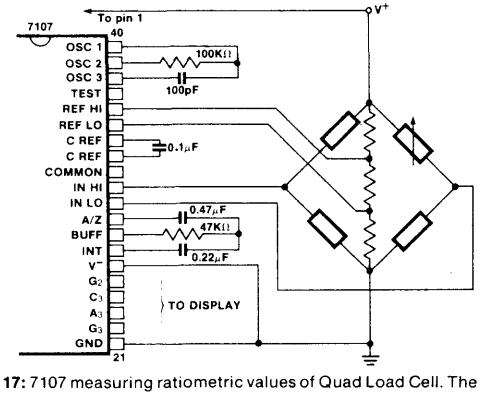


Figure 17: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

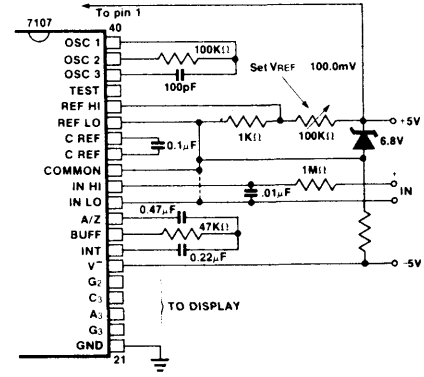


Figure 14: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 12, IN LO may be tied to either COMMON or GND.

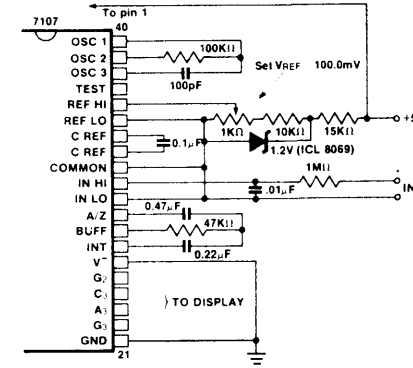


Figure 16: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

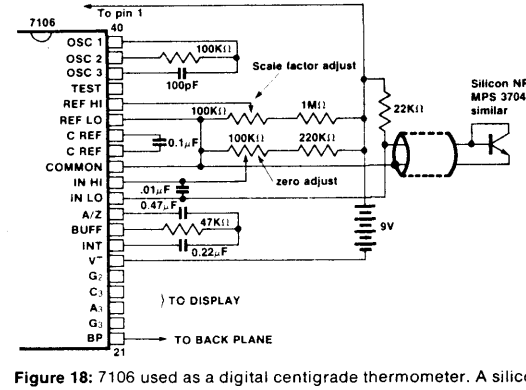


Figure 18: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

TYPICAL APPLICATIONS (Contd.)

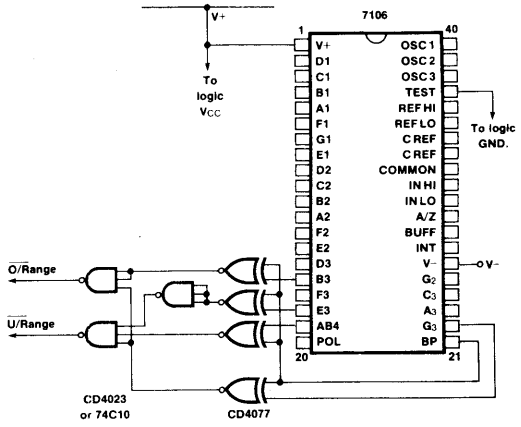


Figure 19: Circuit for developing Underrange and Overrange signals from 7106 outputs.

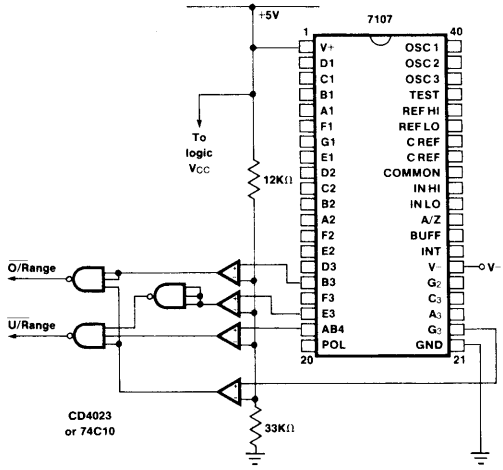


Figure 20: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

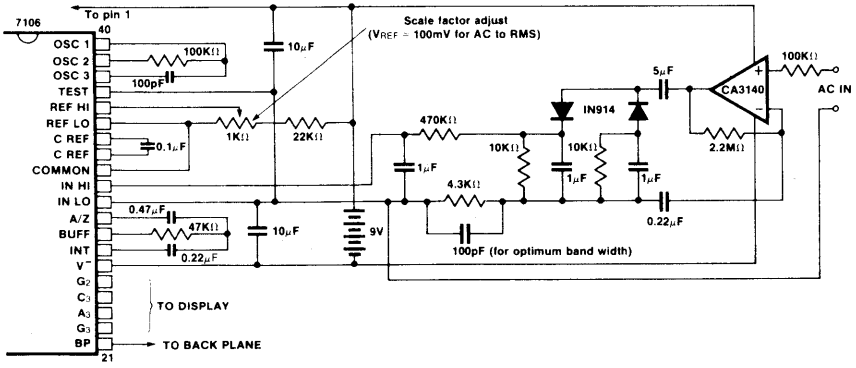


Figure 21: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

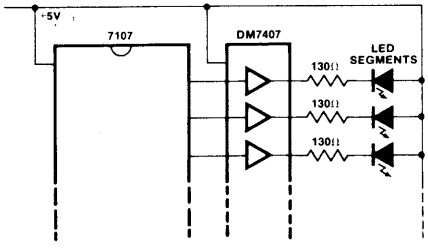


Figure 22: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.

7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

ICL7109 12 Bit Binary A/D Converter for Microprocessor Interfaces

FEATURES

- **12 bit binary (plus polarity and overrange) dual slope integrating analog-to-digital converter.**
- **Byte-organized TTL-compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.**
- **RUN/HOLD input and STATUS output can be used to monitor and control conversion timing.**
- **True differential input and differential reference.**
- **Low noise — typically 15μV p-p.**
- **1pA typical input current.**
- **Operates at up to 30 conversions per second.**
- **On-chip oscillator operates with inexpensive 3.58MHz TV crystal giving 7.5 conversions per second for 60Hz rejection. May also be operated as RC oscillator for other clock frequencies.**
- **Fabricated using MAX-CMOS™ technology combining analog and digital functions on a single low power LSI CMOS chip.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

GENERAL DESCRIPTION

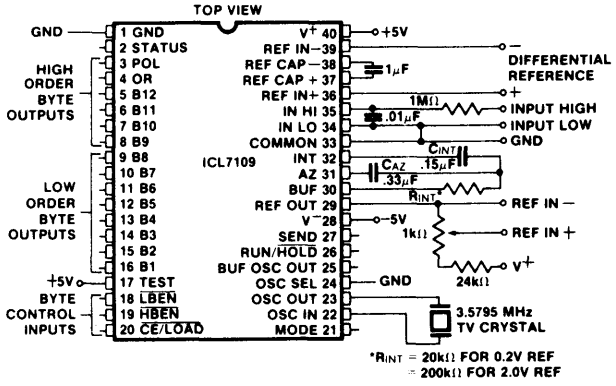
The ICL7109 is a high performance, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1μV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

PIN CONFIGURATION AND TEST CIRCUIT:

(See Figure 1 for typical connection to a UART or Microcomputer)



(OUTLINE DWGS DL, JL, PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7109	−55°C to +125°C	40-Pin Ceramic DIP	ICL7109MDL
7109	−20°C to +85°C	40-Pin Ceramic DIP	ICL7109IDL
7109	−20°C to +85°C	40-Pin CERDIP	ICL7109IJL
7109	0°C to 70°C	40-Pin Plastic DIP	ICL7109CPL

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) ..... $V^+ + 0.3V$ GND − 0.3V
Power Dissipation (Note 3)
Ceramic Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Operating Temperature
Ceramic Package (MDL) ..... $-55°C \le T_A \le +125°C$
(IDL) ..... $-25°C \le T_A \le +85°C$
Plastic Package (CPL) ..... $0°C \le T_A \le +70°C$
Storage Temperature ..... $-55°C \le T_A \le +125°C$
Lead Temperature (soldering, 60 sec.) ..... +300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE I OPERATING CHARACTERISTICS

All parameters with $V^+ = +5V$, $V- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.
Test circuit as shown on page 1.

4

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 409.6mW	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Lo, Common	V-+1.5		V+−1.0	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage current at Input	I_{ILK}	V_{IN} = 0 All devices 25°C ICL7109CPL $0°C \le T_A \le +70°C$ ICL7109IDC $-25°C \le T_A \le +85°C$ ICL7109MDL $-55°C \le T_A \le +125°C$		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	$V^- + 1.5$	$V+ -0.5$ to $V^- + 1.0$	$V^+ - 1.0$	V

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage		V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current			Pins 18, 19, 20 V_{OUT} = V^+ −3V MODE input at GND		5		μA
Control I/O Loading			$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
Input High Voltage		V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			Pins 26, 27 V_{OUT} = V^+ −3V		5		μA
Input Pull-up Current			Pins 17, 24 V_{OUT} = V^+ −3V		25		μA
Input Pull-down Current			Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High	O_{OH}	V_{OUT} = 2.5V		1		mA
	Low	O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High	BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low	BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width		tw		50			ns

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

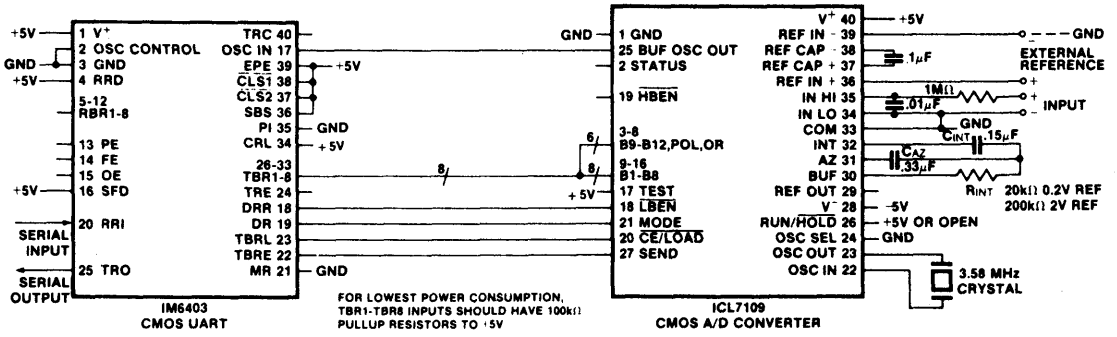


Figure 1A. Typical Connection Diagram UART Interface - To transmit latest result, send any word to UART

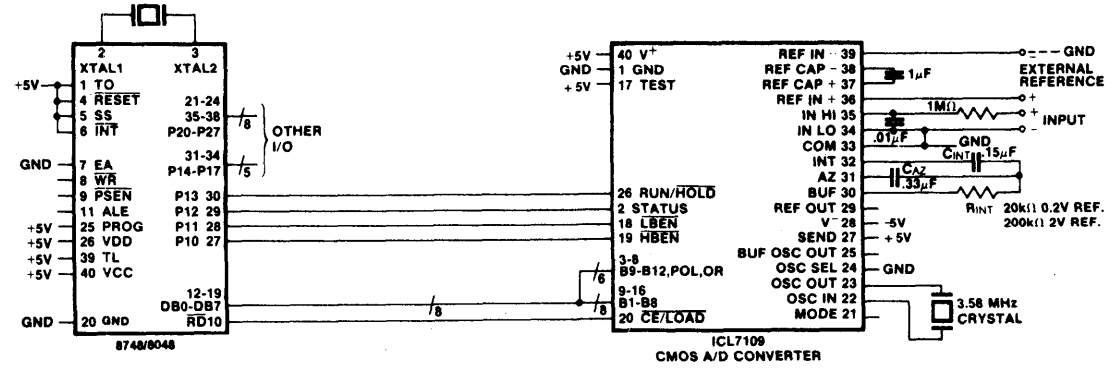


Figure 1B: Typical Connection Diagram Parallel Interface With MCS-48 Microcomputer

TABLE 2 - Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION		
1	GND	Digital Ground, 0V. Ground return for all digital logic		
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.		
3	POL	Polarity - HI for Positive Input.		All three state output data bits
4	OR	Overrange - HI if Overranged.		
5	B12	Bit 12	(Most Significant Bit)	
6	B11	Bit 11		
7	B10	Bit 10		
8	B9	Bit 9		
9	B8	Bit 8		
10	B7	Bit 7	HI = true	
11	B6	Bit 6		
12	B5	Bit 5		
13	B4	Bit 4		
14	B3	Bit 3		
15	B2	Bit 2		
16	B1	Bit 1	(Least Significant Bit)	
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.		
18	$\overline{LBEN}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. - With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.		
19	$\overline{HBEN}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. - With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.		
20	$\overline{CE/LOAD}$	Chip Enable Load - With Mode (Pin 21) low, $\overline{CE/LOAD}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. - With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.		

PIN	SYMBOL	DESCRIPTION
21	MODE	Input Low - Direct output mode where $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19) and $\overline{LBEN}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19), and $\overline{LBEN}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. - Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{HOLD}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data. Connect to + 5V if not used.
28	V^-	Analog Negative Supply - Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V^+ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP	Reference Capacitor Negative
39	REF IN	Differential Reference Input Negative
40	V^+	Positive Supply Voltage - Nominally +5V with respect to GND (Pin 1).

Note: All digital levels are positive true.

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/$\overline{HOLD}$ input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

1. **Auto-Zero Phase**

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. **Signal Integrate Phase**

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage can be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

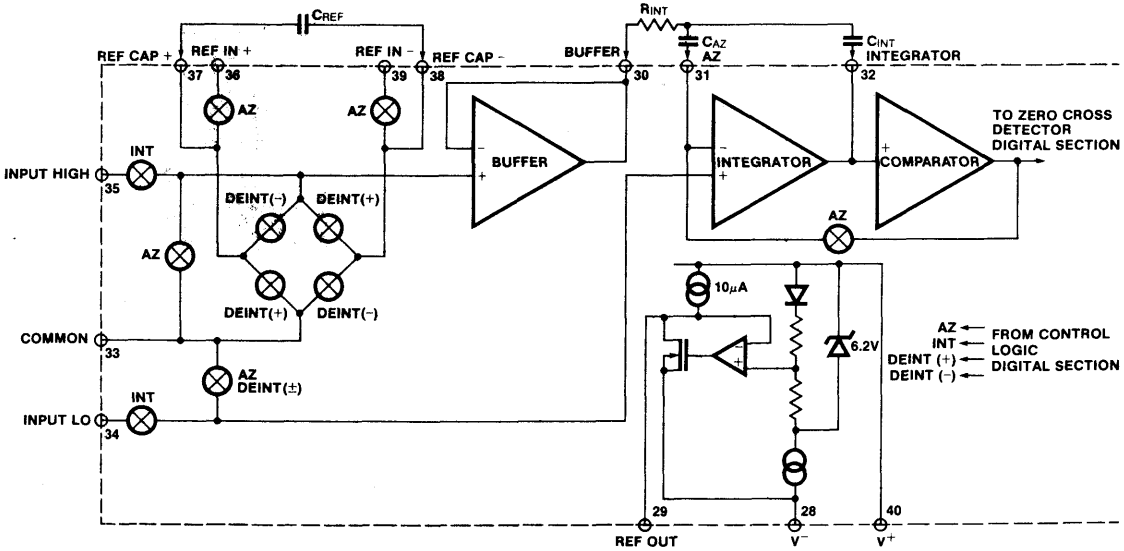


Figure 2: Analog Section

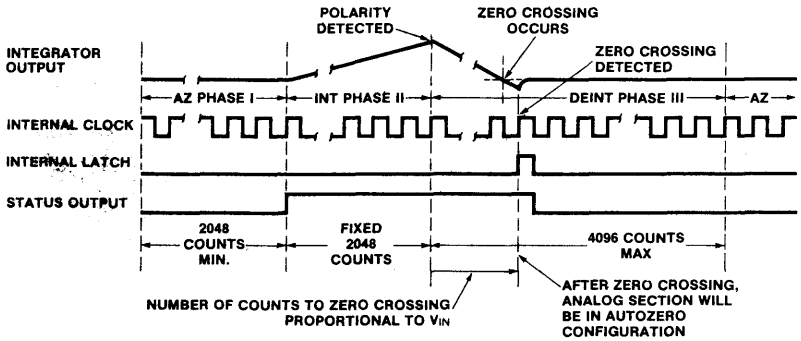


Figure 3: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

3. **De-Integrate Phase**

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and −5V, this allows a 4V full scale integrator swing positive or negative maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by

selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

1. **Integrating Resistor**

   Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

   $$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

2. **Integrating Capacitor**

   The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72KHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

   $$C_{INT} = \frac{(2048 \times \text{clock period})\,(20\mu A)}{\text{integrator output voltage swing}}$$

   An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

3. **Auto-Zero Capacitor**

   The size of the auto-zero capacitor has some influence on the noise of the system; a big capacitor, giving less noise. However, it cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mv full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

   For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

4. **Reference Capacitor**

   A 1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

5. **Reference Voltage**

   The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 34k and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

6. **Reference Sources**

   The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF – (pin 39), and REF + should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V^+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with pin 39.

4

DETAILED DESCRIPTION

Digital Selection

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in the Block Diagram, Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in Table 1 "Operating Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5kΩ pull-up resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/$\overline{\text{HOLD}}$ stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 5 for details.

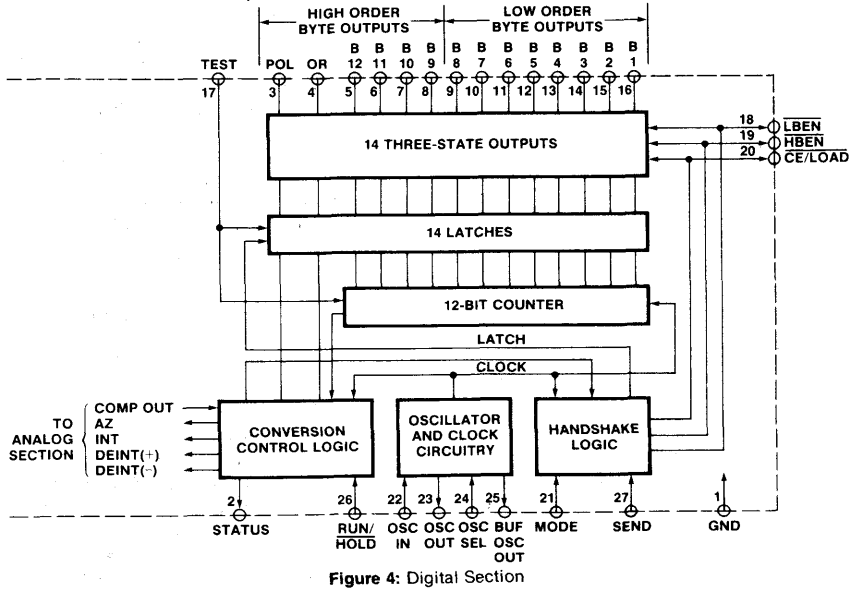


Figure 4: Digital Section

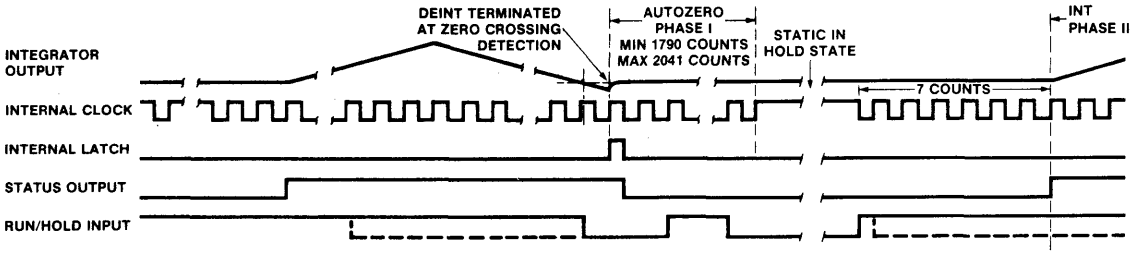


Figure 5: Run/$\overline{\text{Hold}}$ Operation

Using the RUN/$\overline{\text{HOLD}}$ input in this manner allows an easy "convert on demand" interface to be used.The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. When RUN/$\overline{\text{HOLD}}$ goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion.

Alternately, RUN/$\overline{\text{HOLD}}$ can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/$\overline{\text{HOLD}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/$\overline{\text{HOLD}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 6 and Table 3.

Table 3 - Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		210	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

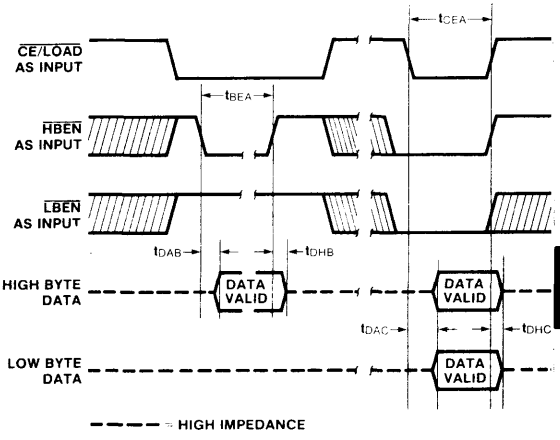


Figure 6: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (See Figures 7 and 8). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry

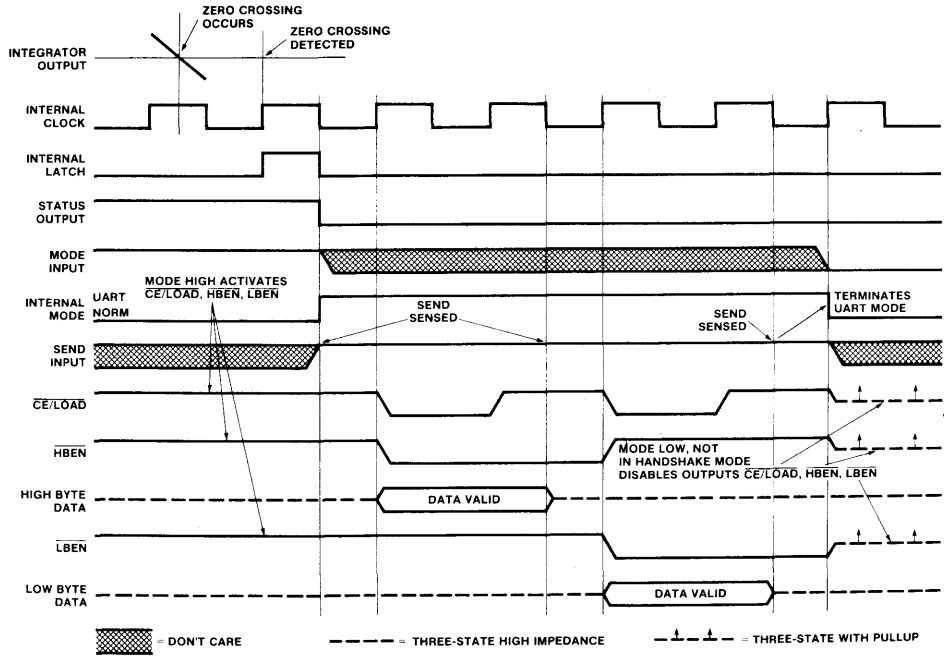


Figure 7: Handshake With Send Held Positive

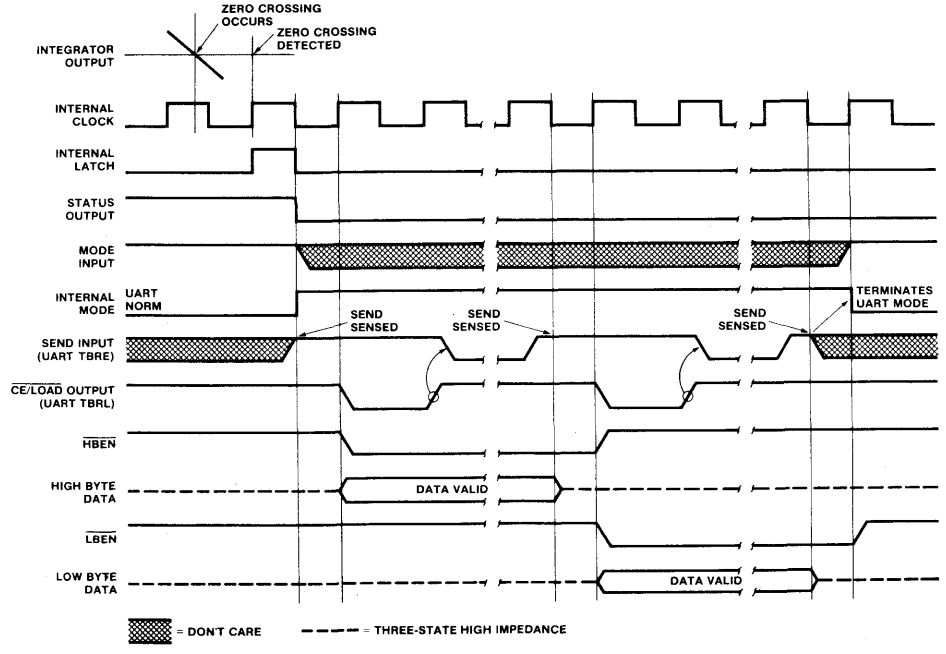


Figure 8: Handshake - Typical UART Interface Timing

into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 9) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 7, 8, and 9).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 7 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 8 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{CE/LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109

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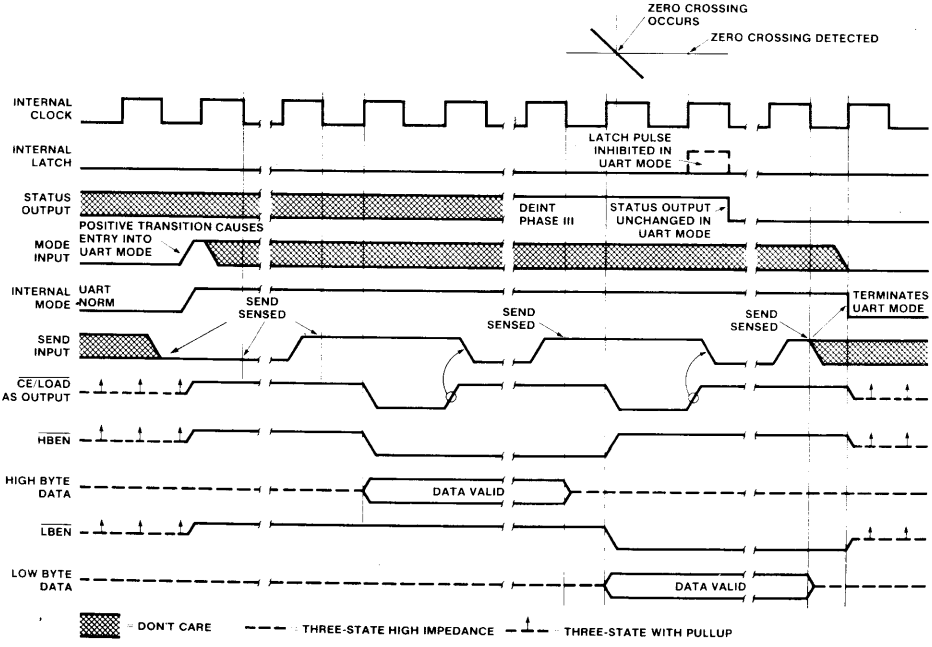

Figure 9: Handshake Triggered By Mode

internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$, and $\overline{LBEN}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{HOLD}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

4

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 10. The circuit will oscillate at a frequency given by f = 0.45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but not less than 50pF).

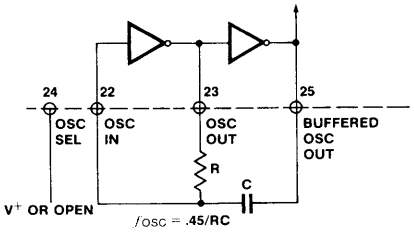

Figure 10: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the

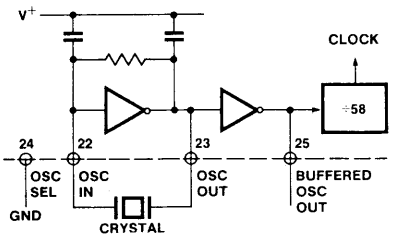

Figure 11: Crystal Oscillator

oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T = (2048 \text{ clock periods}) \times \left(\frac{58}{3.58\text{MHz}}\right) = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V^+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V^+ –GND) voltage (or to V^+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 12 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 12A. Figure 12B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 12C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

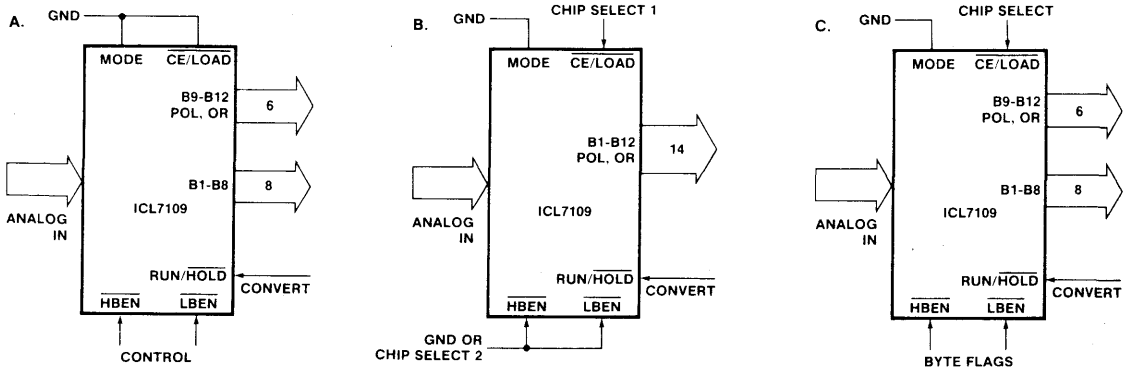

Figure 12: Direct Mode Chip and Byte Enable Combinations

Figure 13 shows an approach to interfacing several ICL7109s to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE/LOAD}$ inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 14 through 19. Figure 14 shows a straightforward application to the Intel MCS-48, -80 and -85 systems via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 15. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data. This application also shows the RUN/$\overline{HOLD}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 16. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/$\overline{HOLD}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system also.

Figure 17 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read by the microprocessor in an 8-bit and a 6-bit word, directly from the ICL7109 to the microprocessor data bus. Again, the high to low transition of the STATUS output generates an interrupt leading to a software routine controlling the two read operations. As before, the RUN/$\overline{HOLD}$ input to the ICL7109 is shown as being under software control.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 1, 18 and 19. It is necessary to

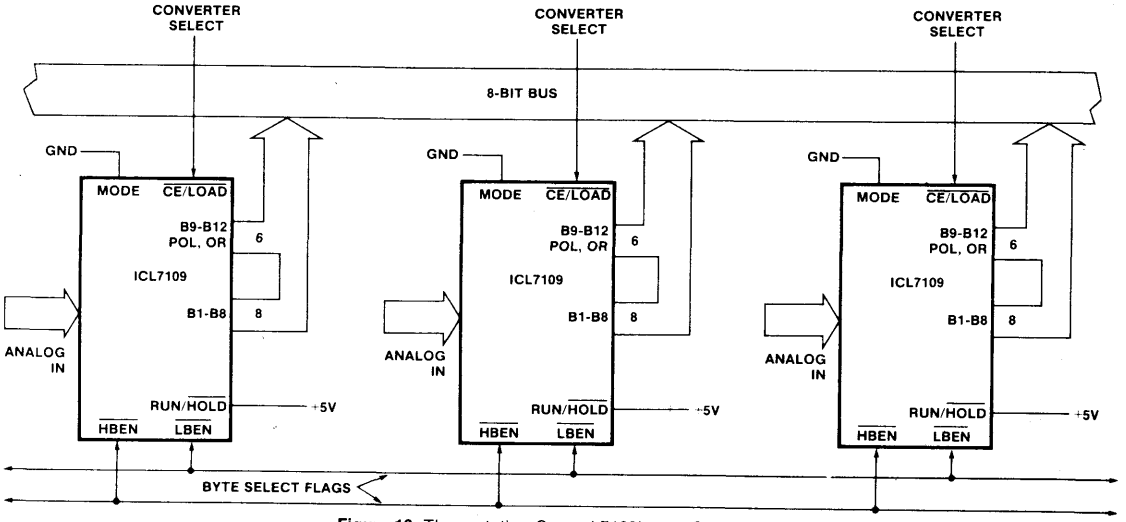

Figure 13: Three-stating Several 7109's to a Small Bus

carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long busses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

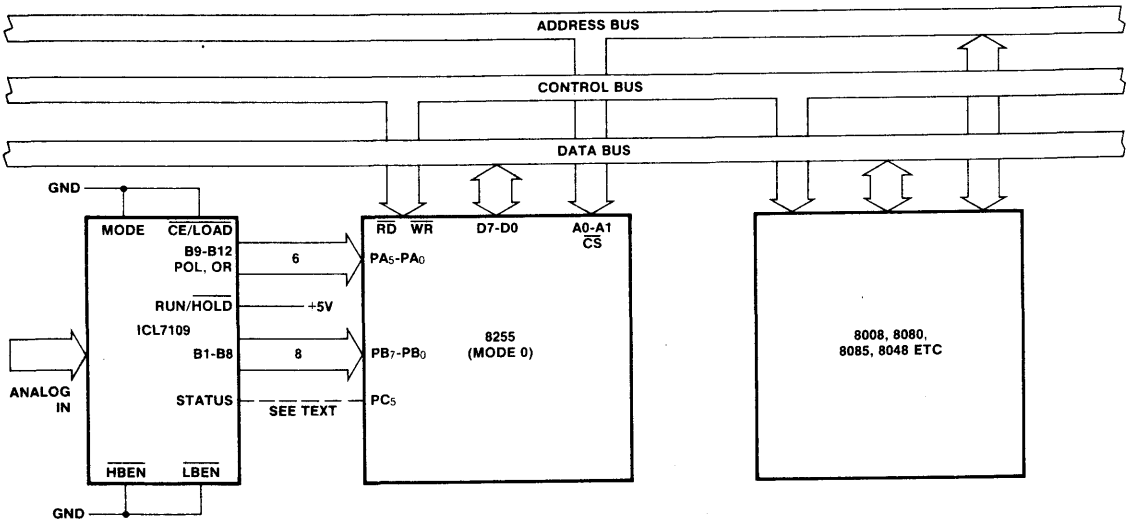

Figure 14: Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

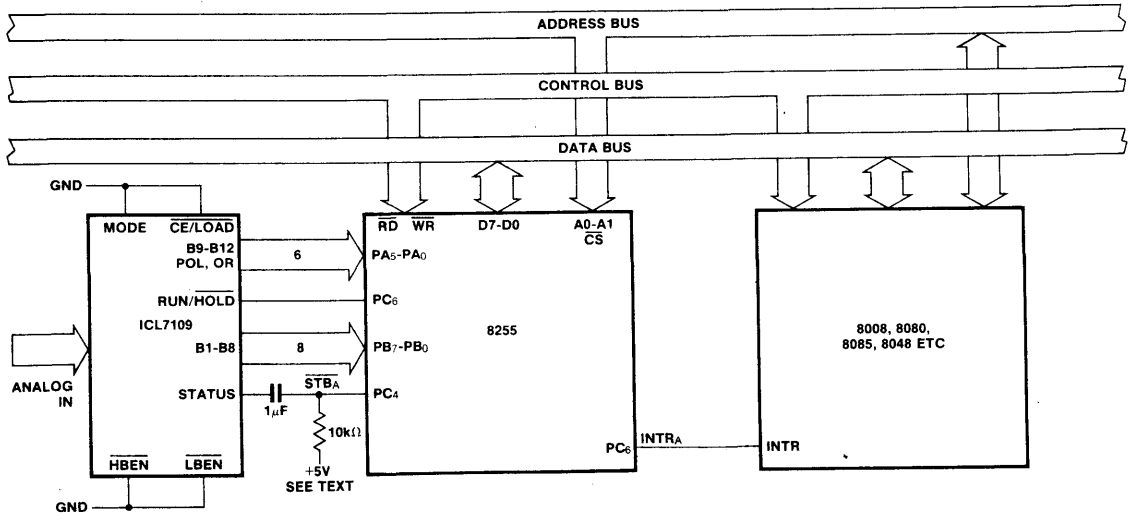

Figure 15: Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers With Interrupt

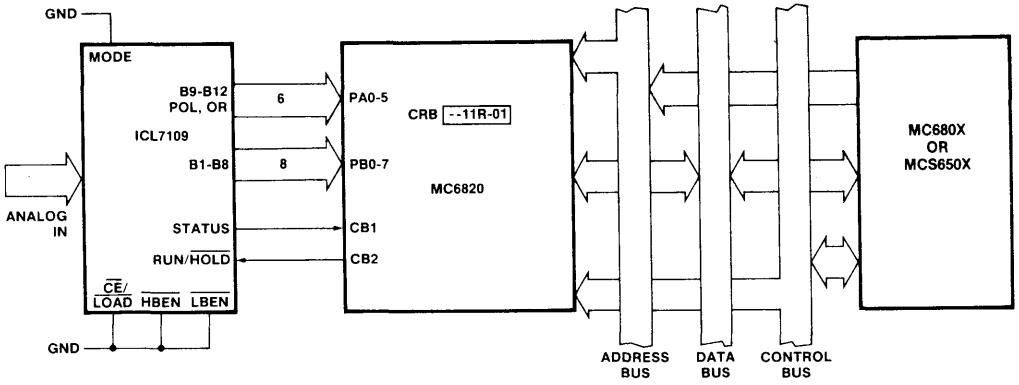

Figure 16: Full-time Parallel Interface to MC680X or MCS650X Microprocessors

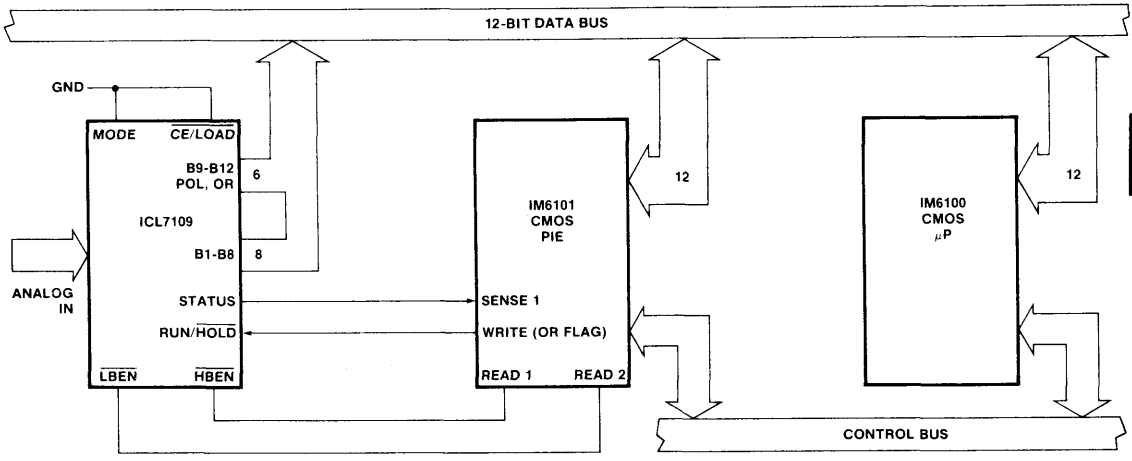

Figure 17: ICL7109-IM6100 Interface Using IM6101 PIE

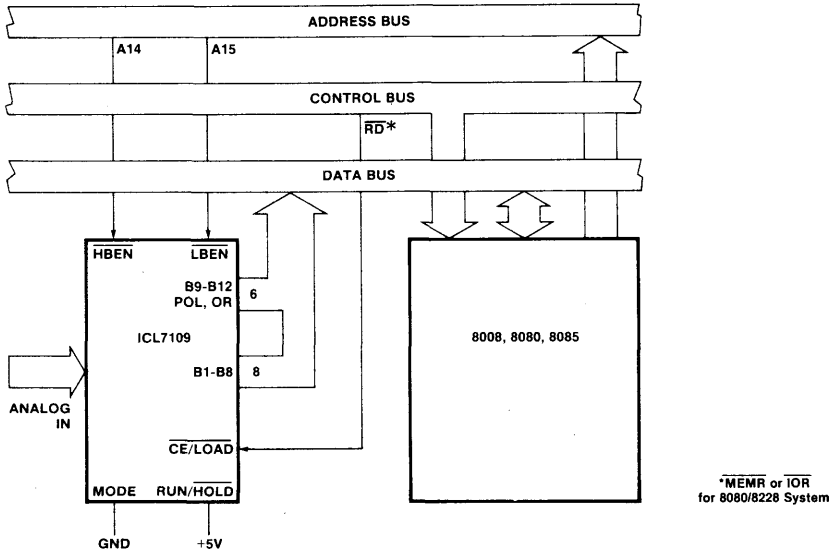

Figure 18: Direct Interface - ICL7109 to 8080/8085

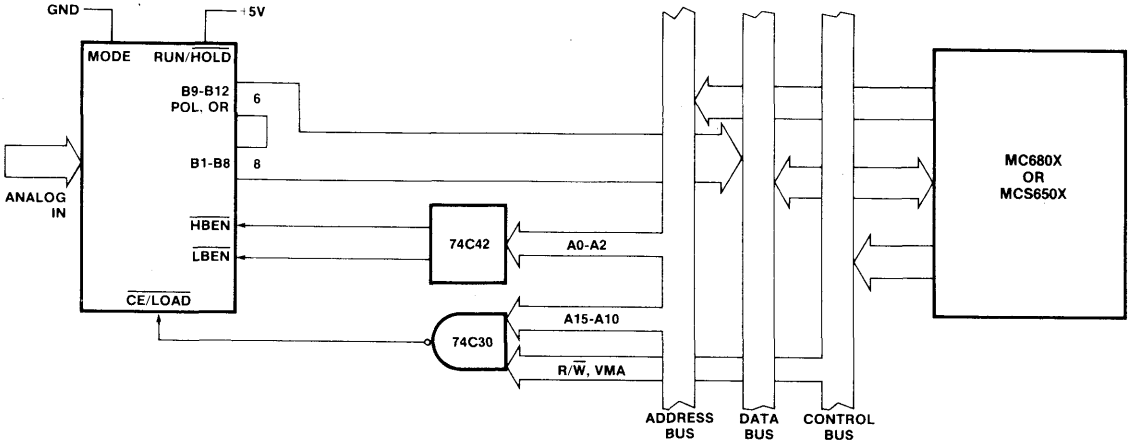

Figure 19: Direct ICL7109 - MC680X Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown on page 3. In this circuit, any word received by the UART causes

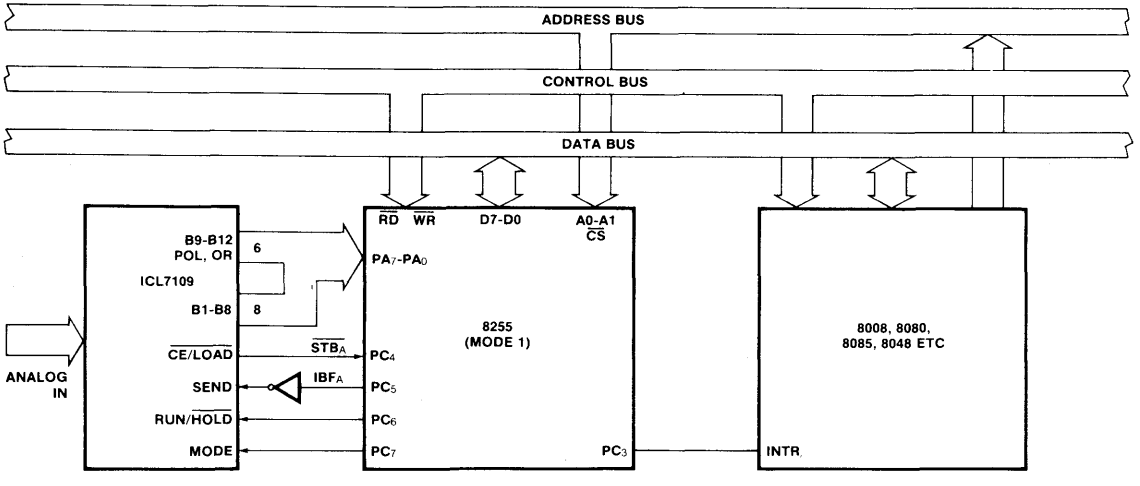

Figure 20: Handshake Interface - ICL7109 to MCS-48, -80, 85

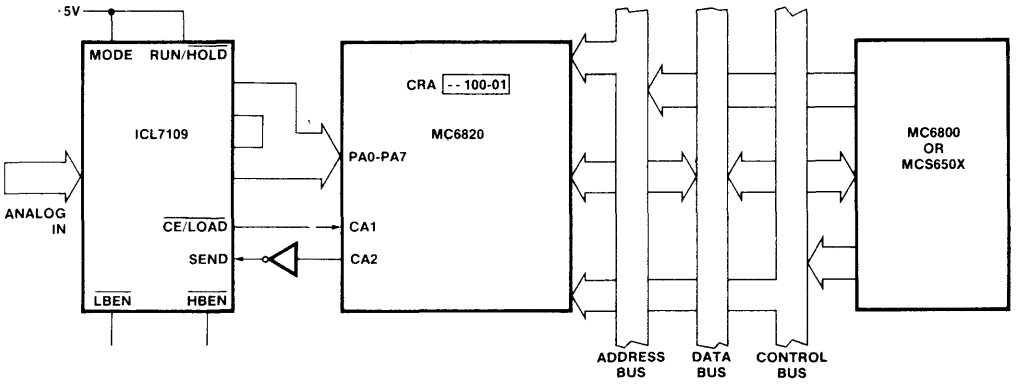

Figure 21: Handshake Interface - ICL7109 to MC6800, MCS650X

the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, $\overline{LBEN}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter - one UART scheme of the Typical Connection to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/$\overline{HOLD}$, and MODE signals may be mixed.

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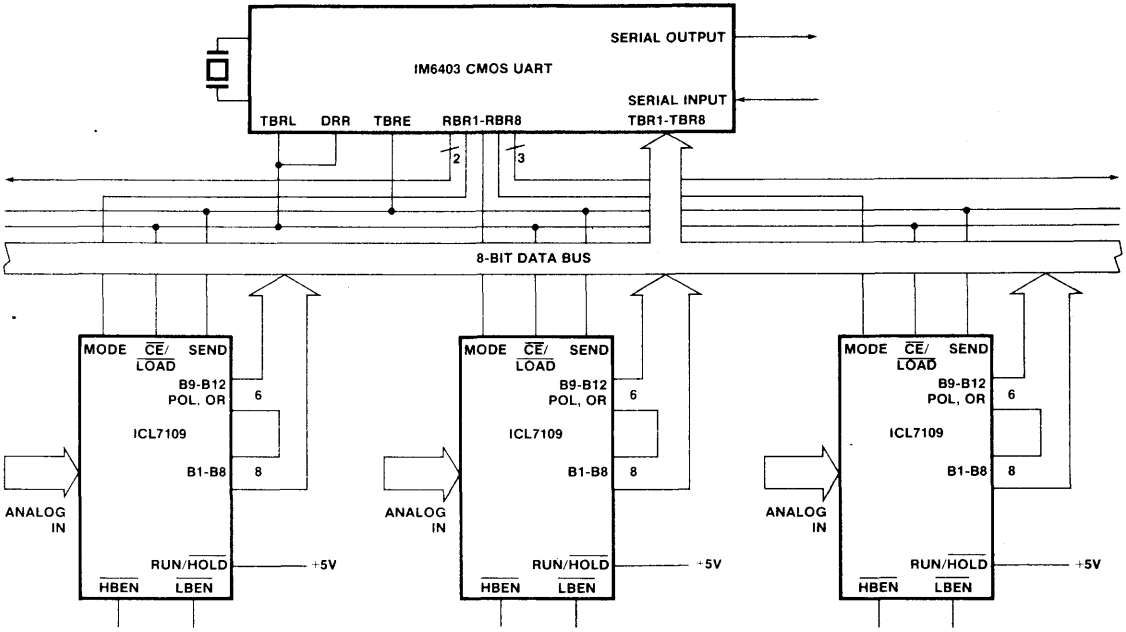


Figure 22: Multiplexing Converters with Mode Input

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

ICL7115

Fast CMOS Monolithic 14-Bit A/D Converter

FEATURES

- **14-bit linearity and resolution (0.003%)**
- **No missing codes**
- **Microprocessor compatible byte-organized buffered outputs**
- **Fast conversion (40μs)**
- **Auto-zeroed comparator for low offset voltage**
- **Low linearity and gain tempco (1ppm/°C, 4ppm/°C)**
- **Low power consumption (60mW)**
- **No gain or offset adjustment necessary (0.006% FS)**
- **Provides 3% useable overrange**
- **FORCE/SENSE and separate digital and analog ground pins for increased system accuracy**

4

GENERAL DESCRIPTION

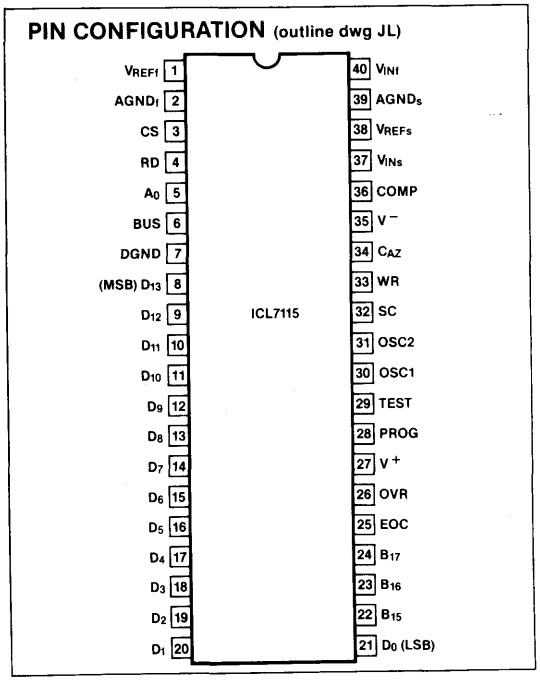
The ICL7115 is the first monolithic 14-bit accurate, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry with an on-chip PROM calibration table circuit to achieve 14-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8, 12, and 16-bit systems.

The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +5V input with a −5V reference or 0V to −5V input with a +5V reference.

The ICL7115 is available in several versions with different accuracies, temperature ranges and packages. A Leadless Chip Carrier (LCC) package is also available; consult factory.

PIN CONFIGURATION (outline dwg JL)



ORDERING INFORMATION

ACCURACY	PACKAGE	TEMPERATURE	PART NUMBER
0.01%	40-Pin CERDIP	0°C to +70°C	ICL7115JCJL
0.01%	40-Pin CERDIP	−25°C to +85°C	ICL7115JIJL
0.01%	LCC	—	—
0.006%	40-Pin CERDIP	0°C to +70°C	ICL7115KCJL
0.006%	40-Pin CERDIP	−25°C to +85°C	ICL7115KIJL
0.006%	LCC	—	—
0.003%	40-Pin CERDIP	0°C to +70°C	ICL7115LCJL
0.003%	40-Pin CERDIP	−25°C to +85°C	ICL7115LIJL
0.003%	LCC	—	—

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to +6.5V
Supply Voltage V^- to DGND ..... +0.3V to −6.5V
V_{REFs}, V_{REFf}, V_{INs}, V_{INf} to DGND ..... +25V to −25V
$AGND_s$, $AGND_f$ to DGND ..... +1V to −1V
Current in FORCE and SENSE Lines 25mA
Digital I/O Pin Voltages ..... −0.3V to V^+ +0.3V
PROG to DGND Voltage ..... V^- to V^+ +0.3V

Operating Temperature Range
ICL7115XCXX ..... 0°C to +70°C
ICL7115XIXX ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
derate above 70°C @ 100mW/°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Note 1: All voltages with respect to DGND, unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V^+ = +5.0V$, $V^- = -5.0V$, $V_{REFs} = +5.0V$, $T_A = +25°C$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		$\overline{SC}$ = High $\overline{SC}$ = Low	14 12			Bits
Total Unadjusted Error					1	LSB
Differential Non-Linearity		Full Operating Temperature Range		1/2		
Overall Accuracy (Note 3)		ICL7115J ICL7115K ICL7115L			0.01 0.006 0.003	% FSR
Full-Scale Error		$T_A = +25°C$ Operating Temperature Range (Note 2)		1/2 1	1 4	LSB ppm/°C
Zero Error		$T_A = +25°C$ Operating Temperature Range (Note 2)			1/8 4	LSB ppm/°C
Power Supply Rejection	PSRR	$T_A = +25°C$ Full Operating Temperature Range		1/16	1/8	LSB
V_{INs}, V_{REFs} Resistance	Z_{IN}, Z_{REF}	(Note 4) Operating Temperature Range	3	5 −300	7	kΩ ppm/°C
Low State Input Voltage	V_{il}	Operating Temperature Range			0.8	V
High State Input Voltage	V_{ih}	Operating Temperature Range	2.4			V
Logic Input Current	I_{iih}	$0 < V_{IN} < V^+$		1	10	μA
Low State Output Voltage	V_{ol}	I_{OUT} = 3.2mA Operating Temperature Range			0.4	V
High State Output Voltage	V_{oh}	I_{OUT} = −200μA Operating Temperature Range	2.8			V
Three-State Output Current	I_{ox}	$0 < V_{OUT} < V^+$		1		μA
Logic Input Capacitance	C_{in}	(Note 2)		15		pF
Logic Output Capacitance	C_{out}	Three-State (Note 2)		15		
Supply Voltage Range	V^+	Functional Operation	4.5		6.0	V
	V^-		−4.5		−6.0	
Supply Current	I^+	Excluding Ladder Current		5		mA
	I^-	F_{CLK} = 1kHz		5		

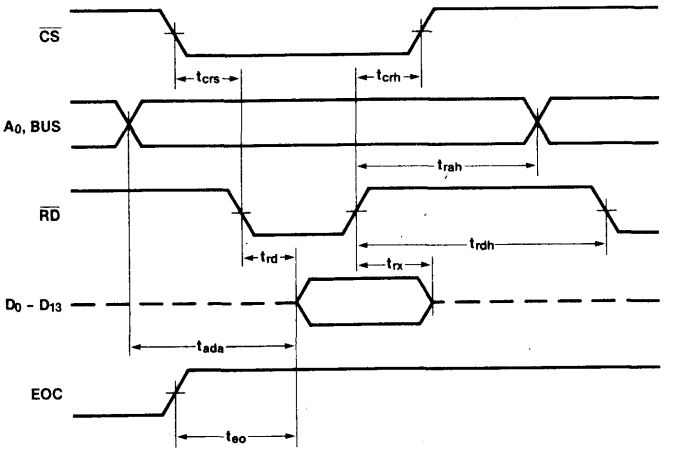
Note 2: Assumes all leads soldered or welded to printed circuit board.
Note 3: Full-scale range (FSR) is 10V (+5V to −5V).
Note 4: Guaranteed by design, not 100% tested in production.

AC ELECTRICAL CHARACTERISTICS $V^+ = +5.0V$, $V^- = -5.0V$, $T_A = +25°C$, unless otherwise noted

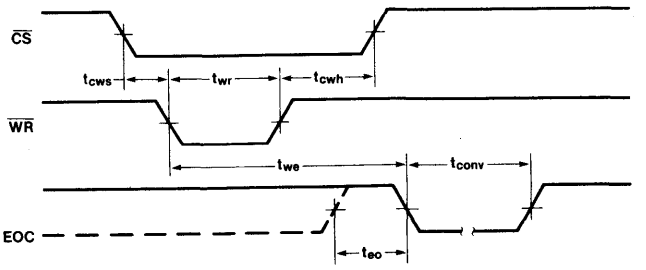
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Conversion Time	t_{conv}	$\overline{SC}$ = High			40	μs
		$\overline{SC}$ = Low			36	
Address to Data Access	t_{ada}			250		ns
ReaD Low to Data	t_{rd}			200		
ReaD High to Three-State	t_{rx}		20		100	
ReaD, Address Hold Time	t_{rah}				0	
ReaD Pulse Width High	t_{rdh}		200			
WRite Pulse Width Low	t_{wr}		200			
EOC High to Data	t_{ed}			200		
CS, WR Set-Up Time	t_{cws}				0	
CS, WR Hold Time	t_{cwh}				0	
CS, ReaD Set-Up Time	t_{crs}				0	
CS, ReaD Hold Time	t_{crh}				0	
EOC Pulse Width High	t_{eo}	Free-Run Mode		0.5		$1/f_{CLK}$
WRite Low to EOC Low	t_{we}	Wait Mode	1		2	

4

Read Cycle Timing



Write Cycle Timing



PIN DESCRIPTION TABLE

PIN	NAME	FUNCTION	
1	V_{REF}	FORCE line for reference input	
2	$AGND_f$	FORCE input for analog ground	
3	$\overline{CS}$	Chip Select enables reading and writing (active low)	
4	$\overline{RD}$	ReaD (active low)	
5	A_0	Byte select (low = D_0 - D_7, high = D_8 - D_{13}, OVR)	
6	BUS	Bus select (low = outputs enabled by A_0, high = all outputs enabled together)	
7	DGND	Digital GrouND return	
8	D_{13}	Bit 13 (most significant)	High Byte
9	D_{12}	Bit 12	
10	D_{11}	Bit 11	
11	D_{10}	Bit 10	
12	D_9	Bit 9	
13	D_8	Bit 8	
14	D_7	Bit 7	Low Byte
15	D_6	Bit 6	
16	D_5	Bit 5	
17	D_4	Bit 4	
18	D_3	Bit 3	
19	D_2	Bit 2	
20	D_1	Bit 1	
21	D_0	Bit 0 (least significant)	

Output Data Bits (High = True)

PIN	NAME	FUNCTION
22	B_{15}	
23	B_{16}	Used for programming only (leave open)
24	B_{17}	
25	EOC	End Of Conversion flag (low = busy, high = conversion complete)
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)
27	V^+	Positive power supply input
28	PROG	Used for programming only. Tie to V^+ for normal operation
29	TEST	Used for programming only. Tie to V^+ for normal operation
30	OSC1	Oscillator inverter input
31	OSC2	Oscillator inverter output
32	$\overline{SC}$	Short cycle input (high = 14-bit, low = 12-bit operation)
33	WR	WRite pulse input (low starts new conversion)
34	C_{AZ}	Auto-zero capacitor connection
35	V^-	Negative power supply input
36	COMP	Used in test, tie to V^-
37	V_{INs}	SENSE line for input voltage
38	V_{REFs}	SENSE line for reference input
39	$AGND_s$	SENSE line for analog ground
40	V_{INf}	FORCE line for input voltage

4

I/O CONTROL TRUTH TABLE

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	BUS	FUNCTION
0	0	x	x	x	Initiates a Conversion
1	x	x	x	x	Disables all Chip Commands
0	1	0	0	0	Low Byte is Enabled
0	1	0	1	0	High Byte is Enabled
0	1	0	x	1	Low and High Bytes Enabled Together
x	x	1	x	x	Disables Outputs (High-Impedance)

TRANSFER FUNCTION TABLE

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
$V_{REF} = -5.0V$	OVR	MSB		LSB
0	0	0	0 0 0 0 0 0 0 0 0 0 0 0	0
+0.0003	0	0	0 0 0 0 0 0 0 0 0 0 0 0	1
+0.150	0	0	0 0 0 0 1 1 1 1 0 1 0 1	1
+2.4997	0	0	1 1 1 1 1 1 1 1 1 1 1 1	1
+2.500	0	1	0 0 0 0 0 0 0 0 0 0 0 0	0
+4.9994	0	1	1 1 1 1 1 1 1 1 1 1 1 1	0
+4.9997	0	1	1 1 1 1 1 1 1 1 1 1 1 1	1
+5.000	1	0	0 0 0 0 0 0 0 0 0 0 0 0	0
+5.0003	1	0	0 0 0 0 0 0 0 0 0 0 0 0	1
+5.150	1	0	0 0 0 0 1 1 1 1 0 1 0 1	1

DETAILED DESCRIPTION

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 1 shows the functional block diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (B_{16}) and the MSB-4 bit (B_{12}). The sequence continues for each bit pair, B_x and B_{x-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion. When the Short Cycle ($\overline{SC}$) input is low, 18 clock cycles are required to complete a 12-bit conversion.

The overflow output of the 17-bit full-adder is also the OVer-Range (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

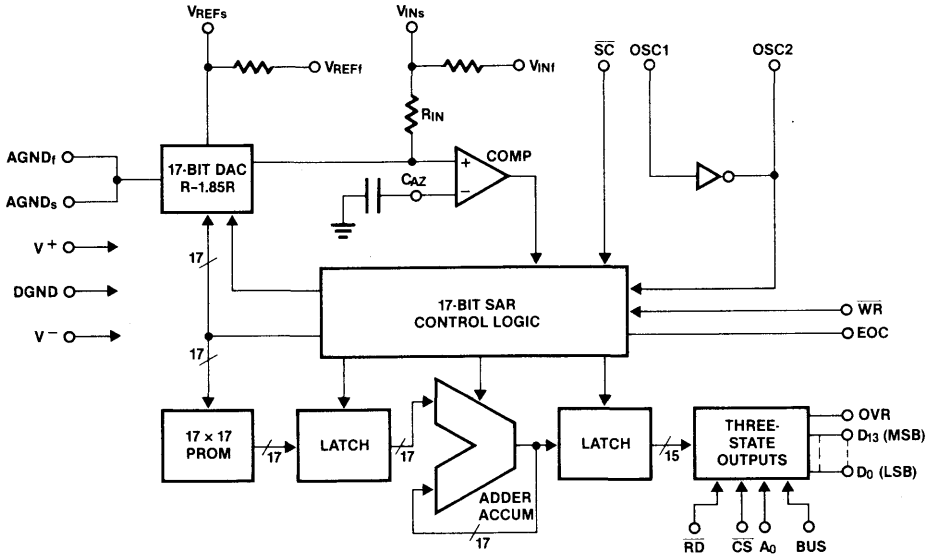


Figure 1. ICL7115 Functional Block Diagram

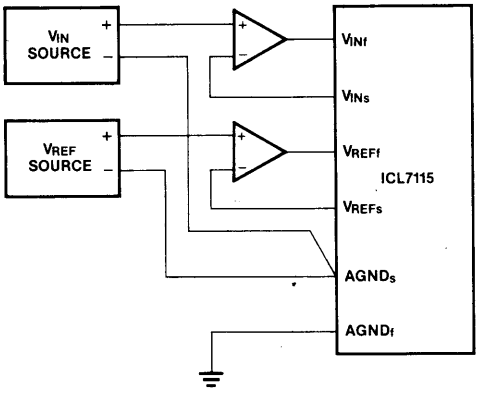


Figure 2. V_{IN} and V_{REF} Input Buffers

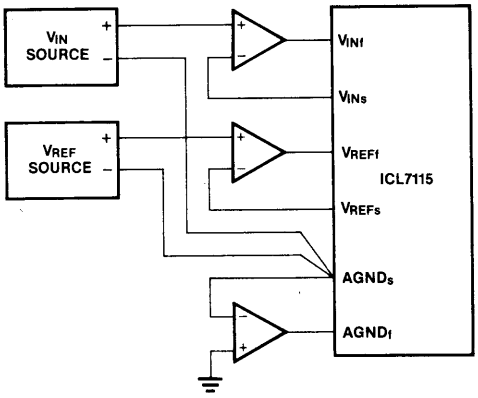


Figure 3. Using a Forced Ground

4

OPTIMIZING SYSTEM PERFORMANCE

In order to maintain full system accuracy when using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

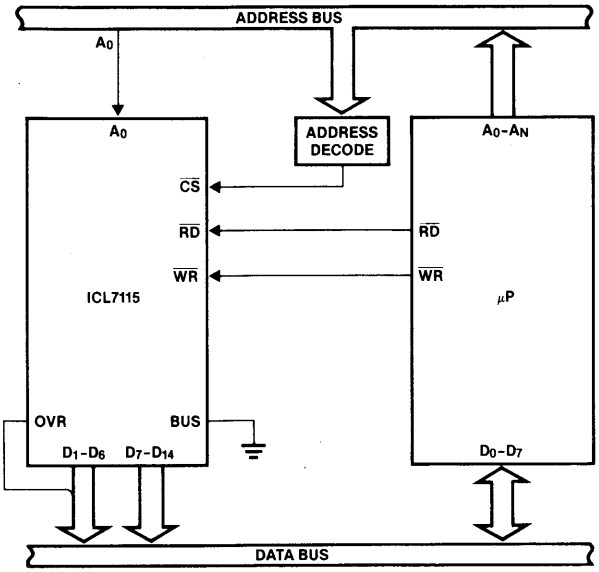
Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115. Figures 2 and 3 illustrate the proper grounding technique for eliminating ground loops. Note that the input voltage *AND* the reference voltage are referred to the analog ground SENSE input. In Figure 2 the FORCE line is the only point that is connected to system analog ground. Figure 3 shows how an external op-amp can be used to force ground. In this example, only the non-inverting input of the op-amp is connected to system analog ground.

The FORCE and SENSE inputs for V_{IN} and V_{REF} are also shown driven by external op-amps. This technique eliminates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than 300mΩ of total series resistance, the result can be a voltage error equivalent to 1 LSB. There is an inconsequential 200Ω resistor in series with the V_{IN} and V_{REF} FORCE inputs. If no op-amps are used for V_{IN} and V_{REF}, connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the V_{IN} and V_{REF} pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers, CS, RD, WR, and bus select inputs (A_0 and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A_0 lines are provided to enable the output data onto either 8-bit or 16-bit data busses. A conversion is initiated by a WR pulse (pin 33) when Chip Select (pin 3) is low. Data is enabled on the bus when the chip is selected and RD (pin 4) is low.

Figure 4 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the WR input to the ICL7115 after the I/O or memory-mapped address decoder has brought the CS input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A_0 enables the LSBs and a high level enables the MSBs.



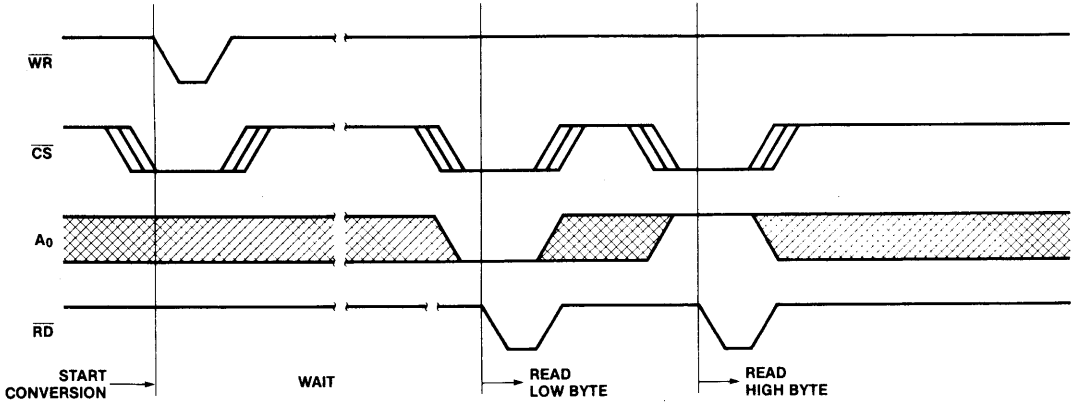
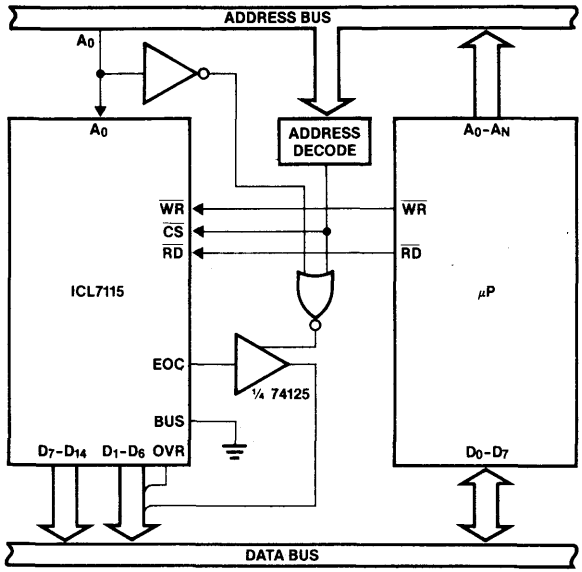


Figure 4. "Start and Wait" Operation

By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 5). In this mode, the A_0 and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the WR line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 6. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 7.



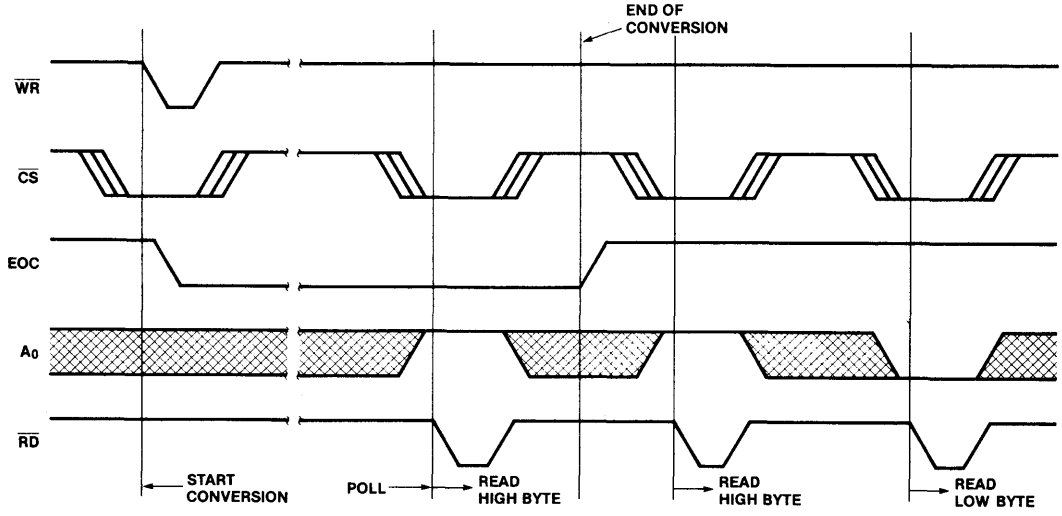
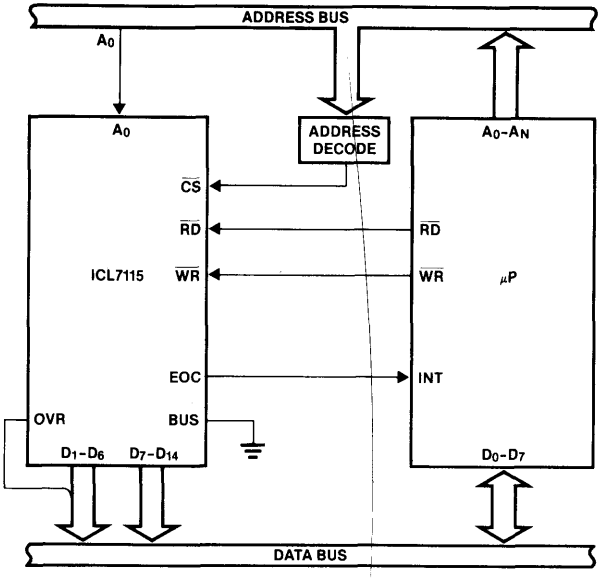


Figure 5. "Start and Poll" Operation



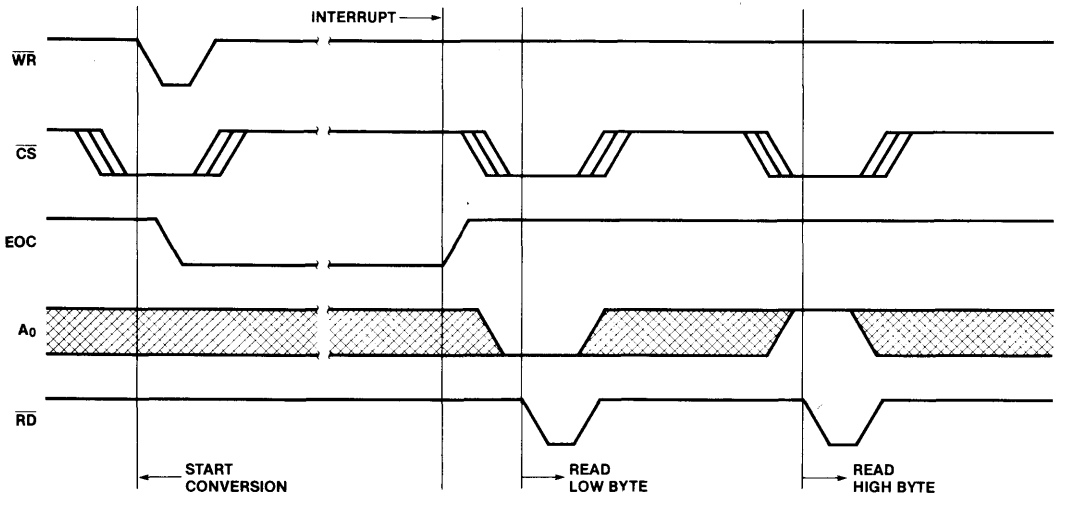
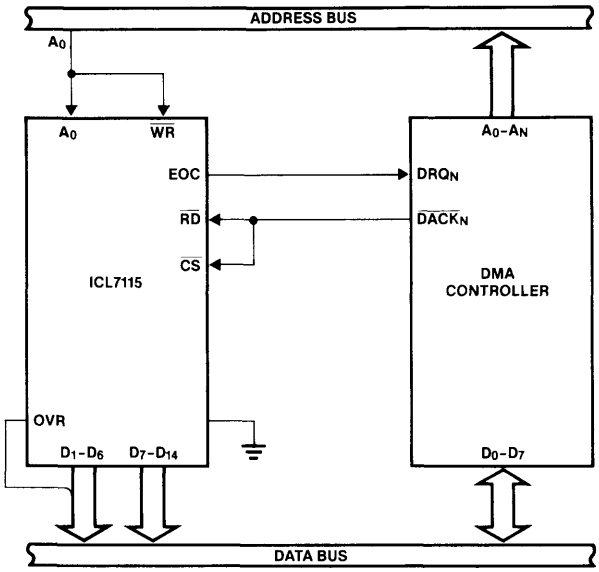


Figure 6. Using EOC as an Interrupt



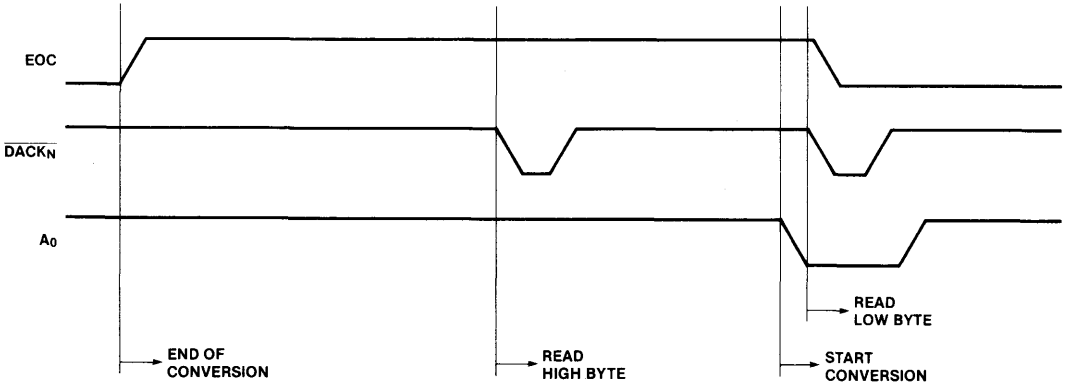


Figure 7. Data to Memory via DMA Controller

APPLICATIONS

Figure 8 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of +5V to −5V is the result of using the current through R_2 to force a 1/2 scale offset on the input amplifier (A_2). The output of A_2 swings from 0V to −5V. The ICL8078-5D0 provides a very stable and accurate +5V for the reference buffer amplifier A_1. The overall gain of the A/D is varied by adjusting the 100kΩ trim resistor, R_5. Since the reference voltage will have a tempco of 1ppm/°C, typically, and the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as stable external resistors are used.

In Figure 8, note that the 0.22μF auto-zero capacitor is connected directly between the C_{AZ} pin and analog ground SENSE. A_3 forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for a conversion time of 40μs. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

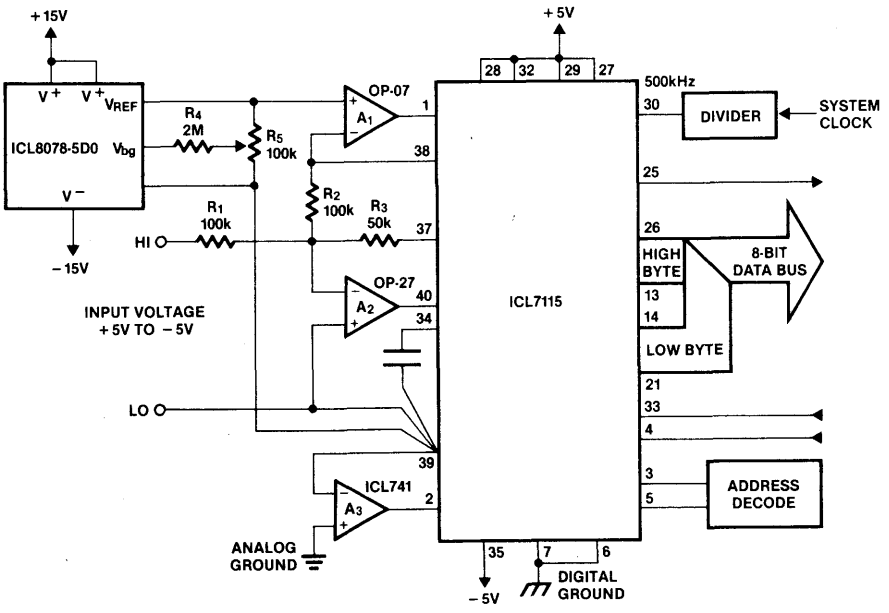


Figure 8. Typical Application with Bipolar Input Range, Forced Ground, and Heated-Substrate Reference

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 9 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 8, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1. A flip-flop in IC_3 sets IC_2's Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from IC_1, IC_2, and A_1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% of full-scale and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

The ICL7115 provides an internal inverter, OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}} \text{ for 14-bit operation}$$

and

$$f_{CLK} = \frac{18}{t_{conv}} \text{ for 12-bit operation}$$

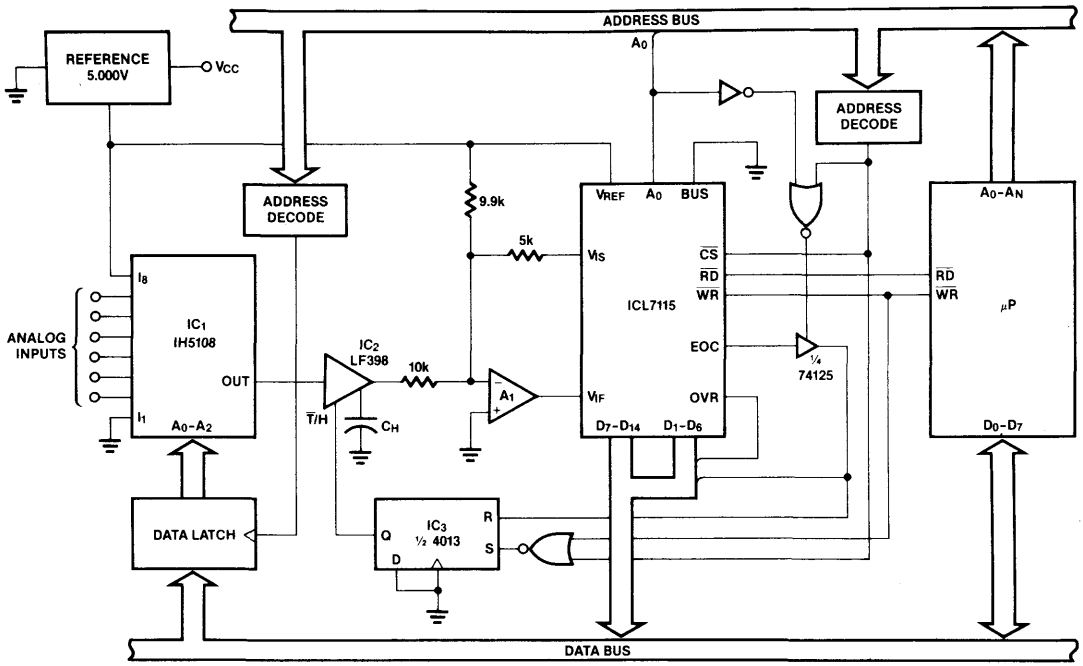
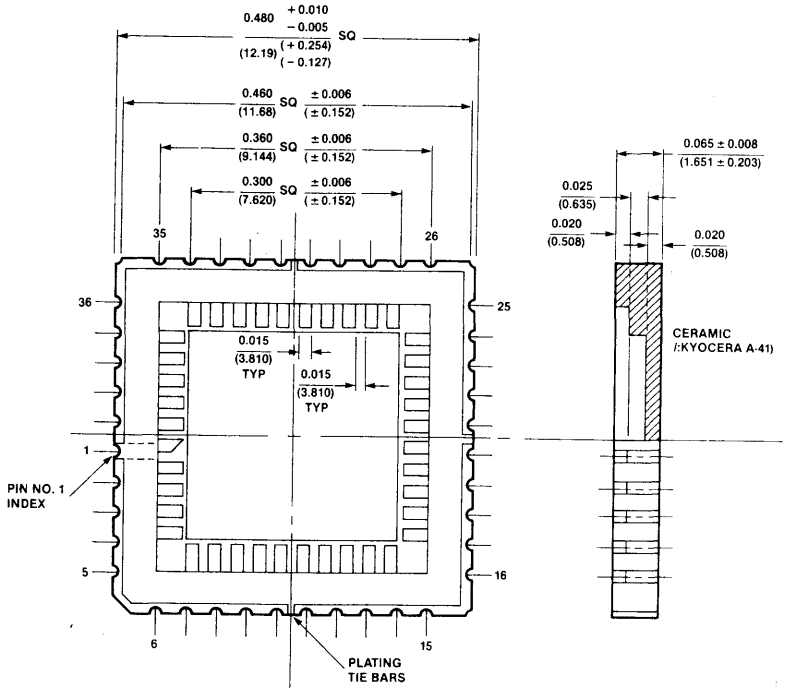
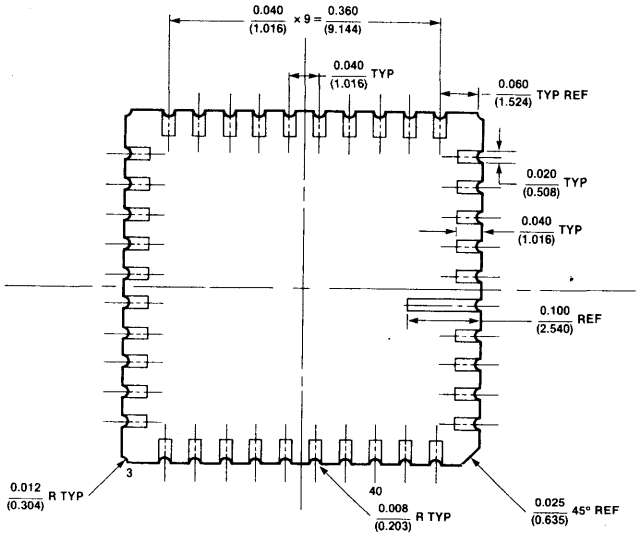


Figure 9. Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

PACKAGE OUTLINES All dimensions are in inches (millimeters)





Note 1: Finish: Gold plated 60 micro inches minimum thickness over nickel plated.
Note 2: Pin number 1 connected to die attach pad ground

Leadless Chip Carrier

ICL7116/7117

3½-Digit Single Chip A/D Converter with Display Hold

FEATURES

- **HOLD Reading Input allows indefinite display hold**
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA input current typical.**
- **True differential input**
- **Direct display drive - no external components required. — LCD ICL7116**
  — LED ICL7117
- **Low noise - less than 15μV pk-pk typical.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**

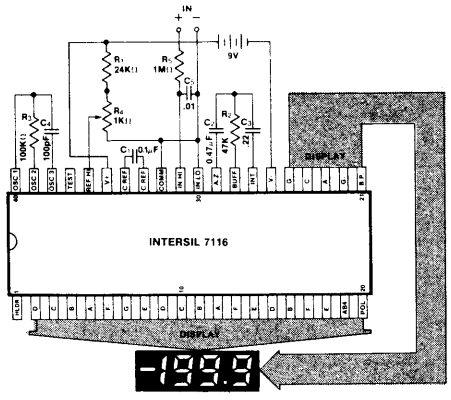
GENERAL DESCRIPTION

The Intersil ICL7116 and 7117 are high performance, low power 3-1/2 digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

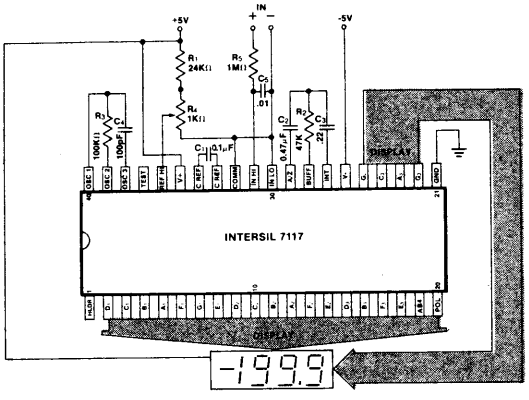
The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7116), enabling a high performance panel meter to be built with the addition of only seven passive components and a display.

4

TYPICAL CONNECTION DIAGRAMS



ICL7116 with Liquid Crystal Display

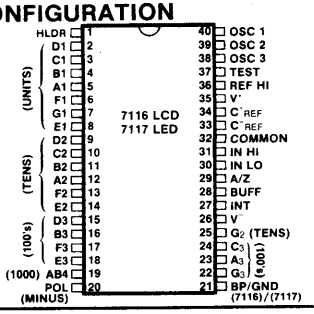


ICL7117 with LED Display

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7116	0°C to +70°C	40-Pin Ceramic DIP	ICL7116CDL
7116	0°C to +70°C	40-Pin Plastic DIP	ICL7116CPL
7116	0°C to +70°C	40 Pin CERDIP	ICL7116CJL
7117	0°C to +70°C	40-Pin Ceramic DIP	ICL7117CDL
7117	0°C to +70°C	40-Pin Plastic DIP	ICL7117CPL
7117	0°C to +70°C	40-Pin CERDIP	ICL7117CJL

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V to V^-
Reference Input Voltage (either input) ..... V to V^-
HLDR, Clock Input ..... Test to V^+
Power Dissipation (Note 2)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

ICL7117

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
HLDR, Clock Input ..... Gnd to V^+
Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ −1.5			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ - V^- = 9V$	4 4	5 5	6 6	V
7117 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

TEST CIRCUITS

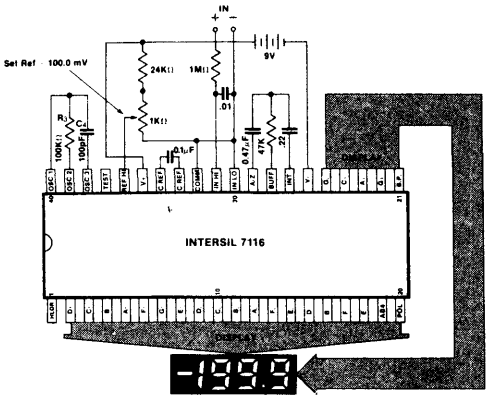


Figure 1: 7116

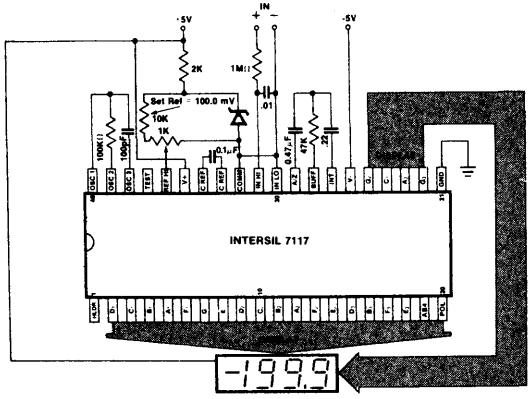


Figure 2: 7117

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

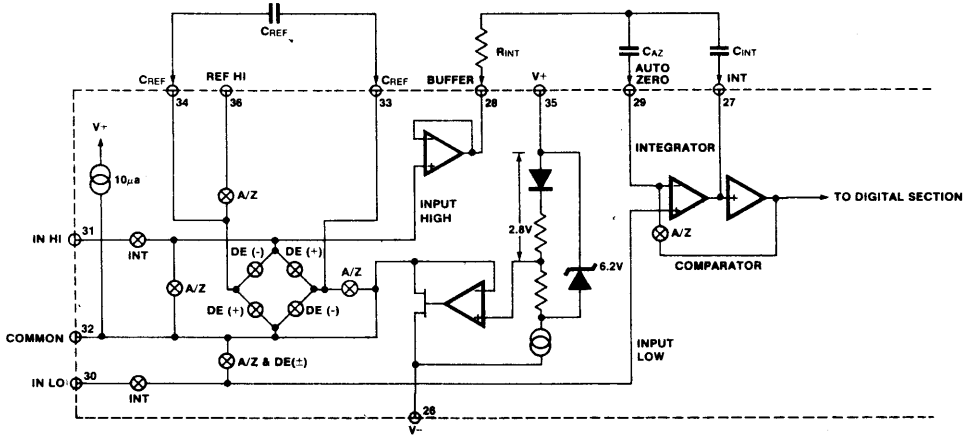


Figure 3: Analog Section of 7116/7117

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{Vin}{Vref})$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

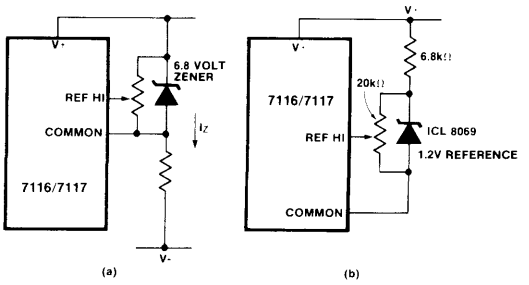


Figure 4: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

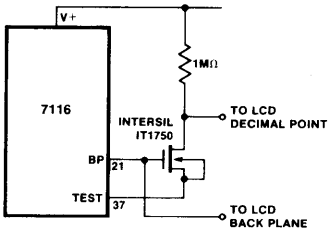


Figure 5: Simple Inverter for Fixed Decimal Point

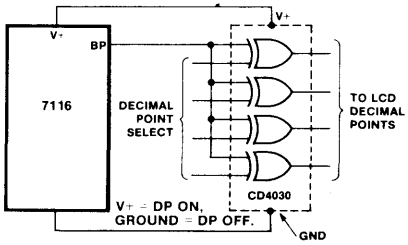


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled to high (to V^+) all segments will be turned on and the display should read - 1888. **[Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]**

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the 7117. It is identical except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "HI". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70k typical resistance to either TEST (7116) or GROUND (7117).

4

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

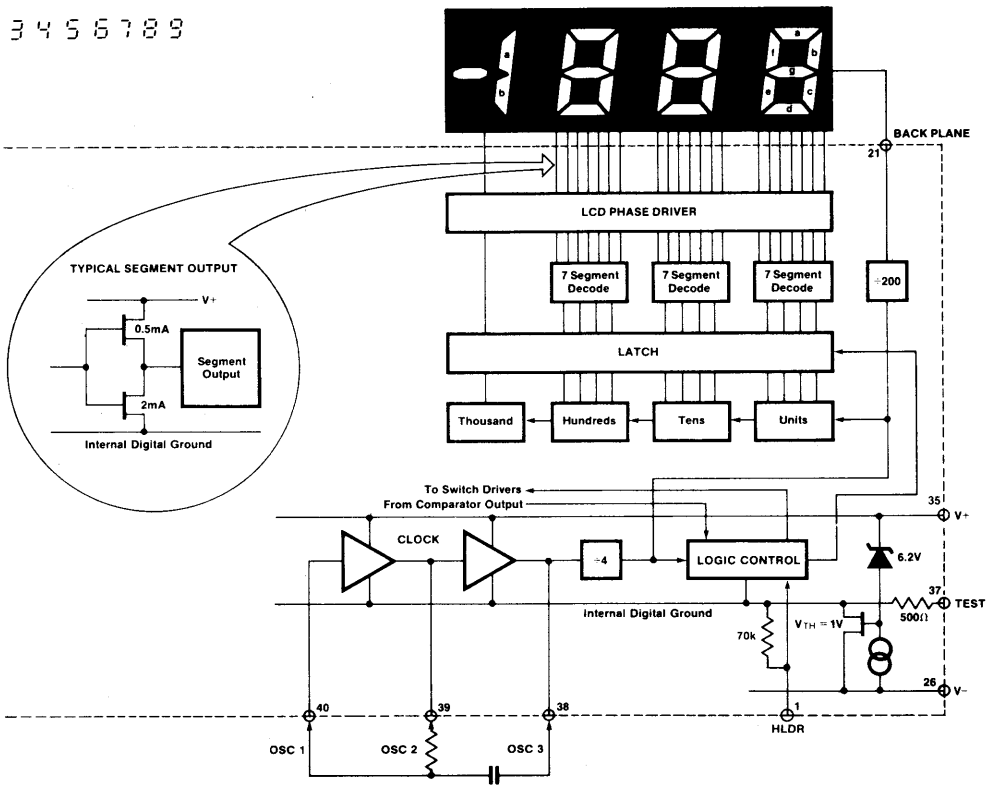


Figure 7: Digital Section 7116

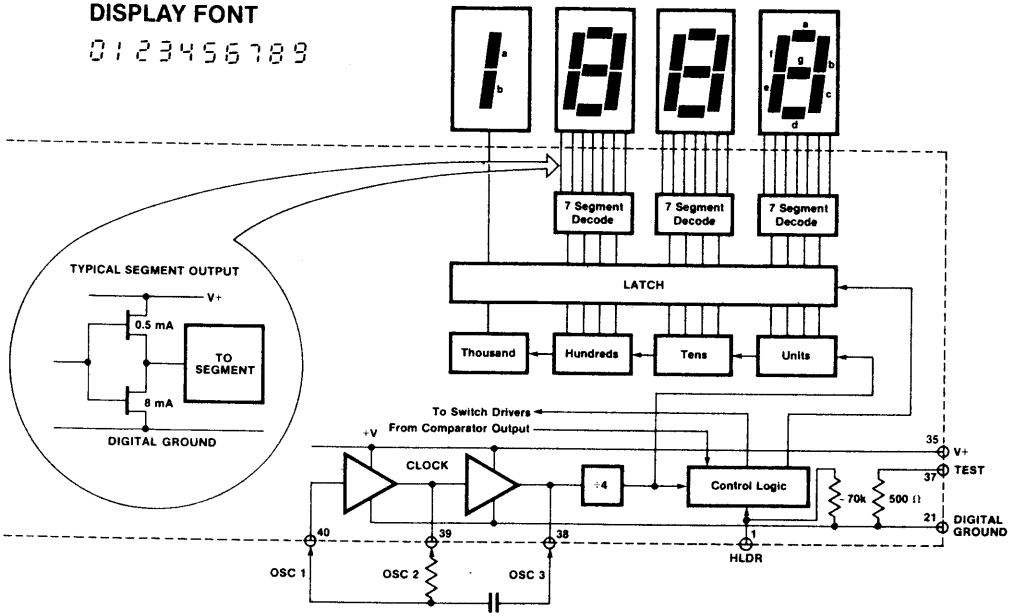


Figure 8: Digital Section 7117

System Timing

Figure 9 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

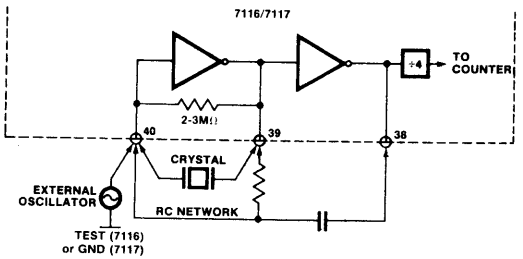


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ±2volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are 0.22 and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

5. Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} = 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

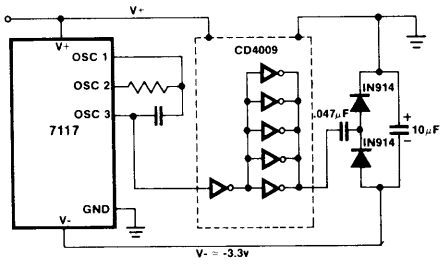


Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

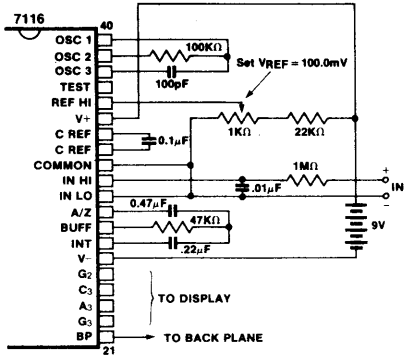


Figure 11: 7116 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

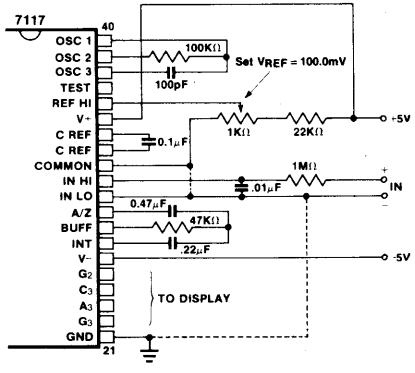


Figure 12: 7117 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)

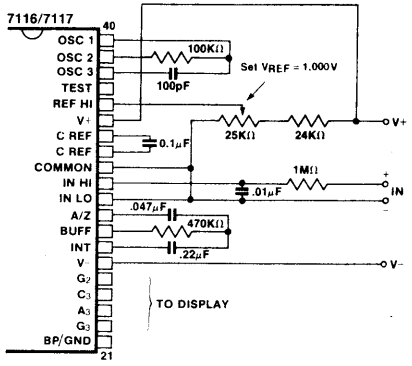


Figure 13: 7116/7117: Recommended component values for 2.000V full scale.

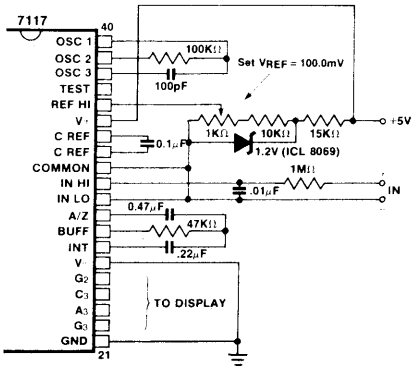


Figure 14: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

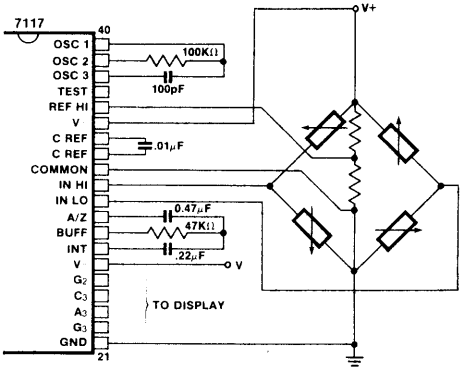


Figure 15: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

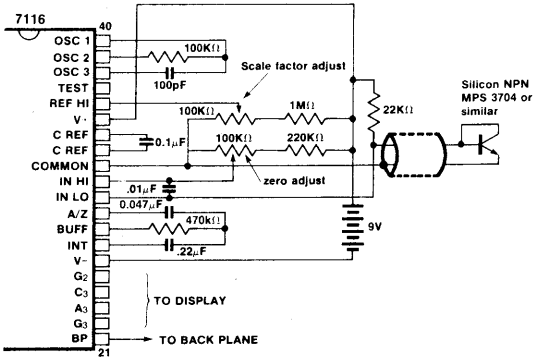


Figure 16: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

APPLICATION NOTES

A016"Selecting A/D Converters," by David Fullagar.
A017"The Integrating A/D Converter," by Lee Evans.
A018"Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A019"4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.
A023"Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032"Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
A046"Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
A047"Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
A052"Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

ICL7126

Single-Chip 3½-Digit Low-Power A/D Converter

FEATURES

- **Guaranteed zero reading for 0 Volts input on all scales**
- **True polarity at zero for precise null detection**
- **1pA typical input current**
- **True differential input and reference**
- **Direct LCD display drive — no external components required**
- **Pin compatible with the ICL7106**
- **Low noise — less than 15μV p-p**
- **On-chip clock and reference**
- **Low power dissipation guaranteed less than 1mW**
- **No additional active circuits required**
- **Evaluation Kit available (ICL7126EV/KIT)**
- **8,000 hours typical 9 Volt battery life**

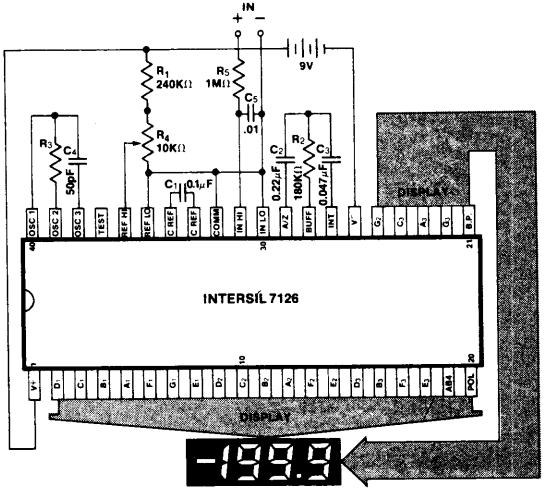
GENERAL DESCRIPTION

The Intersil ICL7126 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is 100μA, ideally suited for 9V battery operation.

The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

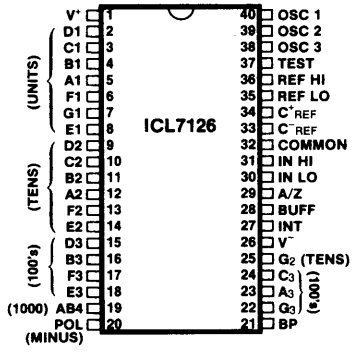
The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

4



ICL7126 with Liquid Crystal Display

PIN CONFIGURATION



ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7126	0°C to +70°C	40-Pin Ceramic DIP	ICL7126CDL
7126	0°C to +70°C	40-Pin Plastic DIP	ICL7126CPL
7126	0°C to +70°C	40-Pin CERDIP	ICL7126CJL
7126 Kit		Evaluation Kits	ICL7126EV/KIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0 (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to pos. supply)	250KΩ between Common & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250KΩ between Common & pos. Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion.
Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less then 50mV.
Note 6: During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 2, increases current by 8μA (typ).

TEST CIRCUITS

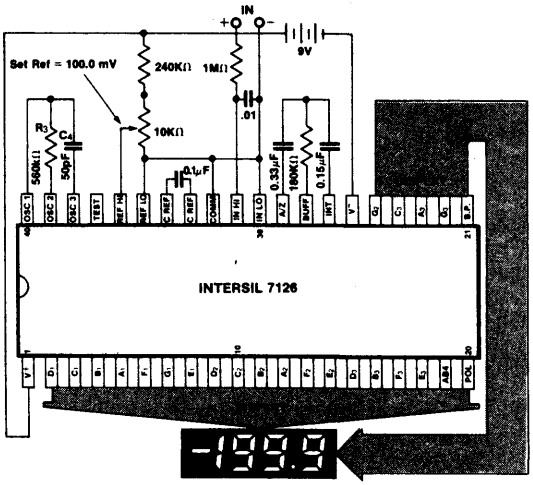


Figure 1: 7126 Clock Frequency 16kHz. (1 reading/sec)

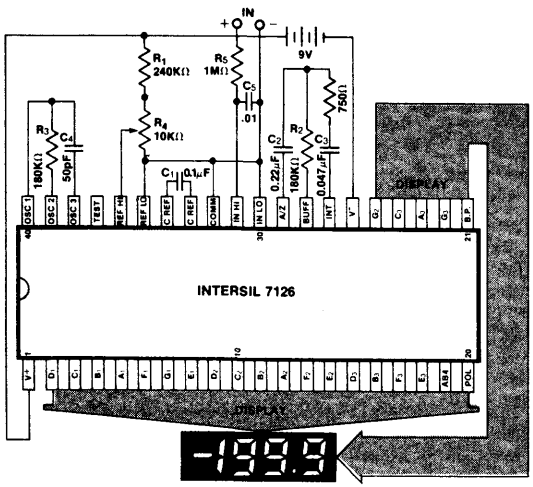


Figure 2: Clock Frequency 48kHZ. (3 readings/sec)

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

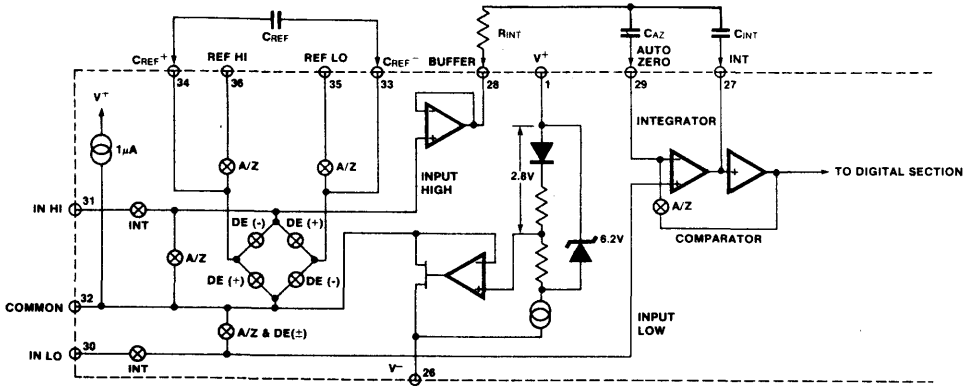


Figure 3: Analog Section of 7126

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less then 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{IN}}{V_{REF}})$.

Differential Input

The input can accept differential voltages anywhere within the common mode rante of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (–) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low

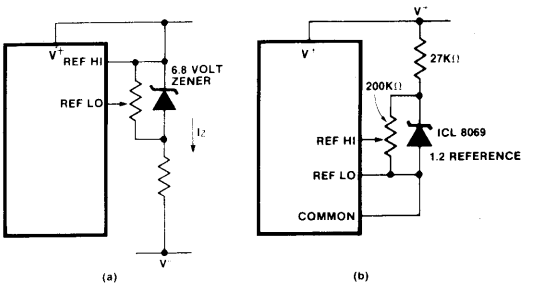


Figure 4: Using an External Reference

output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 100μA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

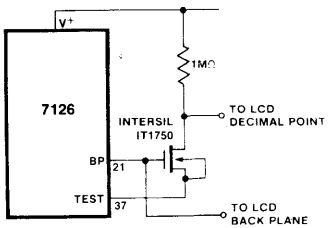


Figure 5: Simple Inverter for Fixed Decimal Point

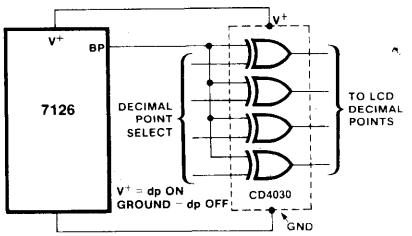


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Figure 7 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

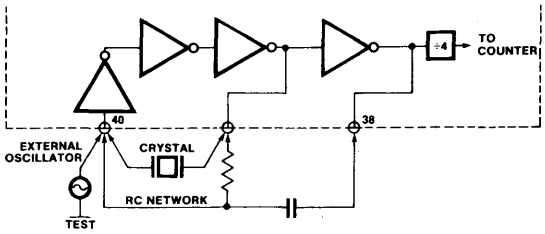


Figure 8: Clock Circuits

System Timing

Figure 8 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000

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DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

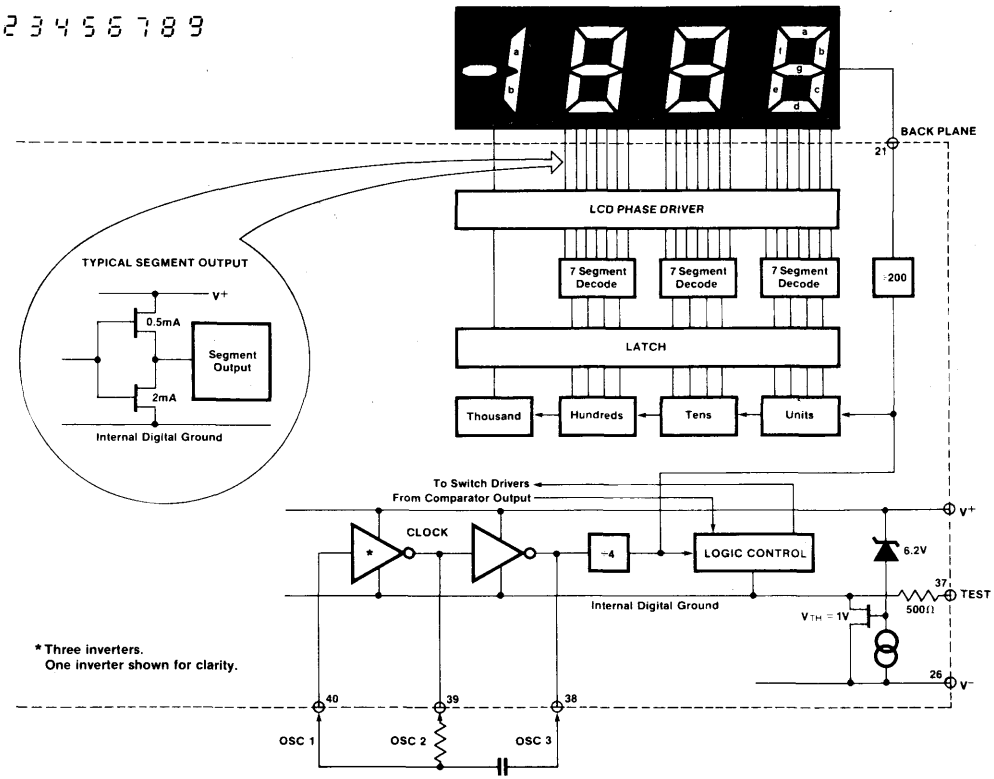


Figure 7: Digital Section

counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8MΩ is near optimum and similarly 180kΩ for a 200.0mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48kHz clock (3 readings/second), R = 180kΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 Volt scale, V_{REF} should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

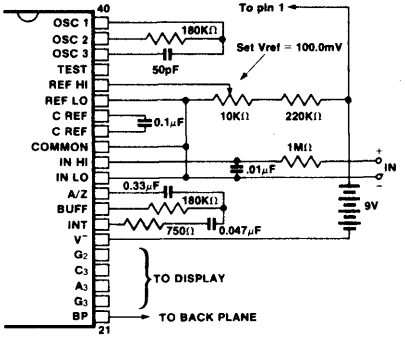


Figure 9: 7126 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

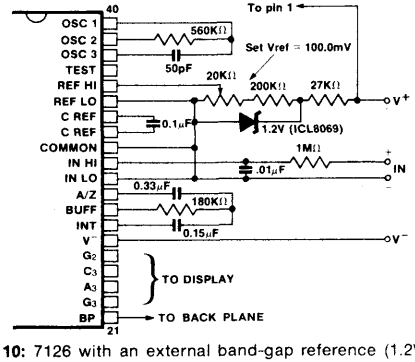


Figure 10: 7126 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.

TYPICAL APPLICATIONS (Contd.)

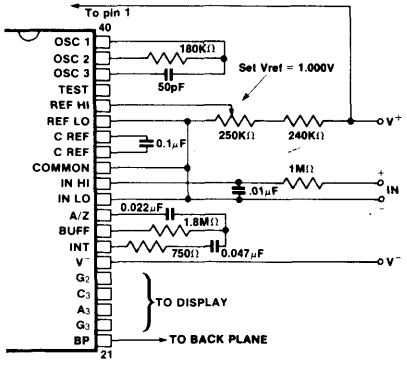


Figure 11: Recommended component values for 2.000V full scale, 3 readings per second. For 1 reading per second, delete 750Ω resistor, change C_{INT}, R_{OSC} to values of Fig. 10.

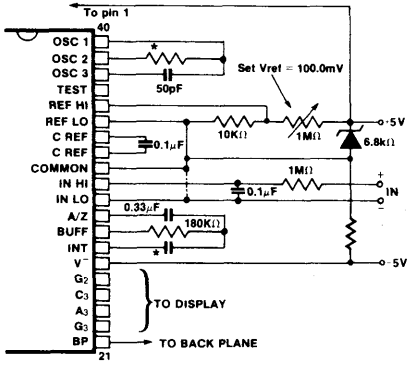


Figure 12: 7126 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

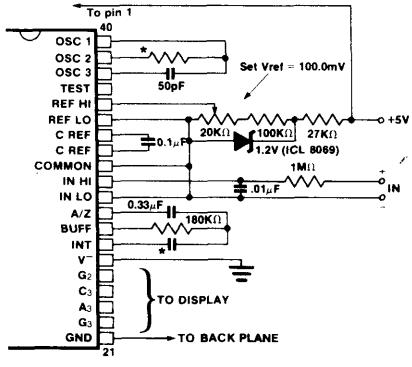


Figure 13: 7126 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

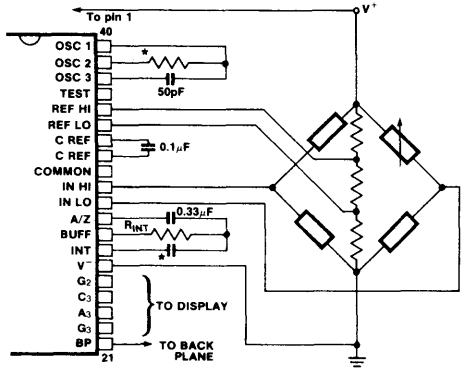


Figure 14: 7126 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

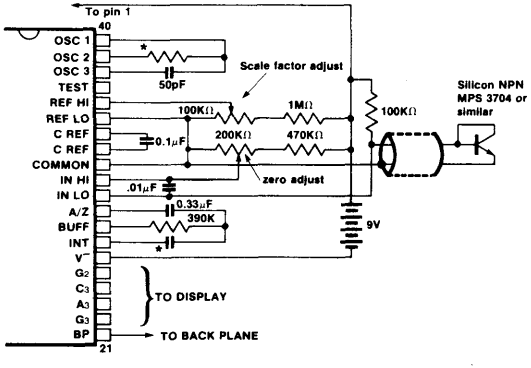


Figure 15: 7126 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

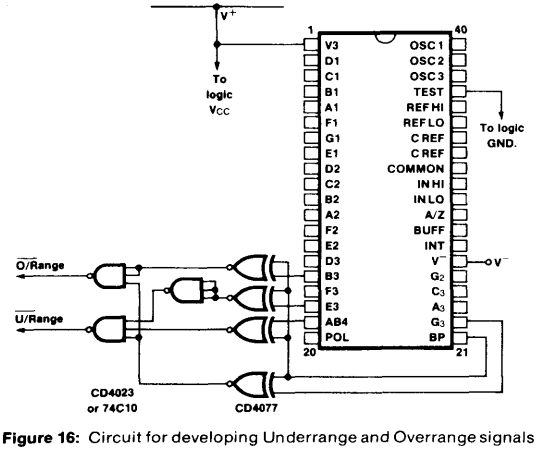


Figure 16: Circuit for developing Underrange and Overrange signals from 7126 outputs.

*Values depend on clock frequency. See Figure 9, 10, 11.

TYPICAL APPLICATIONS (Contd.)

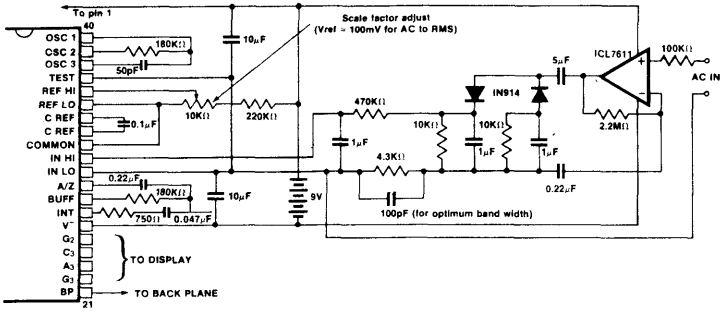


Figure 17: AC to DC Converter with 7126. Test is used as a common mode reference level to ensure compatibility with most op-amps.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

7126 EVALUATION KITS

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

ICL7129

4½-Digit Single-Chip A/D Converter

FEATURES

- ±19,999 count A/D converter accurate to ±1 count
- 10μV resolution on 200mV scale
- 110dB CMRR
- Direct LCD display drive
- True differential input and reference
- Low power consumption
- Decimal point drive outputs
- Overrange and underrange outputs
- Low battery detection and indication
- 10:1 range change input

ORDERING INFORMATION

PART	PACKAGE	TEMPERATURE	ORDER NUMBER
7129	40-Pin CERDIP	0°C to +70°C	ICL7129CJL
7129	40-Pin Plastic	0°C to +70°C	ICL7129CPL
7129	40-Pin Plastic	0°C to +70°C	ICL7129RCPL
7129	Dice	0°C to +70°C	ICL7129C/D
7129	Flat Pack		

GENERAL DESCRIPTION

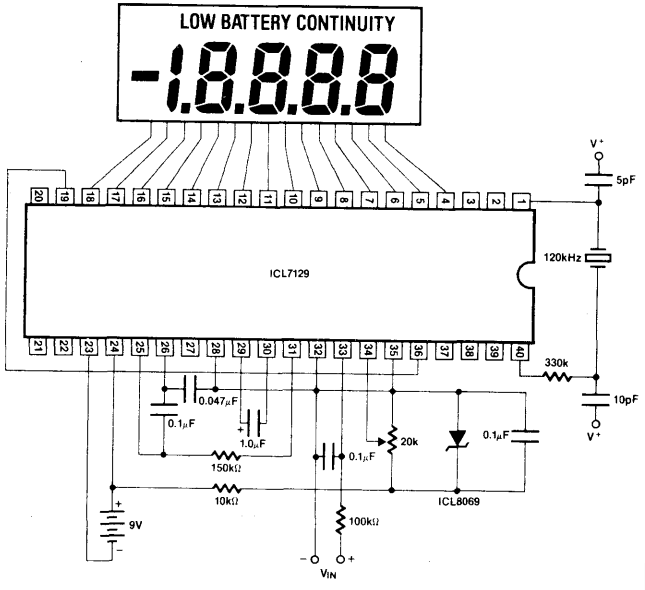
The Intersil ICL7129 is a very high-performance 4½-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. And it is ideal for high-resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10μV/count.

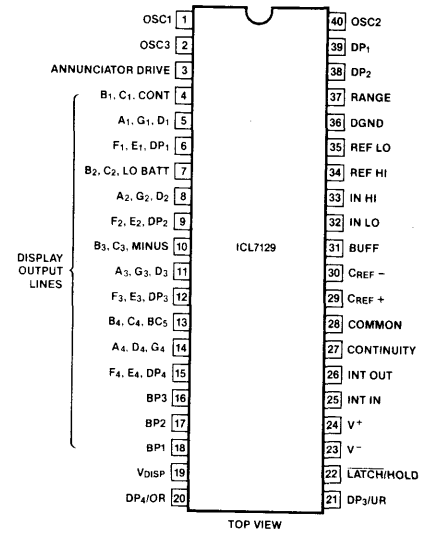
The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible signal. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

4

TYPICAL APPLICATION



PIN CONFIGURATION (outline dwg JL, PL)



ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND – 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+

Power Dissipation (Note 2)
CERDIP package 1000mW
Plastic package 800mW
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... – 65°C to + 160°C
Lead Soldering Temperature ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ± 400μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ± 1mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = + 25°C, f_{CLK} = 120kHz, unless otherwise noted.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0V 200mV Scale	– 0000	0000	+ 0000	Reading
Zero Reading Drift	V_{IN} = 0V 0°C < T_A < + 70°C		± 0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	– V_{IN} = + V_{IN} = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) – 0.5	V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0V 200mV Scale		7.0		μV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33		1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0°C < T_A < + 70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = + 0.1V		0.6		mA
COMMON Source Current	ΔCommon = – 0.1V		12		μA
DGND Voltage	V^+ to Pin 36 V^+ to V^- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = + 0.5V		1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate	f_{CLK} = 120kHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+		50		kΩ

ELECTRICAL CHARACTERISTICS (Continued) V^+ to V^- = 9V, V_{REF} = 1.00V, T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = Hi V_{OUT} Pin 27 = LO	100	200 200	 400	mV
Pull-Down Current	Pins 37, 38, 39		2	10	µA
"Weak Output" Current Sink, Source	Pin 20, 21		3.3		µA
	Pin 27 Sink/Source		3.9		
Pin 22 Source Current Pin 22 Sink Current			40 3		µA

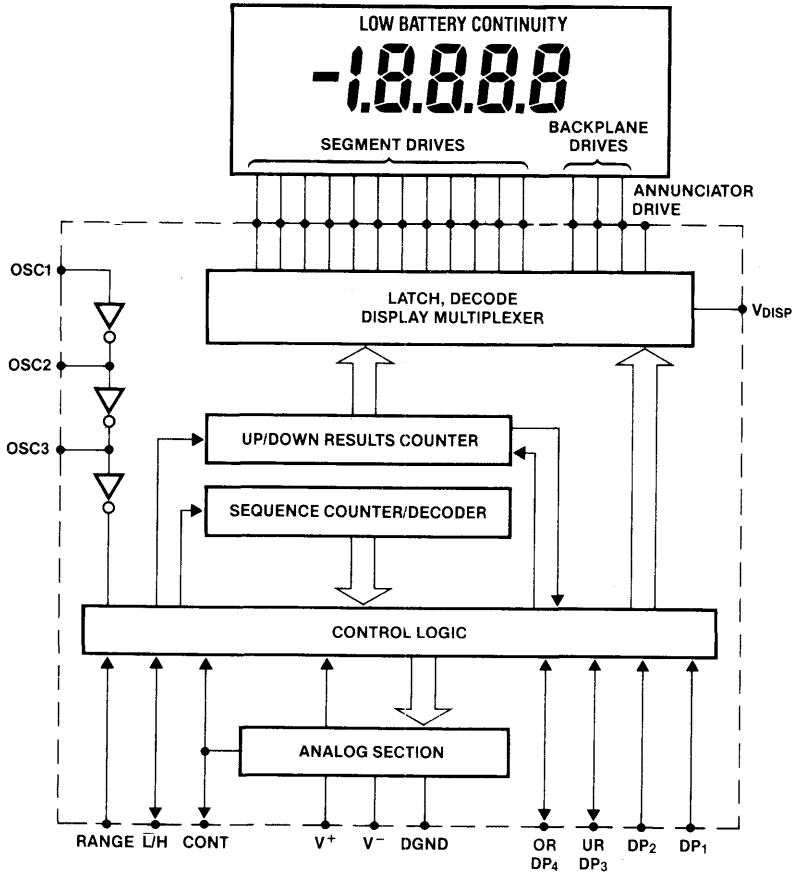


Figure 1. Simplified Block Diagram of ICL7129 Digital Section

Table 1. Pin Assignments and Functions

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	$C_{REF}+$	Positive side of external reference capacitor.
30	$C_{REF}-$	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

DETAILED OPERATION DESCRIPTION

Intersil's ICL7129 is a uniquely designed single-chip A/D converter. It features a new "successive integration" technique to achieve 10μV resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are instead cancelled using digital techniques. Savings in external parts cost are realized as well as improved noise performance and elimination of a source electromagnetic and electrostatic pick-up.

The overall block diagram of the ICL7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 2 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 3 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

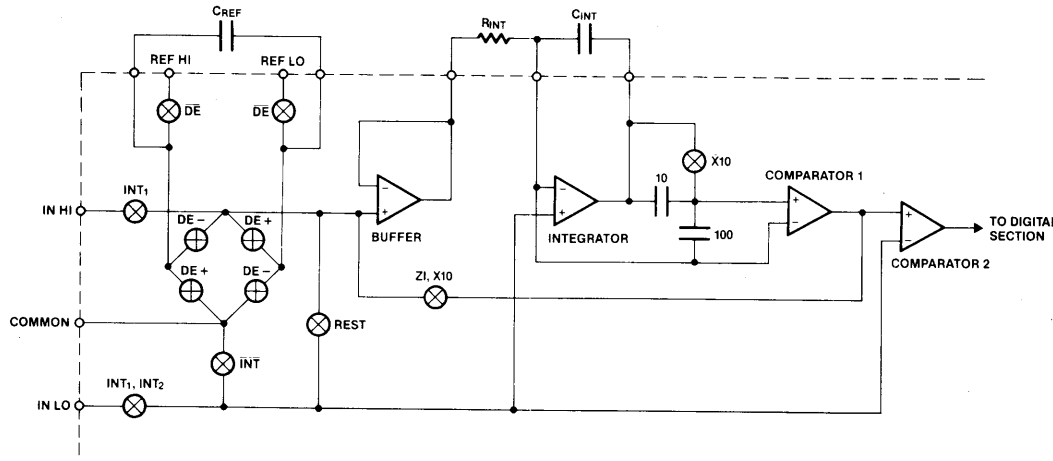


Figure 2. ICL7129 Analog Block Diagram

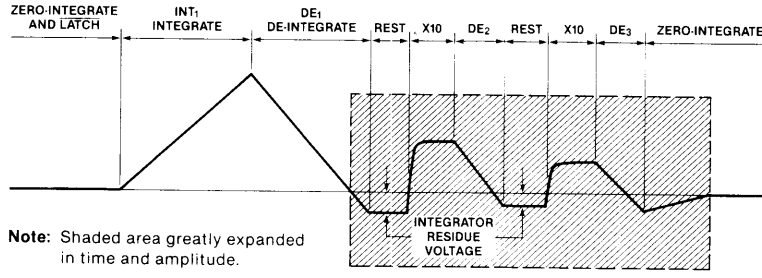


Figure 3. Integrator Waveform for Negative Input Voltage Showing Successive Integration Phases and Residue Voltage

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This was obtained by feeding counts into the results counter at the 3½ digit level during DE_1, into the 4½ digit level during DE_2 and the 5½ digit level for DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.005% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, AND "LOW BATTERY"

The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes (Figure 4). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V^+ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to insure that these outputs are not overloaded. Figure 5 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 6 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12μA while DGND has no source capability.

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V^+ and V^- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V^- rail in Figure 4. As the supply voltage decreases, the n-channel transistor connected to the V-rail eventually turns off and the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

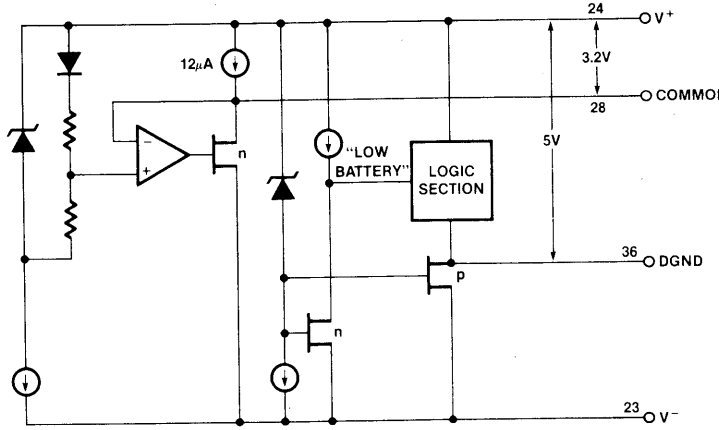


Figure 4. Biasing Structure for COMMON and DGND

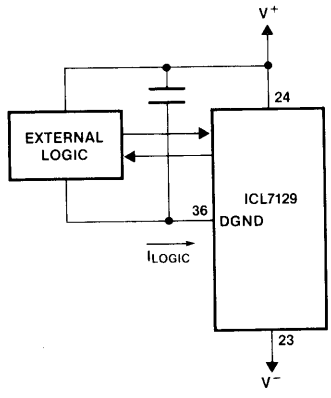


Figure 5. DGND Sink Current

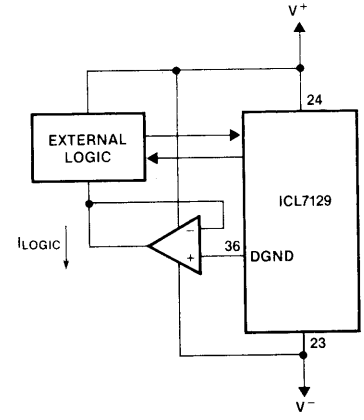


Figure 6. Buffered DGND

I/O PORTS

Four of the pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described on the Pin Assignments and Functions (Table 1). If the output function of the pin is not desired in an application it can easily be overriden by connecting the pin to V^+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 7. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3μA, nominally.

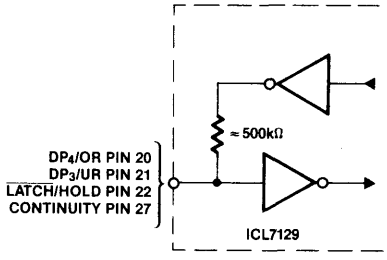


Figure 7. "Weak Output"

LATCH/HOLD, OVERRANGE, AND UNDERRANGE TIMING

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Assignments and Functions (Table 1).

INSTANT CONTINUITY

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 8). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability. Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

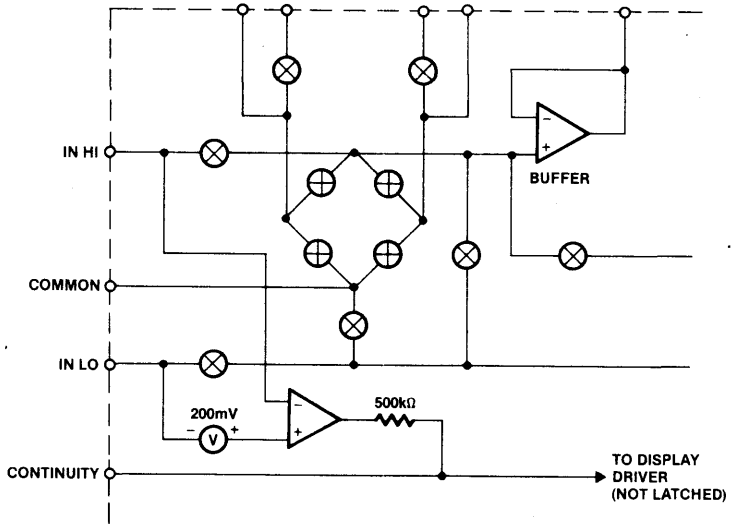


Figure 8. "Instant Continuity" Comparator and Output Structure

DISPLAY CONFIGURATION

The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 9. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

ANNUNCIATOR DRIVE

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V^+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 10 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 11.

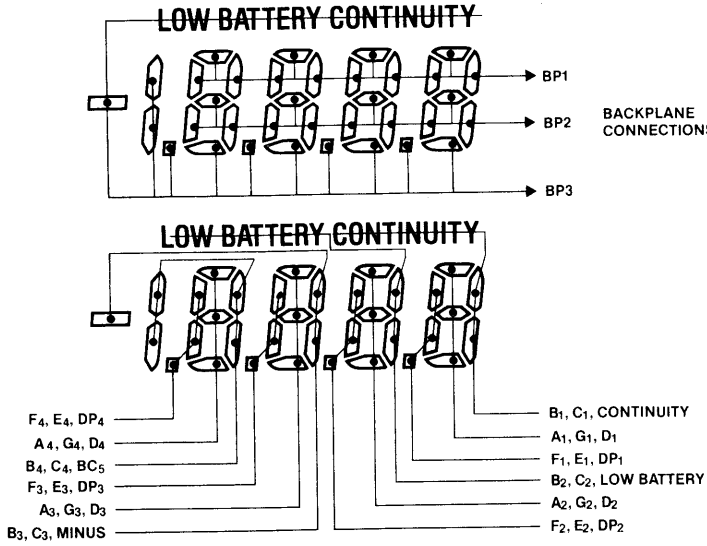


Figure 9. Triplexed Liquid Crystal Display Layout for ICL7129

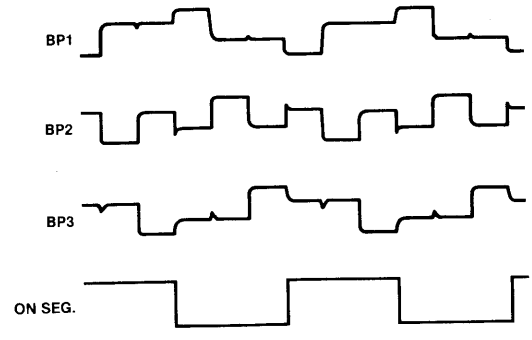


Figure 10. Typical Backplane and Annunciator Drive Waveforms

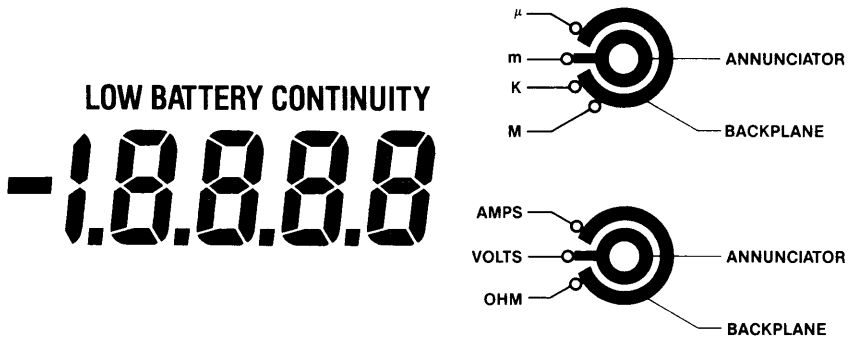


Figure 11. Multimeter Example Showing Use of Annunciator Drive Output

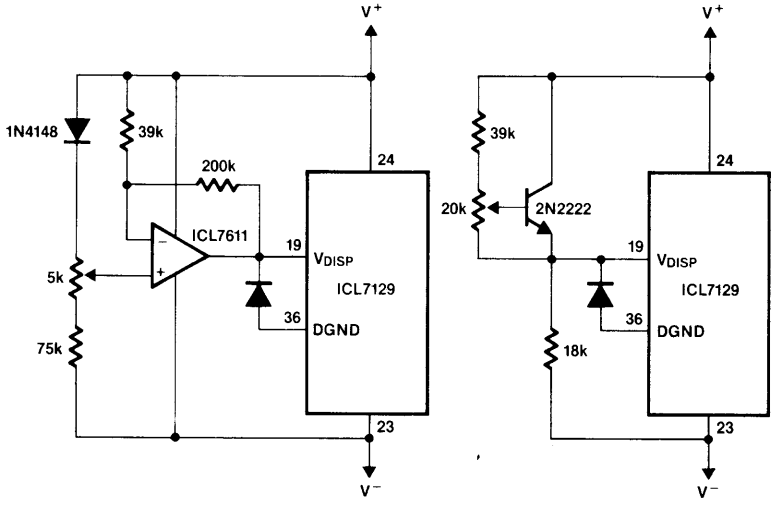


Figure 12. Two Methods for Temperature Compensating the Liquid Crystal Display

DISPLAY TEMPERATURE COMPENSATION

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 12 shows two circuits that can be adjusted to give a temperature compensation of $\approx +10mV/°C$ between V^+ and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected on the chip if V_{DISP} is more negative than DGND.

COMPONENT SELECTION

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is **no** auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150k should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect

rollover error if the swing gets too close to the positive rail (≈0.7V). This gives an optimum swing of ≈2.5V at full-scale. For 150k integrating resistor and 2 conversions per second the value is 0.10μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0μF value is recommended.

CLOCK OSCILLATOR

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

In low resolution applications, where the converter uses only 3½ digits and 100μV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from $f_{OSC} = 0.45/RC$. However, when the converter is used to its full potential (4½ digits and 10μV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 13.

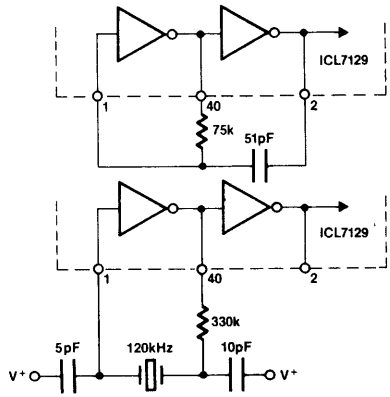


Figure 13. RC and Crystal Oscillator Circuits

POWERING THE ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 14, 15, and 16 show various powering modes that may be used with the ICL7129.

The standard battery connection using a 9V battery is shown on the front page of this data sheet.

The power connection for systems with +5V and −5V supplies available is shown in Figure 14. Notice that measurements are with respect to ground. COMMON is not connected to INPUT LO but is used only as a pre-regulator for the external voltage reference.

It is important to notice that in Figure 14, digital ground of the ICL7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V^+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 5 and 6. In Figure 5, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 6. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

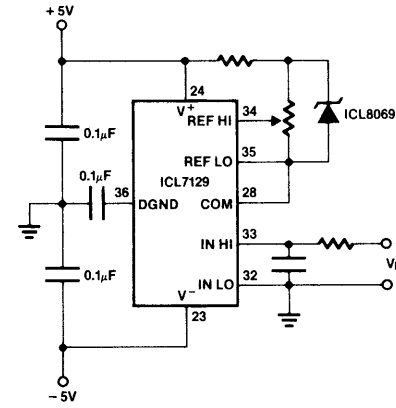


Figure 14. Powering the ICL7129 from +5V and −5V Power Supplies

When a battery voltage between 3.8V and 7V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 15.

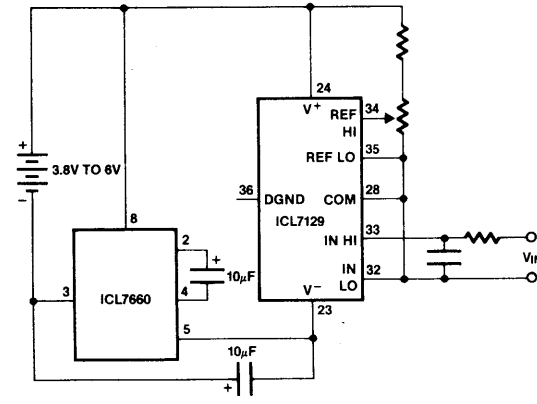


Figure 15. Powering the ICL7129 from a 3.8V to 6V Battery

Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 16 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

VOLTAGE REFERENCES

The COMMON output of the ICL7129 has a temperature coefficient of ±80ppm/°C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram on the front page of this data sheet shows the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129 and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.

Figures 17 and 18 show two other methods for generating precision references that are compatible with the ICL7129. Both reference voltage and input voltage are connected to power supply ground. The use of a 6.2V reference diode is shown in Figure 18. The voltage drop across $R_1 \approx 2.8V$ to minimize rollover error caused by stray capacitance charging or discharging the reference capacitor. The reference voltage in this case is taken with respect to V^+ and is adjusted with the trim potentiometer connected to REF LO (pin 35).

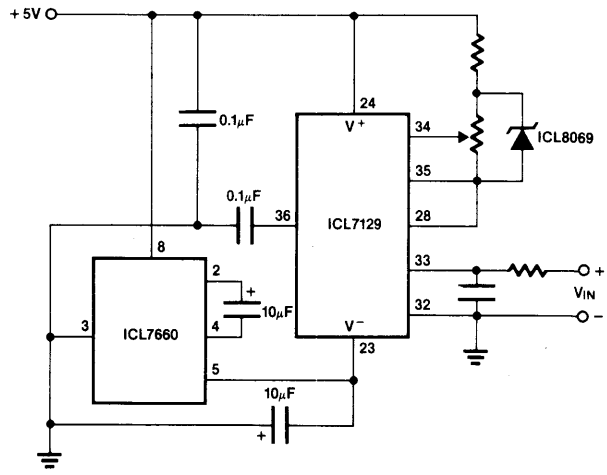


Figure 16. Powering the ICL7129 from a Single Polarity Power Supply

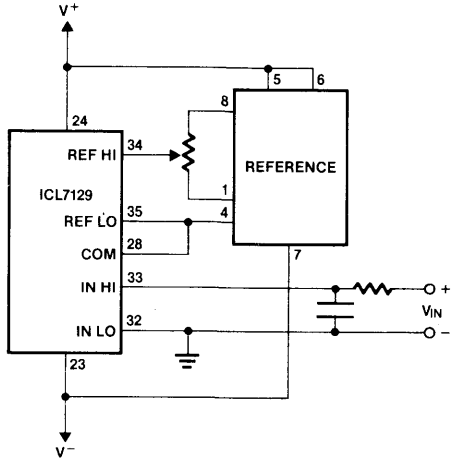


Figure 17. Using a Heated-Substrate 1.000V Reference with the ICL7129

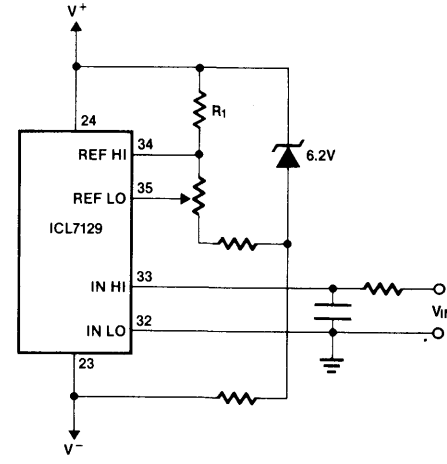


Figure 18. Using a 6.2V Reference Diode with the ICL7129

ICL7134

14-Bit μP-Compatible Multiplying D/A Converter

FEATURES

- **14-bit linearity (0.003% FSR)**
- **No gain adjustment necessary**
- **Microprocessor-compatible with double buffered inputs**
- **Bipolar application requires no extra adjustments or external resistors**
- **Output current settling-time 3μs max (0.9μs typ)**
- **Low linearity and gain temperature coefficients**
- **Low power dissipation**
- **Full four-quadrant multiplication**
- **Full temperature range operation**

4

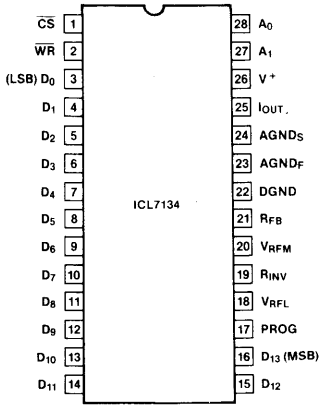
GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistors and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent.

The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

PIN CONFIGURATION



(outline dwg JI)

ORDERING INFORMATION

NON-LINEARITY	TEMPERATURE RANGE		
	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
Bipolar Versions			
0.01% (12-bit)	ICL7134BJCJI	ICL7134BJIJI	ICL7134BJMJI
0.006% (13-bit)	ICL7134BKCJI	ICL7134BKIJI	ICL7134BKMJI
0.003% (14-bit)	ICL7134BLCJI	ICL7134BLIJI	ICL7134BLMJI
Unipolar Versions			
0.01% (12-bit)	ICL7134UJCJI	ICL7134UJIJI	ICL7134UJMJI
0.006% (13-bit)	ICL7134UKCJI	ICL7134UKIJI	ICL7134UKMJI
0.003% (14-bit)	ICL7134ULCJI	ICL7134ULIJI	ICL7134ULMJI

Package: 28-pin CERDIP only

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to DGND) ..... −0.3V to 7.5V
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND ..... ±25V
I_{OUT}, $AGND_F$, $AGND_S$ ..... −0.1V to V^+
Current in $AGND_S$, $AGND_F$ 25mA
An, Dn, $\overline{WR}$, $\overline{CS}$, PROG ..... −0.3V to V^+ +0.3V
Operating Temperature Range
ICL7134XXC ..... 0°C to +70°C
ICL7134XXI ..... −20°C to +85°C
ICL7134XXM ..... −55°C to +125°C

Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 2) 500mW
Derate Linearly Above 70°C @ 10mW/°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: All voltages with respect to DGND.
Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

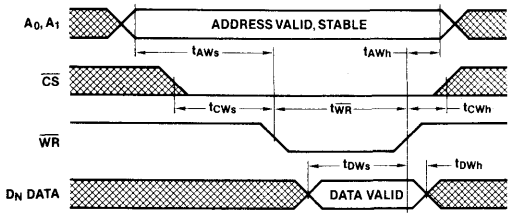
OPERATING CHARACTERISTICS (V^+ = 5V, V_{REF} = 10V, T_A = +25°C unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Resolution				14			Bits
Non-Linearity	J		Test Figure 1 (Notes 1 and 2)			0.010	% FSR
	K					0.006	% FSR
	L					0.003	% FSR
Non-Linearity Temperature Coefficient			Operating Temperature Range		1	2	ppm/°C
Gain Error	J		Test Figure 1 (Notes 1 and 2)			0.020	% FSR
	K					0.012	% FSR
	L					0.006	% FSR
Gain Error Temperature Coefficient					2	8	ppm/°C
Monotonicity	J			14			Bits
	K			14			Bits
	L			14			Bits
I_{OUT} Leakage Current		I_{OLK}	T_A = +25°C			10	nA
			Operating Temperature Range		50		
Power Supply Rejection		PSRR	T_A = +25°C, ΔV^- = ±10%		1	50	ppm/V
			Operating Temperature Range			100	
Output Current Settling Time					0.9	3	µs
Feedthrough Error	ICL7134U		V_{REF} = ±10V, 2kHz Sinewave		250		µVp-p
	ICL7134B				500		
Reference Input Resistance		Z_{REF}	V_{RFL} = V_{RFM} (Unipolar Mode)	4.0		10	kΩ
Output Capacitance		C_{OUT}	DAC Register = All 0's		160		pF
			DAC Register = All 1's		235		
Output Noise			Equivalent Johnson Res.		7		kΩ
Low State Input		V_{INL}	Operating Temperature Range			0.8	V
High State Input		V_{INH}	Operating Temperature Range	2.4			V
Logic Input Current		I_{iin}	$0 \le V_{IN} \le V^+$			1.0	µA
Logic Input Capacitance		C_{iin}	(Note 3)		15		pF
Supply Voltage Range		V^+	Functional Operation	3.5		6.0	V
Supply Current		I^+	(Excluding Ladder)		0.06	0.5	mA
Long Term Stability			1000 Hours, +125°C (Note 3)		10		ppm/√month

Note 1: Full-Scale Range (FSR) is 10V for unipolar mode, 20V (±10V) for bipolar mode.
Note 2: Using internal feedback and reference inverting resistors.
Note 3: Guaranteed by design, not 100% tested in production.

AC CHARACTERISTICS (V^+ =5V, see Timing Diagram)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Address-WRite Set-Up Time (Min)	t_{AWs}				100	ns
Address-WRite Hold Time (Min)	t_{AWh}				0	
Chip Select-WRite Set-Up Time (Min)	t_{CWs}				0	
Chip Select-WRite Hold Time (Min)	t_{CWh}				0	
WRite Pulse Width Low (Min)	$t_{\overline{WR}}$				200	
Data-WRite Set-Up Time (Min)	t_{DWs}				200	
Data-WRite Hold Time (Min)	t_{DWh}				0	



Timing Diagram

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a straight line function between endpoints. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Table 1. Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION	
1	$\overline{CS}$	Chip Select (active low). Enables register write.	
2	$\overline{WR}$	WRite, (active low). Writes in register. Equivalent to $\overline{CS}$.	
3	D_0	Bit 0	Least significant.
4	D_1	Bit 1	Input Data Bits (High = True)
5	D_2	Bit 2	
6	D_3	Bit 3	
7	D_4	Bit 4	
8	D_5	Bit 5	
9	D_6	Bit 6	
10	D_7	Bit 7	
11	D_8	Bit 8	
12	D_9	Bit 9	
13	D_{10}	Bit 10	
14	D_{11}	Bit 11	
15	D_{12}	Bit 12	
16	D_{13}	Bit 13	Most significant.

PIN	SYMBOL	DESCRIPTION	
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{RFL}	V_{REF} for lower bits.	
19	R_{INV}	Summing node for reference inverting amplifier.	
20	V_{RFM}	V_{REF} for MSB only (bipolar).	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force line. Use to carry current from internal Analog GrouND connections. Tied internally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive supply voltage.	
27	A_1	Address 1	Control register lines
28	A_0	Address 0	

TEST CIRCUITS (Unipolar operation shown)

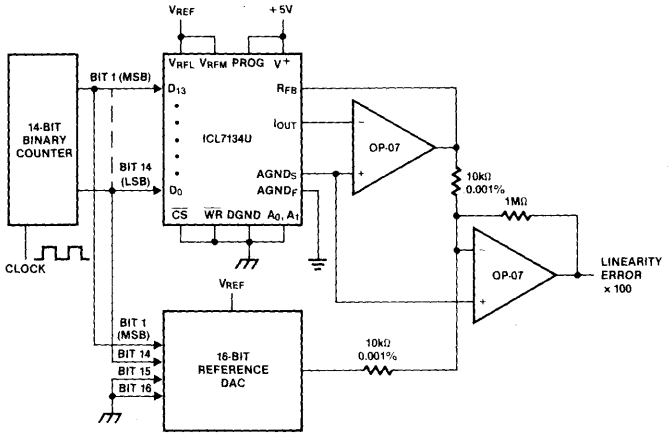


Figure 1. Non-Linearity

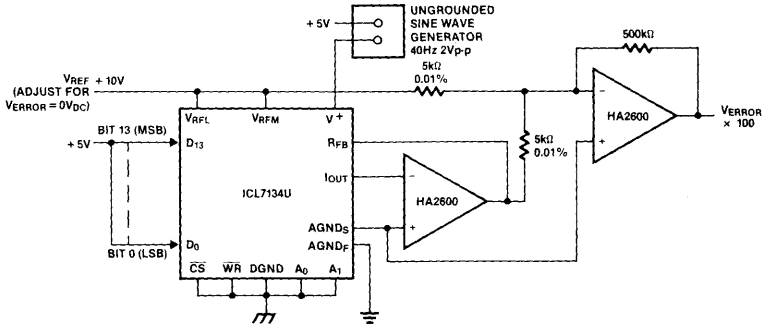


Figure 2. Power Supply Rejection

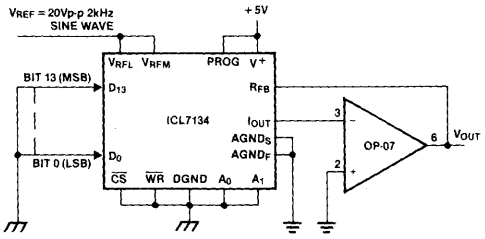


Figure 3. Feedthrough Error

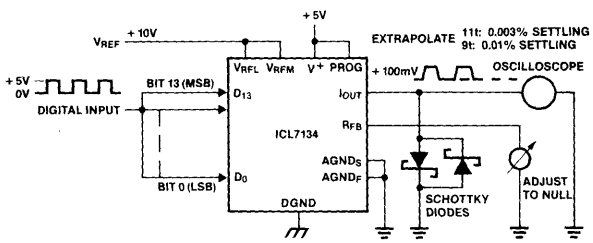


Figure 4. Output Current Settling Time

FUNCTIONAL DIAGRAM

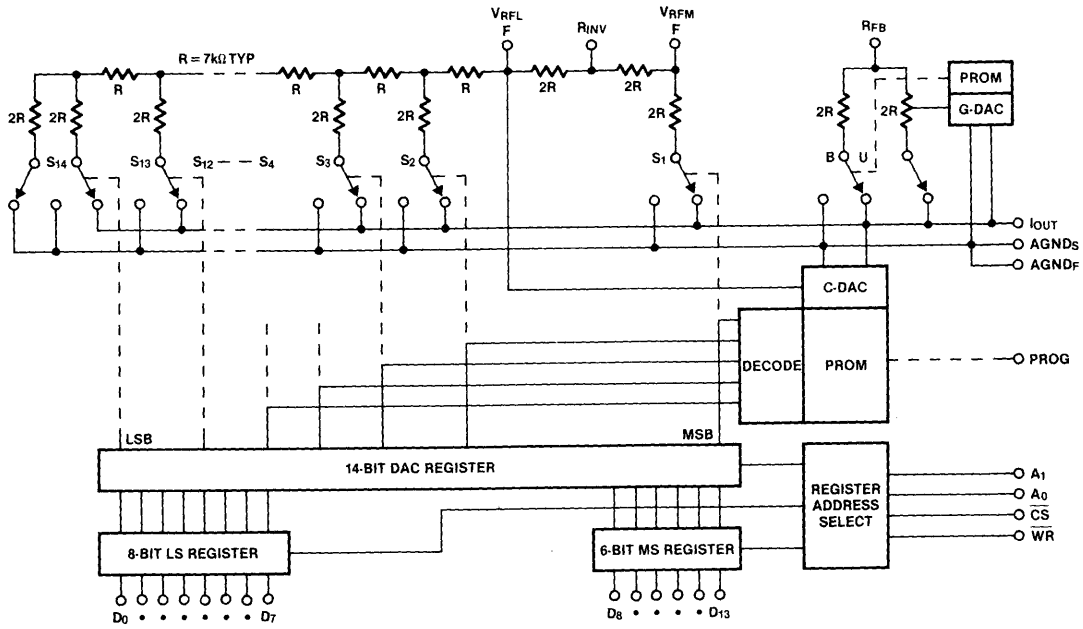


Figure 5. ICL7134 Functional Diagram

DETAILED DESCRIPTION

The ICL7134 consists of a 14-bit primary DAC, two PROM controlled correction DACs, input buffer registers, and microprocessor interface logic (Figure 5). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC, or G-DAC, diverts up to 2% of the feedback resistor's current to Analog GrouND and reduces the gain error to less than 1 LSB, or 0.006%. The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC, or C-DAC. For every combination of the primary DAC's 5 most significant bits, a different C-DAC code is selected. This allows correction of superposition errors, caused by bit interaction on the primary resistor ladder's current output bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method which corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging. These packaging shifts limit the accuracy that can be achieved using wafer level correction methods such as laser trimming, which has also been found to degrade the time stability of thin film resistors at the 14-bit level.

Analog Section

The ICL7134 inherently provides both unipolar and bipolar operation. The bipolar application circuit (Figure 6) requires one additional op-amp but no external resistors. The two on-chip resistors, R_{INV1} and R_{INV2}, together with the op-amp, form a voltage inverter which drives the MSB reference terminal, V_{RFM}, to $-V_{REF}$, where V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL}. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF}, and the R_{INV} pin is left unconnected.

Since the PROM correction codes required are different for bipolar and unipolar operation, the ICL7134 is available in two different versions; the ICL7134U, which is corrected for unipolar operation, and the ICL7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from 'R' in the unipolar device to '2R' in the bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

Digital Section

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations: 1) load the LS-buffer register with the data at inputs D_0 to D_7; 2) load the MS-buffer register with the data at inputs D_8 to D_{13}; 3) load the DAC register with the contents of the MS and LS-buffer registers and 4) load the DAC register directly from the data input pins (see Table 2). The $\overline{CS}$ and $\overline{WR}$ pins must be low to allow data transfers to occur. When direct loading is selected ($\overline{CS}$, $\overline{WR}$, A_0 and A_1 low) the registers are transparent, and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to V^+ (+5V).

Table 2. Data Loading Controls

CONTROL I/P				ICL7134 OPERATION
A_0	A_1	$\overline{CS}$	$\overline{WR}$	
X	X	X	1	No operation, device not selected.
X	X	1	X	
0	0	0	0	Load all registers from data bus.
0	1	0	0	Load LS register from data bus.
1	0	0	0	Load MS register from data bus.
1	1	0	0	Load DAC register from MS and LS register.

Note: Data is latched on LO-HI transition of either $\overline{WR}$ or $\overline{CS}$.

APPLICATIONS

General Recommendations

Ground Loops

Careful consideration must be given to ground loops in any 14-bit accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, the $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 7. Thus output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

Operational Amplifier Selection

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than 25μV) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10V range also requires that the output amplifier has a high open loop gain (A_{VOL} > 400k for effective input offset less than 25μV).

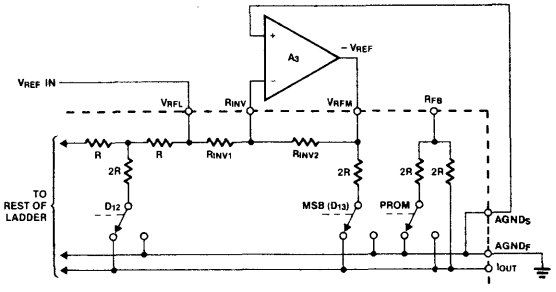


Figure 6. Bipolar Operation, with Inverted V_{REF} to MSB

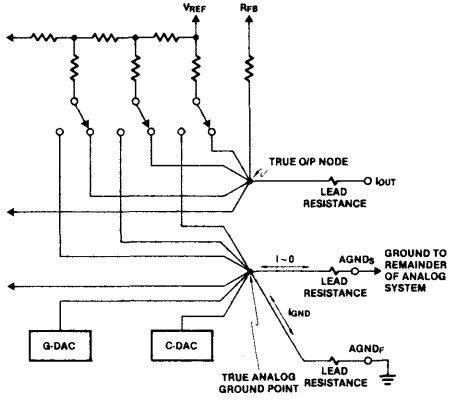


Figure 7. Eliminating Ground Loops

The reference inverting amplifier used in the bipolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than 50μV), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the Analog GrouND line (op-amp A_2 in Figure 9). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than 50μV).

The op-amp requirements can be readily met by use of an ICL7650 chopper stabilized device. For faster settling time, an HA26XX can be used with an ICL7650 providing automatic offset null (see A053 for details).

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

4

Power Supplies

The V^+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V^+, which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V^+ for proper operation.

Unipolar Binary Operation (ICL7134U)

The circuit configuration for unipolar mode operation (ICL7134U) is shown in Figure 8. With positive and negative V_{REF} values the circuit is capable of two-quadrant multiplication. The "digital input code/analog output value" table for unipolar mode is given in Table 3. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers. For applications where the output reference ground point is established somewhere other than at the DAC, the circuit of Figure 9 can be used. Here, op-amp A_2 removes the slight error due to IR voltage drop between the internal Analog GrouND node and the external ground connection. For 13-bit or lower accuracy, omit A_2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.

Table 3. Code Table -Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 1/2^{14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2 + 1/2^{14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2 - 1/2^{14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Zero Offset Adjustment

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V ±50μV at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of the output op-amp, A_1, for a maximum of 0V ±50μV at V_{OUT}.

Gain Adjustment (Optional)

1. Connect all data inputs to V^+, connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Monitor V_{OUT} for a $-V_{REF}(1 - 1/2^{14})$ reading.
3. To decrease V_{OUT}, connect a series resistor of 100Ω or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT}, connect a series resistor of 100Ω or less between A_1 output and the R_{FB} terminal (pin 21).

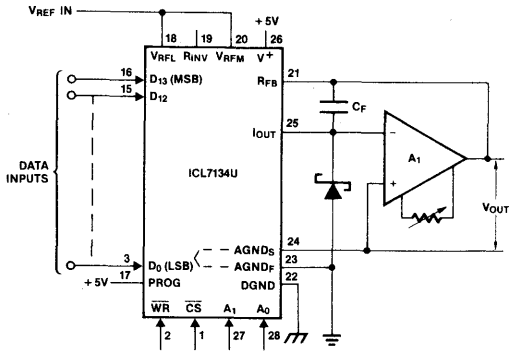


Figure 8. Unipolar Binary, Two-Quadrant Multiplying Circuit

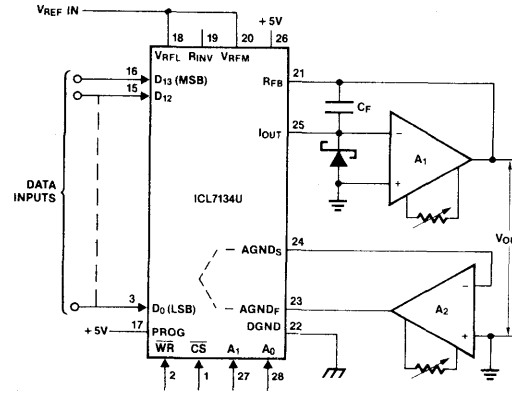


Figure 9. Unipolar Binary Operation with Forced Ground

Bipolar (2's Complement) Operation (ICL7134B)

The circuit configuration for bipolar mode operation (ICL7134B) is shown in Figure 10. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. The "digital input code/analog output value" table for bipolar mode is given in Table 4. Amplifier A_3, together with internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the ICL7134B's feedback resistance is switched to 2R under PROM control, so that the bipolar output range is $+V_{REF}$ to $-V_{REF}(1-1/2^{13})$. Again, the grounding arrangement of Figure 9 can be used, if necessary.

Table 4. Code Table -Bipolar (2's Complement) Operation

DIGITAL INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-1/2^{13})$
0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{13})$
0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF}(1/2^{13})$
1 0 0 0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-1/2^{13})$
1 0 0 0 0 0 0 0 0 0 0 0 0	V_{REF}

Offset Adjustment

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust the offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V $\pm 50\mu V$ at $AGND_S$.
3. Set data to 00000....00. Adjust the offset zero-adjust trim-pot of the output op-amp A_1, for a maximum of 0V $\pm 50\mu V$ at V_{OUT}.
4. Connect D_{13} (MSB) data input to V^+.
5. Adjust the offset zero-adjust trim-pot of op-amp A_3 for a maximum of 0V $\pm 50\mu V$ at the R_{INV} terminal (pin 19).

Gain Adjustment (Optional)

1. Connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Connect D_0, $D_1 \ldots D_{12}$ to V^+, D_{13} (MSB) to DGND.
3. Monitor V_{OUT} for a $-V_{REF}(1-1/2^{13})$ reading.
4. To increase V_{OUT}, connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT}, connect a series resistor of 100Ω or less between the reference voltage and the V_{RFL} terminal (pin 18).

Processor Interfacing

The ease of interfacing to a processor can be seen from Figure 11, which shows the ICL7134 connected to an 8035 or any other MCS-48 processor such as an 8049. The data bus feeds into both register inputs; three port lines, in combination with the $\overline{WR}$ line, control the byte-wide loading into these registers and then the DAC register. A complete DAC set-up requires 4 write instructions to the port, to set up the address and $\overline{CS}$ lines, and 3 external data transfers, one a dummy for the final transfer to the DAC register.

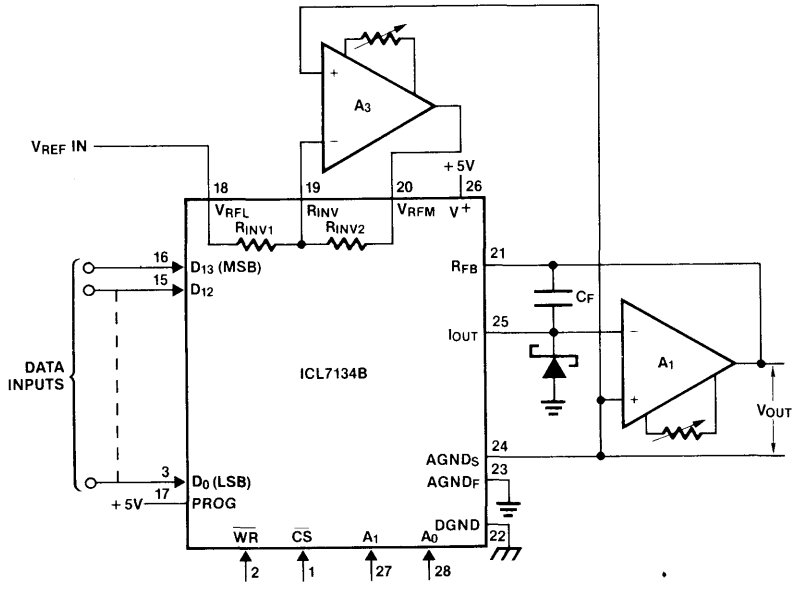


Figure 10. Bipolar (2's Complement), Four-Quadrant Multiplying Circuit

A similar arrangement can be used with the MCS-80 system, using an 8080A, 8228, and 8224 CPU set. Figure 12 shows the circuit, which can be arranged as a memory-mapped interface (using $\overline{\text{MEMW}}$) or as an I/O-mapped interface (using $\overline{\text{I/O WRITE}}$). See A020 and R005 for discussions of the relative merits of memory-mapped versus I/O-mapped interfacing, as well as some other ideas on interfacing with 8080 processors. The MCS-85 family 8085 processor has a very similar interface, except that the control lines available are slightly different, as shown in Figure 13. The decoding of the IO/$\overline{\text{M}}$ line, which controls memory-mapped or I/O-mapped operation, is arbitrary, and can be omitted if not necessary.

Neither the MC-680X nor MCS-650X processor families offer specific I/O operations. Figure 14 shows a suitable interface to either of these systems, using a direct connection. Several other decoding options can be used, depending on the other control signals generated in the system. Note that the MCS-650X family does not require VMA to be decoded with the address lines.

Figure 15 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read directly from the microprocessor data bus in an 8-bit and a 6-bit word. The flag lines control the data destination.

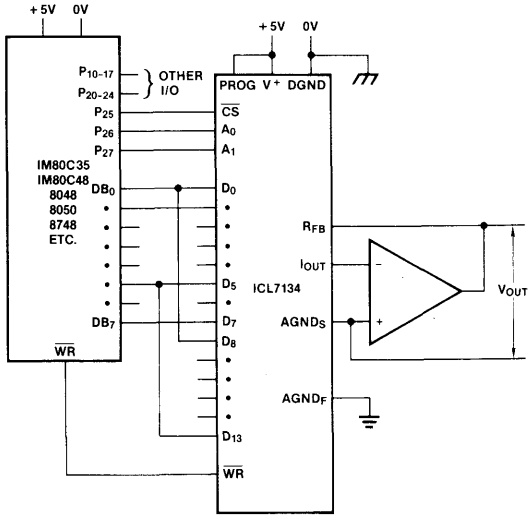


Figure 11. ICL7134 Interface to MCS-48 System

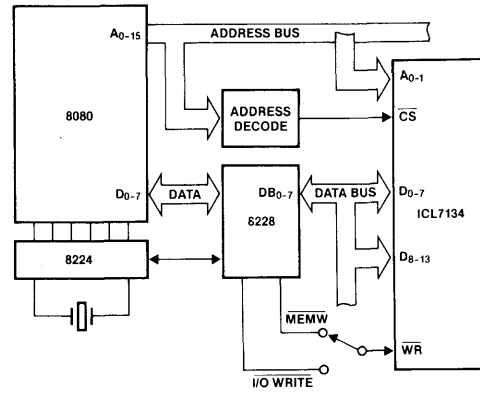


Figure 12. Interface to MCS-80 System

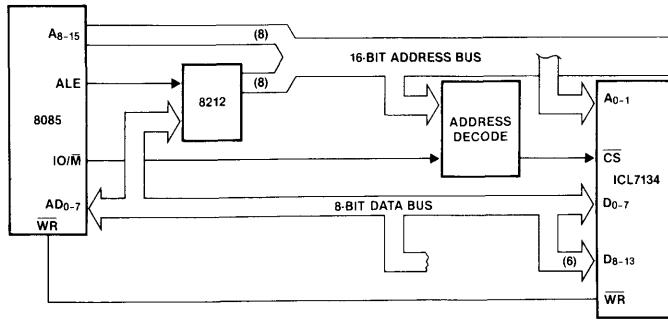


Figure 13. MCS-85 System Interface

Digital Feedthrough

All of the direct interfaces shown above can suffer from a capacitive coupling problem. The 14 data pins, and 4 control pins, all tied to active lines on a microprocessor bus, and in close proximity to the sensitive DAC circuitry, can couple pseudo-random spikes into the analog output. Careful board layout and shielding can minimize the problems (see **PC layout**), and clearly wire-wrap type sockets should never be used. Nevertheless, the inherent capacitance of the package alone can lead to unacceptable digital feedthrough in many cases. The only solution is to keep the digital input lines as inactive as possible. One easy way to do this is to use the peripheral interface circuitry available with all the systems previously discussed. These generally allow only 8 bits to be updated at any one time, but a little ingenuity will avoid difficulties with DAC steps that would result from partial updates. The problem can be solved for the MCS-48 family by tying the 14 port lines to the data input lines, with $\overline{CS}$, A_0 and A_1 held low, and using only the $\overline{WR}$ line to enter the data into the DAC (as shown in Figure 16). $\overline{WR}$ is well separated from the analog lines on the ICL7134, and is usually not a very active line in MCS-48 systems. Additional "protection" can be achieved by gating the processor $\overline{WR}$ line with another port line. The heavy use of port lines can be alleviated by use of the IM82C43 port expander. The same type of technique can be employed in the MCS-80/85 systems by using an 8255 PIA (peripheral interface adapter) (Figure 17) and in the MC-680X and MCS-650X systems by using an MC-6820 (MCS-6520) PIA.

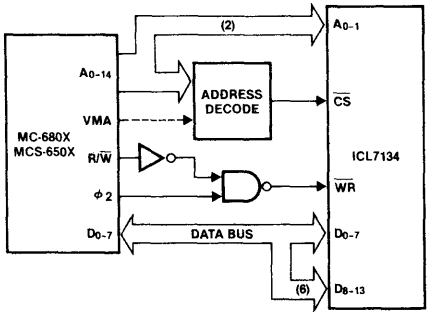


Figure 14. MCS-650X and MC-680X Families' Interface to ICL7134

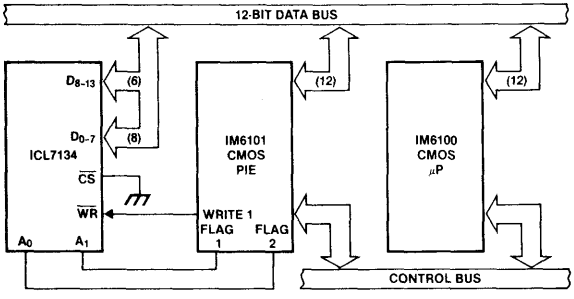


Figure 15. ICL7134 to IM6100 Interface Using IM6101 PIE

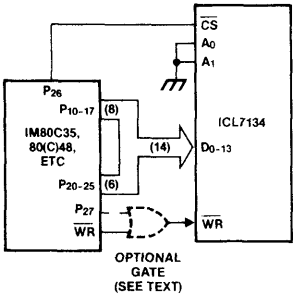


Figure 16. Avoiding Digital Feedthrough in an MCS-48 to ICL7134 Interface

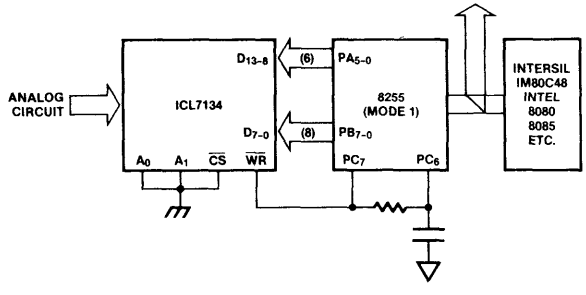


Figure 17. ICL7134 to MCS-48, -80, -85 Interface with Low Feedthrough

Successive Approximation A/D Converters

Figure 18 shows an ICL7134B-based circuit for a bipolar input high speed A/D converter, using two AM25L03s to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2605 front-end amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7650 is probably advisable (see A053). The clock, using two Schmitt trigger TTL gates, runs at a slower rate for the first 8 bits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; if fewer bits are required, it can be moved up accordingly. The circuit will free-run if the HOLD/$\overline{\text{RUN}}$ input is held low, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS output indicates when the device is operating, and the falling edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D_{13}) on an ICL7134U to pin 14 on the first AM25L03, deleting the reference inversion amplifier A_4, and tying V_{RFM} to V_{RFL}.

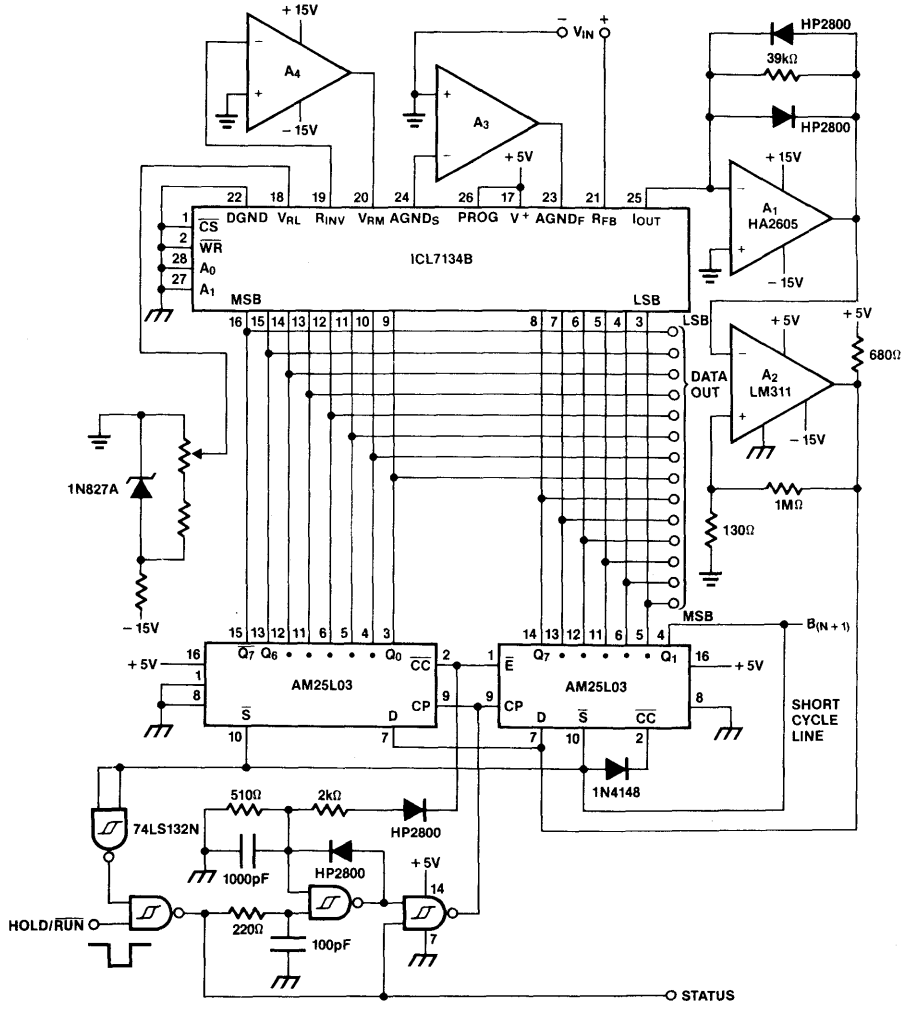


Figure 18. Successive Approximation A/D Converter

PC BOARD LAYOUT

Great care should be taken in the board layout to minimize ground loop and similar "hidden resistor" problems, as well as to minimize digital signal feedthrough. A suitable layout for the ICL7134 is shown in Figure 19, and may be used as a guide.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters," by Dave Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

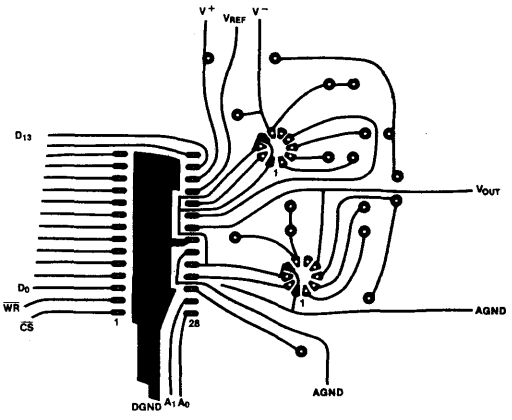
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

A021 "Power A/D Converters Using the ICH8510," by Dick Wilenken.

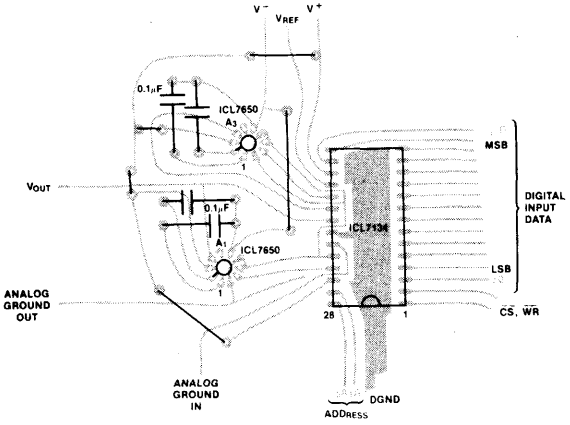
A030 "The ICL7104—A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Most of these are available in the Intersil Data Acquisition Handbook, together with other material.



(a) Printed Circuit Side of Card (Single Sided Board)



(b) Top Side with Component Placement

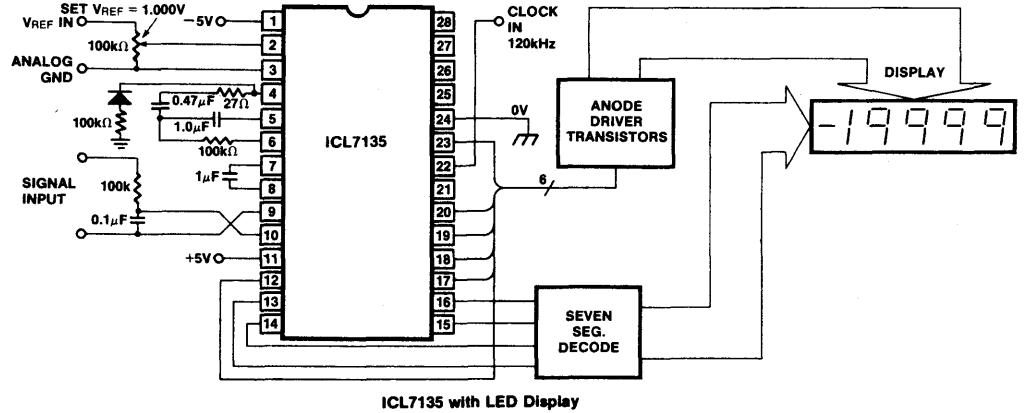
Figure 19. Printed Circuit Board Layout (Bipolar Circuit, see Figure 10)

ICL7135
Precision 4½ Digit Single Chip A/D Converter

FEATURES
- **Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)**
- **Guaranteed zero reading for 0 volts input**
- **1 pA typical input current**
- **True differential input**
- **True polarity at zero count for precise null detection**
- **Single reference voltage required**
- **Over-range and under-range signals available for auto-ranging capability**
- **All outputs TTL compatible**
- **Blinking display gives visual indication of over-range**
- **Six auxiliary inputs/outputs are available for interfacing to UARTs, microprocessors or other complex circuitry**
- **Multiplexed BCD output versatility**

GENERAL DESCRIPTION
The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The Intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDER-RANGE, RUN/HOLD and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

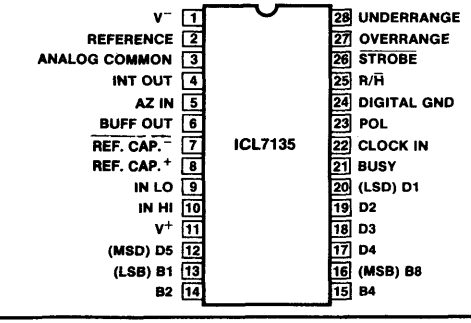


ICL7135 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7135	28-Pin CERDIP	0°C to +70°C	ICL7135CJI
7135	28-Pin Plastic DIP	0°C to +70°C	ICL7135CPI
EV/KIT	Evaluation Kit (PC Board, active, passive components)		ICL135EV/KIT

PIN CONFIGURATION (Outline dwgs JI, PI)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
- Ceramic Package ..... 1000 mW
- Plastic Package ..... 800 mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V^+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

$V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

	CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG	Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
ANALOG	Ratiometric Reading (2)		$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
ANALOG	Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
ANALOG	Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
ANALOG	Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
(Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full scale = 2.000V		15		μV
	Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
	Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le 70°C$		0.5	2	μV/°C
	Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0 \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL INPUTS	Clock In, Run/Hold, See Fig. 2	V_{INH} V_{INL} I_{INL} I_{INH}	 $V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V mA μA
DIGITAL OUTPUTS	All Outputs	V_{OL}	$I_{OL} = 1.6ma$		0.25	0.40	V
DIGITAL OUTPUTS	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	$I_{OH} = -1mA$	2.4	4.2		V
DIGITAL OUTPUTS	BUSY, $\overline{\text{STROBE}}$, OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
DIGITAL SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
DIGITAL SUPPLY	−5V Supply Range	V^-		−3	−5	−8	V
DIGITAL SUPPLY	+5V Supply Current	I^+	$f_C = 0$		1.1	3.0	mA
DIGITAL SUPPLY	−5V Supply Current	I^-	$f_C = 0$		0.8	3.0	
DIGITAL	Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
DIGITAL Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.
Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.
Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

TEST CIRCUIT

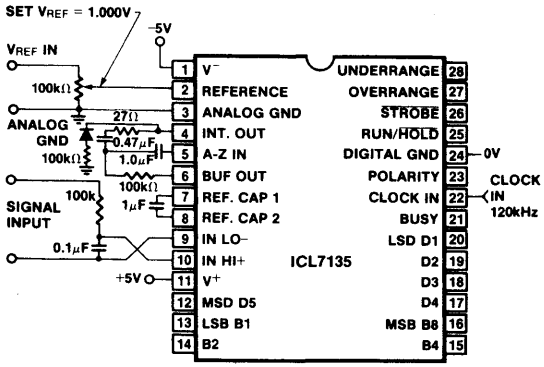


Figure 1: 7135 Test Circuit

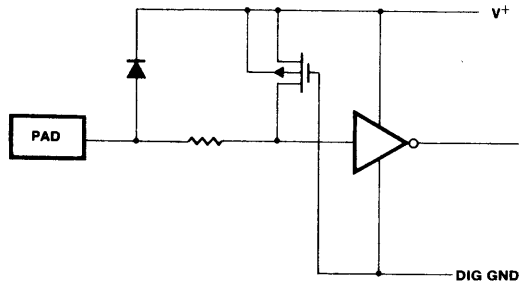


Figure 2: 7135 Digital Logic Input

DETAILED DESCRIPTION

Analog Section

4

Figure 3 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT), (3) deintegrate (DE) and (4) zero integrator (ZI).

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

3. De-Integrate phase

The Third phase is de-integrate, or reference integrate. Input Low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 10,000 ($\frac{V_{IN}}{V_{REF}}$).

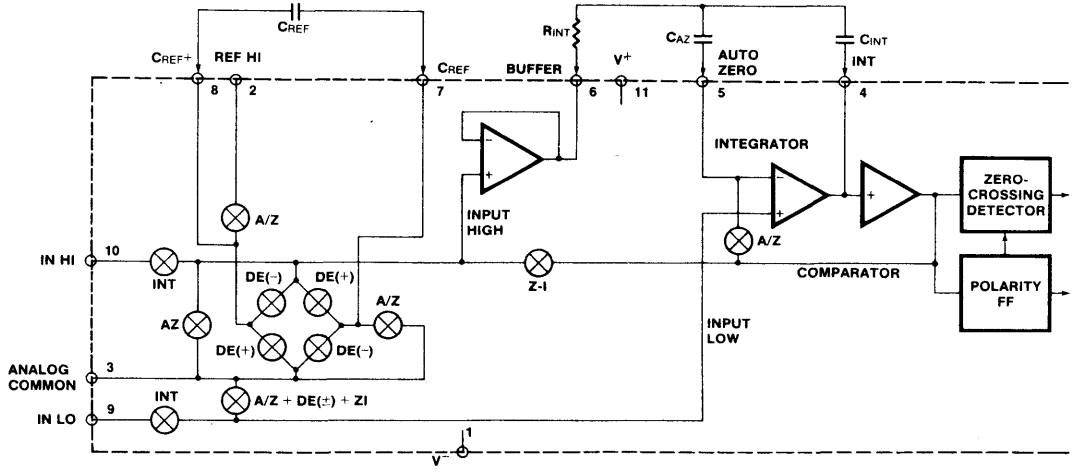


Figure 3: Analog Section of ICL7135

4. Zero Integrator phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog COMMON

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Fig. 4.

DETAILED DESCRIPTION

Digital Section

Figure 5 is the Digital Section of the 7135. It is identical to the 71C03 except that the 4-1/2/3-1/2 digit pin has been eliminated (mask-option; consult factory). The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. RUN/$\overline{\text{HOLD}}$ (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/$\overline{\text{H}}$ is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/$\overline{\text{Hold}}$ is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

2. $\overline{\text{STROBE}}$ (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pules after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

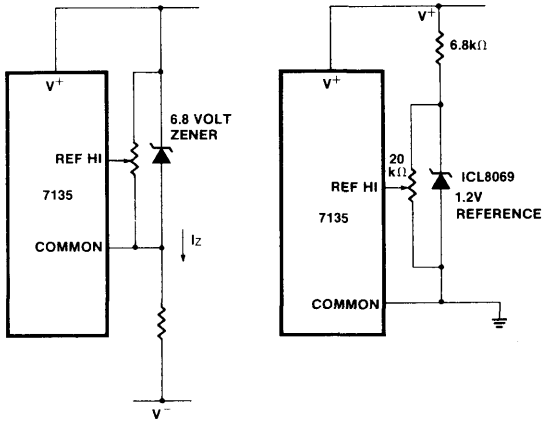


Figure 4: Using an External Reference

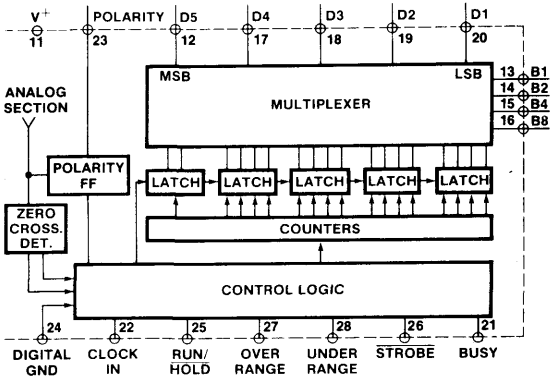


Figure 5: Digital Section 7135

3. BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a $(\overline{ZI} + \overline{AZ})$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

4. OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F-F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

5. UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

6. POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

7. Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This can give a blinking display as a visual indication of over-range.

8. BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver signal.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5 to 40μA give good results, with a nominal of 20μA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.47μF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}} = \frac{(10{,}000)\,(\text{clock period})\,(20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

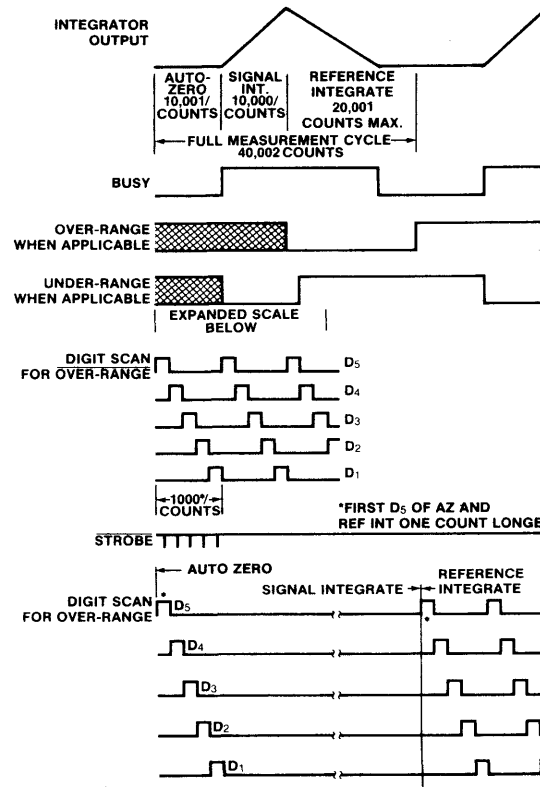


Figure 6: Timing Diagram for Outputs

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified adjustment may be needed. The diode can be any silicon diode, such as a 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166⅔kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

4

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray}.
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray}.

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately 15μV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 30μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

POWER SUPPLIES

The 7135 is designed to work from ±5V supplies. However, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.

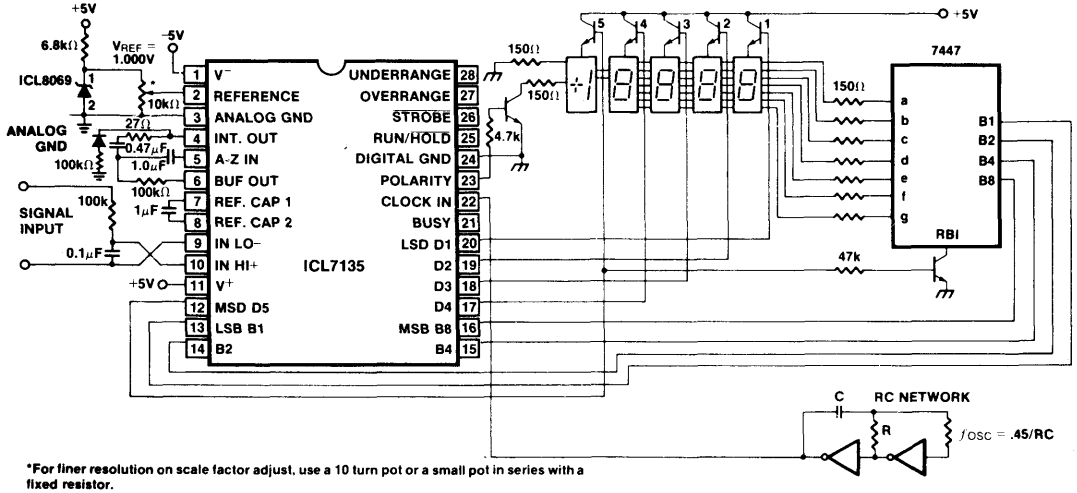
See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 7 shows the complete circuit for a 4-1/2 digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

Figure 8 is similar except the output drives a multiplexed common cathode LED Display with the 7-Common Emitter Transistor Array, for the digit driver transistors, making a lower component count possible. Both versions of the complete circuit will give a blinking display as a visual indication of overrange. A clock oscillator circuit using the ICM7555 CMOS timer is shown.



*For finer resolution on scale factor adjust, use a 10 turn pot or a small pot in series with a fixed resistor.

Figure 7: 4-1/2 Digit A-D Converter with a multiplexed common anode LED display

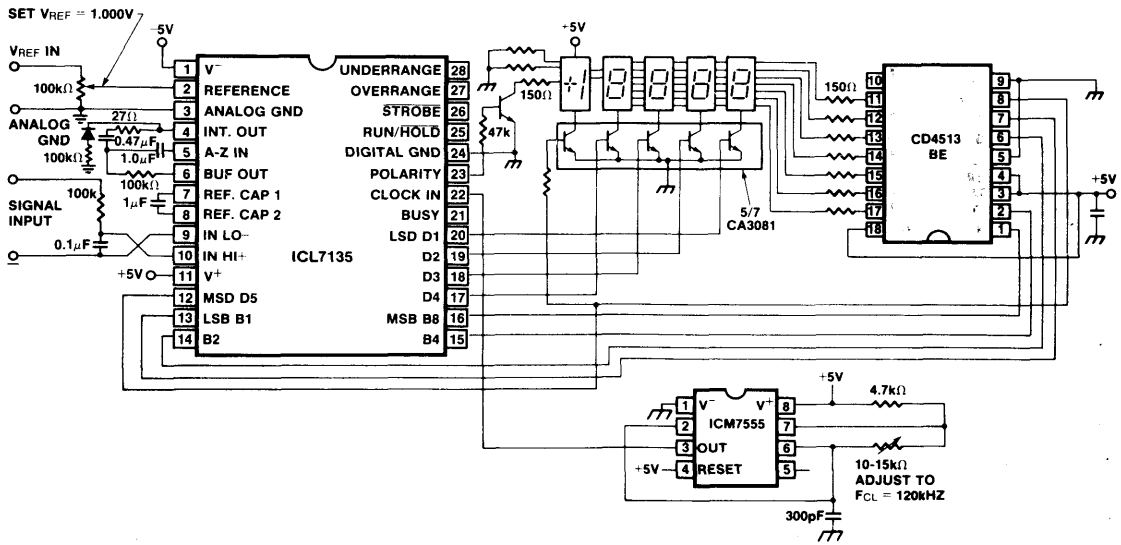


Figure 8: Driving multiplexed common cathode LED displays

A suitable circuit for driving a plasma-type display is shown in Fig. 9. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5k & 3k resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 11. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit (±2.000V) A/D.

Figure 10 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and 'Overrange' is indicated by blanking the 4 full digits.

® Nixie is a registered trademark of Burroughs Corporation.

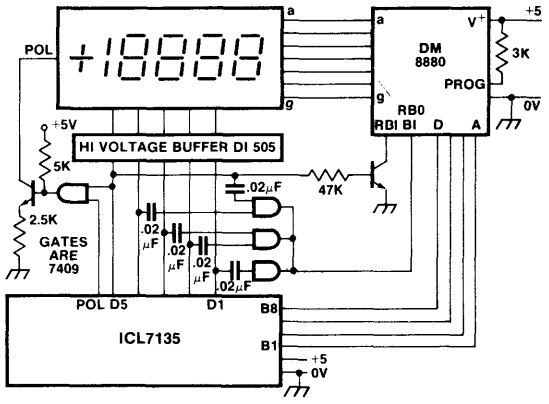


Figure 9: ICL7135 Plasma Display Circuit

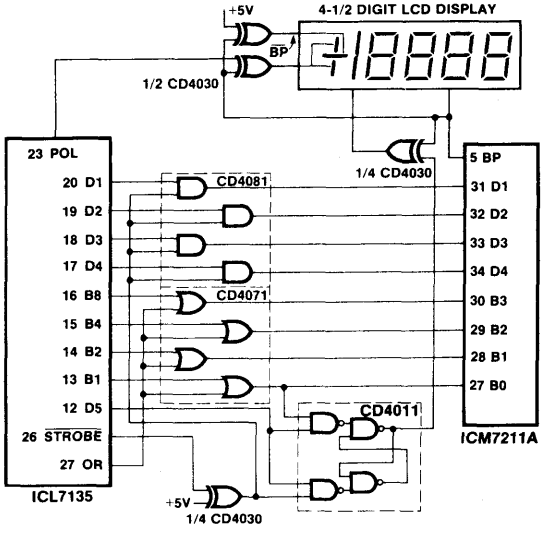


Figure 10: LCD Display with Digit Blanking on Overrange

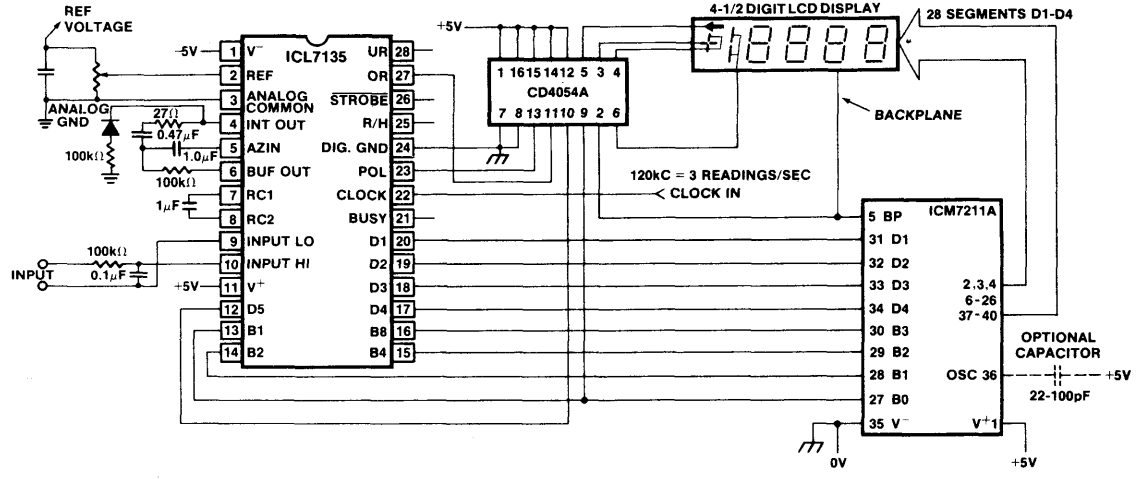


Figure 11: Driving LCD Displays

TYPICAL APPLICATIONS (Contd.)

A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using Intersil's LM311 voltage comparator in positive feedback mode (Figure 12) could minimize any clock frequency shift problem.

The 7135 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from 2 capacitors, and an inexpensive I.C. (Figure 13).

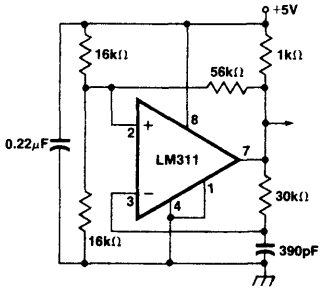


Figure 12: LM311 Clock Source

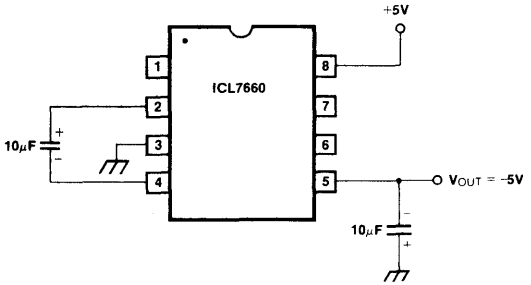


Figure 13: Generating Negative Supply from +5V

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 14 shows a very simple interface between a free-running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 15. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the

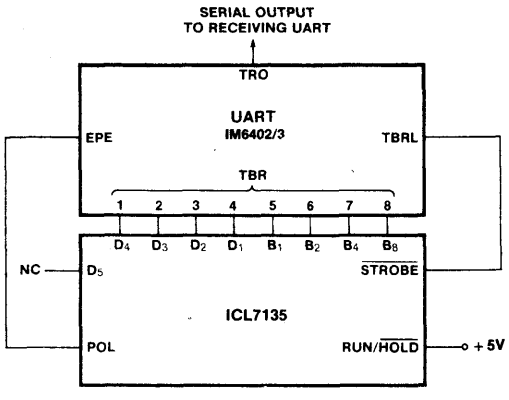


Figure 14: ICL7135 to UART Interface

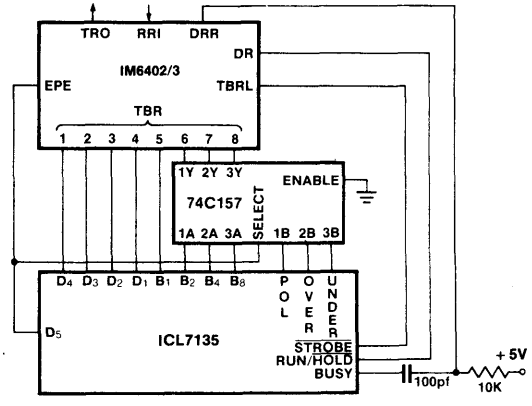


Figure 15: Complex ICL7135 to UART Interface

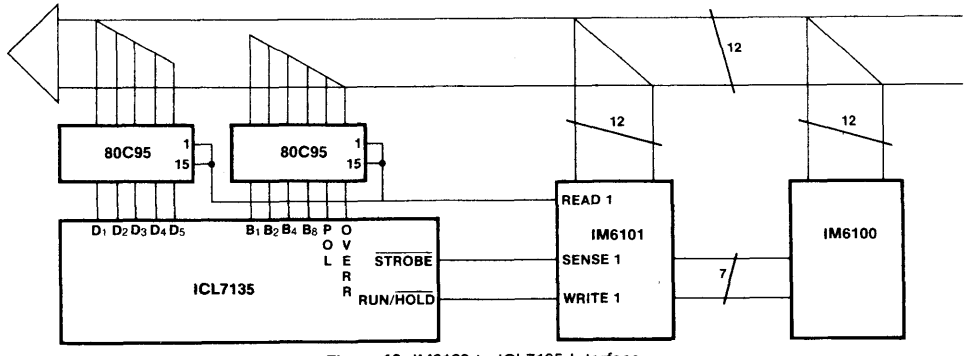


Figure 16: IM6100 to ICL7135 Interface

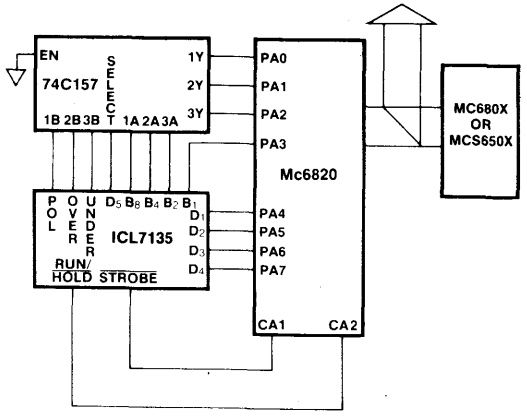


Figure 17: ICL7135 to MC6800, MCS650X Interface

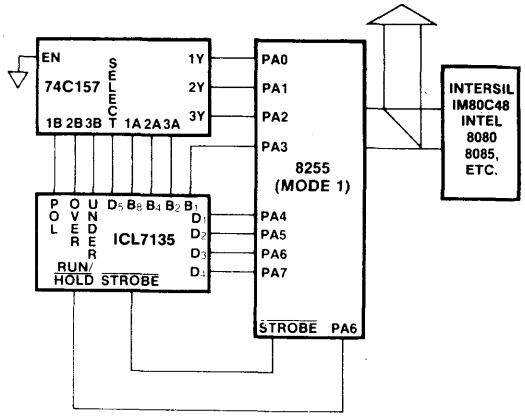


Figure 18: ICL7135 to MCS-48, -80, 85 Interface

transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 16, 17 and 18. The main differences in the circuits are that the IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080/8048 and the MC6800 groups with 8 bit words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word - as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4-1/2 Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort
A028 "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

ICL7136

3½-Digit

Low Power A/D Converter

FEATURES

- **First-reading recovery from overrange gives immediate "OHMS" measurement**
- **Guaranteed zero reading for 0V input**
- **True polarity at zero for precise null detection**
- **1pA typical input current**
- **True differential input and reference**
- **Direct LCD display drive — no external components required**
- **Pin compatible with the ICL7106, ICL7126**
- **Low noise — 15μVp-p without hysteresis or overrange hangover**
- **On-chip clock and reference**
- **Low power dissipation, guaranteed less than 1mW — gives 8,000 hours typical 9V battery life**
- **No additional active circuits required**
- **Evaluation Kit available (ICL7136EV/Kit)**

4

GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100μA, ideally suited for 9V battery operation.

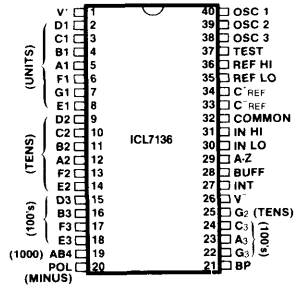
The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

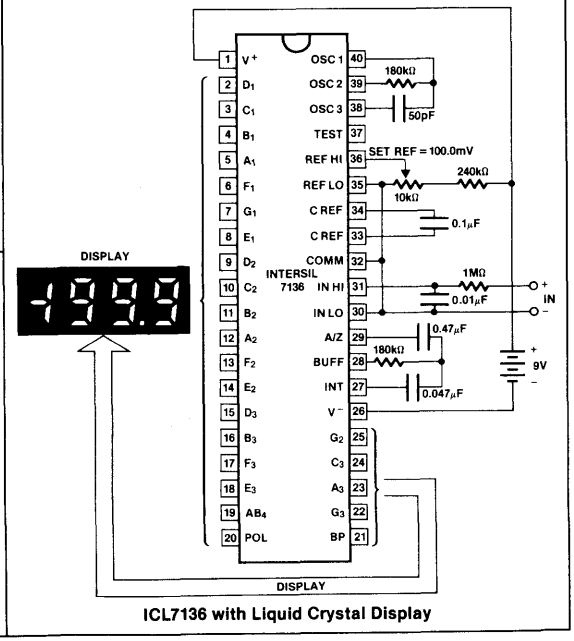
The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

ORDERING INFORMATION

PART	PACKAGE	TEMPERATURE RANGE	ORDER PART NUMBER
7136	40-pin CERDIP	0°C to +70°C	ICL7136CJL
7136	40-pin Ceramic DIP	0°C to +70°C	ICL7136CDL
7136	40-pin Plastic DIP	0°C to +70°C	ICL7136CPL
7136 Kit	Evaluation Kits		ICL7136EV/KIT

PIN CONFIGURATION (Outline dwgs. DL, JL PL)





ICL7136 with Liquid Crystal Display

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion.
Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).
Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

TEST CIRCUITS

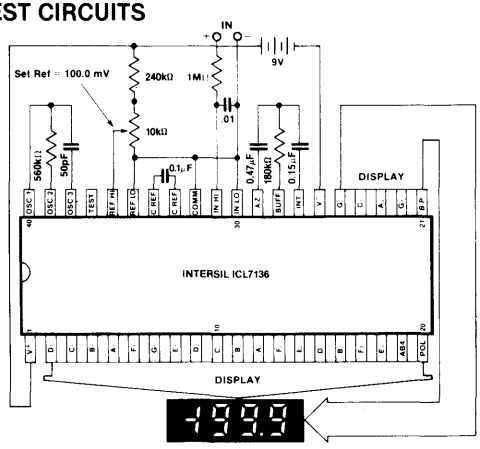


Figure 1. 7136 Clock Frequency 16kHz (1 reading/sec)

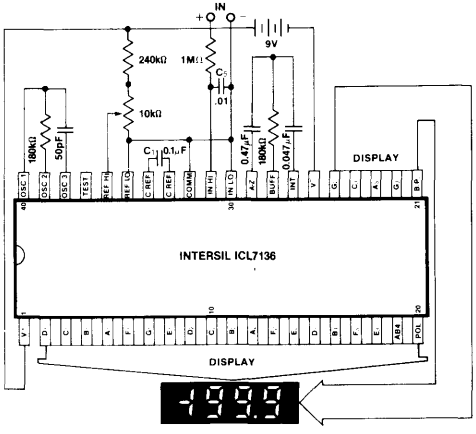


Figure 2. Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION—Analog Section

4

CONVERSION CYCLE

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

1. Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

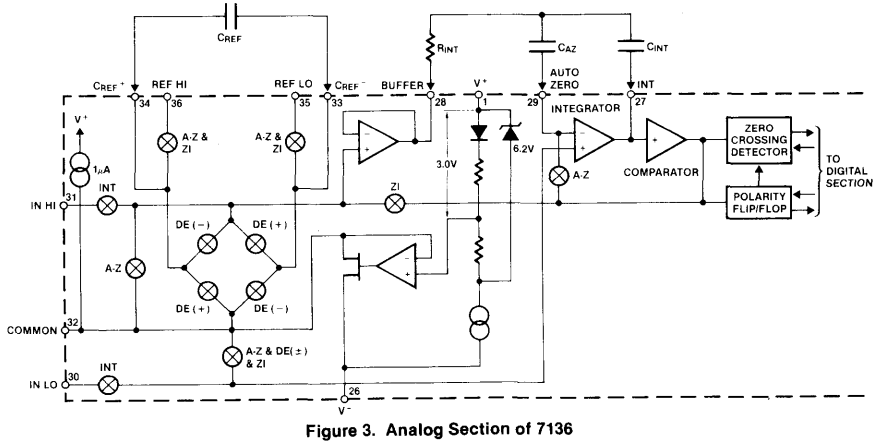


Figure 3. Analog Section of 7136

4. Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

ANALOG COMMON

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\simeq 35\Omega$), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

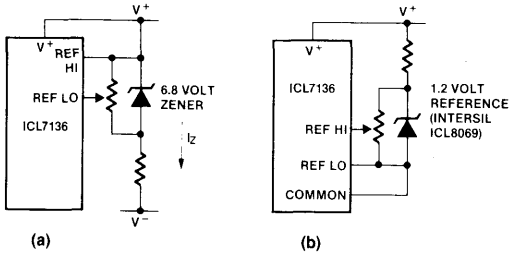


Figure 4. Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

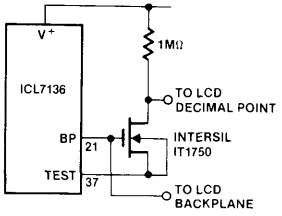


Figure 5. Simple Inverter for Fixed Decimal Point

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

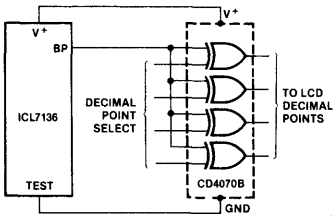


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

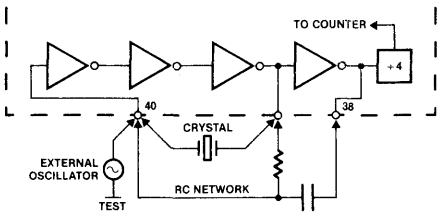


Figure 8. Clock Circuits

DETAILED DESCRIPTION—Digital Section

Figure 7 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

SYSTEM TIMING

Figure 8 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

DISPLAY FONT

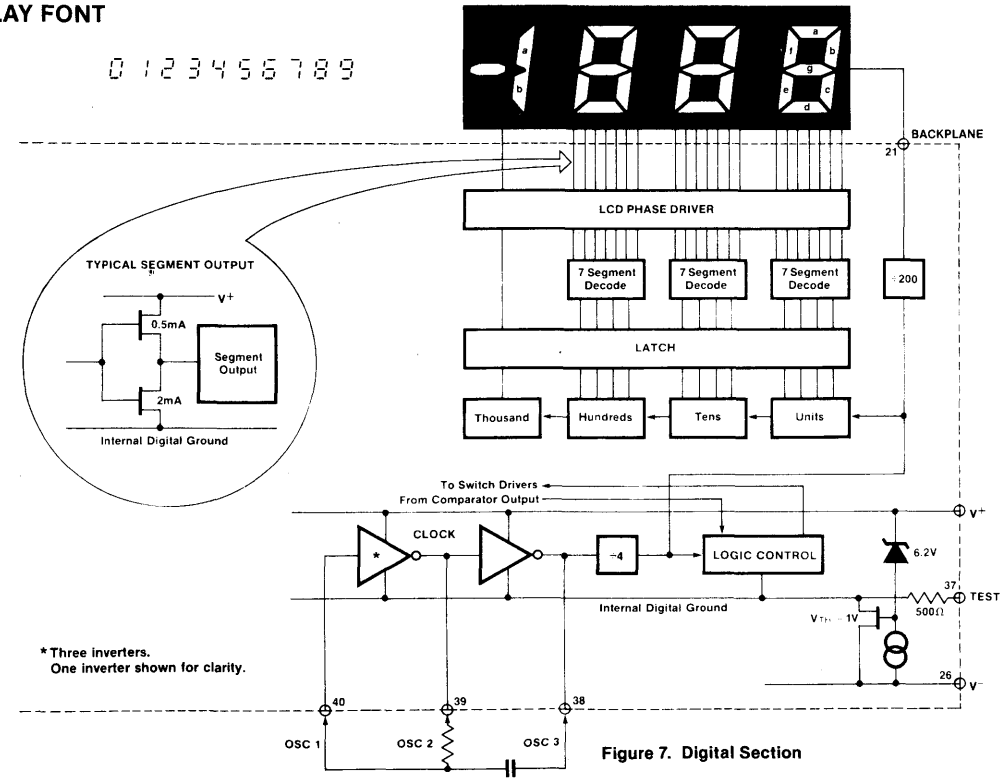


Figure 7. Digital Section

and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

COMPONENT VALUE SELECTION (See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation f ~ 0.45/RC. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

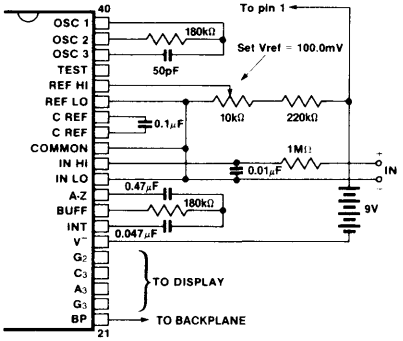


Figure 9. 7136 Using the Internal Reference. Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

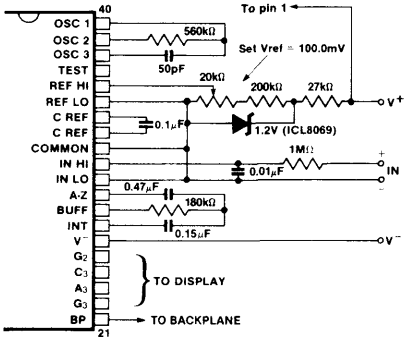


Figure 10. 7136 with an External Band-Gap Reference (1.2V Type). IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

TYPICAL APPLICATIONS (Continued)

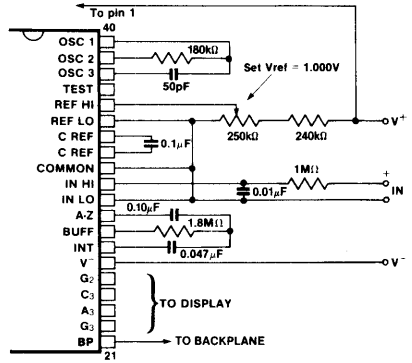


Figure 11. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 10.

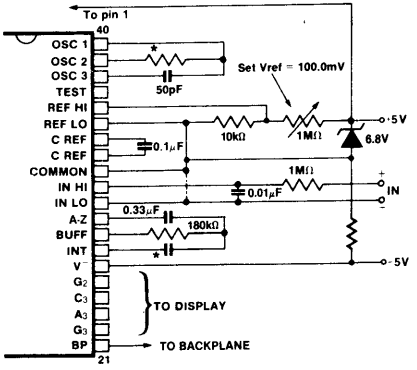


Figure 12. 7136 with Zener Diode Reference. Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

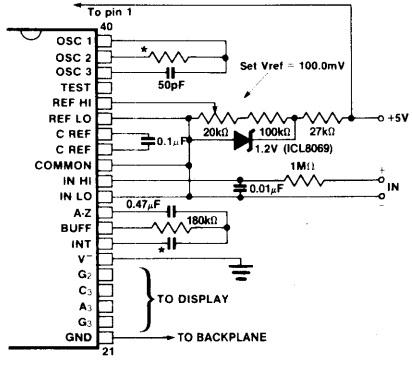


Figure 13. 7136 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

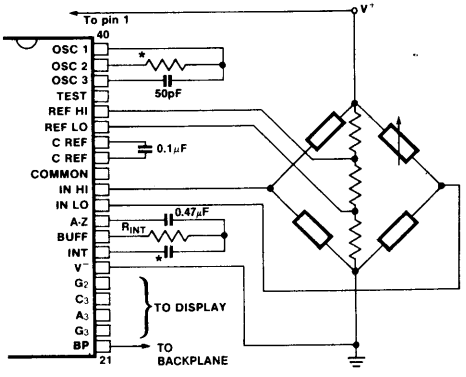


Figure 14. 7136 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

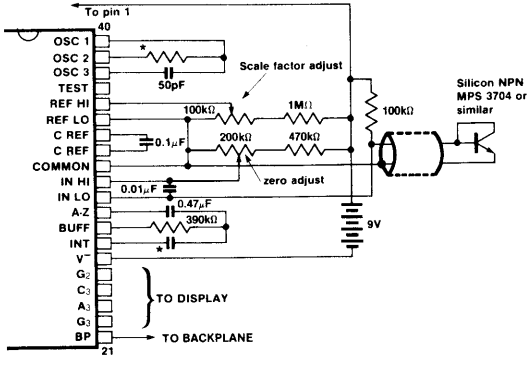


Figure 15. 7136 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL8073/4 and AD590 data sheets for alternative circuits.

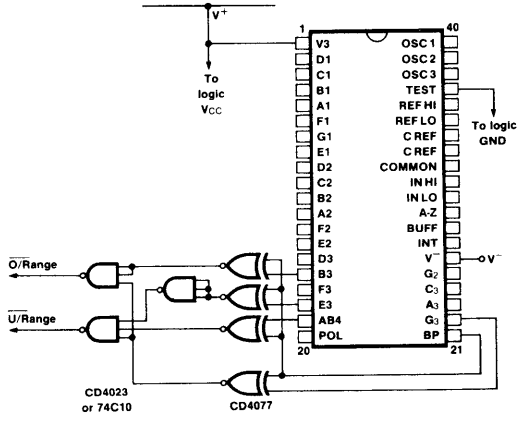


Figure 16. Circuit for Developing Underrange and Overrange Signals from 7136 Outputs.

*Values depend on clock frequency. See Figures 9, 10, 11.

TYPICAL APPLICATIONS (Continued)

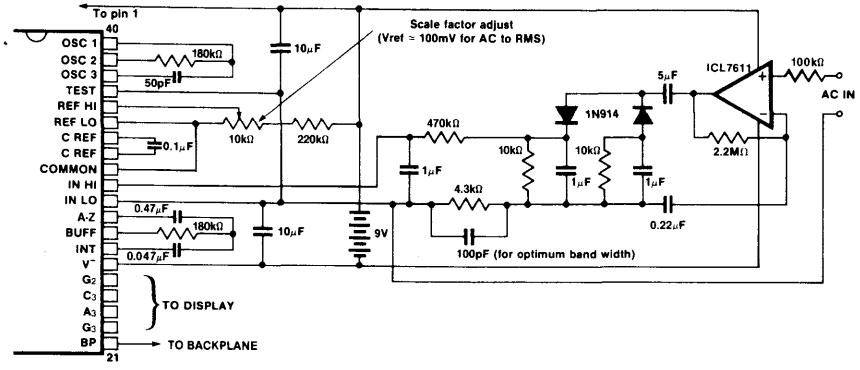


Figure 17. AC to DC Converter with 7136. Test is used as a common-mode reference level to ensure compatibility with most op amps.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

7136 EVALUATION KITS

After purchasing a sample of the 7136, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7136EV/Kit and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

4

ICL7137

3½-Digit
Low Power A/D Converter

FEATURES

- **First-reading recovery from overrange gives immediate "OHMS" measurement**
- **Guaranteed zero reading for 0V input**
- **True polarity at zero for precise null detection**
- **1pA typical input current**
- **True differential input and reference**
- **Direct LED display drive — no external components required**
- **Pin compatible with the ICL7107**
- **Low noise — 15μVp-p without hysteresis or overrange hangover**
- **On-chip clock and reference**
- **Improved rejection of voltage on COMMON pin**
- **No additional active circuits required**
- **Evaluation Kit available (ICL7137EV/Kit)**

4

GENERAL DESCRIPTION

The Intersil ICL7137 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200μA, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

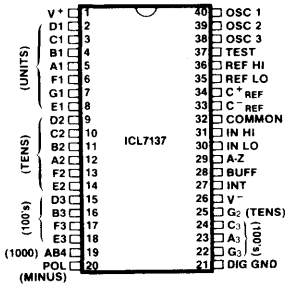
The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

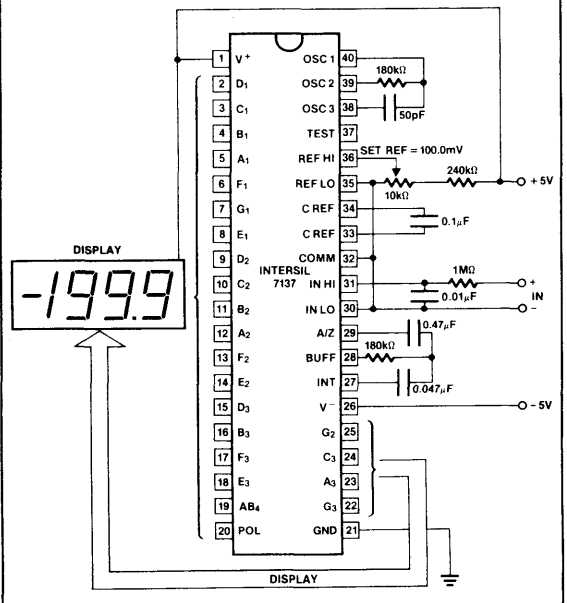
ORDERING INFORMATION*

PART	PACKAGE	TEMPERATURE RANGE	ORDER PART NUMBER
7137	40-pin CERDIP	0°C to +70°C	ICL7137CJL
7137	40-pin Ceramic DIP	0°C to +70°C	ICL7137CDL
7137*	40-pin Plastic DIP	0°C to +70°C	ICL7137CPL
7137 Kit	Evaluation Kit		ICL7137EV/KIT

*Plastic package device is available with reverse-bent leads. Order ICL7137RCPL.

PIN CONFIGURATION* (outline dwgs PL, JL, DL)





ICL7137 with LED Display

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply Current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion.
Note 5: 48kHz oscillator, Figure 2, increases current by 35μA (typ).
Note 6: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

TEST CIRCUITS

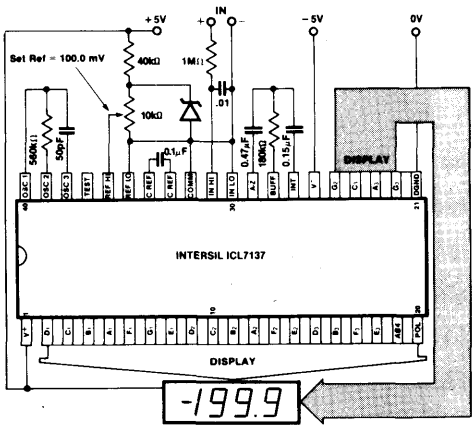


Figure 1. 7137 Clock Frequency 16kHz (1 reading/sec)

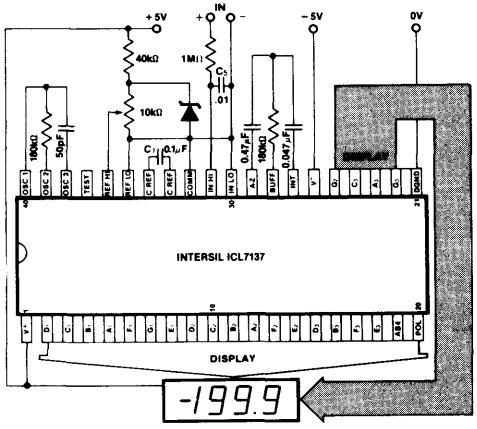


Figure 2. Clock Frequency 48kHz (3 readings/sec)

4

DETAILED DESCRIPTION—Analog Section

CONVERSION CYCLE

Figure 3 shows the Block Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

1. Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

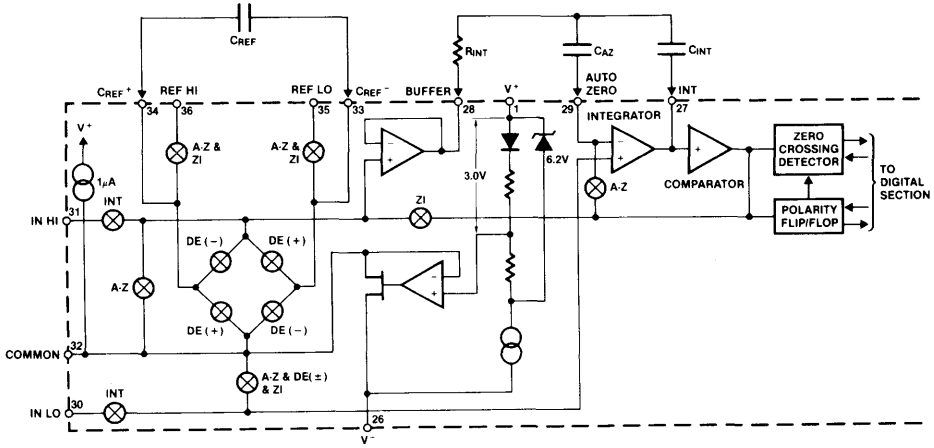


Figure 3. Analog Section of 7137

4. Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

ANALOG COMMON

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (> 7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≃ 35Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (< 7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

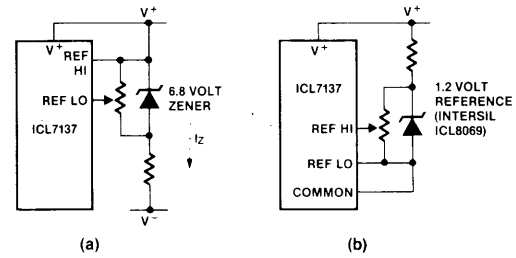


Figure 4. Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin is coupled to the internal digital supply through a 500Ω resistor, and functions as a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10mA under these conditions.

DETAILED DESCRIPTION—Digital Section

Figure 5 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 6 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

SYSTEM TIMING

Figure 7 shows the clock oscillator provided in the 7137. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

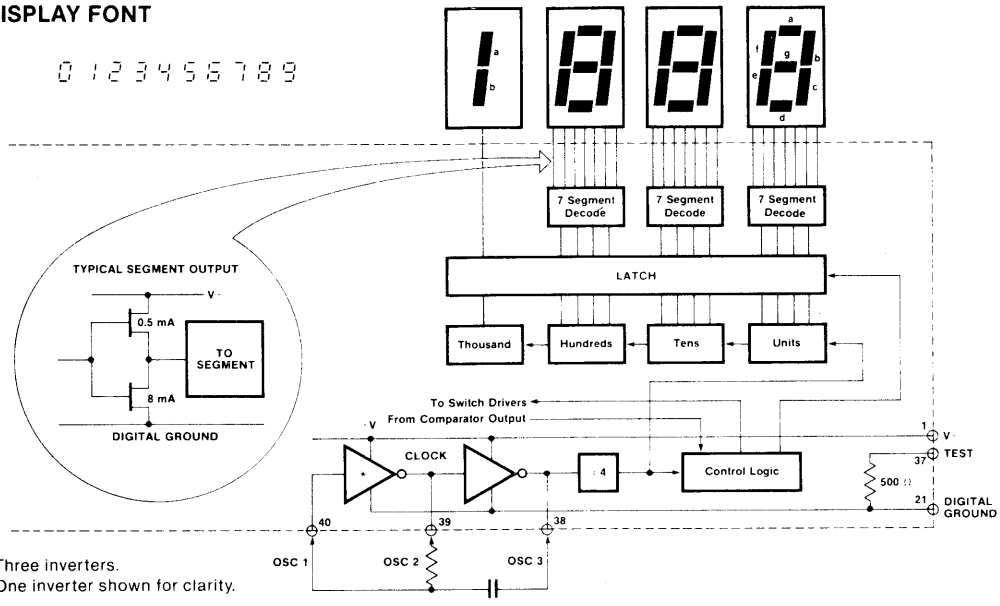


Figure 5. Digital Section

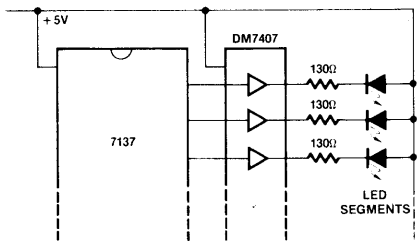


Figure 6. Display Buffering for Increased Drive Current

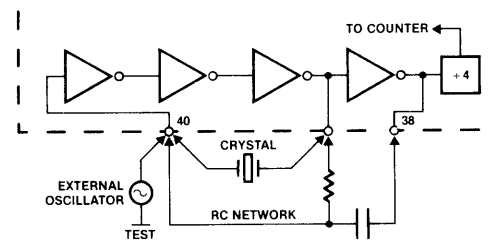


Figure 7. Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts* to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

COMPONENT VALUE SELECTION (See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (see A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, while for 16kHz (1 reading/sec), R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

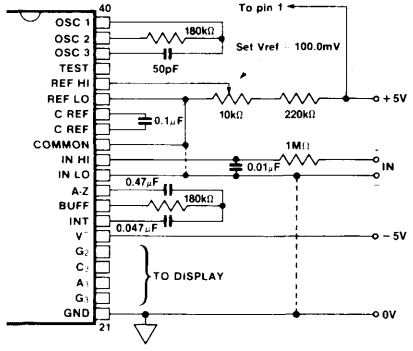


Figure 8. 7137 Using the Internal Reference. Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

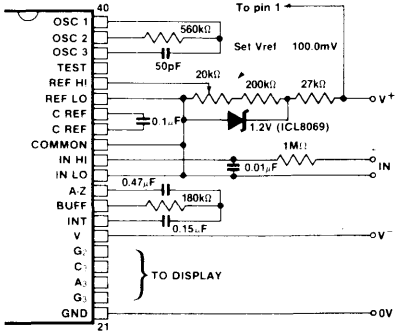


Figure 9. 7137 with an External Band-Gap Reference (1.2V Type). IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

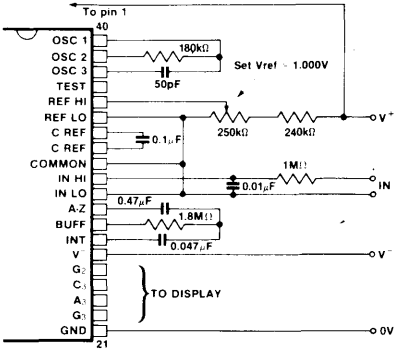


Figure 10. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 9.

TYPICAL APPLICATIONS (Continued)

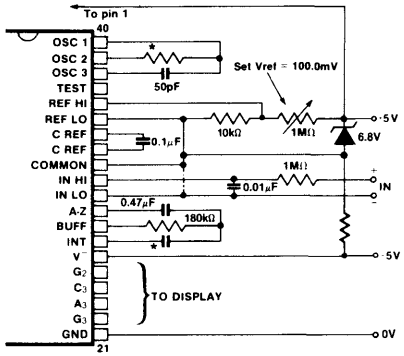


Figure 11. 7137 with Zener Diode Reference. Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 9, IN LO may be tied to COMMON.

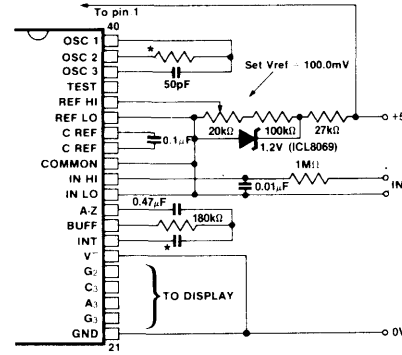


Figure 12. 7137 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

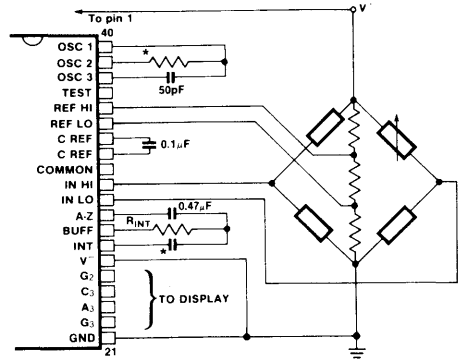


Figure 13. Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

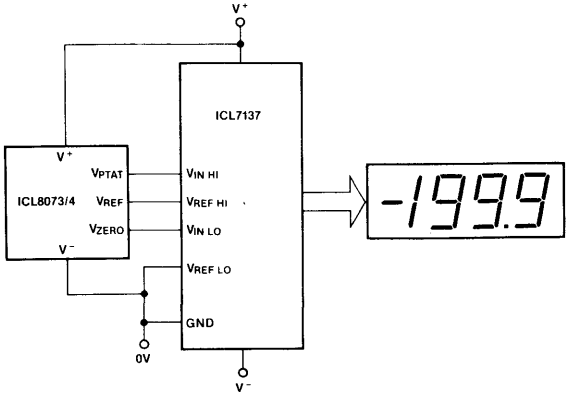


Figure 14. Basic Digital Thermometer. Both the ICL8073 (°C) and ICL8074 (°F) contain all necessary offset and reference (scale-factor) voltages to allow a direct-reading thermometer to be constructed without the need for external adjustments. Component values for 200mV full-scale should be used with the ICL8073, and (ideally) 170mV full-scale for the ICL8074.

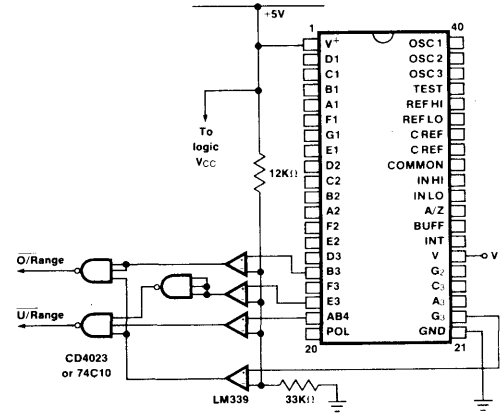


Figure 15. Circuit for developing Underrange and Overrange signals from outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

*Values depend on clock frequency. See Figures 8, 9 and 10.

TYPICAL APPLICATIONS (Continued)

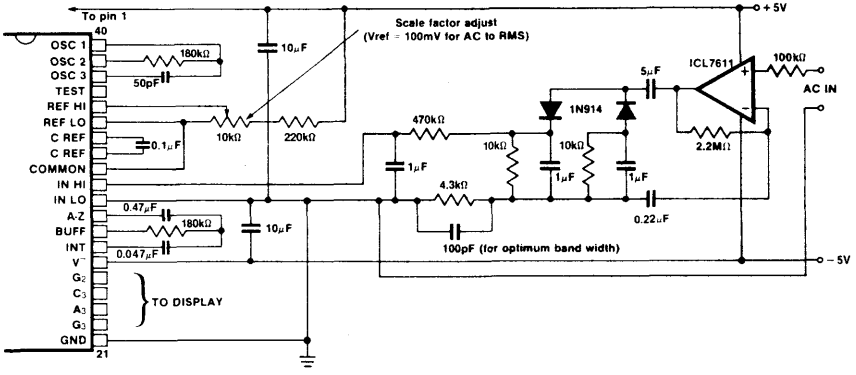


Figure 16. AC to DC Converter with 7137

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

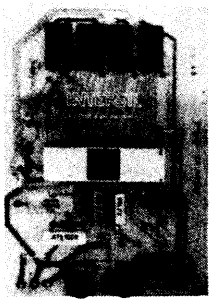
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

7137 EVALUATION KITS

After purchasing a sample of the 7137, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.



To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7137EV/Kit, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, LED display, passive components, and miscellaneous hardware.

ICL7145

16-Bit μP-Compatible Multiplying D/A Converter

FEATURES

- 16-bit resolution
- High linearity—0.003% FSR
- Microprocessor compatible with buffered inputs
- Bipolar application requires no external resistors
- Output current settling time 3μs max (1.0μs typ)
- Low linearity and gain temperature coefficients (1ppm/°C typ)
- Low power dissipation
- Full four-quadrant multiplication
- Full temperature range operation

4

GENERAL DESCRIPTION

The ICL7145 combines a four-quadrant multiplying DAC using thin film resistors and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve 0.003% linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory $\overline{WR}$ite cycle timing and control signal use. The input buffer register is loaded with the 16-bit input, and directly controls the output switches. The register is transparent if $\overline{WR}$ and $\overline{CS}$ are held low.

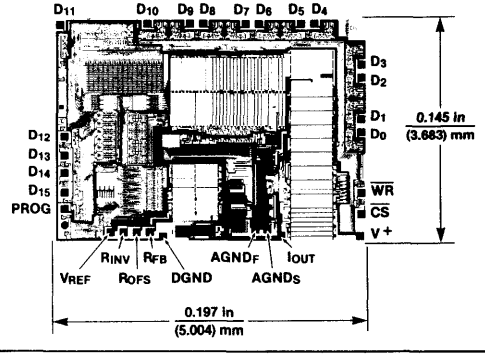
The ICL7145 is designed and programmed for bipolar operation. There is an offset resistor to the output with a reference input which should be connected to $-V_{REF}$, giving the DAC a true 2's complement input transfer function. Two extra resistors to facilitate the reference inversion are included on the chip, so that only an external op amp is needed.

ORDERING INFORMATION

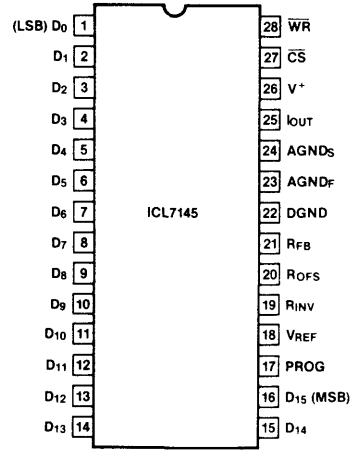
NON-LINEARITY	TEMPERATURE RANGE	
	0°C TO +70°C	−25°C TO +85°C
0.006%	ICL7145JCJI	ICL7145JIJI
0.003%	ICL7145KCJI	ICL7145KIJI

Package: 28-pin CERDIP only

CHIP TOPOGRAPHY



PIN CONFIGURATION (outline dwg JI)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to 7.5V
V_{REF}, R_{OFS}, R_{INV}, R_{FB} to DGND ..... ±25V
Current in $AGND_F$, $AGND_S$ 25mA
D_N, $\overline{WR}$, $\overline{CS}$, PROG, I_{OUT}, $AGND_F$, $AGND_S$ ..... −0.3V to V^+ +0.3V
Operating Temperature
ICL7145C ..... 0°C to +70°C
ICL7145I ..... −25°C to +85°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation (Note 2) 500mW
derate above 70°C @ 10mW/°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Note 1: All voltages with respect to DGND.
Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $V_{REF} = +5V$, $T_A = +25°C$ unless otherwise specified.

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Resolution				16			Bits
Non-Linearity	J		(Notes 3 and 4)			0.006	% FSR
	K					0.003	
Differential Non-Linearity			(Notes 3 and 4)		0.003		% FSR
Non-Linearity Temperature Coefficient			Operating Temperature Range		1		ppm/°C
Gain Error	J		(Notes 3 and 4)			0.04	% FSR
	K					0.02	
Gain Error Temperature Coefficient			Operating Temperature Range		1		ppm/°C
Zero Output Offset		V_{OZ}	$T_A = +25°C$			10	mV
			Operating Temperature Range		10		
Power Supply Rejection Ratio		PSRR	$T_A = +25°C$, $V^+ = 5V \pm 10\%$		1	20	ppm/V
Output Current Settling Time					1	3	μs
Reference Input Resistance		Z_{REF}	V_{REF}	3		6	kΩ
Output Capacitance		C_{OUT}	D_N = All 0s		110		pF
			D_N = All 1s		260		
Output Noise			Equivalent Johnson Resistance		7		kΩ
Low State Input		V_{INl}	Operating Temperature Range			0.8	V
High State Input		V_{INh}	Operating Temperature Range	2.4			
Logic Input Current		I_{LIN}	$0 \le V_{IN} \le V^+$	−1.0		1.0	μA
Logic Input Capacitance		C_{LIN}			15		pF
Supply Voltage Range		V^+	Functional Operation	4.5		5.5	V
Supply Current		I^+	Excluding Ladder		0.5	1.2	mA

Note 3: Full-Scale Range (FSR) is 10V (±5V).
Note 4: Using internal feedback and reference inverting resistors.

AC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $T_A = +25°C$, see Timing Diagram.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select-WRite Set-Up Time	t_{CWs}				0	ns
Chip Select-WRite Hold Time	t_{CWh}				0	
Write Pulse Width Low	$t_{\overline{WR}}$				200	
Data-WRite Set-Up Time	t_{DWs}				200	
Data-WRite Hold Time	t_{DWh}				0	

Timing Diagram

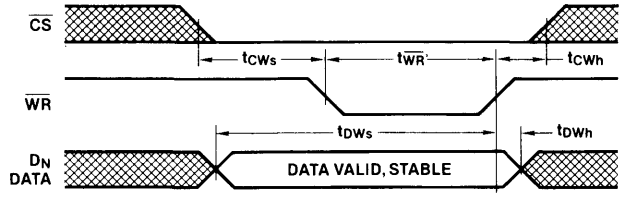


Table 1. Pin Assignment and Function Description

PIN	NAME	DESCRIPTION	
1	D_0	Bit 0	Least Significant Bit
2	D_1	Bit 1	
3	D_2	Bit 2	
4	D_3	Bit 3	
5	D_4	Bit 4	
6	D_5	Bit 5	
7	D_6	Bit 6	
8	D_7	Bit 7	Input Data Bits (High = True)
9	D_8	Bit 8	
10	D_9	Bit 9	
11	D_{10}	Bit 10	
12	D_{11}	Bit 11	
13	D_{12}	Bit 12	
14	D_{13}	Bit 13	
15	D_{14}	Bit 14	
16	D_{15}	Bit 15	Most Significant Bit
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{REF}	V_{REF} input to ladder.	
19	R_{INV}	Summing node for inverting amplifier.	
20	R_{OFS}	Bipolar offset resistor, to $-V_{REF}$.	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force line. Use to carry current from internal Analog GrouND connections. Tiedinternally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current. Tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive supply voltage.	
27	$\overline{CS}$	Chip Select (active low). Enables writing to register.	
28	$\overline{WR}$	WRite (active low). Writes into register. Equivalent to $\overline{CS}$.	

DEFINITION OF TERMS

NON-LINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full-scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

DETAILED DESCRIPTION

The ICL7145 consists of a 16-bit primary DAC, PROM controlled correction DACs, the input buffer registers, and the microprocessor interface logic. The 16-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistors in the ladder, results in excellent temperature stability.

The high linearity is achieved by programming a floating polysilicon gate PROM array which controls the correction DAC. The most significant bits of the DAC register address the PROM array, whose outputs control a 12-bit linearity correction DAC. Thus for every combination of the primary DAC's most significant bits a different C-DAC code is selected, allowing correction of superposition errors caused by bit interaction on the primary ladder's current bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method that corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging, unlike wafer-level trimming methods. Since the thin film resistors do not suffer laser trimming stresses, no degradation of time-stability results.

Also controlled by the onboard PROM, the 6-bit G-DAC reduces gain error to less than 0.02% FSR by diverting to analog ground up to 2% of the current flowing in R_{FB}.

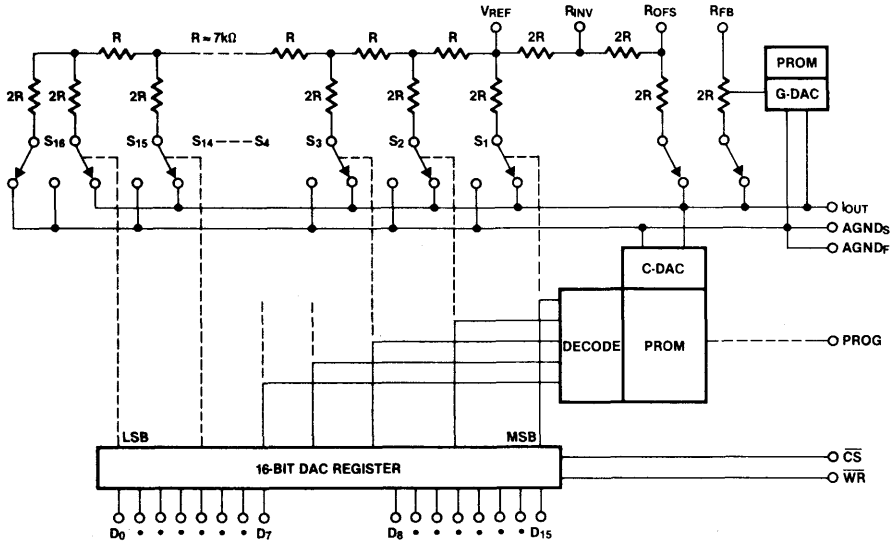


Figure 1. ICL7145 Functional Diagram

APPLICATIONS

Bipolar Operation

The circuit configuration for the normal bipolar mode operation of the ICL7145 is shown in Figure 2. The 2's complement input and positive and negative reference voltage values allow full four-quadrant multiplication. Amplifier A_3, together with the internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit to generate $-V_{REF}$ for the R_{OFS} offset input pin. This will give the nominal "digital input code/analog output value" relationship of Table 2.

Table 2. Code Table—Bipolar Operation

DIGITAL INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1-1/2^{15})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2^{15})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF}\ (1/2^{15})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1-1/2^{15})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	V_{REF}

Amplifier A_1 is the output amplifier. An additional amplifier A_2 may be used to force $AGND_F$ if the ground reference point is established elsewhere than at the DAC, as in Figure 3.

A feedback compensation capacitor, C_F, improves the settling time by reducing ringing. This capacitor is normally in the 10pF-40pF range, depending on layout and the output amplifier selected. If C_F is too small, ringing or oscillation can occur when using an op amp with a high gain-bandwidth. If C_F is too large, the response of the output amplifier will be overdamped and will settle slowly. Figure 6 shows the effect of C_F.

The input circuits of some high speed op amps will sink large currents to their negative supply during power up and power down. The Schottky diode at I_{OUT} limits any negative going transients to less than $-0.4V$, avoiding the SCR latch-up which could result if significant current was injected into the parasitic diode between I_{OUT} and V^- of the ICL7145. This diode is not needed when using the ICL7650 ultra low V_{OS} op amp.

Offset Adjustment

1. Connect all data inputs and $\overline{WR}$ and $\overline{CS}$ to DGND.
2. Adjust the offset zero-adjust of the operational amplifier A_2, if used, for $< \pm 50\mu V$ at $AGND_S$.
3. Set data to 0000....000 (all low). Adjust the offset zero-adjust of output operational amplifier A_1 for $< \pm 50\mu V$ at I_{OUT}. V_{OUT} will be offset from 0V by the bipolar zero error of $\pm$ 10mV.

The bipolar zero error may be trimmed out by adjusting the offset of A_3. The bipolar zero error can be as large as 10mV, but has a typical tempco of only $10\mu V/°C$.

Gain Adjustment

In many systems, gain adjustment will not be needed since the gain of the ICL7145 is accurate to within 0.02% FSR. When system gain must be adjusted, the low gain error limits the required adjustment range to only slightly more than the initial accuracy error of the reference. This is desirable since external gain trims degrade the gain temperature coefficient of a monolithic DAC. This degradation in the gain tempco comes about because, although the internal resistors track each other closely, they have a temperature coefficient of resistance of approximately $-250ppm/°C$.

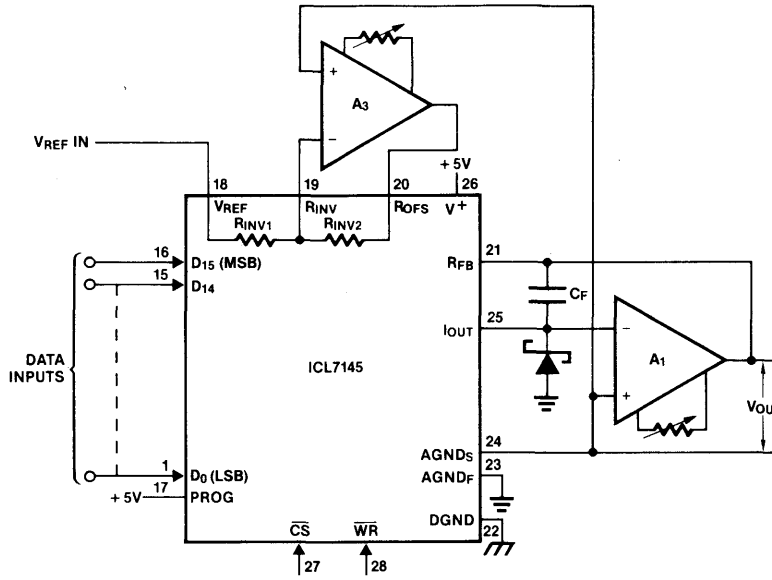


Figure 2. Bipolar Operation, Four-Quadrant

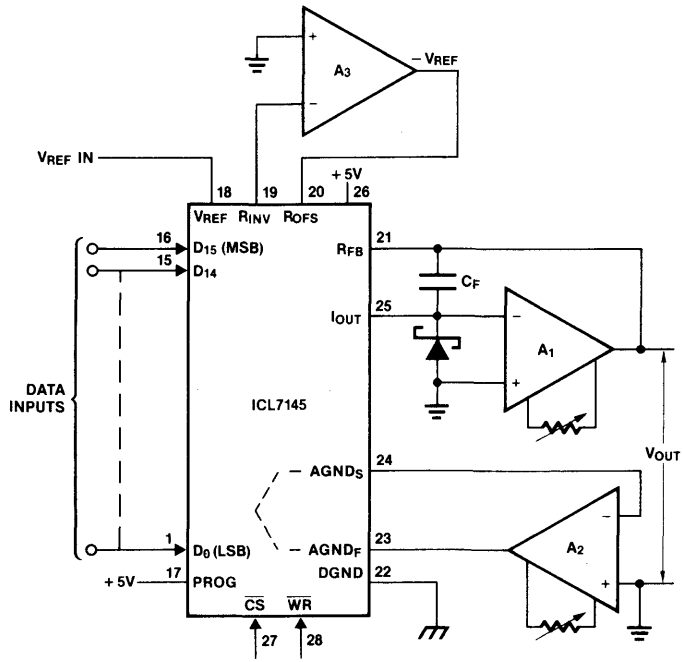


Figure 3. Operation with Forced Ground

To increase V_{OUT}, connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21). To decrease V_{OUT}, connect a resistor of 100Ω or less between the reference voltage and the V_{REF} terminal (pin 18). These resistor values result in a minimum of 1% FSR gain trim and add about 3ppm/°C gain tempco. If only a small gain trim range is needed, the resistor values should be reduced in order to preserve the excellent 1ppm/°C gain tempco.

Digital Interface

The ICL7145 has a 16-bit latch onboard and can interface directly to a 16-bit data bus. Use external latches or peripheral ICs to interface to an 8-bit data bus, as shown in Figure 4. To ensure that the data is written into the onboard latch, the data must be valid 200ns before the rising edge of $\overline{WR}$. The onboard latch is transparent, meaning that if $\overline{WR}$ and $\overline{CS}$ are tied low, the input data is directly applied to the internal R-2R ladder switches. While this simplifies interfacing in non-microprocessor systems it may cause additional glitches in some microprocessor systems. These small glitches will occur if $\overline{WR}$ goes low before data is valid. Data must be valid at the time $\overline{WR}$ goes low to avoid these additional glitches.

All digital interfaces can suffer from capacitive coupling between the digital lines and the analog section. There are two general precautions that will reduce the capacitive coupling problem: 1) reduce stray capacitance between digital lines and analog lines; and 2) reduce the number of transitions on the digital inputs. Careful board layout and shielding can minimize the capacitive coupling (see Figure 5, PCB layout). The activity on the digital input lines can be reduced by using external latches or peripheral interface ICs between the microprocessor bus and the ICL7145. This will reduce the number of transitions on the digital data and control lines of the ICL7145, and thereby reduce the amount of digital noise coupled into the sensitive analog sections.

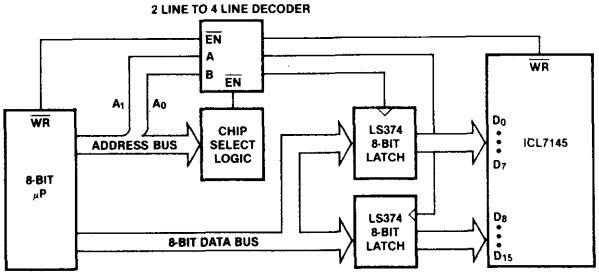
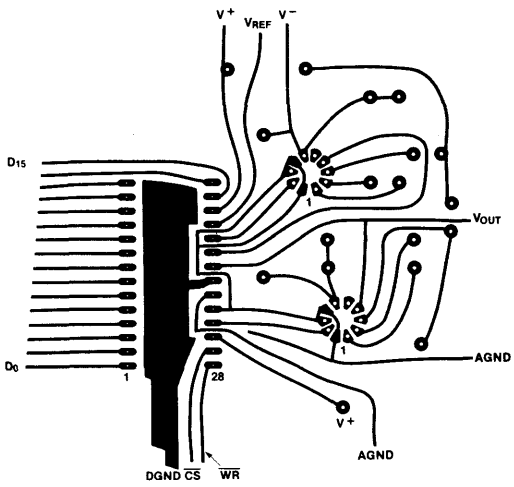


Figure 4. Interface to 8-Bit Microprocessor



Printed Circuit Side of Card (Single Sided Board)

Figure 5a. Printed Circuit Board Layout

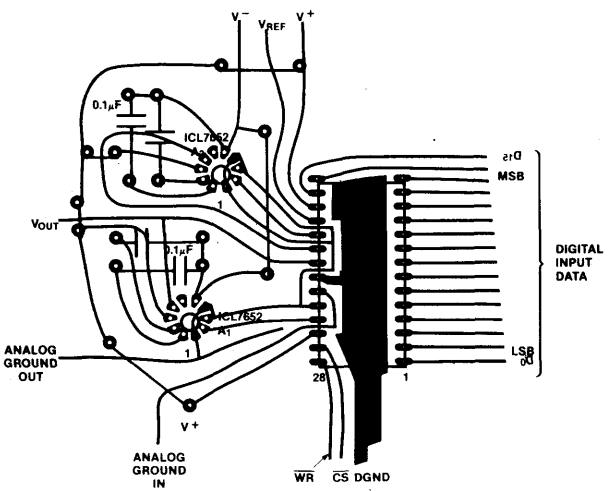


Figure 5b. Top Side with Component Placement

Operational Amplifier Selection

The input offset voltage, input current, gain, and bandwidth of the op amps used affect the circuit performance. Since the output impedance of I_{OUT} varies with the digital input code, A_1's input current will cause a code-dependent error at V_{OUT}, degrading the linearity. The input bias current should be significantly less than 1 LSB current, which is about 10nA. In a similar manner, any offset voltage in A_1 will also cause linearity errors. The offset voltage of the output amplifier should be significantly less than 1 LSB, which is 153μV.

The voltage output settling time is highly dependent on the slew rate and gain-bandwidth of A_1, so for high speed operation a high speed op amp such as the HA2600 is recommended. For applications where high speed is not required, the ICL7650 or ICL7652 can be used for A_1. Since the ICL7650/52 offset voltage is less than 5μV, no offset trimming is needed. To get a full 5V swing, $\pm$ 7.5V supplies should be used for the ICL7650/52. Figures 6 and 7 show typical performance.

Amplifier A_3, which is used to generate the inverted reference, needs only to have a stable offset and to be able to drive a 3kΩ load. Since this is strictly a DC amplifier, the low noise ICL7652 is an ideal choice. Any variation in the offset voltage of A_3 will result in a drift in the bipolar zero, but will not affect the linearity of the ICL7145.

Amplifier A_2, used to generate a high quality ground, also needs a low offset and the ability to sink about 2mA.

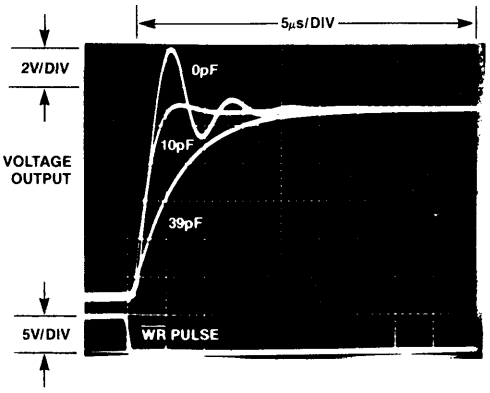
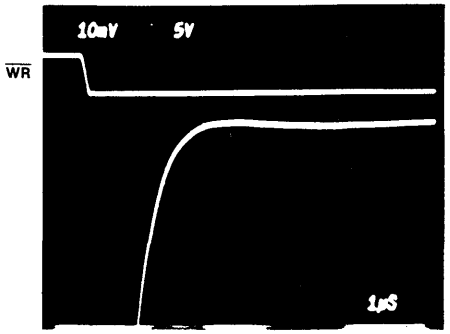


Figure 6. Voltage Output Settling with HA2525-5 Output Amplifier



Upper 50mV of a 10V Step

Figure 7. Voltage Output Settling with LF356 Output Amplifier

Ground Loops

Careful consideration must be given to ground loops in any high accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, $AGND_S$ and $AGND_F$. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 8. Output signals should ideally be referenced to the sense pin $AGND_S$, as shown in the application circuits.

Multiplying Mode Performance

While the ICL7145 can perform full four-quadrant multiplication, full 0.003% linearity is guaranteed only at $V_{REF} = +5V$. This is because the voltage coefficient of resistance of the R-2R ladder and the feedback resistor are significant at the 14- or 16-bit level. This effect is most significant at higher voltages, and adds errors on the order of 0.01% for a ±10V full-scale. While the ICL7145 is tested and specified for $V_{REF} = +5V$, the R-2R ladder has the same voltage across it when $V_{REF} = -5V$. Therefore, voltage coefficients do not add any error with a $-5V$ V_{REF}.

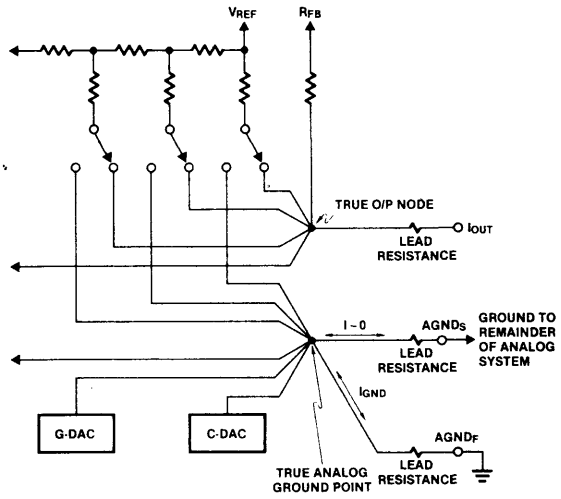


Figure 8. Eliminating Ground Loops

ICL7146 Complete 12-Bit Processor Compatible CMOS DAC

FEATURES

- Low Impedance Voltage Output
- Double-Buffered Processor Interface
- Easy-To-Use Bipolar Offset
- Multiplying Capability
- On-Chip Trimmed Reference
- 7 μSec Settling Time
- No External Gain or Offset Adjustment Required
- Low Power Dissipation 50mW
- No Critical External Components

ORDERING INFORMATION

Part Number	Linearity	Temperature Range	Package
ICL7146LCJI	0.01%	0 to +70°C	CERDIP
ICL7146LIJI		−40°C to +85°C	
ICL7146KCJI	0.02%	0 to +70°C	
ICL7146KIJI		−40°C to +85°C	
ICL7146JCJI	0.05%	0 to +70°C	
ICL7146JIJI		−40°C to +85°C	

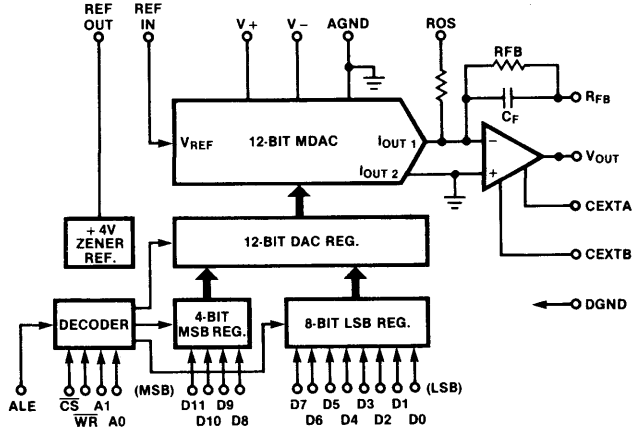
GENERAL DESCRIPTION

The ICL7146 is the first of a series of complete 12-Bit CMOS DAC's. These DAC's feature all of the needed support circuitry to interface to processors and give a voltage output. Contained on the chip are two levels of latches for double buffers, a trimmed reference, a latch controller, and an output buffer amplifier. All devices are accurately trimmed for both gain and offset so that no external trimming is required.

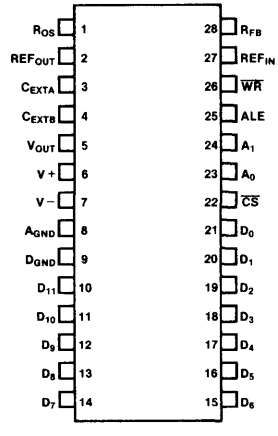
CMOS circuitry is used to keep the power dissipation low, and with all devices contained on a single chip, significant board size reductions are possible. As an alternative to this, many more analog channels could be added to a board and still decrease power consumption. Intersil's patented autostabilized op amp construction eliminates drifts in the zero offset and provides a fast (7 μsec) settling time.

Processor interface is double-buffered with all 12-bits being brought out. The first level of latches is divided into 4 and 8 bit bytes with a 12 bit wide second buffer. Data can be directly entered into any of the three buffers or the buffers can be operated separately.

BLOCK DIAGRAM



PIN CONFIGURATION



Absolute Maximum Ratings (Note 1)

REF_{IN}, R_{FB}, R_{OS} ..... ± 25V
V^+ 6.2V
V^- ..... − 9.0V
REF_{OUT}, V_{OUT}, C_{EXT},
A_{GND} ..... V^- − 0.3V to V^+ + 0.3V
Digital Inputs ..... V^+ + 0.3V to D_{GND} − 0.3V
Storage Temperature Range ..... − 65°C to + 150°C

Streses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: All Voltages with Respect to D_{GND}

Operating Characteristics

$V+ = 5V$, $V- = -5V$, $V_{ref} = 4.00V$, $T_A = 25°C$, $R_L = 20K$, $C_L = 50pF$

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Resolution			12			Bits
Non Linearity J K L					.05 .02 .01	% FSR % FSR % FSR
Differential Linearity J K L		 Guaranteed Monotonic		 ± 3/4 ± 1/2 ± 1/2	 ± 2 ± 1 ± 1	LSB
Gain Error				0.1	0.2	% FSR
Unipolar Zero Error				60	120	μV
Bipolar Zero Code Error		R_{FB} Connected to V_{OUT} R_{OS} Connected to $-V_{REF}$		0.025	0.05	% FSR
Positive Power Supply Rejection Ratio		V+ = 4.5 to 5.5V External Reference		± 0.001	0.005	% FSR/ % V+
Negative Power Supply Rejection Ratio		V− = − 4.5 to − 5.5V External Reference		0	± 0.001	% FSR/ % V+
Voltage Setting Time (Note 1)		To 1/2 LSB		7	10	μs
Feedthrough Error		V_{REF} = 8V P-P, 10 KHz Sine Wave			1	mV P-P
Reference Input Resistance		− 55°C to 125°C	5	10	20	KΩ
Internal Reference Voltage			− 4.04	− 4.00	− 3.96	V
Internal Reference Tempco				25	50	PPM of FSR per °C
Positive Supply Voltage Range	V+	Functional Operation, Internal or External Reference	4.5	5.0	5.5	V
Negative Supply Voltage Range	V−	Functional Operation, External Reference	− 4.5	− 5.0	− 7.5	V
		Functional Operation, Internal Reference	− 4.75	− 5.0	− 7.5	V
Output Voltage Range		R_{FB} connected to V_{OUT}		± 4		V
Output Drive Current			± 2			mA

Operating Characteristics (continued)

$V+ = 5V, V- = -5V, V_{ref} = 4.00V, T_A = 25°C, R_L = 20K, C_L = 50pF$

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Output Amp Bandwidth				2		MHz
Slew Rate				2.5		V/μs
Output Impedance		@D.C.		.02		Ω
Reference Input Range (Note 2)		For design use. Linearity Guar. @4.0V	± 2.0		± 10	V
Logic Low	V_{INL}				0.8	V
Logic High	V_{INH}		2.4			V
Logic Input Current					1	μA
Logic Input Capacitance (Note 1)					8	pF
Positive Supply Current		Inputs = 0V or 5V		4.0	5.0	mA
Negative Supply Current				4.0	5.0	mA
Power Dissipation		Input Code = 5.0V V+ = 5.0V, V− = −5.0V			50	mW
Gain Error Tempco		Internal Ref External Ref		± 30 − 12		PPM of FSR °C
DIGITAL SWITCHING CHARACTERISTICS						
Address $\overline{WR}$ Set-up Time	TAWS		100			nS
Address $\overline{WR}$ Hold Time	TAWH		0			nS
$\overline{CS}$ $\overline{WR}$ Set-up Time	TCWS		0			nS
$\overline{CS}$ $\overline{WR}$ Hold Time	TCWH		0			nS
Write Pulse Width	TWR		200			nS
Data Set-up Time	TDS		200			nS
Data Hold Time	TDH		0			nS
ALE Pulse Width	TLL		200			nS
Address-ALE Set-up Time	TAL		60			nS
Address-ALE Hold Time	TLA		40			nS
$\overline{CS}$-ALE Set-up Time	TCL		30			nS
$\overline{CS}$-ALE Hold Time	TLC		50			nS
$\overline{WR}$ Trailing Edge to ALE	TWL		0			nS

NOTE 1: Guaranteed by design, not 100% tested in production.
NOTE 2: External Op Amp Required for $V_{out} > \pm 4.0V$

DETAILED DESCRIPTION

The ICL7146 is a monolithic 12-bit processor compatible CMOS DAC. It is a complete DAC containing a DAC, a group of latches, a reference, digital control circuitry and an op amp.

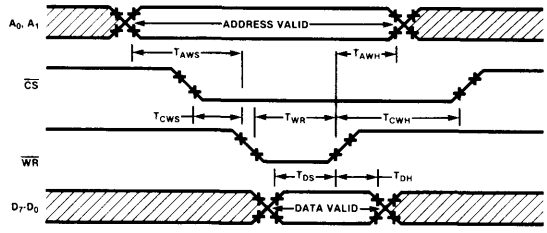
A wide range of applications can be implemented with the ICL7146 laser trimmed 12-bit multiplying DAC. CMOS switches and low tempco thin film resistors provide a stable output current proportional to the input digital code. Two matched and trimmed resistors are provided at the output for current to voltage conversion and for offset generation in bipolar operation.

An on-chip precision auto-stabilized operational amplifier is provided for current to voltage conver-

TIMING DIAGRAMS AND TRUTH TABLES

Non-Multiplexed Bus

TIMING DIAGRAM



TIMING FOR NON-MULTIPLEXED ADDRESS BUS

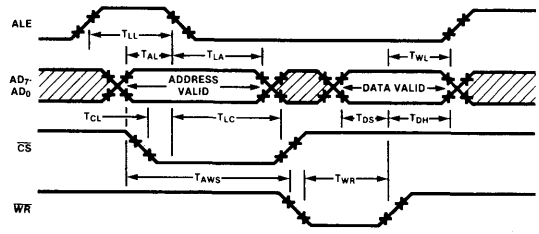
TRUTH TABLE (ALE tied to V+)

CONTROL INPUTS				OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	
X X	X X	X 1	1 X	No Operation Device Not Selected
0	0	0	0	Load All Registers From Data Bus
0	1	0	0	Load LSB Register From Data Bus*
1	0	0	0	Load MSB Register From Data Bus*
1	1	0	0	Load DAC Register From LSB & MSB Register

*Data is latched on low to high transition of $\overline{WR}$ or $\overline{CS}$.

Multiplexed Bus

TIMING DIAGRAM



TIMING FOR MULTIPLEXED ADDRESS BUS

TRUTH TABLE (ALE is latch control input; $\overline{CS}$, A0 & A1 are latched outputs)

CONTROL INPUTS				OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	
X X	X X	X 1	1 X	No Operation Device Not Selected
0	0	0	0	Load All Registers From Data Bus
0	1	0	0	Load LSB Register From Data Bus
1	0	0	0	Load MSB Register From Data Bus
1	1	0	0	Load DAC Register From LSB & MSB Register

4

sion. The auto zeroing technique utilized guarantees extremely low offset and low gain drift over temperature. Two inexpensive capacitors are required for the internal auto zero circuitry. Th op amp has been left open loop for flexibility. The loop can be closed by connecting R_{OS} and R_{fb} to V_{OUT} for full scale voltages less than ±4 volts. An external amplifier can be closed in the loop for applications requiring larger output swing or current. An inexpensive buffer amplifier with no special input characteristics can be used without any system degradation. No external offset trimming is required due to the auto zeroing circuitry.

A zener reference that can be trimmed for both output voltage and temperature drift is provided. This reference is capable of driving an extra load of 200μA above the current required for the DAC ladder. This allows the reference to be used for other devices in the system when required.

Latches on the chip are set up in two levels, the first level connects to the data bus and is internally arranged as three groups of four latches each. The decoding circuitry is designed so that the user may address either the lower eight bits or the upper four bits. This allows the user to hard wire the 4 MSB's directly to the 4LSB's for easy interface to eight bit processors. Or the DAC can be wired directly to a 12 bit or larger data bus. Following the two input latches is another latch that is 12 bits wide. This makes the ICL7146 double-buffered. By double buffering the input of the DAC it is possible to interface the DAC to an eight bit data bus and prevent the DAC from having a major output glitch as the digital code changes. With a single level of latches, say a 4 bit latch and an 8 bit latch connected to an 8 bit data bus the following would occur if an attempt was made to generate a ramp. As the input code was incremented from 000_{HEX} to OFF_{HEX} an even stair case output would occur. But to change the code to 100_{HEX} the processor would either have to change to code to 000 and then to 100, or first to 1FF and then to 100. In the first case the output would go to zero for a full processor cycle. And in the second case it would double

its output value. Neither of these conditions are acceptable in a wide variety of applications. Hence the need for double buffering.

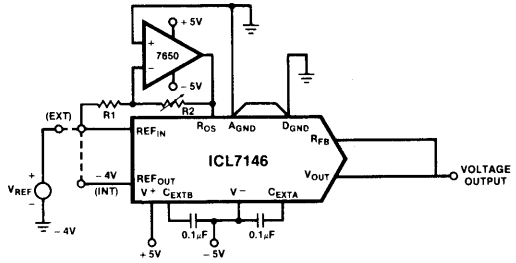
Buffer control is handled by a decoder to ease processor interface requirements. Operation of the decoder is shown in the truth table.

TYPICAL APPLICATIONS
Bipolar Output

Offset Binary Code Table

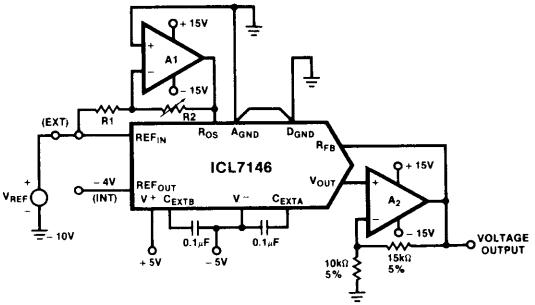
Binary Number In DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

± 4V BIPOLAR OUTPUT:



NOTE 1: A1 should be selected or trimmed for low offset voltage; R1 & R2 are 10KΩ resistors trimmed to a matching of 0.1% or better.

± 10V BIPOLAR OUTPUT:



NOTE 1: A1 should be selected or trimmed for low offset voltage; R1 & R2 are 10KΩ resistors trimmed to a matching of 0.1% or better.

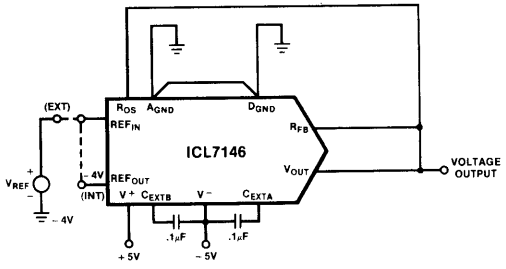
NOTE 2: A2 needs not to have a low offset voltage but it must be fast (>8MHz) to insure stability.

TYPICAL APPLICATIONS
Unipolar Output

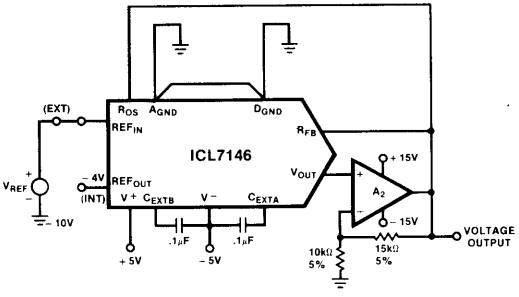
Code Table

Binary Number In DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\,V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0001	0V

+ 4V UNIPOLAR OUTPUT:

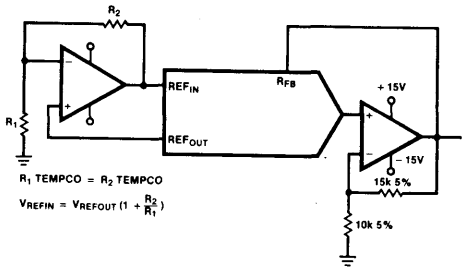


+ 10V UNIPOLAR OUTPUT:



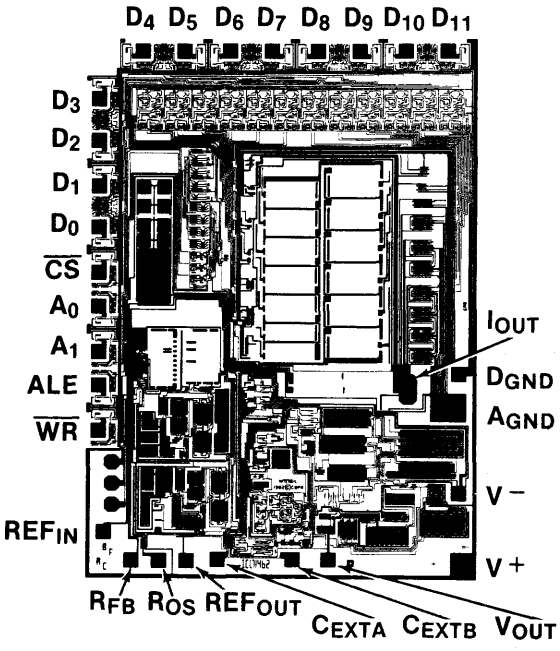
NOTE 1: A2 needs not to have a low offset voltage but it must be fast (>8MHz) to insure stability.

TYPICAL APPLICATIONS (Continued)



USING INTERNAL REF FOR V_{REF} >4V

CHIP TOPOGRAPHY



4

AD7520/7530
AD7521/7531
10 & 12 Bit Monolithic Multiplying D/A Converters

FEATURES
- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20 mW (Max)**
- **Low Nonlinearity Tempco: 2 PPM of FSR/°C (Max)**
- **Current Settling Time: 500 ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **DTL/TTL/CMOS Compatible**
- **Full Input Static Protection**
- **883B Processed Versions Available**

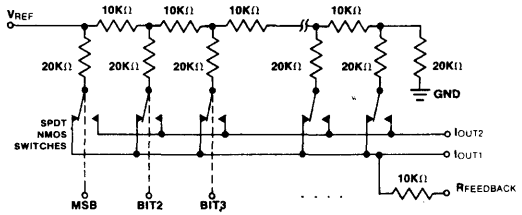
GENERAL DESCRIPTION
The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). INTERSIL thin-film on CMOS processing gives up to 10-bit accuracy with DTL/TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

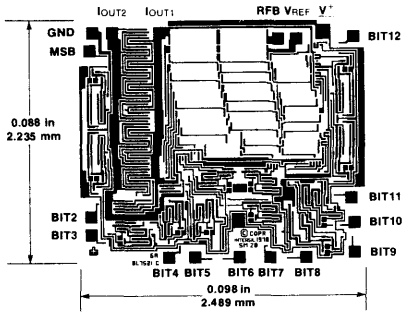
4

FUNCTIONAL DIAGRAM



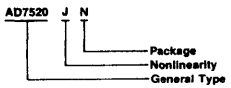
(Switches shown for Digital Inputs "High")
(Resistor values are nominal)

CHIP TOPOGRAPHY



PACKAGE IDENTIFICATION

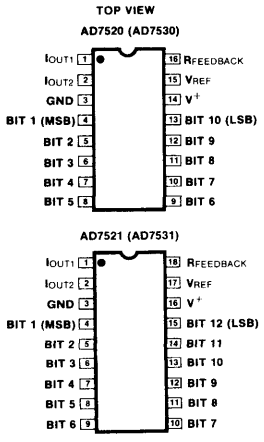
Suffix D: Cerdip package
Suffix N: Plastic DIP package



ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7531JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD

PIN CONFIGURATION (Outline dwgs DE, PE)



INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = 25° C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75°C ..... 450 mW
derate above +75°C @ ..... 6 mW/°C

Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
JD, KD, LD Versions ..... −25°C to 85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION: 1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, TA = 25°C unless otherwise specified)

PARAMETER		AD7520 (AD7530)	AD7521 (AD7531)	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution		10	12	Bits			
Nonlinearity	J S	0.2 (8-Bit)		% of FSR	Max	S, T, U: over −55°C to =125°C	1
	K T	0.1 (9-Bit)		% of FSR	Max		1
	L U	0.05 (10-Bit)		% of FSR	Max	$-10V \le V_{REF} \le = 10V$	1
Nonlinearity Tempco		2		PPM of FSR/°C	Max	$-10V \le V_{REF} \le +10V$	
Gain Error (Note 2)		0.3		% of FSR	Typ		
Gain Error Tempco (Note 2)		10		PPM of FSR/°C	Max		
Output Leakage Current (either output)		200 (300)		nA	Max	Over the specified temperature range	
Power Supply Rejection		±0.005		% of FSR/%	Typ		2
AC ACCURACY Output Current Settling Time		500		nS	Typ	To 0.05% of FSR (All digital inputs low to high and high to low)	6
Feedthrough Error		10		mV pp	Max	V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	5
REFERENCE INPUT Input Resistance (Note 3)		5k 10k 20k		Ω	Min Typ Max	All digital inputs high. I_{OUT1} at ground.	
ANALOG OUTPUT Voltage Compliance (both outputs)		See absolute max. ratings					
Output Capacitance		I_{OUT1} 120 I_{OUT2} 37		pF pF	Typ Typ	All digital inputs high	4
		I_{OUT1} 37 I_{OUT2} 120		pF pF	Typ Typ	All digital inputs low	4
Output Noise (both outputs)		Equivalent to 10kΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold		0.8		V	Max	Over the specified temp range	
High State Threshold		2.4		V	Min		
Input Current (low to high state)		1		μA	Typ		
Input Coding		Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5	
POWER REQUIREMENTS Power Supply Voltage Range		+5 to +15		V			
I^+		5		nA	Typ	All digital inputs at GND	
		2		mA	Max	All digital inputs high or low	
Total Power Dissipation (Including the ladder)		20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Ladder and feedback resistor Tempco is approximately −150ppm/°C.

TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7530, AD7521 and AD7531.

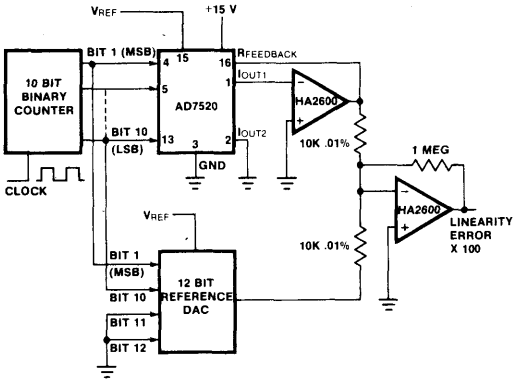


Figure 1. Nonlinearity

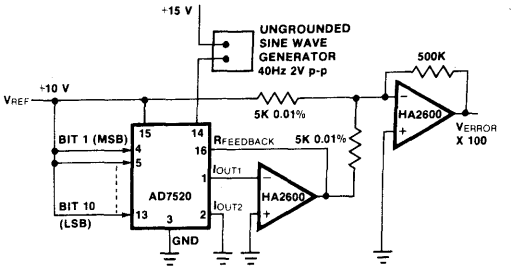


Figure 2. Power Supply Rejection

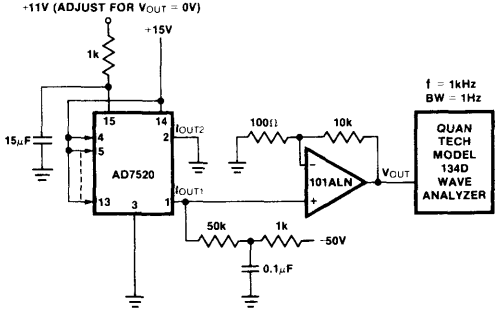


Figure 3. Noise

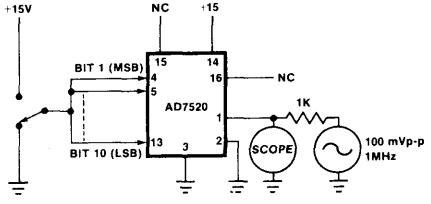


Figure 4. Output Capacitance

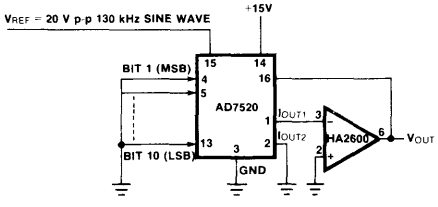


Figure 5. Feedthrough Error

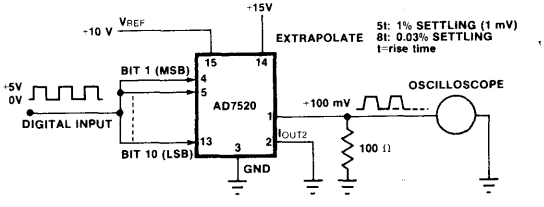


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

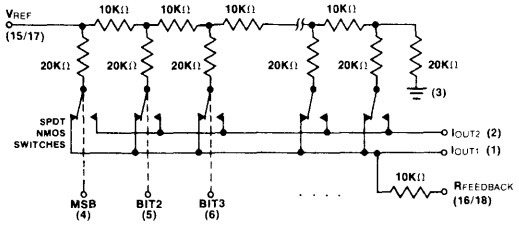
OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. Highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} busses which must be held either at ground or virtual ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 7. 7520/7521 Functional Diagram

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

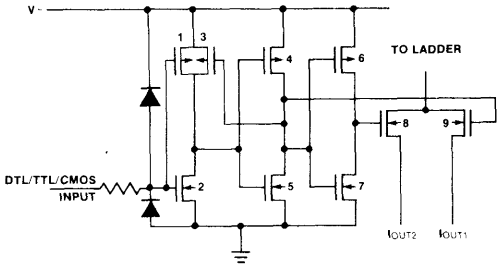


Figure 8. CMOS Switch

APPLICATIONS

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 9. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

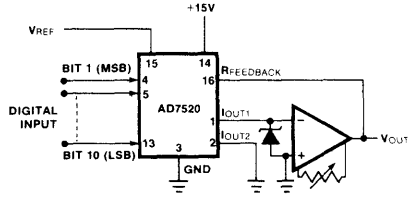


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}(1\text{-}2^{-n})$ reading. (n = 10 for AD7520 (AD7530) and n = 12 for AD7521 (AD7531)).
3. To decrease V_{OUT}, connect a series resistor (0 to 500 ohms) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 500) ohms) in the I_{OUT_1} amplifier feedback loop.

TABLE 1

CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1 - 2^{-n})$
1000000001	$-V_{REF}(1/2 + 2^{-n})$
1000000000	$-V_{REF} / 2$
0111111111	$-V_{REF}(1/2 - 2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. LSB = 2^{-n} V_{REF} 2. n = 10 for 7520, 7530
n = 12 for 7521, 7531

(APPLICATIONS, Cont'd.)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

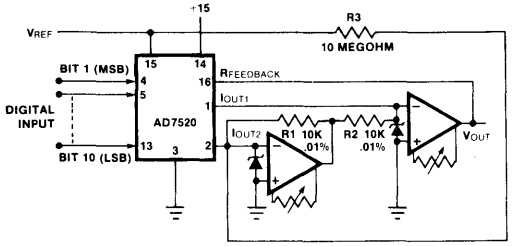


Figure 10. Bipolar Operation (4-Quadant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset zero adjust trimpot for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}(1\text{-}2^{-(n-1)})$ volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 500Ω between V_{OUT} and R_{fb}.
4. To decrease V_{OUT}, connect a series resistor of up to 500Ω between the reference voltage and the V_{REF} terminal.

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1 - 2^{-(n-1)})$
1000000001	$-V_{REF}(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(n-1)})$
0000000001	$V_{REF}(1 - 2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. $LSB = 2^{-(n-1)} V_{REF}$ **2.** n = 10 for 7520 and 7521; n = 12 for 7530 and 7531

POWER DAC DESIGN USING AD7520

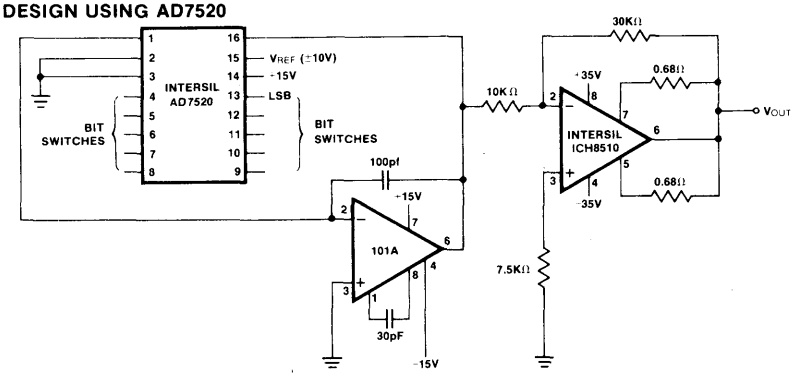


Figure 11. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 11. An INTERSIL IH8510 power amplifier (1 Amp continuous output at up to ±25 V) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the IH8510, by using a 25 V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

(APPLICATIONS, Cont'd.)

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 12, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

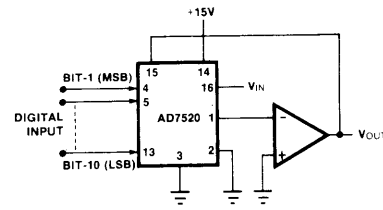


Figure 12. Analog/Digital Divider

For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al., Electronics, Dec. 9, 1976

AD7523
8 Bit Monolithic Multiplying D/A Converters

FEATURES

- **8, 9 and 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Fast settling time: 100 nS**
- **Four quadrant multiplication**
- **883B Processed versions available**

GENERAL DESCRIPTION

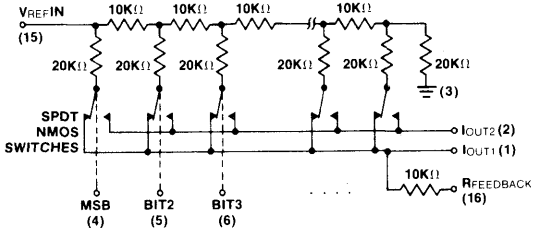
The Intersil AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with DTL/TTL/CMOS compatible operation.

Intersil AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

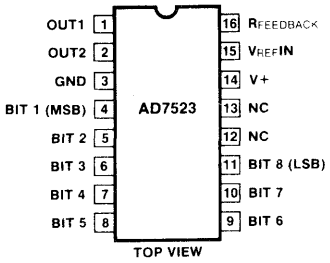
Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



TOP VIEW

OUTLINE DRAWINGS
DE,PE

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−20°C to +85°C	−55°C to +125°C
0.2% (8 Bit)	AD7523JN	AD7523AD	AD7523SD
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD

AD7523 T D

- D — Package: D — 18-Pin CERDIP DIP; N — 18-Pin Plastic DIP
- T — Nonlinearity and Temperature Range: J, K, L — Commercial 0°C to +70°C; A,B,C — Industrial −20°C to +85°C; S,T,U — Military −55°C to +125°C
- AD7523 — Basic Part Number

INTERSIL

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... −0.3 to VDD
Output Voltage Compliance ..... −0.3 to VDD
Power Dissipation (package)
Plastic
up to +70°C 670mW
derates above +70°C by ..... 8.3mW/°C
Ceramic
up to 75°C 450mW
derates above 75°C by ..... 6mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than VDD and lower than GND to any terminal except V_{REF} + R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

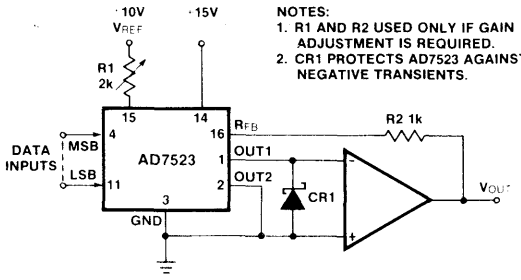
SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		8	8	Bits	Min	
Nonlinearity (Note 2)	(±1/2 LSB)	±0.2	±0.2	% of FSR	Max	
	(±1/4 LSB)	±0.1	±0.1	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V
	(±1/8 LSB)	±0.05	±0.05	% of FSR	Max	V_{OUT1} = V_{OUT2} = 0V
Monotonicity		Guaranteed				
Gain Error (Note 2)		±1.5	±1.8	% of FSR	Max	Digital inputs high.
Nonlinearity Tempco (Note 2 and 3)		2		PPM of FSR/°C	Max	−10V V_{REF} +10V
Gain Error Tempco (Note 2 and 3)		10		PPM of FSR/°C	Max	
Output Leakage Current (either output)		±50	±200	nA	Max	V_{OUT1} = V_{OUT2} = 0
AC ACCURACY (Note 3)						
Power Supply Rejection (Note 2)		0.02	0.03	% of FSR/%	Max	V^+ = 14.0 to 15.0V
Output Current Settling Time		150	200	nS	Max	To 0.2% of FSR, R_L = 100Ω
Feedthrough Error		±1/2	±1	LSB	Max	V_{REF} = 20V pp, 200KHz sine wave. All digital inputs low.
REFERENCE INPUT		5K		Ω	Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high. I_{OUT1} at ground.
Temperature Coefficient (Note 3)		−500		ppm/°C	Max	
ANALOG OUTPUT (Note 3)						Both outputs.
Voltage Compliance (Note 4)		−100mV to V^+				See maximum ratings.
Output Capacitance	C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
	C_{OUT2}	30		pF	Max	
	C_{OUT1}	30		pF	Max	All digital inputs low (VINL)
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (V_{INL})		0.8		V	Max	Guarantees DTL/TTL and CMOS (0.5
High State Threshold (V_{INH})		2.4		V	Min	max, 14.5 min) levels
Input Current (per input)		±1		μA	Max	V_{IN} = 0V or +15V
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		4		pF	Max	
POWER REQUIREMENTS						Accuracy is tested and guaranteed at
Power Supply Voltage Range		+5 to +16		V		V^+ = +15V, only.
I^+		100		μA	Max	All digital inputs low or high.

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

APPLICATIONS
UNIPOLAR OPERATION



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. CR1 PROTECTS AD7523 AGAINST NEGATIVE TRANSIENTS.

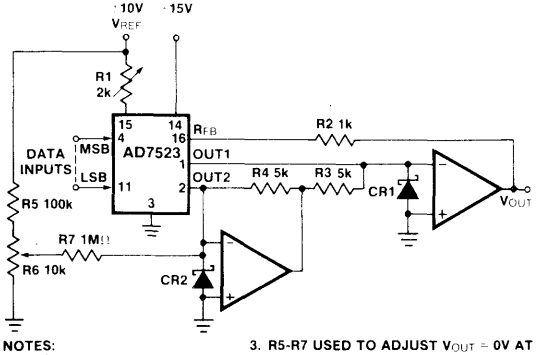
Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: 1 LSB = $(2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION



NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5-R7 USED TO ADJUST V_{OUT} = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 2. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

Note: 1LSB = $(2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7523

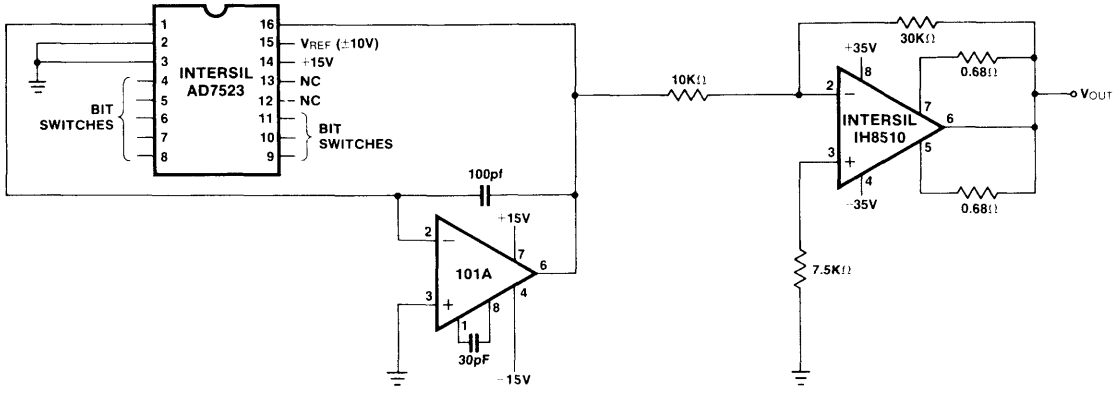


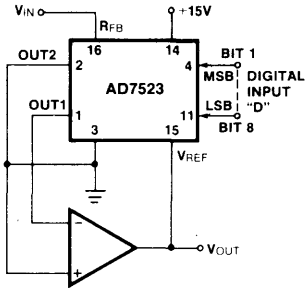
Figure 3. The Basic Power DAC

A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 3. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the IH8510, by using a 25 volts reference for the DAC.

APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



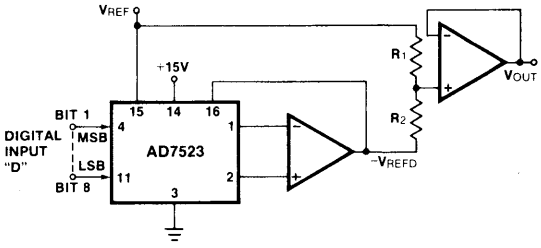
$V_{OUT} = -V_{IN/D}$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \cdots \frac{BIT8}{2^8}$$

$$\left(0 \leq D \leq \frac{255}{256}\right)$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right] \quad \text{WHERE:} \quad D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \cdots \frac{BIT\ 8}{2^8}$$

$$\left(0 \leq D \leq \frac{255}{256}\right)$$

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al., Electronics, Dec. 9, 1976

AD7533
10 Bit Monolithic Multiplying D/A Converters

FEATURES

- Lowest cost 10-bit DAC
- 8, 9 and 10 bit linearity
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS direct interface
- +5 to +15 volts supply range
- Low power dissipation
- Fast settling time
- Four quadrant multiplication
- Direct AD7520 equivalent
- 883B Processed versions available

GENERAL DESCRIPTION

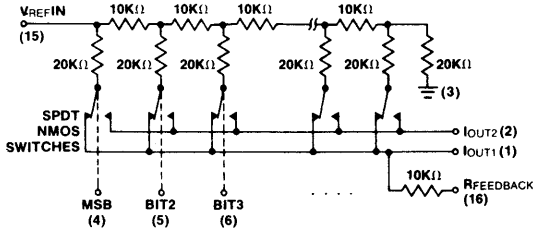
The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC).

Intersil's thin-film resistors on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V power range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation.

Pin and function equivalent to Industry Standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

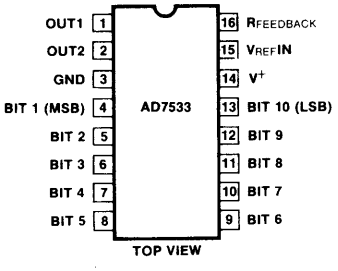
Application of AD7533 includes programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION

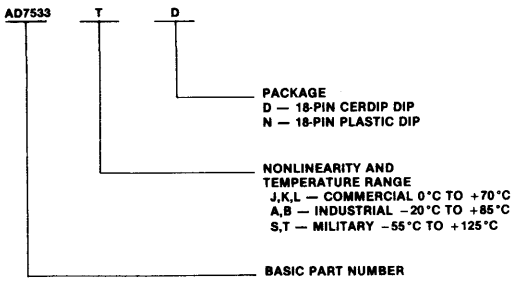


(Outline dwg DE, PE)

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-20°C to +85°C	-55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

PACKAGE IDENTIFICATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... −0.3V, +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... −0.3V to V^+
Output Voltage Compliance ..... −0.3 to V^+
Power Dissipation (package)
Ceramic
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C
Plastic
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2} = 0$ unless otherwise specified.)

PARAMETER		T_A +25°C	T_A MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		10	10	Bits	Min	
Nonlinearity (Note 2)		±0.2	±0.2	% of FSR	Max	
		±0.1	±0.1	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V
		±0.05	±0.05	% of FSR	Max	$V_{OUT1} = V_{OUT2}$ = 0V
Gain Error (Note 2 and 5)		±1.4	±1.5	% of FS	Max	Digital Inputs = V_{INH}
Output Leakage Current (either output)		±50	±200	nA	Max	V_{REF} = ±10V
AC ACCURACY						
Power Supply Rejection (Note 2 and 3)		0.005	0.008	% of FSR/%	Max	V^+ = 14.0 to 17.0V
Output Current Settling Time		600 (Note 6)	800 (Note 3)	nS	Max	To 0.05% of FSR, R_L = 100Ω
Feedthrough Error (Note 3)		±0.05	±0.1	% FSR	Max	V_{REF} = ±10V, 100kHz sine wave. Digital inputs low.
REFERENCE INPUT		5K			Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high.
Temperature Coefficient		−300		ppm/°C	Typ	
ANALOG OUTPUT						Both outputs.
Voltage Compliance (Note 4)		−100mV to V^+				See maximum ratings.
Output Capacitance (Note 3)	C_{OUT1}	100		pF	Max	All digital inputs high (V_{INH})
	C_{OUT2}	35		pF	Max	
	C_{OUT1}	35		pF	Max	All digital inputs low (V_{INL})
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (VINL)		0.8		V	Max	
High State Threshold (VINH)		2.4		V	Min	
Input Current (I_{IN})		±1		μA	Max	V_{IN} = 0V and V^+
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		5		pF	Max	
POWER REQUIREMENTS						
V_{DD}		+15 ±10%		V		Rated Accuracy
Power Supply Voltage Range		+5 to +16		V		
I^+		2		mA	Max	Digital Inputs = V_{INL} to V_{INH}
		100	150	μA	Max	Digital Inputs = 0V or V^+

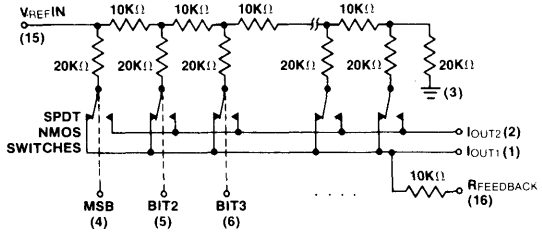
NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = − (V_{REF}) • (1023/1024)
6. Sample tested to ensure specification compliance.
7. 100% screened to MIL-STD-883, method 5004, para. 3.1.1. through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I^+ @ +25°C and +125°C (SD, TD, UD) or +25°C and +85°C (AD, BD, CD).

Specifications subject to change without notice.

GENERAL CIRCUIT INFORMATION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 1. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 1

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 2). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

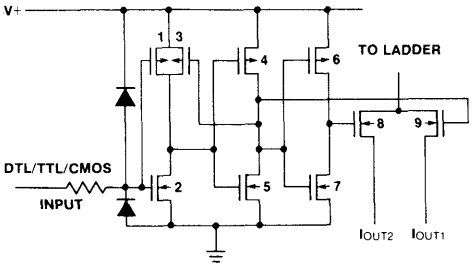
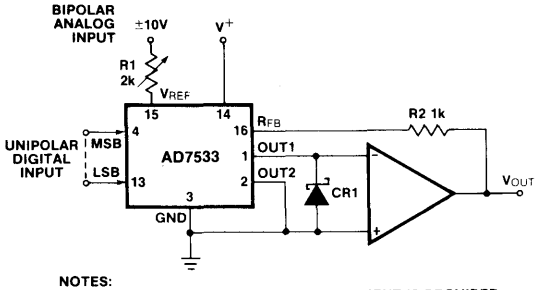


Figure 2

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082-2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS.

Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:

1. Nominal Full Scale for the circuit of Figure 3 is given by

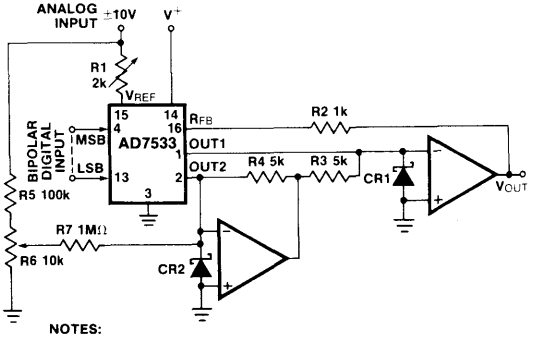
$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

Table 1. Unipolar Binary Code

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. SCHOTTKY DIODES CR1 AND CR2 (HP5082-2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS

Figure 4. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:

1. Nominal Full Scale Range for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7533

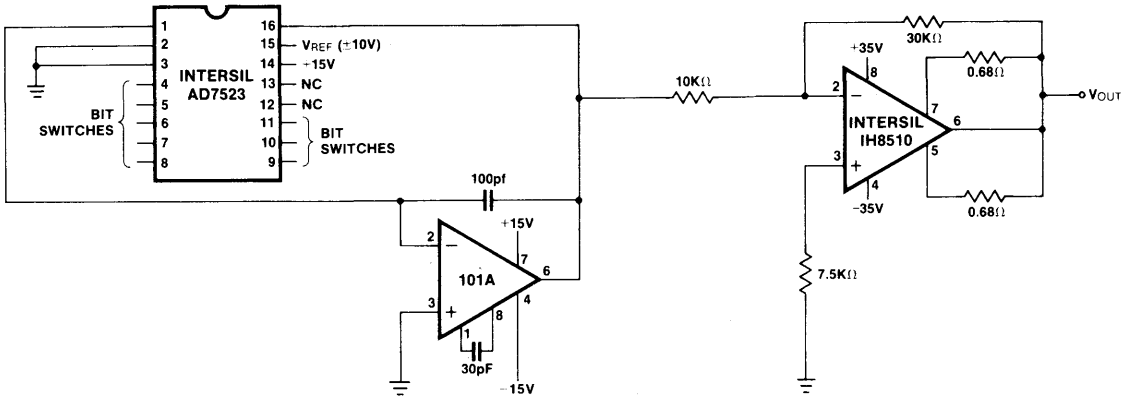
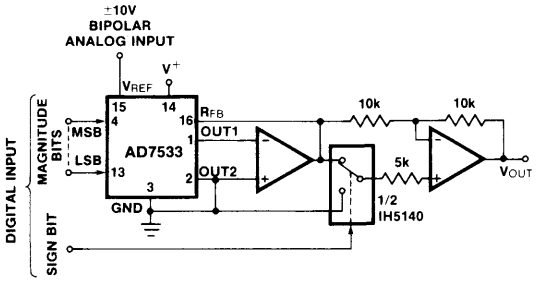


Figure 5. The Basic Power DAC

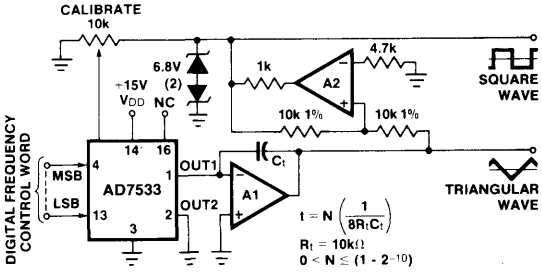
A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 5. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the 101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR



INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

AD7541
12 Bit Monolithic Multiplying D/A Converters

FEATURES

- **12 bit linearity (0.01%)**
- **Pretrimmed gain**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Low power dissipation (20mW)**
- **Current settling time: 1μs to 0.01% of FSR**
- **Four quadrant multiplication**
- **883B Processed versions available**

GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

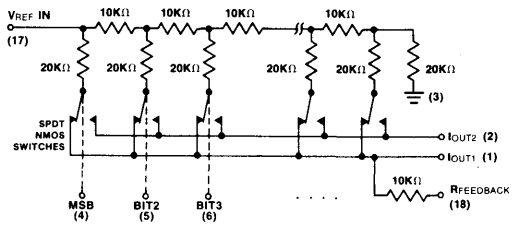
Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

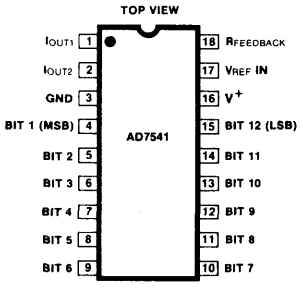
4

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



(Outline dwg DN, PN)

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−20°C to +85°C	−55°C to +125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	—	—

AD7541 T D

PACKAGE
D — 18-PIN CERDIP DIP
N — 18-PIN PLASTIC DIP

NONLINEARITY AND TEMPERATURE RANGE
J,K,L — COMMERCIAL 0°C TO +70°C
A,B — INDUSTRIAL −20°C TO +85°C
S,T — MILITARY −55°C TO +125°C

BASIC PART NUMBER

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C

Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD Versions ..... −20°C to +85°C
SD, TD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1)							
Resolution		12	12	Bits	Min		
Nonlinearity (Note 2)	S J	±0.020	±0.024	% of FSR	Max		
	T K	±0.010	±0.012	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V	1
	L	±0.010	±0.012	% of FSR	Max	V_{OUT1} = V_{OUT2} = 0V	
		Guaranteed Monotonic					
Gain Error (Note 2)		±0.3	±0.4	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V	
Output Leakage Current (either output)		±50	±200	nA	Max	V_{OUT1} = V_{OUT2} = 0	
AC ACCURACY (Note 3)							
Power Supply Rejection (Note 2)		±0.01	±0.02	% of FSR/%	Max	V^+ = 14.5 to 15.5V	2
Output Current Settling Time		1		µS	Max	To 0.01% of FSR	6
Feedthrough Error		1		mV pp	Max	V_{REF} = 20V pp, 10 kHz. All digital inputs low.	5
REFERENCE INPUT		5K		Ω	Min		
Input Resistance		10K			Typ	All digital inputs high.	
		20K			Max	I_{OUT1} at ground.	
ANALOG OUTPUT						Both outputs.	
Voltage Compliance (Note 4)		−100mV to V^+				See maximum ratings.	
Output Capacitance (Note 3)	C_{OUT1}	200		pF	Max	All digital inputs high (V_{INH})	4
	C_{OUT2}	60		pF	Max		
	C_{OUT1}	60		pF	Max	All digital inputs low (V_{INL})	4
	C_{OUT2}	200		pF	Max		
Output Noise (both outputs)		Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS							
Low State Threshold (VINL)		0.8		V	Max		
High State Threshold (VINH)		2.4		V	Min		
Input Current		±1		µA	Max	V_{IN} = 0 or V^+	
Input Coding		Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5.	
Input Capacitance (Note 3)		8		pF	Max		
POWER REQUIREMENTS						Accuracy is not guaranteed	
Power Supply Voltage Range		+5 to +16		V		over this range	
I^+		2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)		20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

TEST CIRCUITS

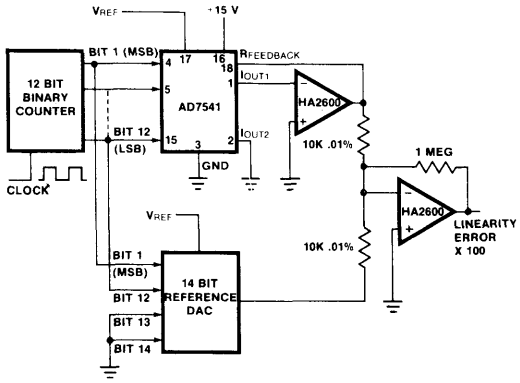


Figure 1. Nonlinearity

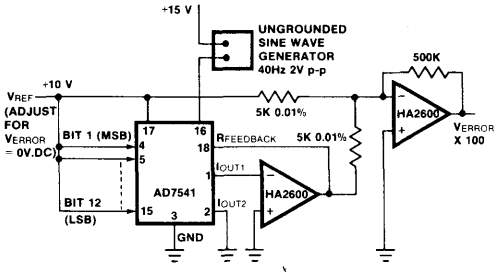


Figure 2. Power Supply Rejection

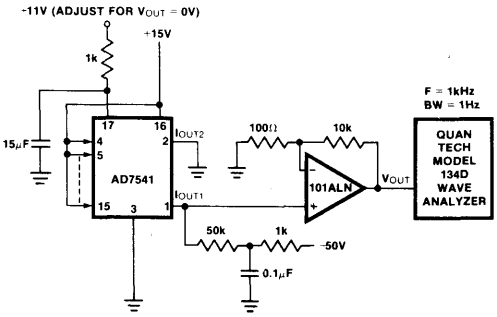


Figure 3. Noise

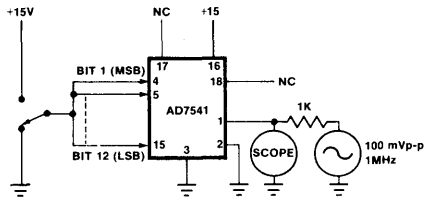


Figure 4. Output Capacitance

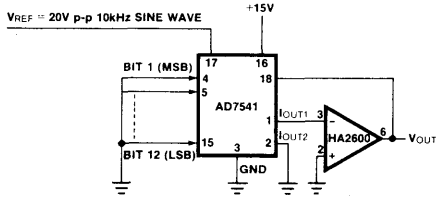


Figure 5. Feedthrough Error

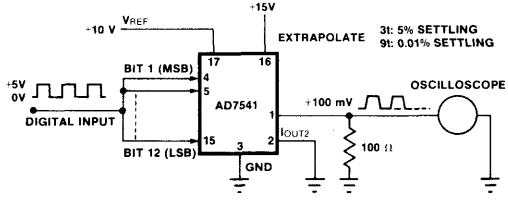


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

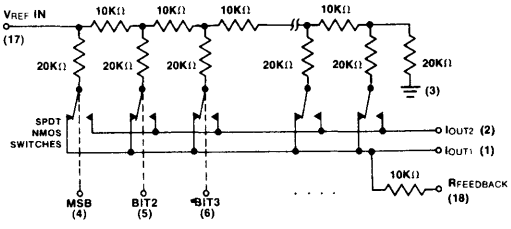
The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.



(Switches shown for Digital Inputs "High")

Figure 7. AD7541 Functional Diagram

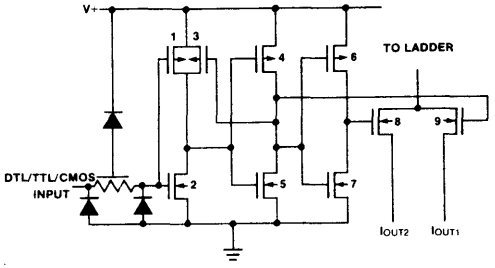


Figure 8. CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu V$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V^+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

APPLICATIONS, Continued

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. Schottky diode (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

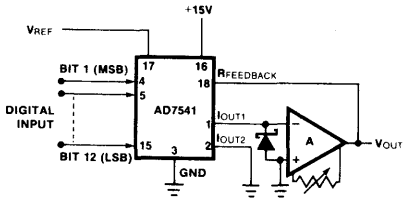


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

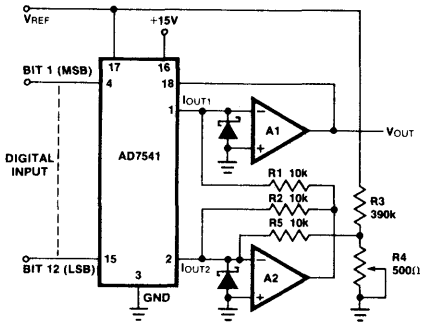
TABLE 1

Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{12})$
100000000001	$-V_{REF}(1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}(1/2 - 1/2^{12})$
000000000001	$-V_{REF}(1/2^{12})$
000000000000	0

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 10. Bipolar Operation (4-Quadrant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2

Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{11})$
100000000001	$-V_{REF}(1/2^{11})$
100000000000	0
011111111111	$V_{REF}(1/2^{11})$
000000000001	$V_{REF}(1 - 1/2^{11})$
000000000000	V_{REF}

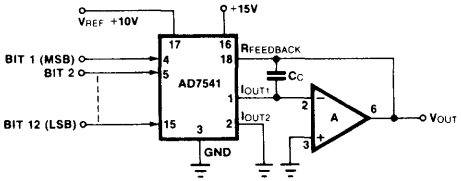


Figure 11. General DAC Circuit with Compensation Capacitor, C_C.

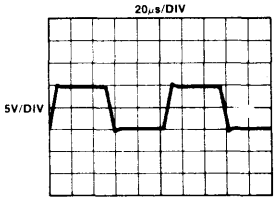


Figure 12. AD7541 Response with: A = Intersil 741HS

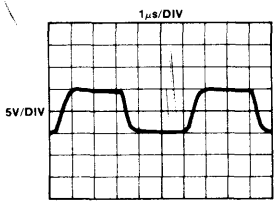


Figure 13. AD7541 Response with: A = Intersil 2515
C_C = 15pF

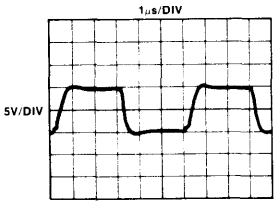


Figure 14. AD7541 Response with: A = Intersil 2520

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, alsodepends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5kΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

Three typical circuits and the resultant waveforms are shown in Figures 11 to 14. A low-cost general purpose (Intersil 741HS), a low-cost high-speed (Intersil 2515) and a high-speed fast-settling (Intersil 2520) amplifier cover the principal application areas.

4

INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

ICL8018A/8019A/8020A
Quad Current Switch for D/A Conversion

FEATURES
- **TTL Compatible: LOW—0.8V HIGH—2.0V**
- **12 Bit Accuracy**
- **40 nsec, Switching Speed**
- **Wide Power Supply Range**
- **Low Temperature Coefficient**

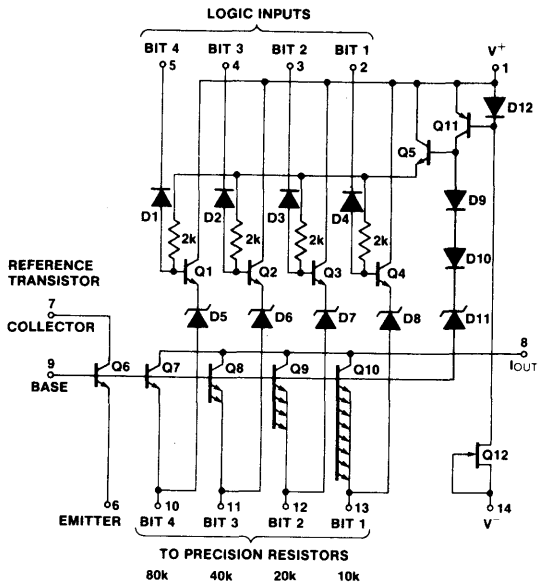
APPLICATIONS:
- D/A-A/D Converters
- Digital Threshold Control
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

4

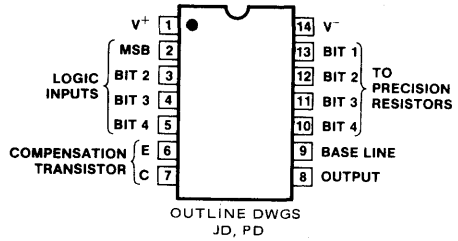
GENERAL DESCRIPTION
The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-to-analog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

SCHEMATIC DIAGRAM
EQUIVALENT CIRCUIT



PIN DIAGRAM



OUTLINE DWGS
JD, PD

ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
Individual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

***NOTE:** Units ordered in equal quantities will be matched such that the V_{be}'s of the 8019 will be within ±10mV of the 8018 compensating transistor, and the V_{be}'s of the 8020 will be within ±50mV. The ICL8018 - X matched sets consist of one 8018, one 8019, and one 8020. The 8019 - X contains one 8019 and one 8020, while the 8020 - X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Logic Input Voltage ..... −2V to V^+
Output Voltage ..... $V_{BASELINE}$ to +20V
$V_{BASELINE}$ ..... V^- to +5V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ICL8018AM
ICL8019AM ..... −55°C to +125°C
ICL8020AM
ICL8018AC
ICL8019AC ..... 0°C to +70°C
ICL8010AC
Lead Temperature (soldering 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($4.5V \leq V^+ \leq 20V$, $V^- = -15V$, $T_A = 25°C$, V @ pin 6 = −5V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Error					
ICL8018A	V_{INHI} = 5.0V			±.01	
ICL8019A	V_{INLO} = 0.0V			±0.1	%
ICL8020A				±1	
Error Temperature Coefficient					
ICL8018A			± 2	± 5	ppm/°C
ICL8019A			± 2	± 25	
ICL8020A			± 2	± 50	
Settling Time To ± 1/2 LSB, R_L = 1kΩ					
8 BIT			100		
12 BIT			200		ns
Switching Time To Turn On LSB			40		ns
Output Current (Nominal)					
BIT 1 (MSB)			1.0		mA
BIT 2			0.5		
BIT 3			0.25		
BIT 4 (LSB)			0.125		
Zero Output Current	V_{IN} = 5.0V		10	50	nA
Output Voltage Range		$V_{BASELINE}$ +1V		+10	V
Input Coding-Complimentary Binary (See Truth Table)					
Logic Input Voltage	ΔI_{OUT} <400nA				
"0" (Switch ON)				0.8	V
"1" (Switch OFF)		2.0			
Logic Input Current					
"0"	V_{IN} = 0V		−1.0	−2	mA
"1" (into device)	V_{IN} = 5V		0.01	0.1	μA
Power Supply Rejection					
V^+			.005		%/V
V^-			.0005		
Supply Voltage Range					
V^+		4.5	5	20	V
V^-		−10	−15	−20	
Supply Current (V_{SUPP} = ±20V)					
I^+			7	10	mA
I^-			1	3	

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 1. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see fig. 2. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

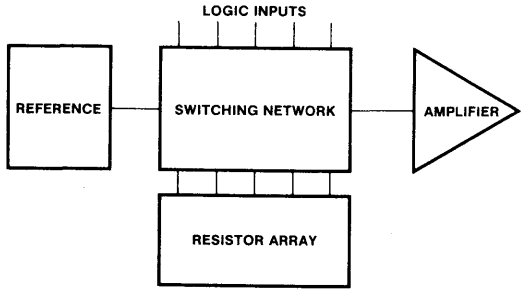


Figure 1: Elements of a D/A Converter

4

Logic Input	Nominal Output Current (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Figure 2: Truth Table

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Truth Table) each output corresponding to a particular logic input word.

Note that **maximum output** of the quad switch is $1 + 1/2 + 1/4 + 1/8 = 1\text{-}7/8 = 1.875$ mA. If this series of bits were continued as $1/16 + 1/32 + 1/64 \ldots\ldots$ **$1/2^{(n-1)}$**, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output**. The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be $\frac{4095}{4096} \times 10V$. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output**.

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic**. This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within ±1/2 LSB of an N bit converter. Since the 8018A family has been desiged with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Figure 3.

Bits of Resolution	±1/2 LSB Error % Full Scale	Number of Time Constants	Number of Rise Times
8	.2 %	6.2	2.8
10	.05%	7.6	3.4
12	.01%	9.2	4.2
Rise Time (10%-90%) = 2.2 R_L C_{eff}			

Figure 3: Settling Time vs. Rise Time Resistor Load

CIRCUIT OPERATION

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage

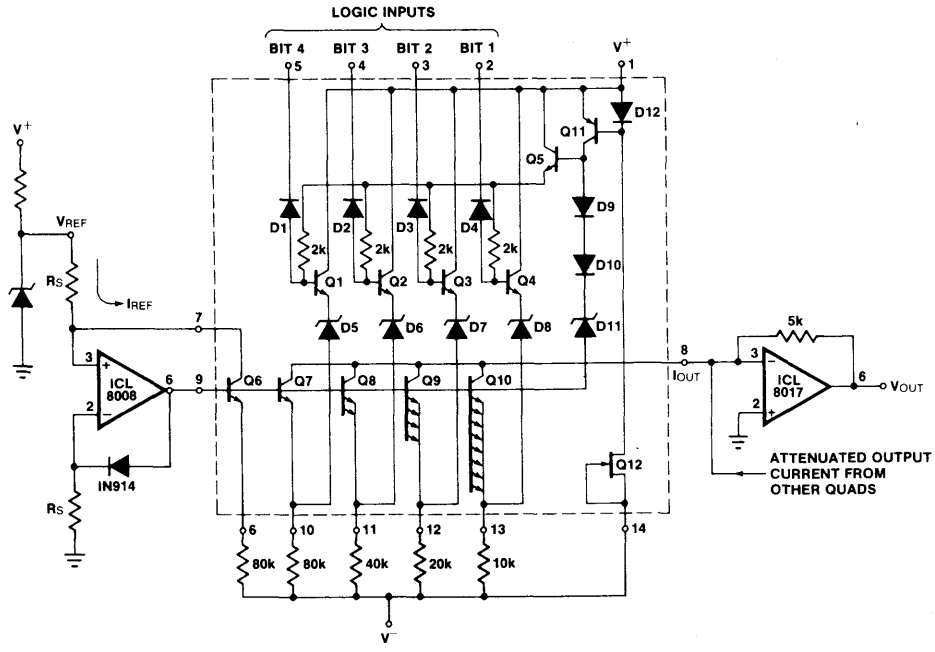


Figure 4: Typical Circuit

and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80k resistor in the emitter of Q_6. Since this resistor is connected to −15V, this puts the emitter of Q_6 at nearly −5V and the common base line at one V_{BE} more positive at −4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to −15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or 125μA. Q_8 has 40k in the emitter so that its collector current will be twice I_{REF} or 250μA. In the same way, the 20k and 10k in the emitters of Q_9 and Q_{10} contribute .5 mA and 1 mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

EXPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A converters, the 8018A is readily expanded to 8 and 12 bits with the addition of other quads and resistor dividers as shown in Figure 5.

To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., $I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16\,(1 + 1/2 + 1/4 + 1/8) + 1/256\,(1 + 1/2 + 1/4 + 1/8) = 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and 80k resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions; hence, the three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

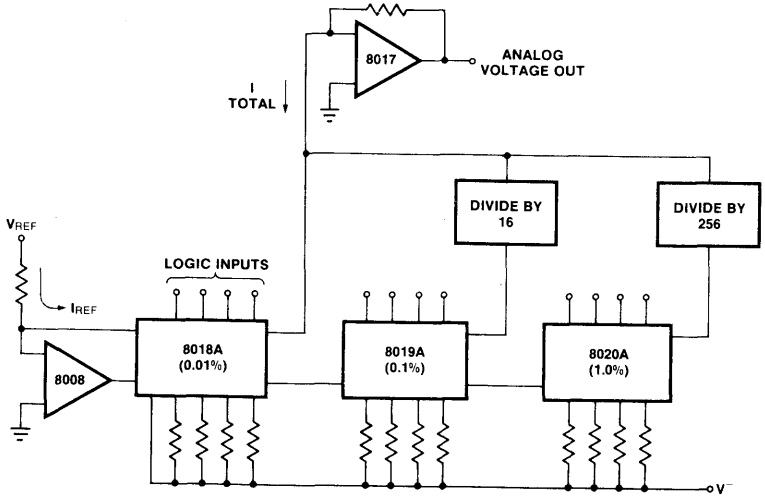


Figure 5: Expanding the Quad Switch

4

GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the 8018A switches currents determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

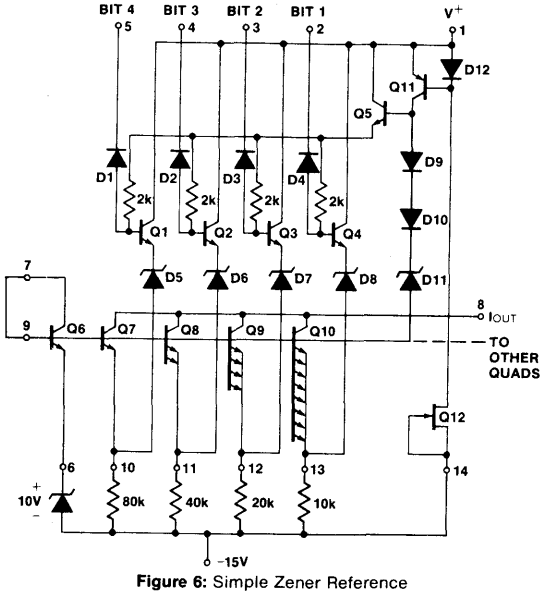


Figure 6: Simple Zener Reference

The zener current will be typically 1 mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. Holding the V^- supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

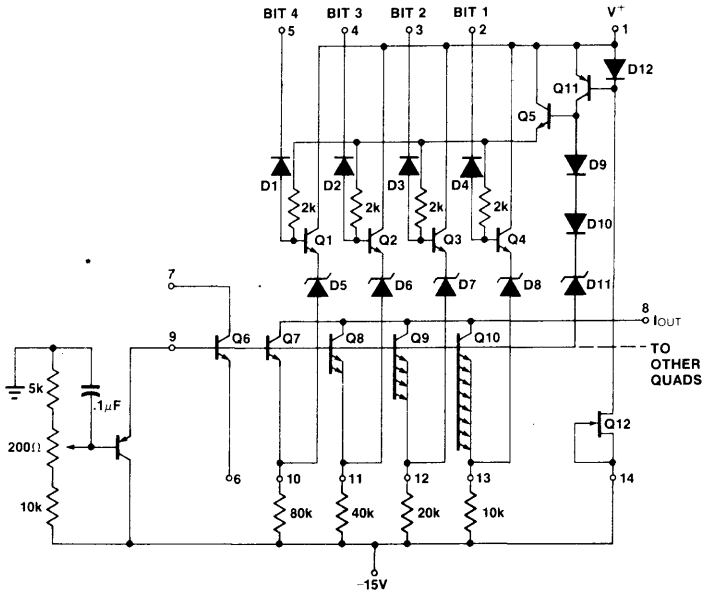
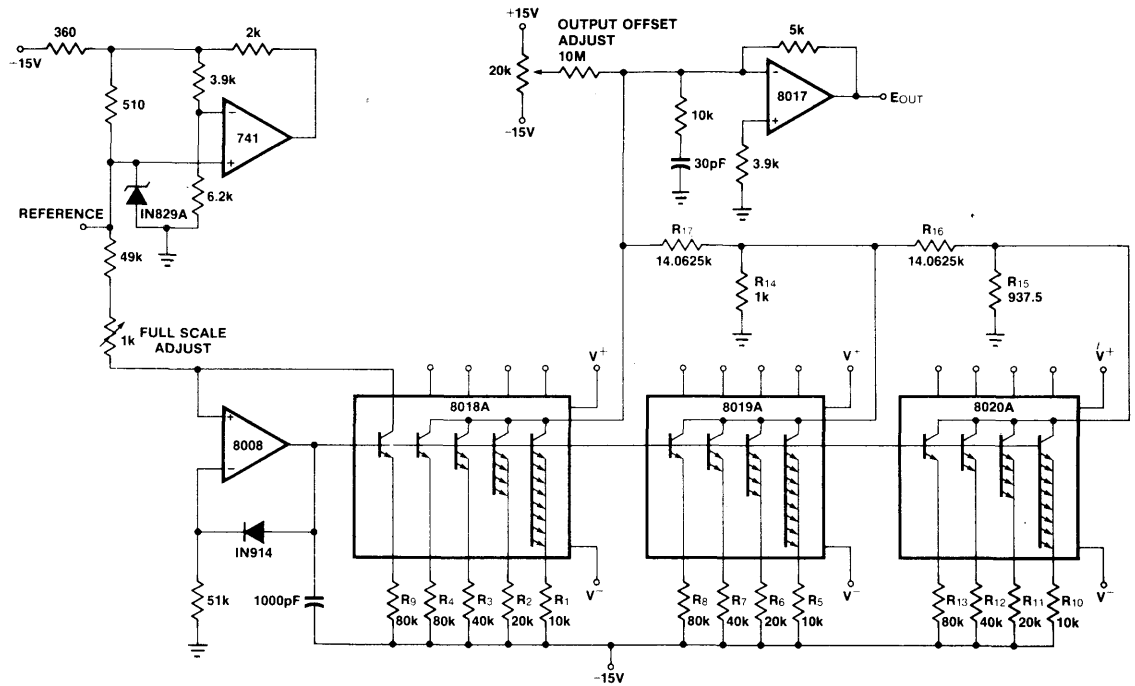


Figure 7: PNP Reference



NOTE: ALL RESISTORS RATIO TO R_1 UNLESS OTHERWISE NOTED.

TOLERANCE TABLE		
R_1	10k	0.1% ABS
R_2	20k	0.0122%
R_3	40k	0.0244%
R_4	80k	0.0488%
R_5	10k	0.096%
R_6	20k	0.195%
R_7	40k	0.391%
R_8	80k	0.781%
R_9	80k	0.1%
R_{10}	10k	0.5% ABS
R_{11}	20k	RATIO TO R_{10} 1%
R_{12}	40k	RATIO TO R_{10} 1%
R_{13}	80k	RATIO TO R_{10} 1%
R_{14}	1k	1% ABS
R_{15}	937.5Ω	1% ABS
R_{16}	14.0625k	RATIO TO R_{15} 1%
R_{17}	14.0625k	RATIO TO R_{14} 0.1%

Figure 8

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

4

PRACTICAL D/A CONVERTERS

The complete circuit for a high performance 12 bit D/A converter is shown in Figure 8. This circuit uses the "full compensation reference" described above to set the base line drive at the proper level, the temperature compensated zener is stabilized using an op-amp as a regulated supply, and the circuit provides a very stable, precise voltage reference for the D/A converter. The 16:1 and 256:1 resistor divider values are shown for a straight binary system; for a binary coded decimal system the dividers would be 10:1 and 100:1 (BCD is frequently encountered in building programmable voltage sources).

The analog output current of the 8018A current switches is converted to an output voltage using the 8017 as shown. The output amplifier must have low input bias current (small compared with the LSB current), low offset voltage and offset voltage drift, high slew rate and fast settling time. The input compensation shown helps improve pulse response by providing a finite impedance at high frequencies for a point that is virtual ground at DC.

An alternative bias scheme is shown in Figure 9. In this case, the bias at the common base line is fixed by inverting op-amp A_4, the gain of which is adjusted to give −5.0 volts at the emitter of the reference transistor. With the bias at the common base line fixed, the regular circuit of A_1 uses the internal reference transistor and drives the bus connecting all the precision resistors. This isolates the precision resistors from V^- fluctuations. Zener D_3 and constant current source Q_1 keep the regulating 8008 op-amp in mid-range. There are several alternative bias schemes depending on power supplies available. If −20 volts is used for V^-, the bottom of the precision resistor will be at −15 and operation will be the same as the standard circuit. If only −15V is available for V^- the gain of the output transconductance amplifier can be increased by 30% to allow use of a smaller switching currents with 7 volts across the precision resistors.

MULTIPLYING DAC

The circuit of Figure 9 is also convenient to use as a one quadrant multiplying D/A converter. In a multiplying DAC, the analog output is proportional to the product of a digital number and an analog signal. The digital number drives the logic inputs, while the analog signal replaces the constant reference voltage, and produces a current to set up the regulating 8008 op-amp. To vary the magnitude of currents being switched, the voltage across all the 10k, 20k, 40k and 80k resistors must be modulated according to the analog input. An analog input of 0 to +10 volts and an 80k resistor at the input to the 8008 will fulfill this requirement.

CALIBRATING THE 12 BIT D/A CONVERTER

1. With all logic inputs high (ones) adjust the output amplifier offset for zero volts out.
2. Put in the word 0000 1111 1111 (Quad 1 maximum output Quad 2 and 3 off) and adjust full scale pot for V_O of 15/16 (10V) where full scale output is to be 10 volts.
3. Put in the word 1111 0000 1111 and trim the Quad 2 divider for V_O of 15/256 (10V). This adjustment compensates for V_{BE} mismatches between quads although matched sets are available (see data sheet).
4. Put in the word 1111 1111 0000 and trim the Quad 3 divider for V_O of 15/4096 (10V).
5. Finally, with all bits ON (all 0's) readjust the full scale factor pot for

$$V_O = 4095/4096\ (10V)$$

SYSTEM INTERFACE REQUIREMENTS

Using the 8018A series in practical circuits requires consideration of the following interface requirements.

Logic Levels: The 8018A is designed to be compatible with TTL, DTL and RTL logic drive systems. The one constraint imposed on the external voltage levels is that the emitters of the conducting current switch transistors be in the vicinity of −5V; this will be the same as the voltage on Pin 6 if the reference transistor is used. When using other than −5V at Pin 6, the direct bearing on logic threshold should be considered.

Power Supplies: One advantage of the ICL8018A is its tolerance of a wide range of supply voltage. The positive supply voltage need only be large enough (greater than +4.5V) to keep Q_{11} out of saturation, and the negative supply needs to be more negative than −10V to ensure constant current operation of Q_{12}. The maximum supply voltage of ±20V is dictated by transistor breakdown voltages. It is often convenient to use ±15V supplies in systems with op-amps and other I.C.'s. These supplies tend to be better regulated and free from high current transients found on supplies used to power TTL Logic. As with any high speed circuit, attention to layout and adequate power supply decoupling will minimize switching effects.

Ground: High resolution D/A, e.g., 12 bits require fairly large logic drive currents. The change from all bits ON to all bits OFF is a considerable change in supply current being returned to ground. Because of this, it is usually advisable to maintain separate ground points for the analog and digital sections.

Resistors: Each quad current switch requires a set of matched resistors scaled proportional to their binary currents as R, 2R, 4R and 8R. For a 10V resistor voltage drop and "2 mA" full scale output current, resistor values of 10k, 20k, 40k and 80k are convenient. Other resistor values can be used, for example, to increase total output current. The

individual switched currents can be increased up to 100% of their nominal values. The overall accuracy of the complete D/A converter depends on the accuracy of the reference, the accuracy of the quad current switch and tolerance of resistor matching. Because of the binary progression of switched currents, the tolerance of 80k/10k match can be twice that of the 40k/10k which, in turn, can be twice the tolerance of the 20k/10k ratio and still have equal output current errors. The current dividers between quads allows use of less well matched sets of resistors further along in the D/A just as it allows use of .01%, 0.1%, and 1% accurate quad current switches. There are several manufacturers producing the complete precision resistor networks required to implement up to 12 bit D/A converters. Contact Intersil for additional information.*

*Resistor Ladder Networks are manufactured by the following companies:

Micro Networks Corporation
5 Barbara Lane
Worcester, Massachusetts 01604
Tel. (617) 756-4635

Allen-Bradley Company
1201 S. Second Street
Milwaukee, Wisconsin 53204
Tel. (414) 671-2000

Hycomp, Inc.
146 Main Street
Maynard, Massachusetts 01754
Tel. (617) 897-4578

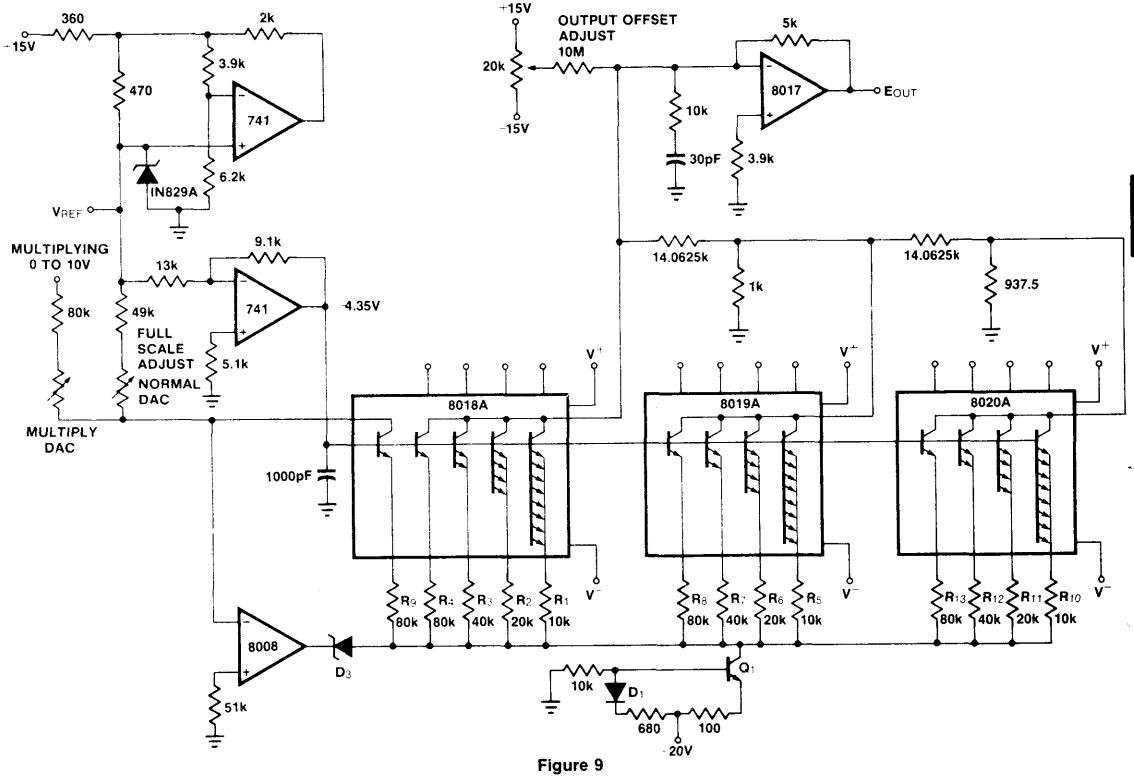


Figure 9

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.
A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.

ICL8052/ICL7104 and ICL8068/ICL7104

16/14/12 Bit Binary A/D Converter Pairs for μProcessors

FEATURES

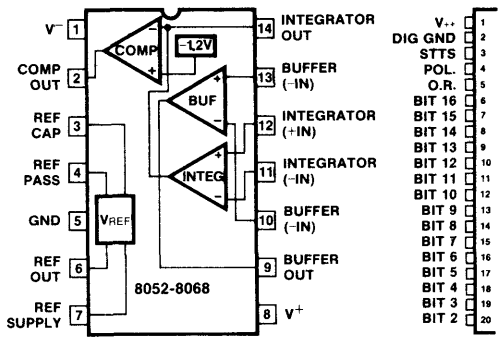
- 16 bit binary three-state latched outputs plus polarity and overrange. Also 14 and 12 bit versions.
- Ideally suited for interface to UARTs, microprocessors, or other complex circuitry.
- Conversion on demand or continuously.
- Handshake byte-serial transmission synchronously or on demand.
- Guaranteed zero reading for zero volts input.
- True polarity at zero count for precise null detection.
- Single reference voltage for true ratiometric operation.
- Onboard clock and reference.
- Auto-Zero; Auto-Polarity
- Accuracy guaranteed to 1 count.
- All outputs TTL compatible.
- ±10V analog input range
- Status signal available for external sync, A/Z in preamp, etc.

4

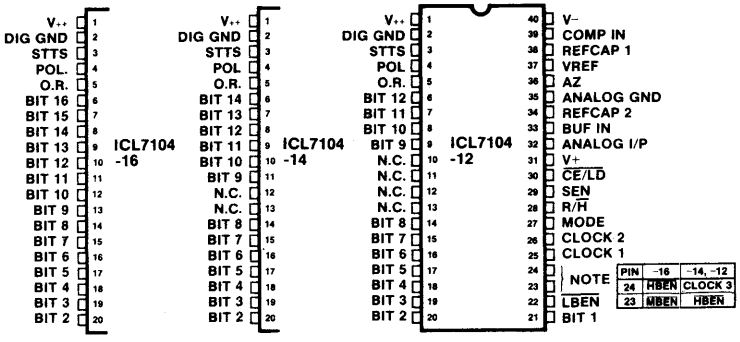
GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7014-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

PIN CONFIGURATIONS



(OUTLINE DWGS DD,JD,PD)



(OUTLINE DWGS DL,JL,PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14-Pin Plastic DIP	ICL8052CPD
8052	0°C to 70°C	14-Pin Ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14-Pin Plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14-Pin Ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14-Pin CERDIP	ICL8068CJD
8068A	0°C to 70°C	14-Pin CERDIP	ICL8068ACJD

Part	Temp. Range	Package	Order Number
7104 12-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-12CJL
7104 12-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-12CPL
7104 12-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-12CDL
7104 14-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-14CJL
7104 14-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-14CPL
7104 14-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-14CDL
7104 16-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-16CJL
7104 16-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-16CPL
7104 16-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-16CDL

ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] 500mW
Storage Temperature ..... −65°C to +150°C

8052, 8068

Supply Voltage ..... ±18V
Differential Input Voltage(8068) ..... ±30V
(8052) ..... ±6V
Input Voltage[2] ..... ±15V
Output Short Circuit Duration,
All Outputs[3] ..... Indefinite
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

7104

V+ Supply (GND to V+) 12V
V++ to V− 32V
Positive Supply Voltage (GND to V++) 17V
Negative Supply Voltage (GND to V−) 17V
Analog Input Voltage (Pin 32-39)[4] ..... V+ to V−
Digital Input Voltage ..... V+ +0.3V
(Pins 2-30)[5] ..... GND −0.3V

Notes:

1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.
2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.
4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V- = −15V, Ta = 25°C)

CHARACTERISTICS		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input	CLOCK 1	I_{IN}	Vin = +5V to 0V	±2	±7	±30	μA
Comparator I/P	COMP IN (Note 1)	I_{IN}	Vin = 0V to +5V	−10	±0.001	+10	μA
Inputs with Pulldown	MODE	I_{IH}	Vin = +5V	+1	+5	+30	μA
		I_{IL}	Vin = 0V	−10	±0.01	+10	μA
Inputs with Pullups	SEN, R/$\overline{H}$	I_{IH}	Vin = +5V	−10	±0.01	+10	μA
	$\overline{LBEN}$, $\overline{MBEN}$, $\overline{HBEN}$, $\overline{CE/LD}$ (Note 2)	I_{IL}	Vin = 0V	−30	−5	−1	μA
Input High Voltage	All Digital Inputs	V_{IH}		2.5	2.0	—	V
Input Low Voltage	All Digital Inputs	V_{IL}			1.5	1.0	V
Digital Outputs Three-Stated On	$\overline{LB\ EN}$, $\overline{MB\ EN}$ (16 only), $\overline{HB\ EN}$, $\overline{CE/LD}$ (Note 3)	V_{OL}	I_{OL} = 1.6 mA	—	.27	.4	V
		V_{OH}	I_{OH} = −10μA		4.5	—	V
	BIT n, POL, OR	V_{OH}	I_{OH} = −240μA	2.4	3.5	—	V
Digital Outputs Three-Stated Off	BIT $\overline{n}$, POL, OR	I_{OL}	0 ≤ Vout ≤ V+	−10	±.001	+10	μA
Non-Three-State Digital Output	STTS	V_{OL}	I_{OL} = 3.2 mA	—	.3	.4	V
		V_{OH}	I_{OH} = −400μA	2.4	3.3	—	V
	CLOCK 2	V_{OL}	I_{OL} = 320μA		0.5		V
		V_{OH}	I_{OH} = −320μA		4.5		V
	CLOCK 3 (-12, -14 ONLY)	V_{OL}	I_{OL} = 1.6 mA		.27	.4	V
		V_{OH}	I_{OH} = −320μA	2.4	3.5		V
Switch	Switch 1	$r_{DS(on)}$		—	25k		Ω
	Switches 2,3	$r_{DS(on)}$		—	4k	20k	Ω
	Switches 4,5,6,7,8,9	$r_{DS(on)}$		—	2k	10k	Ω
	Switch Leakage	$I_{D(off)}$		—	15		pA
Clock	Clock Freq. (Note 4)			DC	200	400	kHz
Supply Currents	+5V Supply Current All outputs high impedance	I+	Freq. = 200 kHz		200	600	μA
	+15V Supply Current	I++	Freq. = 200 kHz		.3	1.0	mA
	−15V Supply Current	I−	Freq. = 200 kHz		25	200	μA
Supply Voltage Range	Logic Supply	V+	Note 5	4.0		+11.0	V
	Positive Supply	V++		+10.0		+16.0	V
	Negative Supply	V−		−16.0		−10.0	V

Note 1: This spec applies when not in Auto-Zero phase.
Note 2: Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.
Note 3: Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.
Note 4: Clock circuit shown in Figs. 10 and 11.
Note 5: V+ must not be more positive than V++.

8068 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8068 MIN	8068 TYP	8068 MAX	8068A MIN	8068A TYP	8068A MAX	UNITS
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I_{SC}	Output Short-Circuit Current			5	10		5	10	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total				14		8	14	mA

4

8052 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	75		20	75	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20	100		20	100	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\ Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/7104

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8068A/7104-12			8068A/7104-14			8068A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-.000	±.000	+.000	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	$V_{in} = V_{Ref}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-4V \le V_{in} \le +4V$		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		3			2			2		μV
Leakage Current at Input (2)	V_{in} = 0V		200	265		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V 0°C ≤ T_A ≤ 70°C		1	5		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient (3)	V_{in} = +4V 0 ≤ T_A ≤ 50°C (ext. ref. 0 ppm/°C)		2	5		2	5		2	5	ppm/°C

SYSTEM ELECTRICAL CHARACTERISTICS: 8052/7104

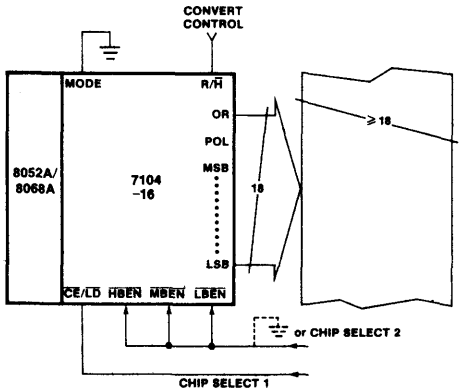
(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8052/7104-12			8052A/7104-14			8052A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-.000	±.000	+.000	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3)	$V_{in} = V_{Ref}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		20 50			30			30		μV
Leakage Current at Input (2)	V_{in} = 0V		30	80		20	30		20	30	pA
Zero Reading Drift	V_{in} = 0V 0° ≤ T_A ≤ 70°C		1	5		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 70°C (ext. ref. 0 ppm/°C)		3	15		2	5		2	5	ppm/°C

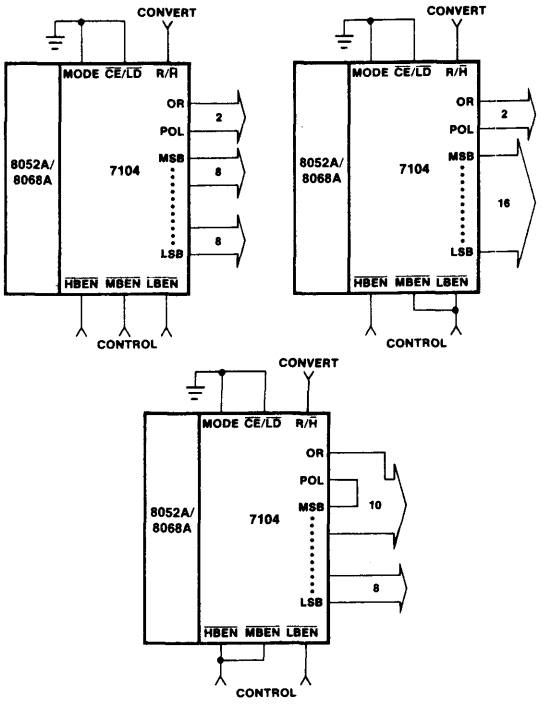
Note 1: Tested with low dielectric absorption integrating capacitor.

Note 2: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\ Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 3: The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.



Full 18 Bit Three State Output



Various Combinations of Byte Disables

AC CHARACTERISTICS (V++ = +15V, V+ = +5V, V− = −15V)

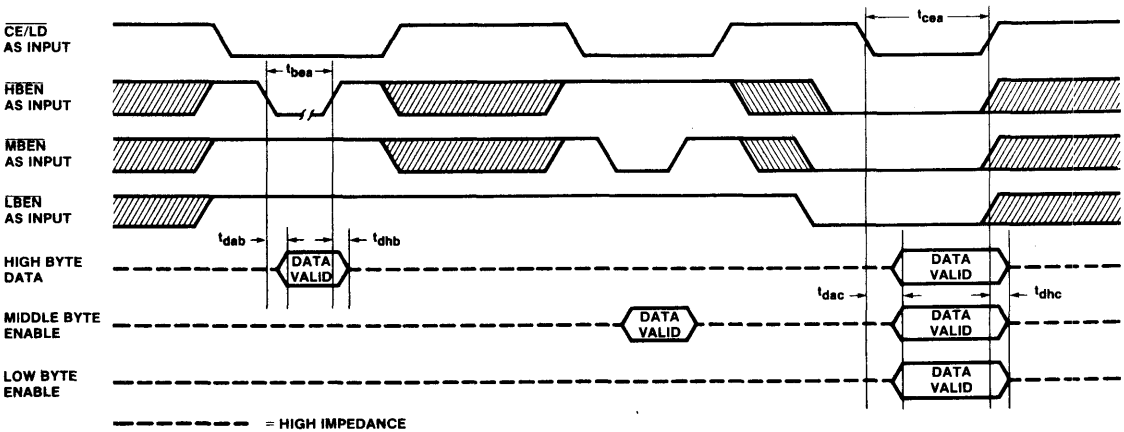
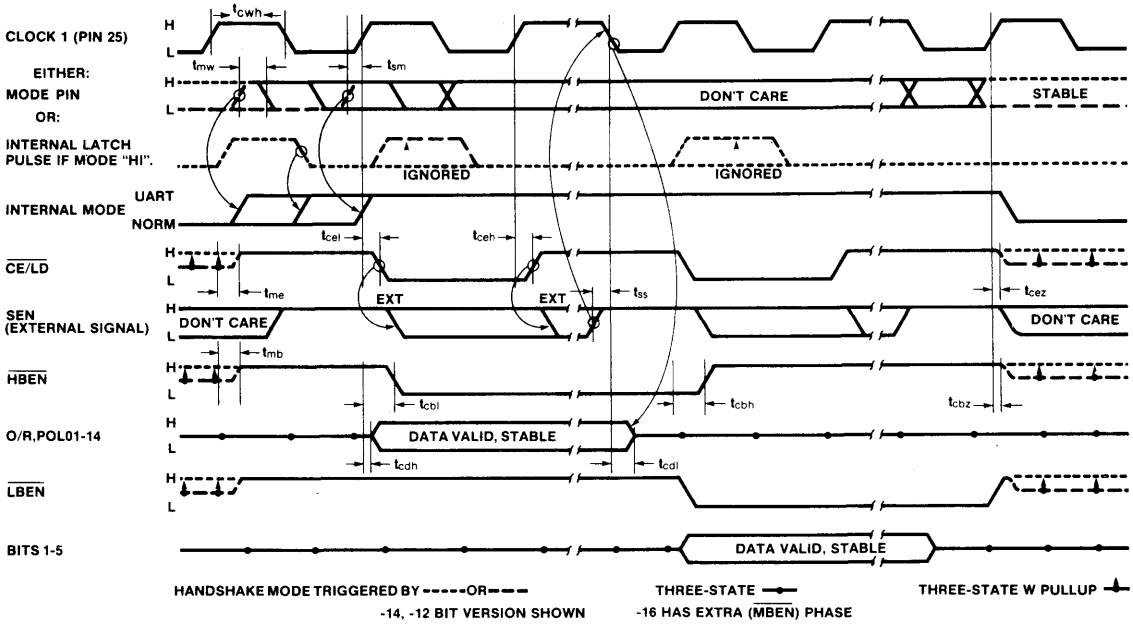


TABLE 1: Direct Mode Timing Requirements (Note: Not tested in production)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{bea}	$\overline{XBEN}$ Min. Pulse Width	400	300		ns
t_{dab}	Data Access Time from $\overline{XBEN}$		300	400	
t_{dhb}	Data Hold Time from $\overline{XBEN}$		200	250	
t_{cea}	$\overline{CE/LD}$ Min. Pulse Width	450	350		
t_{dac}	Data Access Time from $\overline{CE/LD}$		350	450	
t_{dhc}	Data Hold Time from $\overline{CE/LD}$		280	350	
t_{cwh}	CLOCK 1 High Time	1250	1000		

TABLE 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{mw}	MODE Pulse (minimum)		20		ns
t_{sm}	MODE pin set-up time		-150		
t_{me}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t_{mb}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		
t_{cel}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t_{ceh}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t_{cbl}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		
t_{cbh}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		
t_{cdh}	CLOCK 1 high to data enabled delay		1100		
t_{cdl}	CLOCK 1 low to data disabled delay		1100		
t_{ss}	Send ENable set-up time		-350		
t_{cbz}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		
t_{cez}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		
t_{cwh}	CLOCK 1 High Time	1250	1000		



Timing Relationships In Handshake Mode

TABLE 3: Pin Assignment and Function Description

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(++)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output .HI during Integrate and Deintegrate until data is latched .LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14 BIT 12	-16 -14 -12	(Most significant bit)
7	BIT 15 BIT 13 BIT 11	-16 -14 -12	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes. HIGH = true
8	BIT 14 BIT 12 BIT 10	-16 -14 -12	
9	BIT 13 BIT 11 BIT 9	-16 -14 -12	
10	BIT 12 BIT 10 nc	-16 -14 -12	
11	BIT 11 BIT 9 nc	-16 -14 -12	
12	BIT 10 nc nc	-16 -14 -12	
13	BIT 9 nc nc	-16 -14 -12	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit
22	$\overline{\text{LBEN}}$		Low Byte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE}}/\overline{\text{LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 8, 9 and 10.
	$\overline{\text{MBEN}}$	-16	Mid Byte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22)
23	$\overline{\text{HBEN}}$	-14 -12	High Byte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
	$\overline{\text{HBEN}}$	-16	High Byte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22).
24	CLOCK3	-14 -12	RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or oscillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO;Direct output mode where $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 9). If HI, enables $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 7 & 8 at conversion completion.
28	R/$\overline{\text{H}}$	Run/$\overline{\text{Hold}}$; Input HI-conversions continuously performed every 2^{17} (-16) 2^{15} (-14) or 2^{13} (-12) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{\text{CE}}/\overline{\text{LD}}$	$\overline{\text{C}}$hip-$\overline{\text{E}}$nable/$\overline{\text{L}}$oa$\overline{\text{D}}$. With MODE (pin 27) LO, $\overline{\text{CE}}/\overline{\text{LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{L}}$oa$\overline{\text{D}}$ strobe (-ve going) used in handshake mode. See Figures 7 & 8.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN.IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side)
38	REFCAP1	REFerence CAPacitor (positive side)
39	COMP-IN	COMParator INput from 8052/8068
40	V(-)	Negative Supply Voltage. Nominally -15V.

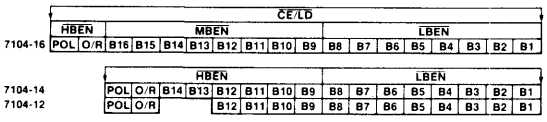


TABLE 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins.

Fig. 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to fig. 2 below.

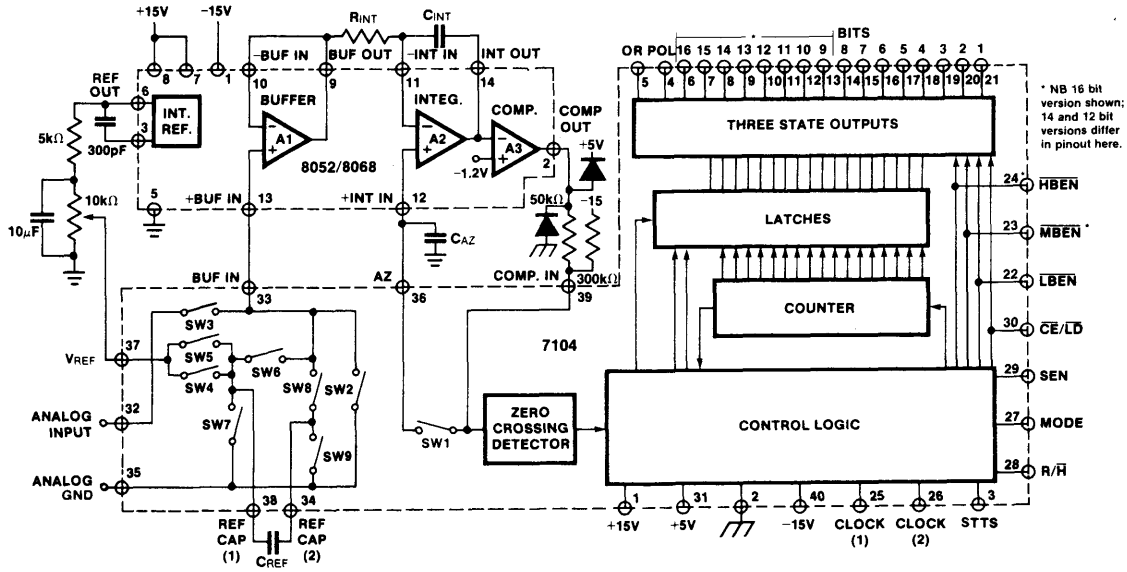


Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter Functional Block Diagram

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/$\overline{\text{Hold}}$ pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for −16; 32,368 for −14; and 8092 for −12 clock periods per cycle (see Figure conversion timing).

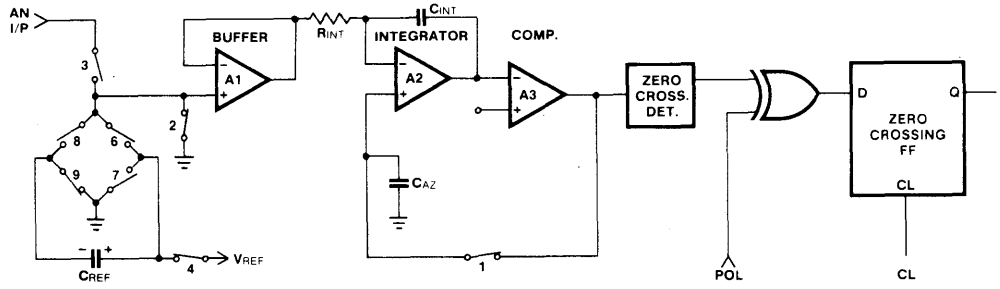


Figure 2A: Phase I Auto-Zero

1. Auto-Zero Phase I Fig. 2A

During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to V_{REF}.

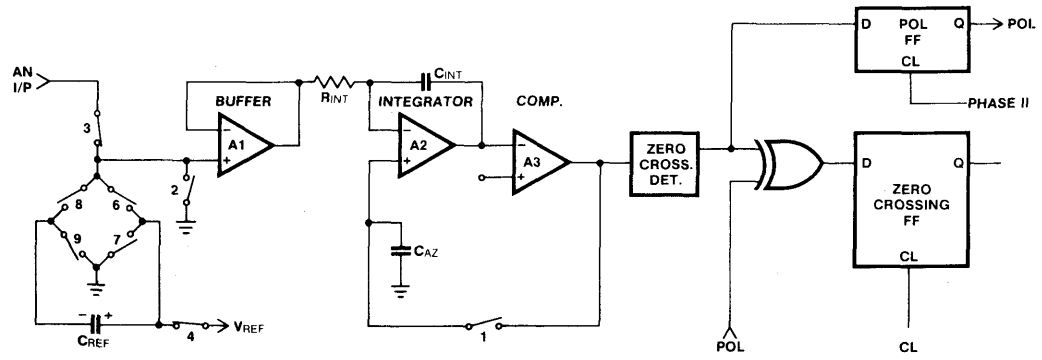


Figure 2B: Phase II Integrate Input

2. Input Integrate Phase II Fig. 2B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

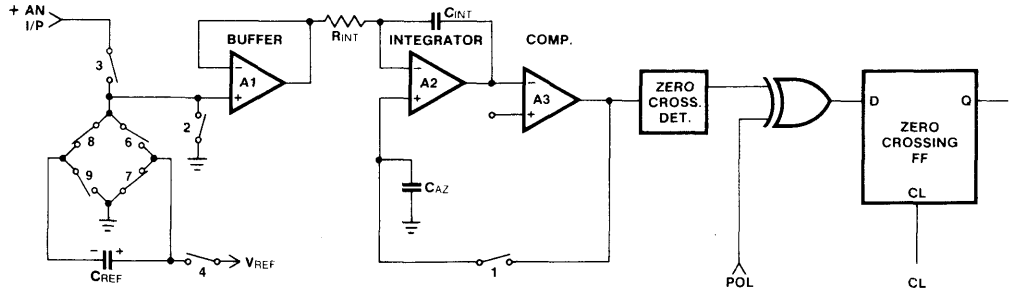


Figure 2C: Phase III + Deintegrate

Deintegrate Phase III Fig. 2C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{REF}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).

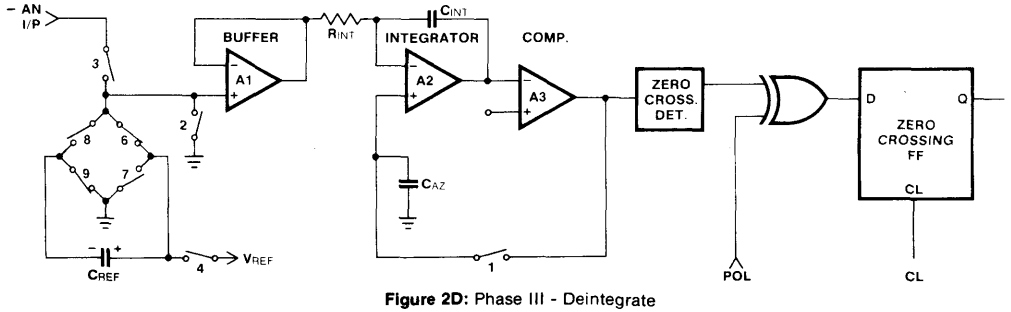


Figure 2D: Phase III - Deintegrate

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 4. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

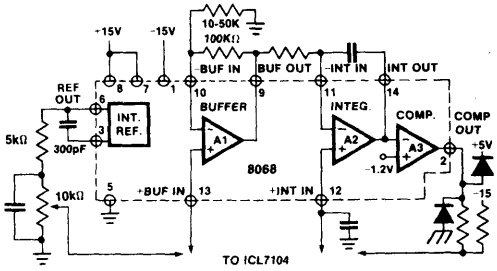


Figure 4: Adding Buffer Gain to ICL8068

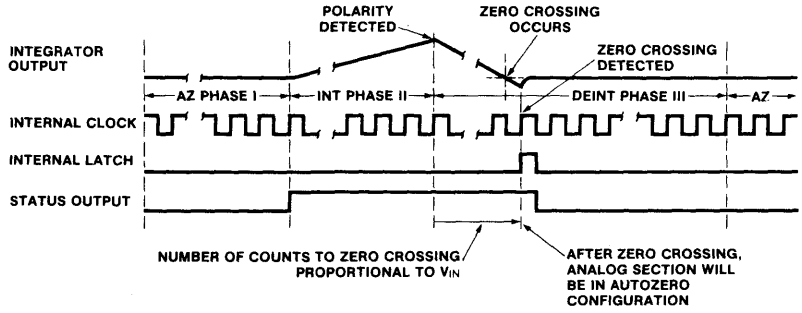
Table 5: Typical Component Values

V++ = +15V, V+ = 5V, V− = −15V, Clock Freq = 200 kHz

ICL8052/8068 with	ICL7104-16			ICL7104-14		ICL7104-12		UNITS
Full scale V_{IN}	200	800	4000	100	4000	50	4000	mV
Buffer Gain	10	1	1	10	1	10	1	
R_{INT}	100	43	200	47	180	27	200	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	.022	.022	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	.47	.47	μF
C_{ref}	10	1.0	1.0	10	1.0	4.7	4.7	μF
V_{REF}	100	400	2000	50	2000	25	200	mV
Resolution	3.1	12	61	6.1	244	12	980	μV

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.



	COUNTS		
	Phase I	Phase II	Phase III
-16	32768	32768	65536
-14	8192	8192	16384
-12	2048	2048	4096

Figure 3: Conversion Timing

4

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\left[\begin{array}{l}\text{(32768 for -16}\\ \text{(8192 for -14 X clock period)}\\ \text{(2048 for -12}\end{array}\right] \text{ X } (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale (100...000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16, 14 or 12 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 5 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 and 7104-12, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Run/Hold Input

When the Run/Hold input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16, 32768 for 7104-14 and 8192 for 7104-2 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 6 for details.

Using the Run/Hold input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/Hold low. When Run/Hold goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). Run/Hold may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/Hold can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/Hold input can be provided by connecting it to the CLOCK3 (-12, -14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

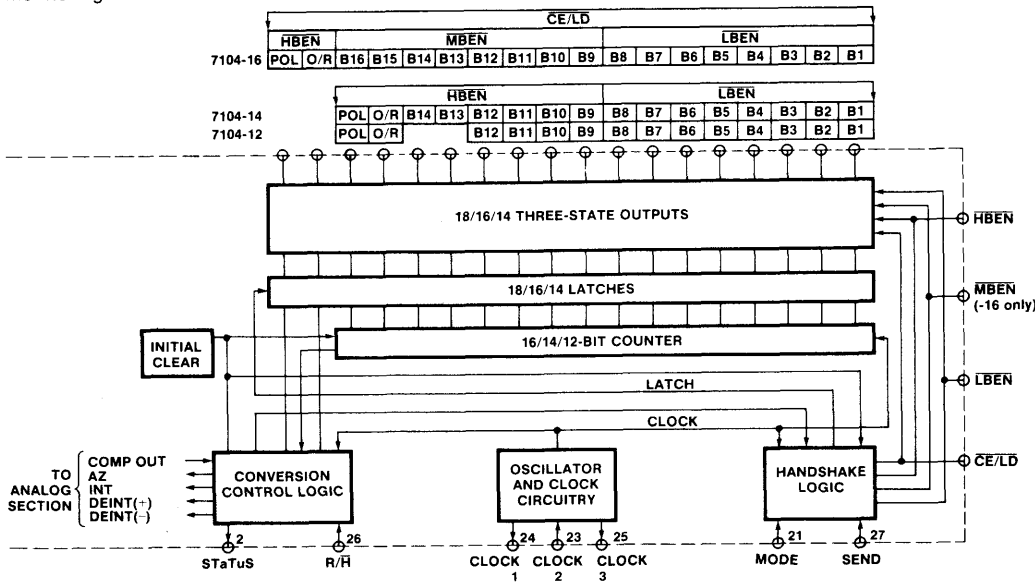


Figure 5: Digital Section

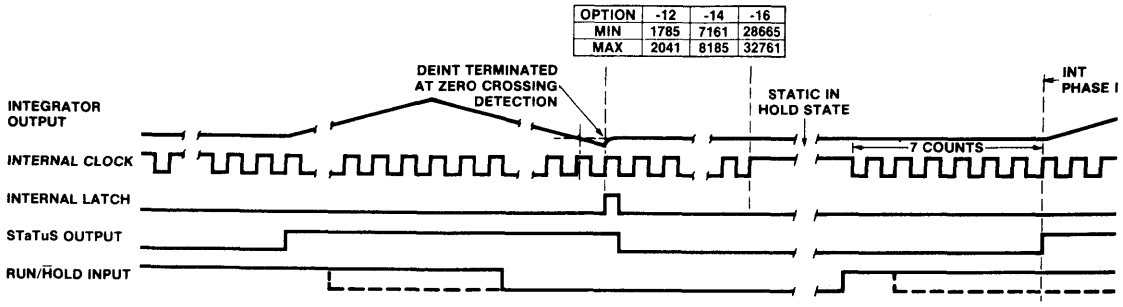


Figure 6: Run/Hold Operation

If the Run/$\overline{\text{H}}$old input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/$\overline{\text{H}}$old to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs[bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes]are accessible under control of the byte and chip ENable terminals as inputs. These $\overline{\text{EN}}$able inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip $\overline{\text{EN}}$able input is low, taking a byte $\overline{\text{EN}}$able input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

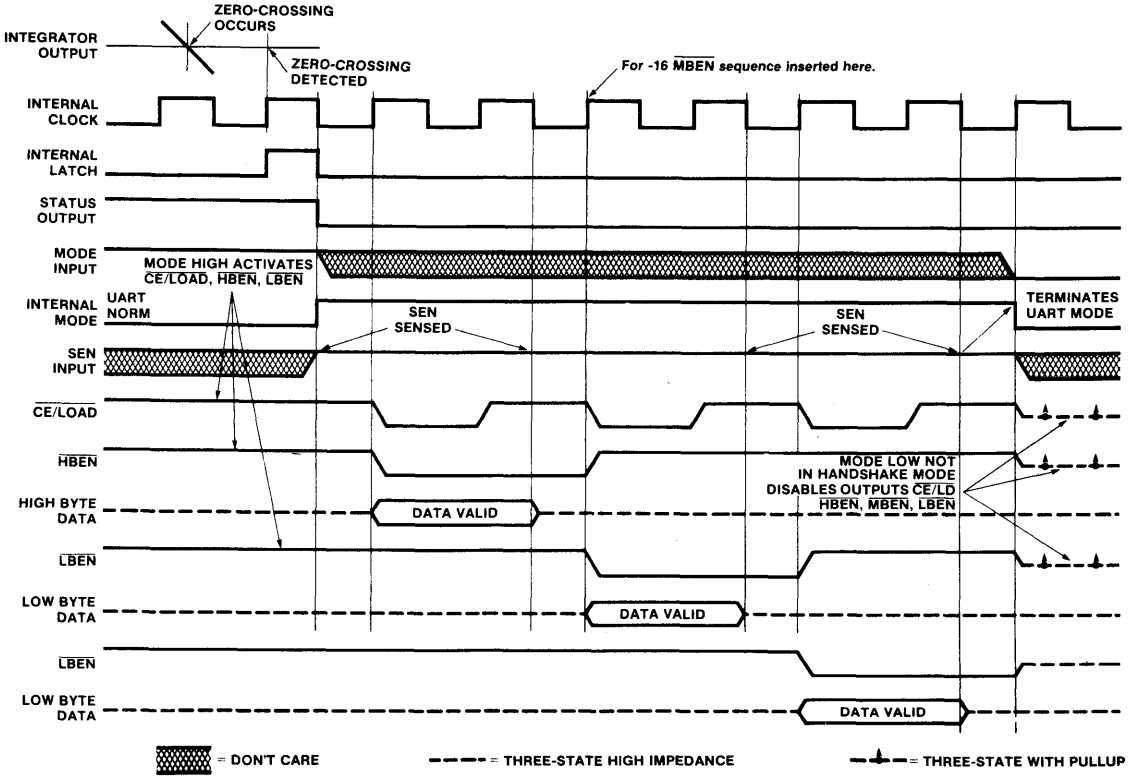


Figure 7: Handshake With SEN Held Positive

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte $\overline{\text{EN}}$able inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14, -12) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte $\overline{\text{EN}}$able terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send $\overline{\text{EN}}$able pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte $\overline{\text{EN}}$able line goes low, and the Chip $\overline{\text{EN}}$able/LoaD line (pin 30) ($\overline{\text{CE}}$/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte $\overline{\text{EN}}$able pin will be cleared high, and (unless finished) the $\overline{\text{CE}}$/$\overline{\text{LD}}$ and the next byte $\overline{\text{EN}}$able pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte $\overline{\text{EN}}$able pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 7, 8, and 9, and Table 2.

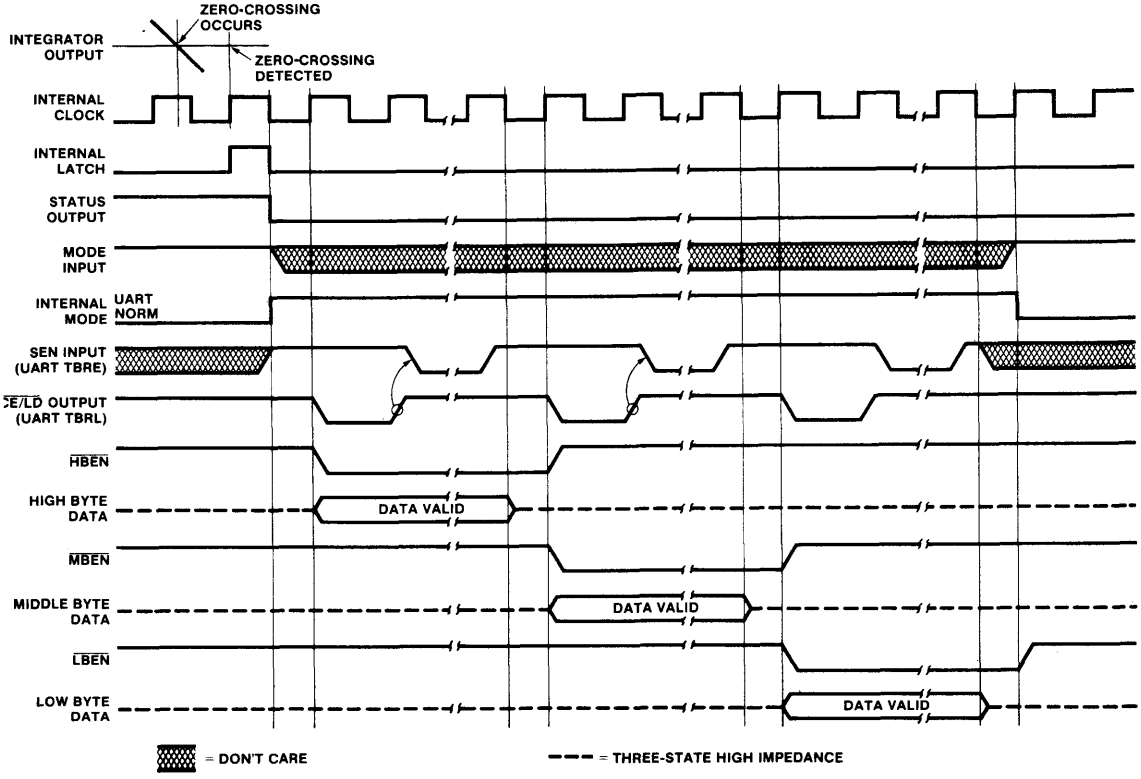


Figure 8: Handshake - Typical UART Interface Timing

Figure 7 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE}/\overline{LD}$, $\overline{LBEN}$, $\overline{MBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE}/\overline{LD}$ and the $\overline{HBEN}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bis 9-14) outputs are enabled. The $\overline{CE}/\overline{LD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{EN}$able remains low for two clock periods. Thus the $\overline{CE}/\overline{LD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{EN}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{CE}/\overline{LD}$, $\overline{MBEN}$ and $\overline{LBEN}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14, -12).

Figure 8 shows an output sequence where the SENinput is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART.

The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion

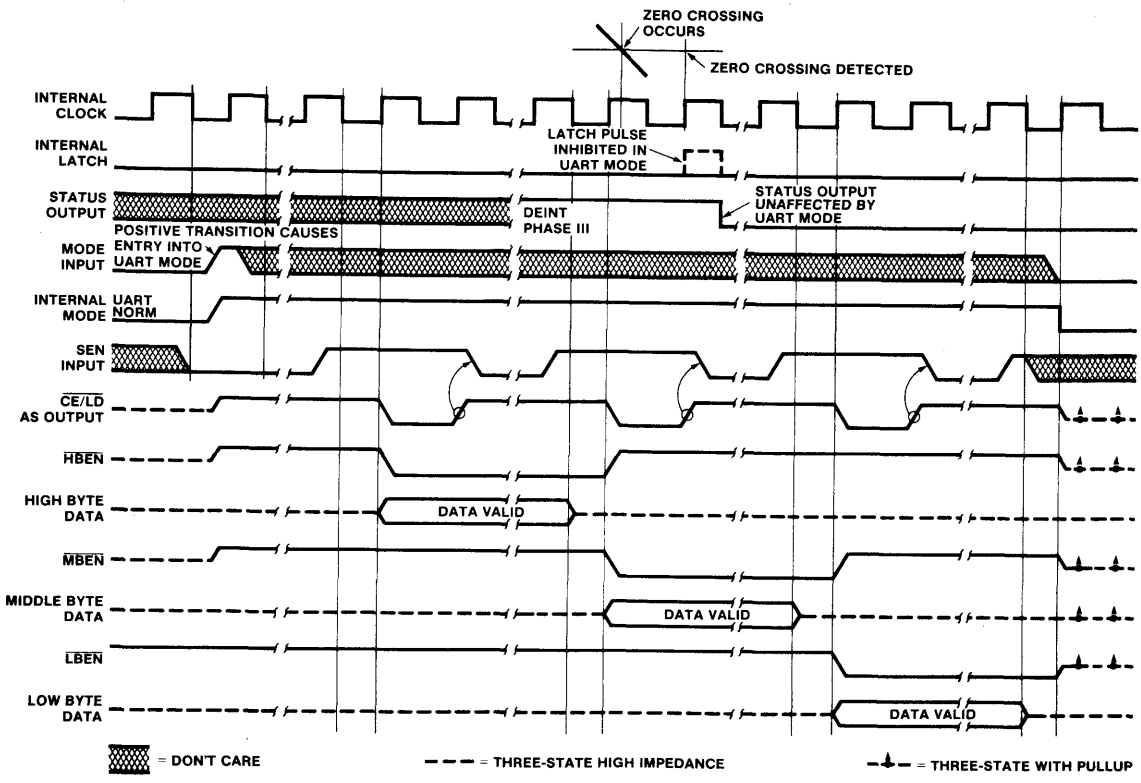


Figure 9: Handshake Triggered By Mode

except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 11 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/$\overline{\text{Hold}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" FF cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" FF should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to buss conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE FF will be cleared as fast as possible (see Fig. 7 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 and -12 are provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 10 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. A 50-100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14), 2048 (-12) clock periods is close to an integral multiple of the 60Hz period.

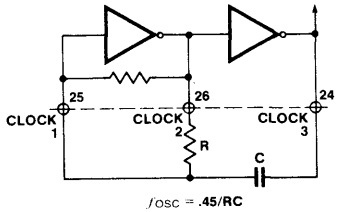


Figure 10: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 11 shows a crystal oscillator circuit, which can be used with all 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

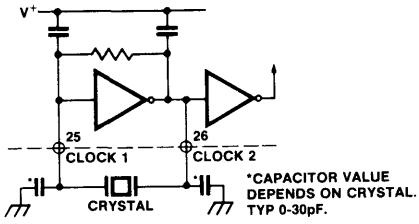


Figure 11: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V^+ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 12.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar
A017 "The Integrating A/D Converter", by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A025 "Building a Remote Data Logging Station", by Peter Bradshaw
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

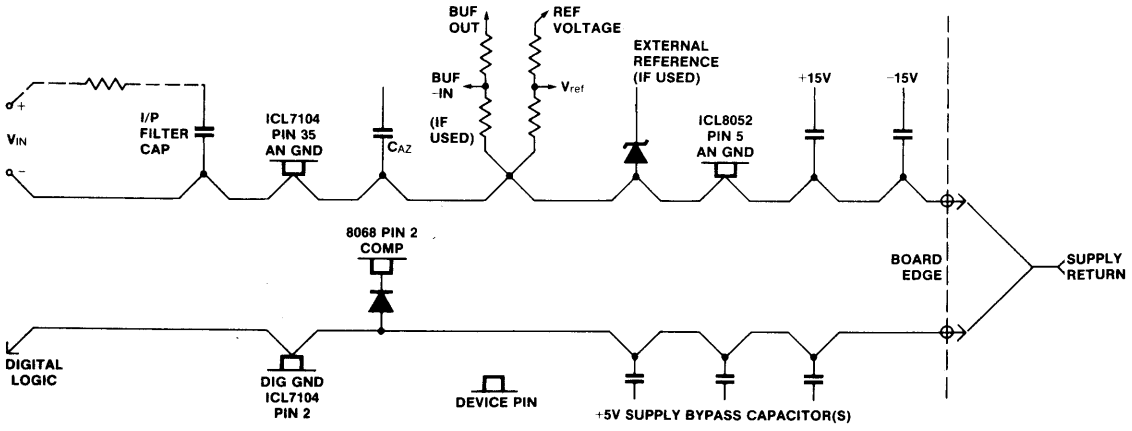


Figure 12: Grounding Sequence

Linear

Amplifiers

Driver Amplifier for Power Transistors — Page
ICL8063 5-182

Driver Amplifier for Actuators, Motors
ICH8510/20/30 5-214
ICH8515 5-222

Instrumentation Commutating Auto-Zero
ICL7605/6 5-63

Log-Antilog
ICL8048/49 5-174

Operational Chopper Stabilized
ICL7650 5-88
ICL7652 5-96

Operational, FET Input
LH0042 **
AD503 **
SU/NE536 **
μA740 **
ICL8007 5-139
ICL8043 5-167
ICH8500 5-208

Operational, General Purpose
OP-05 5-8
OP-07 5-16
LM101/301A **
LM107/307 **
LM108/308 5-24
μA741 **
ICL741HS 5-44
AD741K **
ICL741LN 5-46
μA748 **
μA777 5-49
LH2101/2301 **
LH2108/2308 5-55
IH5101 **
ICL8008 5-142

Operational, High Speed
ICL8017 5-151

Operational, Low Power
LM4250 **
ICL76XX Series 5-73
ICL8021-23 5-155

Video
μA733 **
NE/SE592 5-38
NE592-8 5-41

Voltage Followers
LM102/302 **
LM110/310 **
LH2110/2310 **

Comparators

Dual
LH2111/2311 **

Low Power
ICL8001 5-135

Precision
LM111/311 **

Sample and Hold

IH5110-15 5-57

Temperature Sensor

AD590 5-28

Voltage Reference

ICL8069 5-190
ICL8075-9 5-192
ICL8211/12 5-198

Voltage Regulators

LM100/300 **
LM105/305 **
μA723 **
ICL7663/4 5-111

Special Function

Multiplier
ICL8013 5-144

Voltage Converter
ICL7660 5-104

Waveform Generator
ICL8038 5-158

Low Battery Detectors
ICM7201 **
ICL7665 5-121
ICL8211/12 5-198

Power Mos Driver
ICL7667 5-128

** Not appearing in this catalog. Contact local sales representative for specific product information.

Operational Amplifiers — General Purpose

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (typ) (MHz)	I_{SUPP} (mA)	T_A (°C)	Packages*	Remarks
108	Low Level, Uncompensated	2.0	2.0	50,000	1.0	0.6	−55, +125	J, F, T	
108LN	Guaranteed Noise 108	2.0	2.0	50,000	1.0	0.6	−55, +125	T	$70nV/\sqrt{Hz}$ @10Hz
308	Low Level, Uncompensated	7.5	7.0	25,000	1.0	0.8	0, +70	F, J, P, T	
308LN	Guaranteed Noise 308	7.5	7.0	25,000	1.0	0.8	0, +70	T	$70nV/\sqrt{Hz}$ @10Hz
777	General Purpose Comparator	0.7	25	150,000	0.8	2.5	−55, +125	P, T	
777C	General Purpose Comparator	0.7	25	150,000	0.8	2.5	0, +70	P, T	
8008M	Low Bias Current, Compensated	5.0	10	20,000	1.0	2.8	−55, +125	J, T	
8008C	Low Bias Current, Compensated	6.0	25	20,000	1.0	2.8	0, +70	J, P, T	
LH2108	Dual Super Beta	2.0	3.0	25,000	1.0	0.4	−55 to +125	D	Build to Order
LH2108A	Dual Super Beta	0.5	3.0	40,000	1.0	0.4	−55 to +125	D	
LH2308	Dual Super Beta	7.5	10	15,000	1.0	0.4	0 to +70	D	
LH2308A	Dual Super Beta	0.5	10	60,000	1.0	0.4	0 to +70	D	

Operational Amplifiers — Low Power Programmable

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (MHz)	I_{SUPP} (μA)	@ I_{set} (μA)	@ V_s (V)	T_A (°C)	Packages*
8021M	Programmable, Compensated	3.0	20	50,000	0.27	40	30	+6.0	−55 to +125	J, T
8021C	Programmable, Compensated	6.0	30	50,000	0.27	50	30	+6.0	0, +70	T
8022M	Dual 8021M	3.0	20	50,000	0.27	40	30	+6.0	−55 to +125	J, F
8022C	Dual 8021C	6.0	30	50,000	0.27	50	30	+6.0	0, +70	J, P
8023M	Triple 8021M	3.0	20	50,000	0.27	40	30	+6.0	−55 to +125	J
8023C	Triple 8021C	6.0	30	50,000	0.27	50	30	+6.0	0 to +70	J, P
7611	CMOS	2.0	0.001	100,000	1.4	20	–	–	C,I,M	T, P
7612	CMOS, Extended CMVR	2.0	0.001	100,000	1.4	20	–	–	C,I,M	T, P
7613	CMOS, Input Protected to ± 200V	2.0	0.001	100,000	1.4	20	–	–	C,I,M	T, P
7631	CMOS, Triple	5.0	0.001	100,000	1.4	60	–	–	C,I,M	D, P
7632	CMOS, Triple, Uncompensated	5.0	0.001	100,000	1.4	60	–	–	C,I,M	D, P

Operational Amplifiers — CMOS

Type	Description	Compensation	Offset Null	V_{OS} Selection	I_{OS}	I_B	Output Swing	Input CMR	Packages*
7611	Single, Selectable I_Q	Internal	Yes	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, T
7612	Single, Selectable I_Q Extended CMVR	Internal	Yes	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}+300mV$	$V_{SUPP}-100mV$	P, T
7613	Single, Selectable I_Q Input Protected to ± 200V	Internal	Yes	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, T
7614	Single, Fixed I_Q	External	Yes	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, T
7615	Single, Fixed I_Q Input Protected	External	Yes	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, T
7621	Dual, Fixed I_Q	Internal	No	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, T
7622	Dual, Fixed I_Q	Internal	Yes	2, 5, 15mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, J
7631	Triple, Selectable I_Q	Internal	No	5, 10, 20mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, J
7632	Triple, Selectable I_Q	None	No	5, 10, 20mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, J
7641	Quad, Fixed I_Q	Internal	No	5, 10, 20mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, J
7642	Quad, Fixed I_Q	Internal	No	5, 10, 20mV	0.5pA	1pA	$V_{SUPP}-100mV$	$V_{SUPP}-100mV$	P, J
7650	Chopper Stabilized	Internal	–	0.01mV	–	10pA	$V_{SUPP}-100mV$	–	P, T

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

Operational Amplifiers — FET Input (also see Operational Amplifier, CMOS)

Type	Description	V_{OS} (mV)	I_b (μA)	A_{VOL} (V/V)	GBW (typ) (MHz)	Slew Rate (V/μs)	I_{SUPP} (mA)	T_A (°C)	Packages*	Remarks
8007M	General Purpose, Compensated	20	20	50,000	1.0	6	5.2	−55, +125	T	
8007AM	8007M, Low I_b	30	1.0	20,000	1.0	2.5	6	−55, +125	T	
8007C	General Purpose, Compensated	50	50	20,000	1.0	6	6	0, +70	T	All BIFET amplifiers offer low noise— see data sheets
8007AC	8007C, Low I_b	30	1.0	20,000	1.0	2.5	6	0, +70	T	
8043M	Dual 8007M	20	20	50,000	1.0	6.0	6	−55, +125	J	
8043C	Dual 8007C	50	50	20,000	1.0	6.0	6.8	−55, +125	J, P	
8500	MOSFET Input, Compensated	50	0.1	20,000	0.7	0.5	2.7	−25, +85	T	
8500A	MOSFET Input, Super Low I_b	50	0.01	20,000	0.7	0.5	2.7	−25, +85	T	

Operational Amplifiers — High Performance

Type	Description	V_{OS} (mV)	I_b (pA)	A_{VOL} (V/V)	GBW (MHz)	Slew Rate (V/μs)	I_{SUPP} (mA)	T_A (°C)	Packages*
8017M	High Speed, Inverting	5.0	200	25,000	10	130	7.0	−55, +125	T, F
8017C	High Speed, Inverting	7.0	200	25,000	10	130	8.0	0, +70	T, F
OP-05	Low Bias, Low Drift	0.07	700	500,000	0.6	0.2	4.0	−55, +125	T, J
OP-07	Ultra Stable	0.025	300	500,000	0.6	0.17	4.0	−55, +125	T, J

Operational Amplifiers—High Slew Rate

Type	Description	V_{OS} (mV)	I_b (pA)	A_{VOL} (V/V)	GBW (MHz)	Slew Rate (V/μS)	I_{SUPP} (mA)	T_A (°C)	Packages*
8017M	High speed, inverting	5.0	200	25,000	10	130	7.0	-55 + 125	T,F
8017C	High speed, inverting	7.0	200	25,000	10	130	8.0	0 + 70	T,F

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

Precision Operational Amplifiers, $V_{SUPP} = \pm 2V$ to $\pm 8V$

Type	Description	V_{OS} (μV)	ΔV_{OS} ($\mu V/°C$)	ΔV_{OS} (μV/year)	A_V (dB min)	Slew Rate (V/μs)	I_{BIAS} (pA)	Packages*	T_A (°C)
ICL7650C	Chopper Stabilized	±1	±0.01	100nV/$\sqrt{month}$	126	2.5	+1.5	J, P, T	0 to +70
ICL7650I	Chopper Stabilized	±1	±0.01	100nV/$\sqrt{month}$	126	2.5	+1.5	J, P, T	−25 to +85
ICL7652	Chopper Stabilized	±1	±0.7	100nV/$\sqrt{month}$	120	0.5	+1.5	J, P, T	−20 to +85

Precision Instrumentation Amplifiers, $V_{SUPP} = \pm 2V$ to $\pm 5V$, $I_{SUPP} = 1.7mA$

Type	Description	V_{OS} (μV)	ΔV_{OS} ($\mu V/°C$)	ΔV_{OS} (μV/year)	A_V (dB min)	Packages*	T_A (°C)
ICL7605C	Compensated	±2	±0.01	0.5	90	J, P	0 to +70
ICL7605I	Compensated	±2	±0.01	0.5	90	J, P	−25 to +85
ICL7605M	Compensated	±2	±0.05	0.5	90	J, P	−55 to +125
ICL7606C	Uncompensated	±2	±0.01	0.5	90	J, P	0 to +70
ICL7606I	Uncompensated	±2	±0.01	0.5	90	J, P	−25 to +85
ICL7606M	Uncompensated	±2	±0.05	0.5	90	J, P	−55 to +125

Precision Voltage References

Type	Description	
ICL8069	Low Voltage Reference	The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA.
ICL8075-9	Ultra Precision Temperature Stabilized Voltage References	The ICL8075-9 is a family of precision laser-trimmed voltage references that incorporate a substrate heater to produce extremely low overall voltage temperature coefficients. The series of devices is produced so that exact voltages are available for the most popular A/D and D/A converters. This avoids the necessity to perform adjustments in most cases, and reduces the problems with trim range and temperature coefficient loss in all others.

Video Amplifiers

Type	Description	Gains (typ) (V/V)	Bandwidths (typ) (MHz)	e_n μV(rms)	Output Offset (V)	I_{SUPP} (mA)	T_A (°C)	Packages*
NE/SE592	Gain Selectable Video Amp	400, 100, 10	40, 90	12	0.75	10	0, +70/−55, +125	J,T
NE592-8	Gain Selectable Video Amp	400, 100, 10	40	12	0.75	10	0, +70	P

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

Comparators

Type	Description	V_{OS} (mV)	I_b (nA)	A_V (V/mV)	t_{pd} (ns)(typ)	I_{SUPP} (mA)	V_{OL} (V)	I_{OL} (mA)	T_A (°C)	Packages*
8001M	Low Power Comparator	3	100	15	250	2	0.5	2	−55, +125	T
8001C	Low Power Comparator	5	250	15	250	2	0.4	2	0, +70	T

Notes: t_{pd} measured for 100mV step with 5mV overdrive.
I_{SUPP} measured for V_{SUPP} + ± 15V.

Power Amplifiers

Type	Description	Use	Output Current (A)	Output Swing (V)	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	Slew Rate (V/μs)	Quiescent I_{SUPP} (mA)	T_A (°C)
ICH8510M	Hybrid Power Amplifier		1.0	± 26	3.0	250	100,000	0.5	40	−55, +125
ICH8510I	Hybrid Power Amplifier		1.0	± 26	6.0	500	100,000	0.5	50	−25, +85
ICH8515I	Hybrid Power Amplifier		1.25	± 12	6.0	500	100,000	0.5	80	−20°C - +85°C
ICH8515M	Hybrid Power Amplifier	Servo	1.5	± 12	3.0	250	100,000	0.5	70	−55°C - +125°C
ICH8520M	Hybrid Power Amplifier	and	2.0	± 26	3.0	250	100,000	0.5	40	−55, +125
ICH8520I	Hybrid Power Amplifier	Actuator	2.0	± 26	6.0	500	100,000	0.5	50	−25, +85
ICH8530M	Hybrid Power Amplifier		2.7	± 25	3.0	250	100,000	0.5	40	−55, +125
ICH8530I	Hybrid Power Amplifier		2.7	± 25	6.0	500	100,000	0.5	50	−25, +85
ICL8063C	Monolithic Power Amplifier	Power Transistors	2.0	± 27	50		6		250	0, +70
ICL8063M	Monolithic Power Amplifier		2.0	± 27	75		6		300	−55, +125

Note 1: Specifications apply at ± 30V supplies.
Note 2: All units packaged in 8 lead TO-3 can.
Note 3: Fully protected against inductive current flow.
Note 4: Externally settable output current limiting.

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

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Special Function Circuits

Type	Description	Accuracy	V_{SUPP} (V)	T_A (°C)	Packages*
AD590	Temperature transducer — output linear at 1μA/°K	±1°C	40 to 30	−55 to +150	F, H
ICL7667C	Dual Power MOS Driver	—	22	0, +70	J, P, T
ICL7667M	Dual Power MOS Driver	—	22	−55, +125	J, T
8013AM	Four quadrant multiplier. Output proportional to algebraic products	±0.5%	±15	−55, +125	T
8013BM	of two input signals. Features ±0.5% accuracy; internal op amp	±1.0%	±15	−55, +125	T
8013CM	for level shift, division and square root functions; full ±10V	±2.0%	±15	−55, +125	T
8013AC	input/output range; 1MHz bandwidth.	±0.5%	±15	0, +70	T
8013BC		±1.0%	±15	0, +70	T
8013CC		±2.0%	±15	0, +70	T
8038AM	Simultaneous Sine, Square, and Triangle wave outputs T^2L com-	1.5%	±5 to ±15	−55, +125	J
8038AC	patible to 28V over frequency range from 0.01Hz to 1.0MHz.	1.5%	±5 to ±15	0, +70	J
8038BM	Low distortion (<1%); high linearity (0.1%); low frequency drift with temperature (50ppm/°C max); variable duty cycle (2%–98%).	3.0%	±5 to ±15	−55, +125	J
8038BC		3.0%	±5 to ±15	0, +70	P
8038CC	External frequency modulation.	5.0%	±5 to ±15	0, +70	P
8048BC	Log amp 1V/decade (Adjustable). 120dB range.	±30mV	±15	0, +70	J, P
8048CC	with current input. Error referred to output.	±60mV	±15	0, +70	J, P
8049BC	Antilog amplifier adjustable scale factor.	±10mV	±15	0, +70	J, P
8049CC	Error referred to input.	±30mV	±15	0, +70	J, P
8211M	Micropower voltage detector/indicator/voltage regulator/		2 to 30	−55, +125	T
8211C	programmable zener. Contains 1.15V micropower reference		2 to 30	0, +70	P, T
8212M	plus comparator and hysteresis output. Main output		2 to 30	−55, +125	T
8212C	inverting (8212) or non-inverting (8211).		2 to 30	0, +70	P, T

Note: All parameters are specified at $V_{SUPP} = \pm 15V$ and $T_A = +25°C$ unless otherwise noted.

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CMOS Power Supply Circuits

Type	Description	
ICL7660	Voltage Converter	The ICL7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5V to −10.0V.
ICL7663 ICL7664	Positive Regulator Negative Regulator	The ICL7663 (positive) and ICL7664 (negative) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 16V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 40μA, regardless of load.
ICL7665	Programmable Micropower Voltage Detector	The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only ~ 3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction.

OP-05

Low Bias Low Drift Operational Amplifier

FEATURES

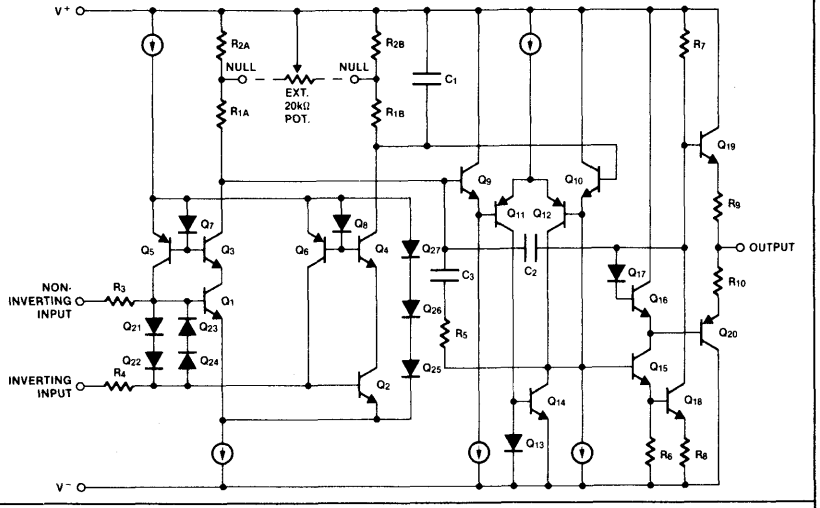
- Low noise (0.6μV, 0.1Hz-10Hz)
- Low drift with time and temperature
- Low V_{OS} (0.15mV max)
- High CMRR, PSRR
- High A_{VOL} (300k min)
- High R_{diff} (>30MΩ)
- High R_{CM}
- Internally compensated
- Industry standard (741) pin configuration

GENERAL DESCRIPTION

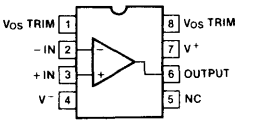
The OP-05 series of monolithic operational amplifiers combines high performance in low signal level applications with the flexibility of a fully protected, internally compensated op amp. OP-05 characteristics include low offset voltage and bias current and high gain, input impedance, CMRR and PSRR.

The OP-05 is a plug-in replacement for 725, 108A and unnulled 741 devices, allowing instant performance improvement without redesign. It is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high gain active filters, buffers, integrators, and sample and hold amplifiers.

SIMPLIFIED SCHEMATIC



PIN CONFIGURATIONS



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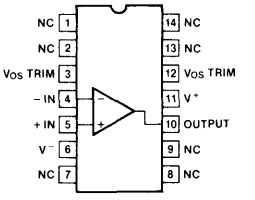

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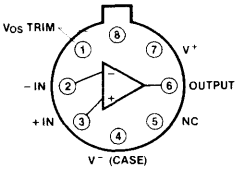

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ORDERING INFORMATION

PART	TEMPERATURE RANGE	PACKAGE	ORDER #
OP-05		dice	OP-05/D
OP-05	−55°C to +125°C	14-pin CERDIP	OP-05Y*
OP-05	−55°C to +125°C	TO-99	OP-05J
OP-05A	−55°C to +125°C	14-pin CERDIP	OP-05AY*
OP-05A	−55°C to +125°C	TO-99	OP-05AJ
OP-05C	0°C to +70°C	8-pin MiniDIP	OP-05CP
OP-05C	0°C to +70°C	14-pin CERDIP	OP-05CY*
OP-05C	0°C to +70°C	TO-99	OP-05CJ
OP-05E	0°C to +70°C	8-pin MiniDIP	OP-05EP
OP-05E	0°C to +70°C	14-pin CERDIP	OP-05EY*
OP-05E	0°C to +70°C	TO-99	OP-05EJ

*Not directly interchangeable with LM108A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-05A, OP-05 ..... −55°C to +125°C
OP-05E, OP-05C ..... 0°C to +70°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: Maximum package power dissipation vs ambient temperature.

Package Type	Maximum Rated Ambient Temperature	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-In-Line (Y)	100°C	10.0mW/°C
MiniDIP (P)	36°C	5.6mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS These specifications apply for $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.07	0.15		0.2	0.5	mV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	(Note 1)		0.2	1.0		0.2	1.0	μV/mo
Input Offset Current	I_{OS}			0.7	2.0		1.0	2.8	nA
Input Bias Current	I_{BIAS}			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)		14	30		14	30	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance- Differential Mode	R_{diff}		30	80		20	60		MΩ
Common-Mode	R_{CM}			200			200		GΩ
Input Common-Mode Voltage Range	CMVR		±13.5	±14.0		±13.5	±14.0		V
Common-Mode Rejection Ratio	CMRR	CMVR = ±13.5V	114	126		114	126		dB
Power Supply Rej. Ratio	PSRR	V_{SUPP} = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3V	300 150	500 500		200 150	500 500		V/mV
Maximum Output Voltage Swing	±V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.17		0.1	0.17		V/μs
Closed Loop Bandwidth	BW	A_V = +1.0 (Note 2)	0.4	0.6		0.4	0.6		MHz
Open Loop Output Res.	R_O	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	Pd			90	120		90	120	mW
		V_{SUPP} = ±3V		4	6		4	6	
Offset Adjustment Range		R_P = 20kΩ		4			4		mV

OPERATING CHARACTERISTICS (Continued)

These specifications apply for $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.2	0.5		0.3	1.3	mV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	(Note 1)		0.3	1.5		0.4	2.0	μV/mo
Input Offset Current	I_{OS}			1.2	3.8		1.8	6.0	nA
Input Bias Current	I_{BIAS}			$\pm$1.2	$\pm$4.0		$\pm$1.8	$\pm$7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.38	0.65	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	nV/$\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)		14	30		15	35	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	pA/$\sqrt{Hz}$
Input Resistance- Differential Mode Common-Mode	 R_{diff} R_{CM}		 15 	 50 160	 	 8 	 33 120	 	 MΩ GΩ
Input Common-Mode Voltage Range	CMVR		$\pm$13.5	$\pm$14.0		$\pm$13.0	$\pm$14.0		V
Common-Mode Rejection Ratio	CMRR	CMVR = $\pm$ 13.5V	110	123		100	120		dB
Power Supply Rejection Ratio	PSRR	V_{SUPP} = $\pm$ 3V to $\pm$ 18V	94	107		90	104		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$	200 150	500 500		120 100	400 400		V/mV
Maximum Output Voltage Swing	$\pm V_O$	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	$\pm$12.5 $\pm$12.0 $\pm$10.5	$\pm$13.0 $\pm$12.8 $\pm$12.0		$\pm$12.0 $\pm$11.5	$\pm$13.0 $\pm$12.8 $\pm$12.0		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.17		0.1	0.17		V/μs
Closed Loop Bandwidth	BW	A_{VCL} = +1.0 (Note 2)	0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$		60			60		Ω
Power Consumption	Pd	 V_{SUPP} = $\pm$ 3V		90 4	120 6		95 4	150 8	mW
Offset Adjustment Range		$R_P = 20k\Omega$		4			4		mV

Note 1: Long term input offset voltage stability refers to the average trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{OS} during the first 30 operating days is typically 25μV. Parameter is not 100% tested; 90% of units meet this specification.

Note 2: Parameter is not 100% tested; 90% of units meet this specification.

OPERATING CHARACTERISTICS (Continued)

These specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.10	0.24		0.3	0.7	mV
Input Offset Voltage Drift Without External Trim With External Trim	$\Delta V_{OS}/\Delta T$	$R_P = 20k\Omega$ (Average Tested)		 0.3 0.2	 0.9 0.5		 0.7 0.3	 2.0 1.0	µV/°C
Input Offset Current	I_{OS}			1.0	4.0		1.8	5.6	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	(Average Tested)		5	25		8	50	pA/°C
Input Bias Current	I_{BIAS}			±1.0	±4.0		±2.0	±6.0	nA
Input Bias Current Drift	$\Delta I_{BIAS}/\Delta T$	(Average Tested)		8	25		13	50	pA/°C
Input Common-Mode Voltage Range	CMVR		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rej. Ratio	CMRR	CMVR = ±13.0	110	123		110	123		dB
Power Supply Rej. Ratio	PSRR	$V_{SUPP} = \pm 3V$ to $\pm 18V$	94	106		94	106		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400		150	400		V
Output Voltage Swing	$\pm V_O$	$R_L \geq 2k\Omega$	±12.0	±12.6		±12.0	±12.6		V

OPERATING CHARACTERISTICS

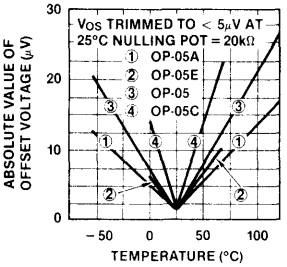
These specifications apply for $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.25	0.6		0.35	1.6	mV
Input Offset Voltage Drift Without External Trim With External Trim	$\Delta V_{OS}/\Delta T$	$R_P = 20k\Omega$ (Average Tested)		 0.7 0.2	 2.0 0.6 (Note 2)		 1.2 0.4	 4.5 1.5 (Note 2)	µV/°C
Input Offset Current	I_{OS}			1.4	5.3		2.0	8.0	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	(Average Tested)		8	35		12	50	pA/°C
Input Bias Current	I_{BIAS}			±1.5	±5.5		±2.2	±9.0	nA
Input Bias Current Drift	$\Delta I_{BIAS}/\Delta T$	(Average Tested)		13	35		18	50	pA/°C
Input Common-Mode Voltage Range	CMVR		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rej. Ratio	CMRR	CMVR = ±13.0	107	123		97	120		dB
Power Supply Rej. Ratio	PSRR	$V_{SUPP} = \pm 3V$ to $\pm 18V$	90	104		86	100		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450		100	400		V/mV
Output Voltage Swing	$\pm V_O$	$R_L \geq 2k\Omega$	±12.0	±12.6		±11.0	±12.6		V

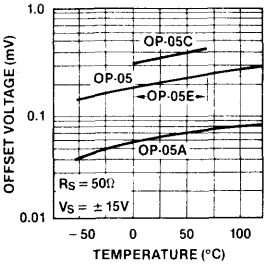
Note 2: Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

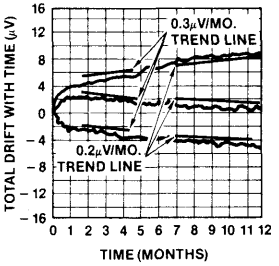
Trimmed Offset Voltage vs Temperature



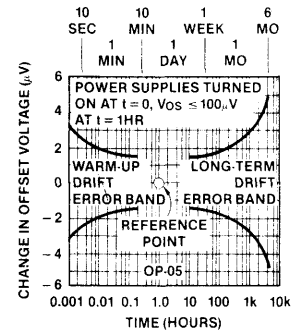
Untrimmed Offset Voltage vs Temperature



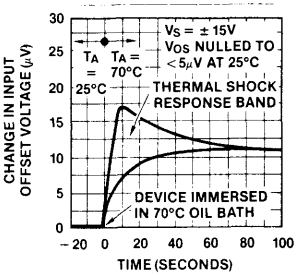
Typical Offset Voltage Stability vs Time



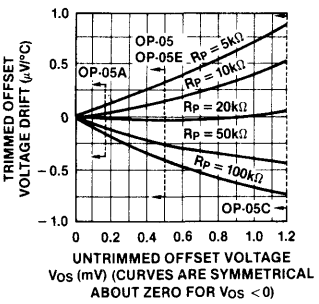
Offset Voltage Drift with Time



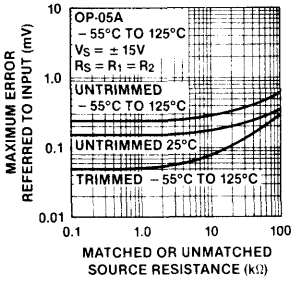
Offset Voltage Change Due to Thermal Shock



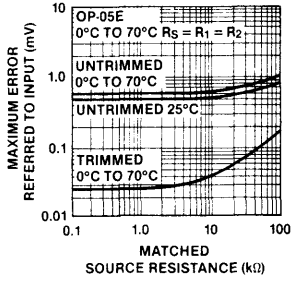
Trimmed Offset Voltage Drift as a Function of Trimming Potentiometer (R_P) Size and V_{OS}



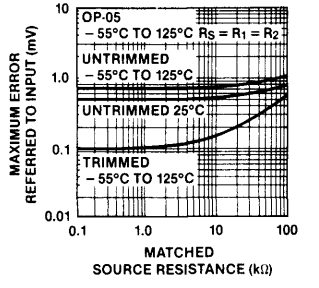
Maximum Error vs Source Resistance



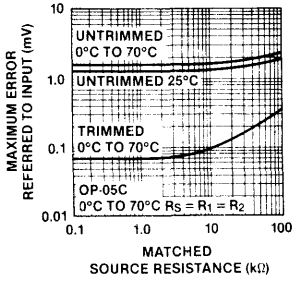
Maximum Error vs Source Resistance



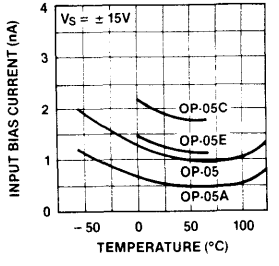
Maximum Error vs Source Resistance



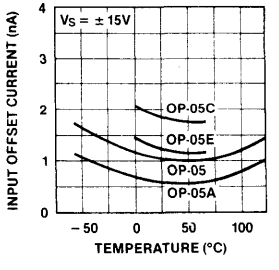
Maximum Error vs Source Resistance



Input Bias Current vs Temperature

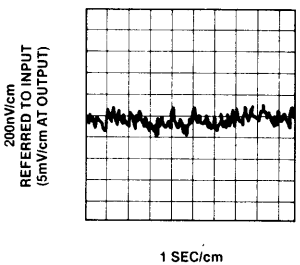


Input Offset Current vs Temperature

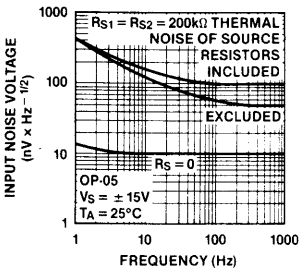


TYPICAL PERFORMANCE CURVES (Continued)

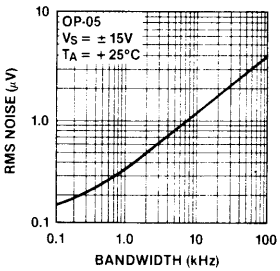
OP-05 Low Frequency Noise



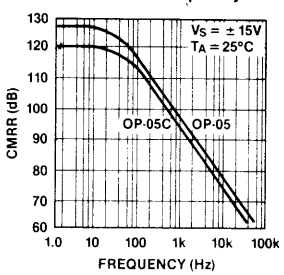
Input Spot Noise Voltage vs Frequency



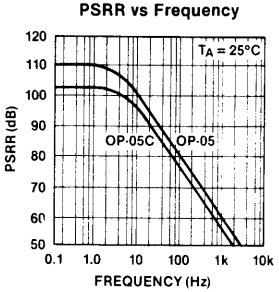
Input Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)



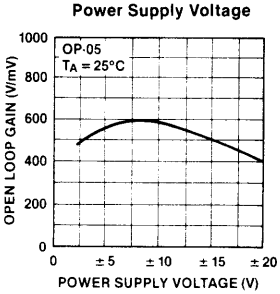
CMRR vs Frequency



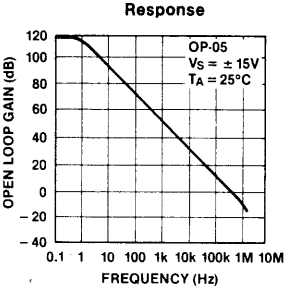
PSRR vs Frequency



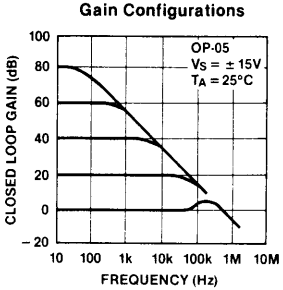
Open Loop Gain vs Power Supply Voltage



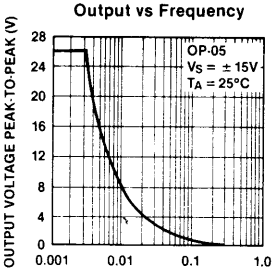
Open Loop Frequency Response



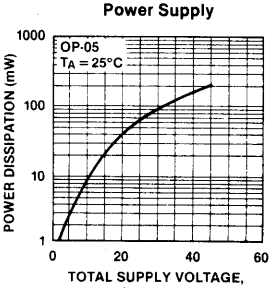
Closed Loop Response for Various Gain Configurations



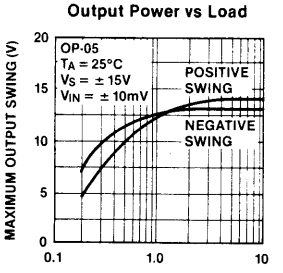
Maximum Undistorted Output vs Frequency



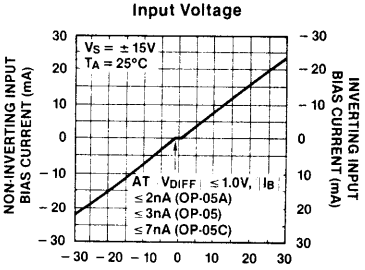
Power Consumption vs Power Supply



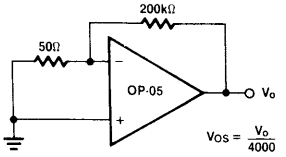
Output Power vs Load



Input Bias Current vs Differential Input Voltage



TEST CIRCUITS



Offset Voltage Test Circuit

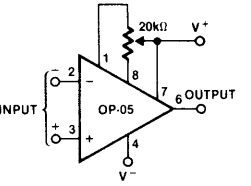
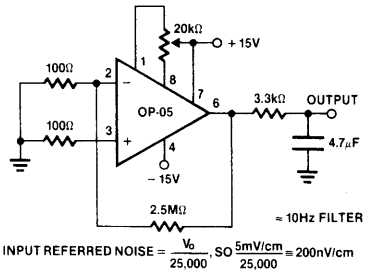


Figure 1. Offset Nulling Circuit



Low Frequency Noise Test Circuit

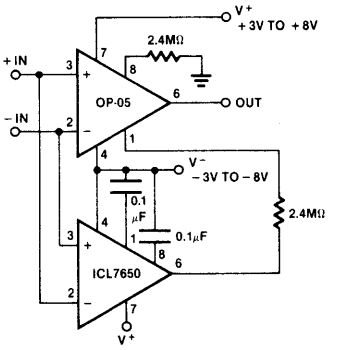


Figure 2. Auto-Nulling Circuit for OP-05

APPLICATIONS

OP-05 Series devices may be fitted directly to 725 and 108/108A* Series sockets with or without removal of external compensation components. Additionally, OP-05 may be fitted to unnulled 741 Series sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation (see Figure 1). The OP-05 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Figure 2 shows how it is possible to combine the low noise and output drive capability of the OP-05 with the low offset and drift of the ICL7650 chopper stabilized op-amp to yield a circuit which has a V_{OS} of less than 5μV (typically 1μV), temperature drift of $<0.01\mu V/°C$, long term drift of less than 1μV per year and input noise voltage of $10nV/\sqrt{Hz}$, while at the same time driving loads of up to 2kΩ.

Figure 3 shows an OP-05 used as a low-noise preamplifier for a 16-bit dual slope A/D converter. The preamp is autozeroed by using a simple sample-and-difference system keyed by the STATUS output of the A/D chip pair(see A030 for details).

*"J" package only

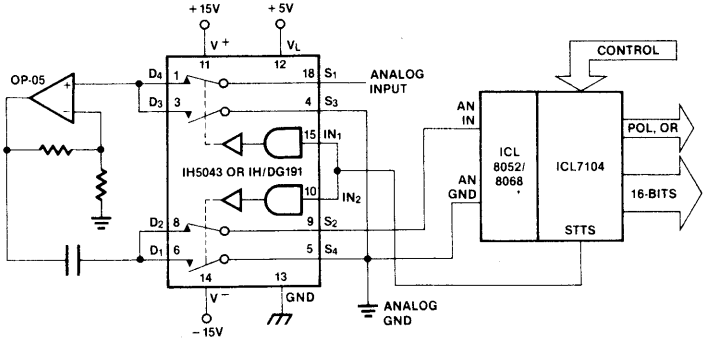
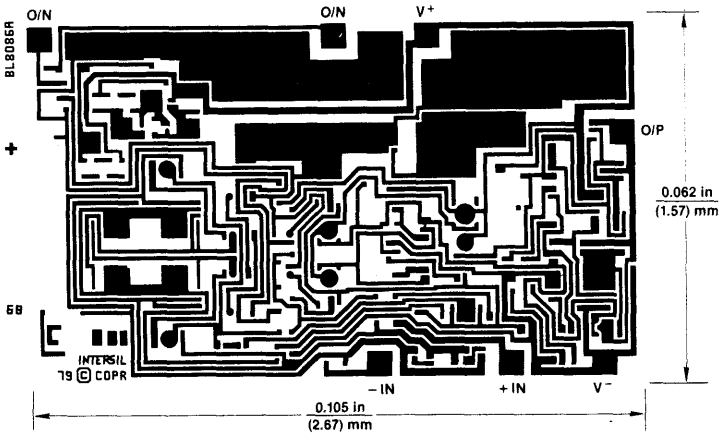


Figure 3. Auto-Zeroed Low Noise Preamp for 16-Bit A/D

CHIP TOPOGRAPHY



OP-07

Ultra-Low Offset Voltage Op Amp

FEATURES

- Ultra-low V_{OS} (10μV typ.)
- Ultra-low V_{OS} drift (0.2μV/°C)
- Ultra-stable vs time (0.2μV/month)
- Ultra-low noise (0.35μV_{p-p})
- No external components required
- Large input voltage range (±14.0V)
- Wide supply voltage range (±3V to ±18V)
- Fits 725, 108A/308A, 741, AD510 sockets

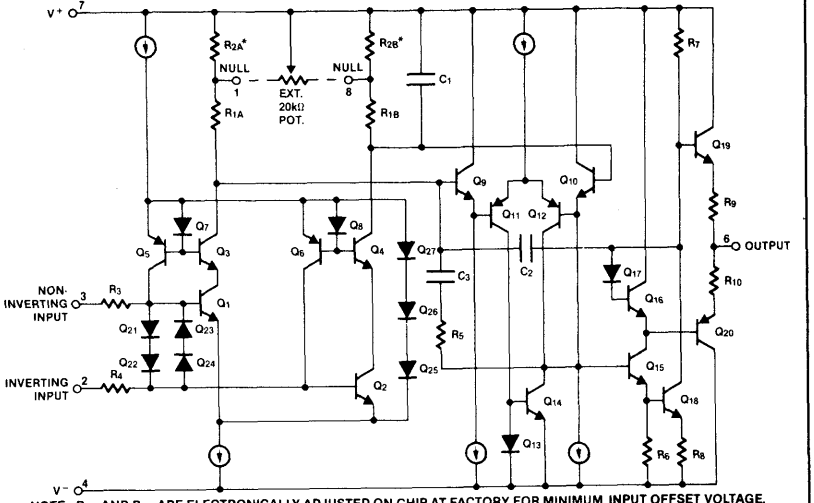
GENERAL DESCRIPTION

The OP-07 series of monolithic operational amplifiers provides high performance through the use of a low noise, chopper-less bipolar input transistor amplifier circuit. The elimination of external components for offset nulling, frequency compensation and device protection permits optimization of system design, while excellent device interchangeability provides reduced system assembly time and eliminates or reduces field recalibrations.

The outstanding common-mode rejection provides maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

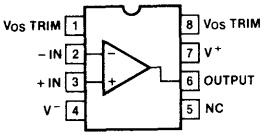
5

SIMPLIFIED SCHEMATIC Pin numbers for 8-pin packages only

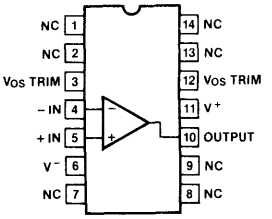


NOTE: R_{2A} AND R_{2B} ARE ELECTRONICALLY ADJUSTED ON-CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

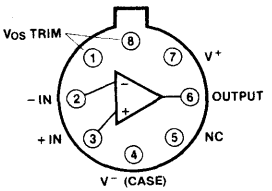
PIN CONFIGURATIONS



(outline dwgs JA, PA)



(outline dwg JD)



(outline dwg TY)

ORDERING INFORMATION

PART	PACKAGE			
	TO-99	8-PIN CERDIP	8-PIN MiniDIP	14-PIN* CERDIP
TEMPERATURE RANGE: −55°C to +125°C				
OP-07	OP-07J	OP-07Z	—	OP-07Y
OP-07A	OP-07AJ	OP-07AZ	—	OP-07AY
TEMPERATURE RANGE: 0°C to +70°C				
OP-07C	OP-07CJ	OP-07CZ	OP-07CP	OP-07CY
OP-07D	OP-07DJ	—	OP-07DP	—
OP-07E	OP-07EJ	OP-07EZ	OP-07EP	OP-07EY

For dice order # OP-07/D

*Not directly interchangeable with LM108A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-07A, OP-07 ..... −55°C to +125°C
OP-07E, OP-07C, OP-07D ..... 0°C to +70°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: Maximum package power dissipation vs ambient temperature.

Package Type	Max. Amb. Temp. for Full Rating	Derate Above Max. Ambient Temp.
TO-99 (J)	80°C	7.1mW/°C
Dual-In-Line (Y)	100°C	10.0mW/°C
MiniDIP (P)	36°C	5.6mW/°C
8-Pin CERDIP (Z)	75°C	6.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

These specifications apply for V_{SUPP} = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		10	25		30	75	μV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	(Note 2)		0.2	1.0		0.2	1.0	μV/mo
Input Offset Current	I_{OS}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_{BIAS}			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)		0.35	0.6		0.35	0.6	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)		14	30		14	30	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance Differential Mode Common-Mode	 R_{diff} R_{CM}		 30	 80 200		 20	 60 200		 MΩ GΩ
Input Common-Mode Voltage Range	CMVR		±13.0	±14.0		±13.0	±14.0		V
Common-Mode Rejection Ratio	CMRR	CMVR = ±13.0V	110	126		110	126		dB
Power Supply Rej. Ratio	PSRR	V_{SUPP} = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V, V_{SUPP} = ±3V	300 150	500 500		200 150	500 500		V/mV
Maximum Output Voltage Swing	$\pm V_O$	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.17		0.1	0.17		V/μs
Closed Loop Bandwidth	BW	A_V = +1.0 (Note 3)	0.4	0.6		0.4	0.6		MHz
Open Loop Output Res.	R_O	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	Pd	 V_{SUPP} = ±3V		75 4	120 6		75 4	120 6	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4		mV

OPERATING CHARACTERISTICS (Continued)

These specifications apply for $V_{SUPP} = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		30	75		60	150		60	150	μV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	(Note 2)		0.3	1.5		0.4	2.0		0.5	3.0	μV/mo
Input Offset Current	I_{OS}			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current	I_{BIAS}			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)		0.35	0.6		0.38	0.65		0.38	0.65	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5		10.5 10.2 9.8	20.0 13.5 11.5	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)		14	30		15	35		15	35	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
Input Resistance Differential Mode	R_{diff}		15	50		8	33		7	31		MΩ
Input Resistance Common-Mode	R_{CM}			160			120			120		GΩ
Input Common-Mode Voltage Range	CMVR		±13.0	±14.0		±13.0	±14.0		±13.0	±14.0		V
Common-Mode Rejection Ratio	CMRR	CMVR = ±13.0V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	PSRR	V_{SUPP} = ±3V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V, V_{SUPP} = ±3V	200 150	500 500		120 100	400 400		120 —	400 —		V/mV
Maximum Output Voltage Swing	$\pm V_O$	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5 —	±13.0 ±12.8 ±12.0		±12.0 ±11.5 —	±13.0 ±12.8 —		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.17		0.1	0.17		0.1	0.17		V/μs
Closed Loop Bandwidth	BW	A_{VOL} = +1.0 (Note 3)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$		60			60			60		Ω
Power Consumption	Pd			75	120		80	150		80	150	mW
		V_{SUPP} = ±3V		4	6		4	8		4	8	
Offset Adjustment Range		R_P = 20kΩ		±4			±4			±4		mV

Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured 5 minutes after power supply application at −55°C, +25°C and +125°C.

Note 2: Long term input offset voltage stability refers to the average trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{OS} during the first 30 operating days is typically 25μV. Parameter is not 100% tested; 90% of units meet this specification.

Note 3: Parameter is not 100% tested; at least 90% of units meet this specification.

OPERATING CHARACTERISTICS (Continued)

These specifications apply for $V_{SUPP} = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		25	60		60	200	μV
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	(Average Tested)							μV/°C
Without External Trim				0.2	0.6		0.3	1.3	
With External Trim		$R_P = 20k\Omega$ (Note 3)		0.2	0.6		0.3	1.3	
Input Offset Current	I_{OS}			0.8	4.0		1.2	5.6	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	(Average Tested)		5	25		8	50	pA/°C
Input Bias Current	I_{BIAS}			±1.0	±4.0		±2.0	±6.0	nA
Input Bias Current Drift	$\Delta I_{BIAS}/\Delta T$	(Average Tested)		8	25		13	50	pA/°C
Input Common-Mode Voltage Range	CMVR		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rej. Ratio	CMRR	CMVR = ±13.0	106	123		106	123		dB
Power Supply Rej. Ratio	PSRR	$V_{SUPP} = \pm 3V$ to $\pm 18V$	94	106		94	106		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400		150	400		V/mV
Output Voltage Swing	$\pm V_O$	$R_L \geq 2k\Omega$	±12.0	±12.6		±12.0	±12.6		V

OPERATING CHARACTERISTICS

These specifications apply for $V_{SUPP} = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		45	130		85	250		85	250	μV
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	(Average Tested)						(Note 3)			(Note 3)	μV/°C
Without External Trim				0.3	1.3		0.5	1.8		0.7	2.5	
With External Trim		$R_P = 20k\Omega$		0.3	1.3		0.4	1.6		0.7	2.5	
								(Note 3)			(Note 3)	
Input Offset Current	I_{OS}			0.9	5.3		1.6	8.0		1.6	8.0	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	(Average Tested) (Note 3)		8	35		12	50		12	50	pA/°C
Input Bias Current	I_{BIAS}			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Input Bias Current Drift	$\Delta I_{BIAS}/\Delta T$	(Average Tested) (Note 3)		13	35		18	50		18	50	pA/°C
Input Common-Mode Voltage Range	CMVR		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rej. Ratio	CMRR	CMVR = ±13.0	103	123		97	120		94	106		dB
Power Supply Rej. Ratio	PSRR	$V_{SUPP} = \pm 3V$ to $\pm 18V$	90	104		86	100		86	100		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450		100	400		100	400		V/mV
Output Voltage Swing	$\pm V_O$	$R_L \geq 2k\Omega$	±12.0	±12.6		±11.0	±12.6		±11.0	±12.6		V

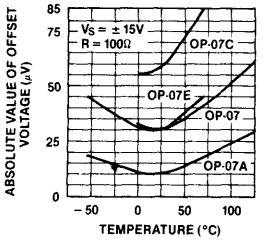
Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured 5 minutes after power supply application at −55°C, +25°C and +125°C.

Note 2: Long term input offset voltage stability refers to the average trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{OS} during the first 30 operating days is typically 25μV. Parameter is not 100% tested; 90% of units meet this specification.

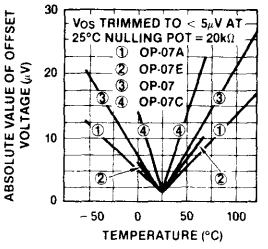
Note 3: Parameter is not 100% tested; at least 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

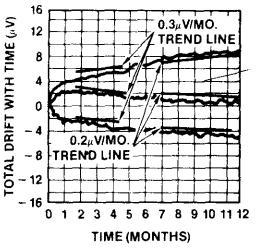
Untrimmed Offset Voltage vs Temperature



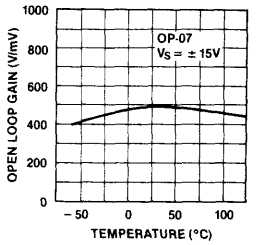
Trimmed Offset Voltage vs Temperature



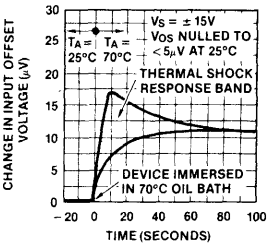
Typical Offset Voltage Stability vs Time



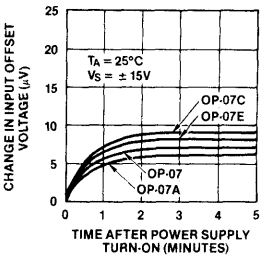
Open Loop Gain vs Temperature



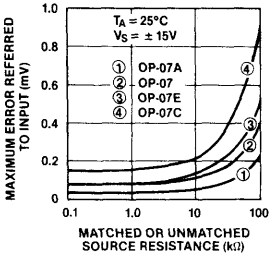
Offset Voltage Change Due to Thermal Shock



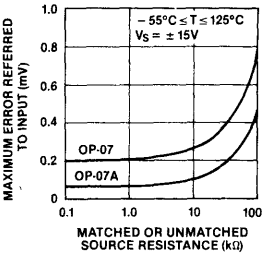
Warm-Up Drift



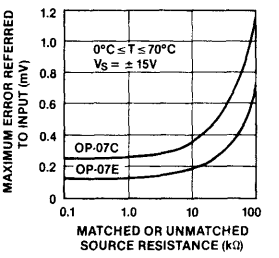
Maximum Error vs Source Resistance



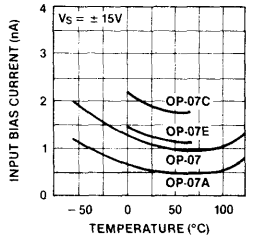
Maximum Error vs Source Resistance



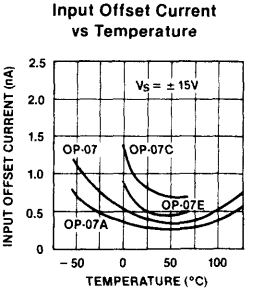
Maximum Error vs Source Resistance



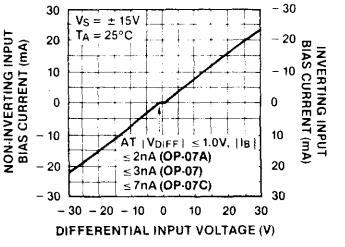
Input Bias Current vs Temperature



Input Offset Current vs Temperature

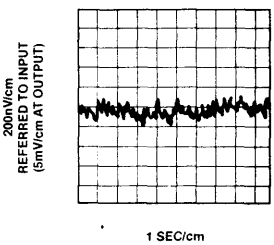


Input Bias Current vs Differential Input Voltage

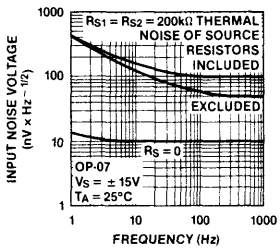


TYPICAL PERFORMANCE CURVES (Continued)

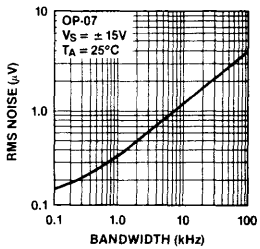
OP-07 Low Frequency Noise



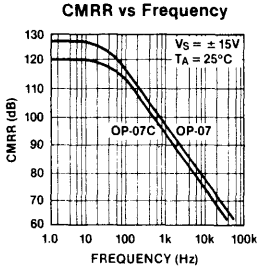
Total Input Noise Voltage vs Frequency



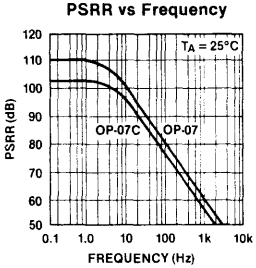
Input Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)



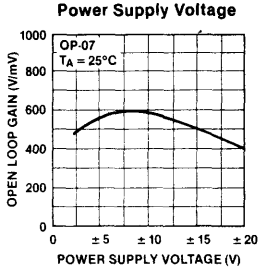
CMRR vs Frequency



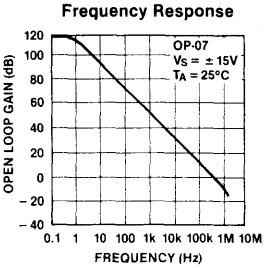
PSRR vs Frequency



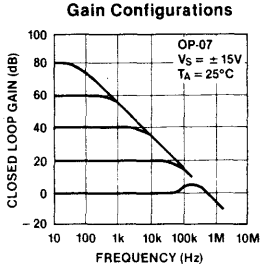
Open Loop Gain vs Power Supply Voltage



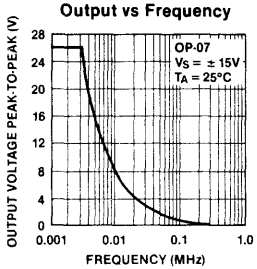
Open Loop Frequency Response



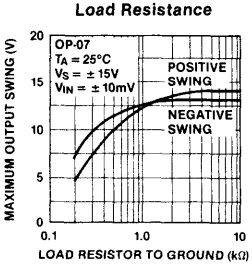
Closed Loop Response for Various Gain Configurations



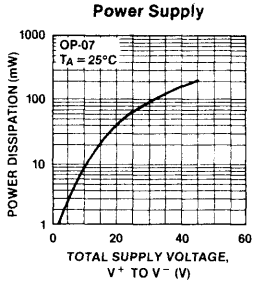
Maximum Undistorted Output vs Frequency



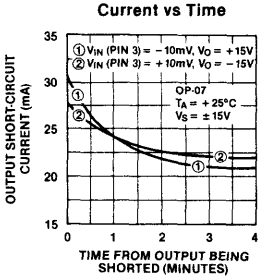
Output Voltage vs Load Resistance



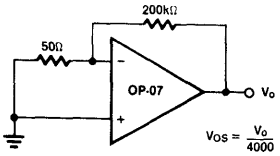
Power Consumption vs Power Supply



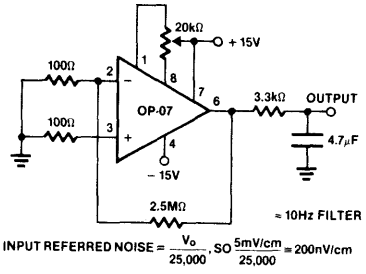
Output Short-Circuit Current vs Time



TEST CIRCUITS



Offset Voltage Test Circuit



Low Frequency Noise Test Circuit

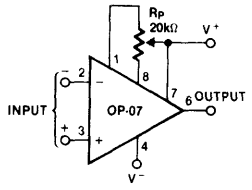


Figure 1. Offset Nulling Circuit

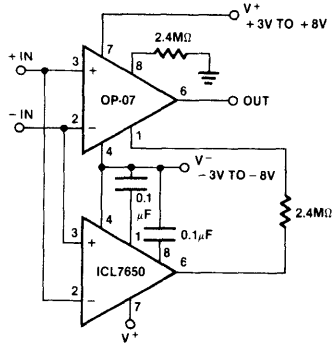


Figure 2. Auto-Nulling Circuit for OP-07

APPLICATIONS

OP-07 series devices may be inserted directly in 725 and 108/108A* series sockets with or without removal of external compensation components. Additionally, the OP-07 may be fitted to unnulled 741 series sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation (see Figure 1). The OP-07 provides stable operation with load capacitances up to 500pF and ± 10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

*except "Y" package

Figure 2 shows how it is possible to combine the low noise and output drive capability of the OP-07 with the low offset and drift of the ICL7650 chopper stabilized op-amp to yield a circuit which has a V_{OS} of less than 5μV (typically 1μV), temperature drift of $<0.01\mu V/°C$, long term drift of less than 1μV per year and input noise voltage of $10nV/\sqrt{Hz}$, while at the same time driving loads of up to 2kΩ.

The exceptional input characteristics of the OP-07 are used to advantage in Figure 3 with the ICL7134B 14-bit monolithic DAC. Both the reference inversion amplifier, A_3, and the output amplifier, A_1, require offset voltages and input currents of around 25μV and 2nA respectively, to maintain the required accuracy.

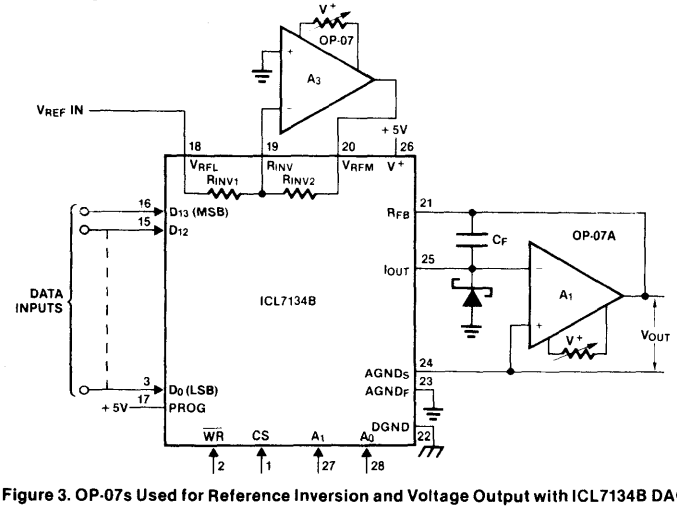
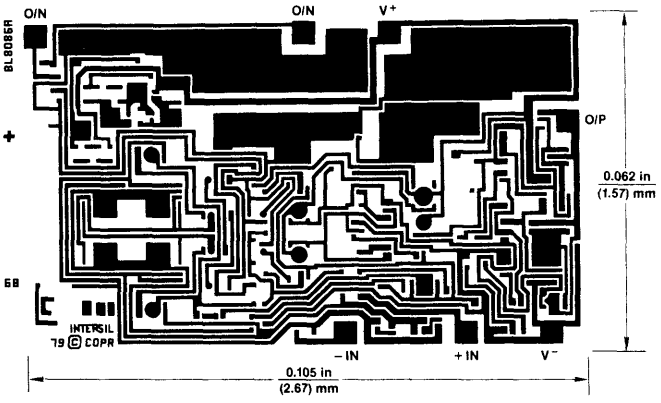


Figure 3. OP-07s Used for Reference Inversion and Voltage Output with ICL7134B DAC

CHIP TOPOGRAPHY



LM108/A, LM308/A
Low Level Operational Amplifiers

FEATURES

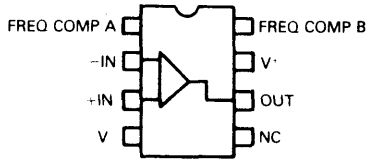
- Input Bias Current – 2 nA max to 7 nA max
- Input Offset Current – 0.2 nA max to 1 nA max
- Input Offset Voltage – 0.5 mV max to 7.5 mV max
- $\Delta Vos/\Delta T$ – 5 $\mu V/°C$ to 30 $\mu V/°C$
- $\Delta Ios/\Delta T$ – 2.5 pA/°C to 10 pA/°C
- Pin for Pin Replacement for 101A/301A

GENERAL DESCRIPTION

These differential input, precision amplifiers provide low input currents and offset voltages competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of >2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor. The LM108A and LM308A are high performance selections from the 108/308 amplifier family.

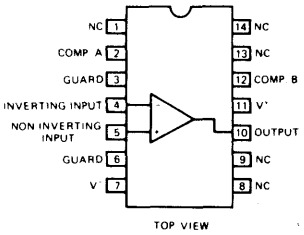
5

PIN CONFIGURATIONS



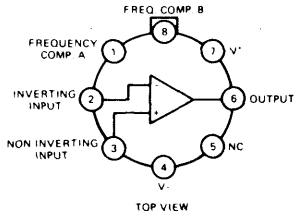
(outline dwg PA)

DUAL-IN-LINE PACKAGE



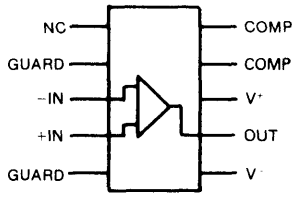
TOP VIEW

(outline dwg JD)



TOP VIEW

(outline dwg TY)



(outline dwg FB-1)

ORDERING INFORMATION

Part number	TO-99 Can	8 pin MiniDIP	14 pin CERDIP	10 pin Flatpak	Dice
LM108A LM308A	LM108AH* LM308AH	– LM308AN	LM108AJ LM308AJ	LM108AF LM308AF	LM108A/D LM308A/D
LM108 LM308	LM108H* LM308H	– LM308N	LM108J LM308J	LM108F LM308F	LM108/D LM308/D

*If 883B processing is desired add /883B to order number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
108, 108A	±20V
308, 308A	±18V
Internal Power Dissipation (Note 1)	
Metal Can (TO-99	500 mW
DIP	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
108, 108A	−55°C to +125°C
308, 308A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

PARAMETER	CONDITIONS	308			308A			108			108A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20V								0.3	0.6		0.3	0.6	mA
	V_S = ±15V		0.3	0.8		0.3	0.8							mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10\ k\Omega$	25	300		80	300		50	300		80	300		V/mV
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10\ k\Omega$	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	T_A = +125°C, V_S = ±20V								0.15	0.4		0.15	0.4	mA

NOTE 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.

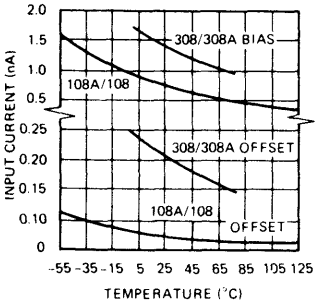
NOTE 2: The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

NOTE 3: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

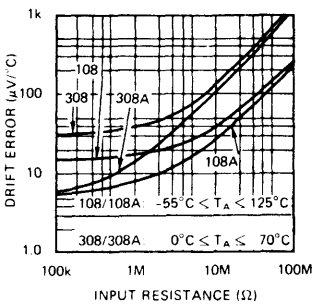
NOTE 4: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V for the 108, and 108A and −5V to −15V for the 308 and 308A.

TYPICAL PERFORMANCE CURVES

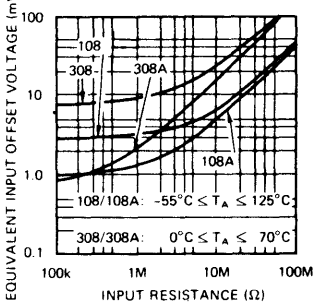
INPUT CURRENTS



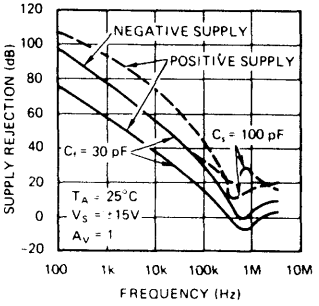
MAXIMUM DRIFT ERROR



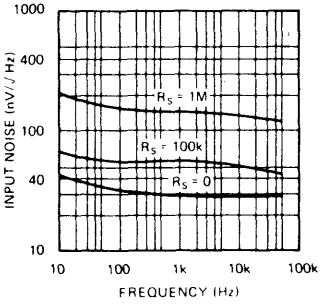
MAXIMUM OFFSET ERROR



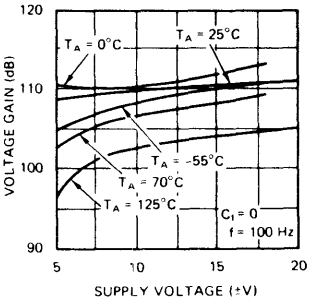
POWER SUPPLY REJECTION



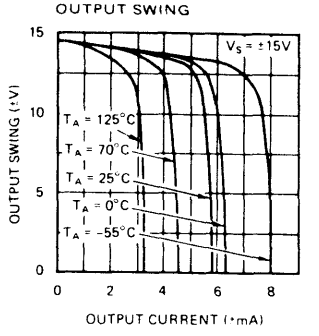
INPUT NOISE VOLTAGE



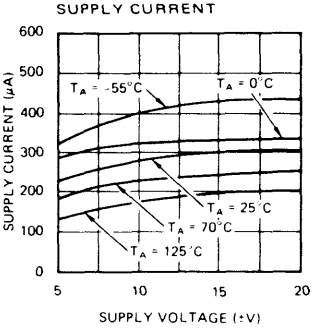
VOLTAGE GAIN



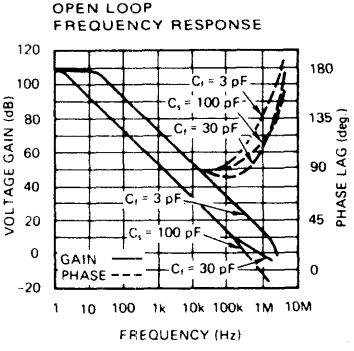
OUTPUT SWING



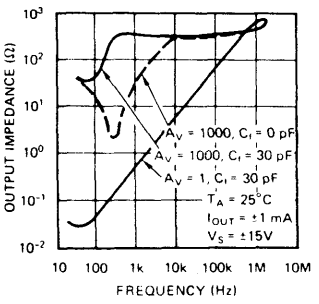
SUPPLY CURRENT



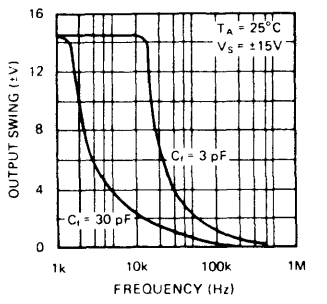
OPEN LOOP
FREQUENCY RESPONSE



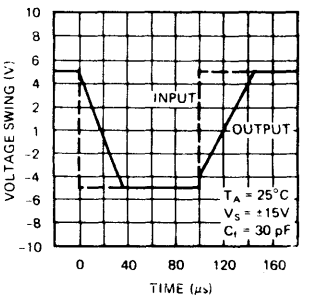
CLOSED LOOP
OUTPUT IMPEDENCE



LARGE SIGNAL
FREQUENCY RESPONSE



VOLTAGE FOLLOWER
PULSE RESPONSE



GUARDING

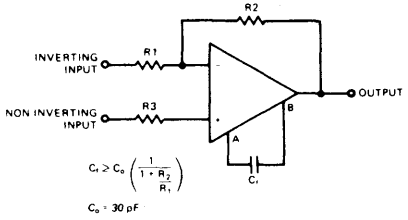
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

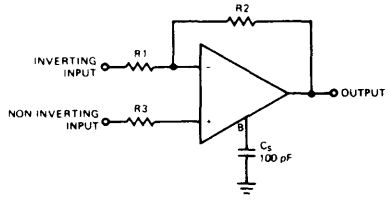
The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration).

FREQUENCY COMPENSATION CIRCUITS

STANDARD CIRCUIT



ALTERNATE CIRCUIT: IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.



AD590

Temperature Transducer

FEATURES

- **Linear current output: 1 μA/°K**
- **Wide range: −55°C to +150°C**
- **Two-terminal device: Voltage in/current out**
- **Laser trimmed to ±0.5°C calibration accuracy (AD590M)**
- **Excellent linearity: ±0.5°C over full range (AD590M)**
- **Wide power supply range: +4V to +30V**
- **Sensor isolation from case**
- **Low cost**

GENERAL DESCRIPTION

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

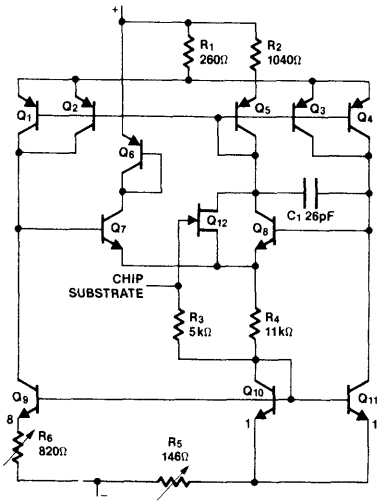
The AD590 should be used in any temperature-sensing application between −55°C and +150°C (0°C and 70°C for TO-92) in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance-measuring circuitry and cold-junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

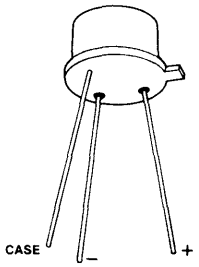
The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

5

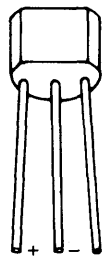
SCHEMATIC DIAGRAM

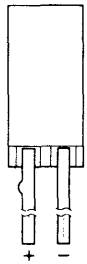


PIN CONFIGURATIONS



(outline dwg TO-52)





(outline dwg DH)

SUBSTRATE
(LEAVE FLOATING)

(outline dwg TO-92)

ORDERING INFORMATION

TO-52 and Ceramic Package:
Operate −55°C to +150°C
TO-92:
Operate 0°C to +70°C

NON-LINEARITY (°C)	TO-52 PACKAGE	CERAMIC PACKAGE	TO-92 PACKAGE
±3.0	AD590IH	AD590IF	AD590IZR
±1.5	AD590JH	AD590JF	AD590JZR
±0.8	AD590KH	AD590KF	AD590KZR
±0.4	AD590LH	AD590LF	—
±0.3	AD590MH	AD590MF	—

INTERSIL

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Forward Voltage (V^+ to V^-) ..... +44V
Reverse Voltage (V^+ to V^-) ..... −20V
Breakdown Voltage (Case to V^+ or V^-) ..... ±200V
Storage Temperature Range ..... −65°C to +175°C

Rated Performance Temperature Range
TO-92 ..... 0°C to +70°C
TO-52, Ceramic ..... −55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (Typical values at T_A = +25°C, V^+ = 5V unless otherwise noted)

CHARACTERISTICS	AD590I	AD590J	AD590K	AD590L	AD590M	UNITS
Output Nominal Output Current @ +25°C (298.2°K)	298.2	298.2	298.2	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μA/°K
Calibration Error @ +25°C (Notes)	±10.0 max	±5.0 max	±2.5 max	±1.0 max	±0.5 max	°C
Absolute Error (−55°C to +150°C) Without External Calibration Adjustment	±20.0 max	±10.0 max	±5.5 max	±3.0 max	±1.7 max	°C
With External Calibration Adjustment	±5.8 max	±3.0 max	±2.0 max	±1.6 max	±1.0 max	°C
Non-Linearity	±3.0 max	±1.5 max	±0.8 max	±0.4 max	±0.3 max	°C
Repeatability (Note 2)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C
Long Term Drift (Note 3)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C/month
Current Noise	40	40	40	40	40	$pA/\sqrt{Hz}$
Power Supply Rejection $+4 < V^+ < +5V$	0.5	0.5	0.5	0.5	0.5	μA/V
$+5 < V^+ < +15V$	0.2	0.2	0.2	0.2	0.2	μA/V
$+15V < V^+ < +30V$	0.1	0.1	0.1	0.1	0.1	μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	10^{10}	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	20	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	V

Notes
1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between −55°C and +150°C (0°C and 70°C for TO-92).
3. Conditions: Constant +5V, constant +125°C.
4. Leakage current doubles every +10°C.
5. Mechanical strain on package (especially TO-92) may disturb calibration of device.

5

TRIMMING OUT ERRORS

The ideal graph current vs temperature for the AD590 is a straight line, but as Figure 1 shows, the actual shape is slightly different. Since the sensor is limited to the range of −55°C to +150°C (0°C to 70°C for TO-92), it is possible to optimize the accuracy by trimming. Trimming also permits extracting maximum performance from the lower-cost sensors.

The circuit of Figure 2 trims the slope of the AD590 output. The effect of this is shown in Figure 3.

The circuit of Figure 4 trims both the slope and the offset. This is shown in Figure 5. The diagrams are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over the whole range, or over any selected part of the range. In fact, it is possible to adjust the I-grade device to give less than 0.1°C error over the range 0°C to 90°C and less than 0.05°C error from 25°C to 60°C.

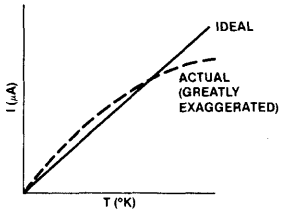


Figure 1. Trimming Out Errors

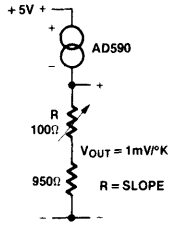


Figure 2. Slope Trimming

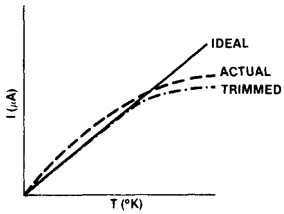


Figure 3. Effect of Slope Trim

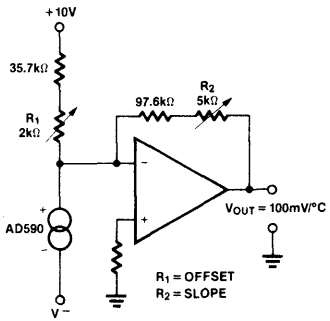
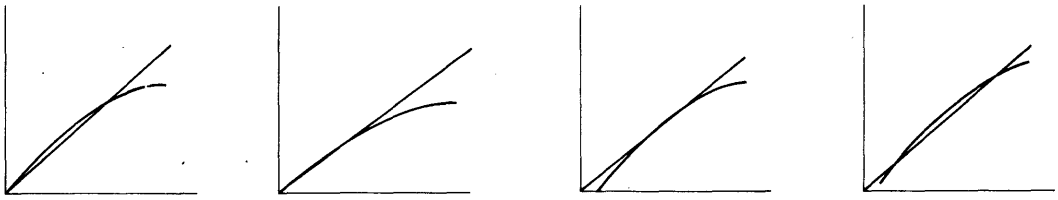


Figure 4. Slope and Offset Trimming



a) Untrimmed b) Trim One: Offset c) Trim Two: Slope d) Trim Three: Offset Again

Figure 5. Effect of Slope and Offset Trimming

ACCURACY

Maximum errors over limited temperature spans, with $V_S = +5V$, are listed by device grade in the following tables. The tables reflect the worst-case linearities, which invariably occur at the extremities of the specified temperature range. The trimming conditions for the data in the tables are shown in Figures 2 and 3.

All errors listed in the tables are ± °C. For example, if ±1°C maximum error is required over the +25°C to +75°C range (i.e., lowest temperature of +25°C and span of 50°C), then the trimming of a J-grade device, using the single-trim circuit (Figure 2), will result in output having the required accuracy over the stated range. An M-grade device with no trims will have less than ±0.9°C error, and an I-grade device with two trims (Figure 3) will have less than ±0.2° error. If the requirement is for less than ±1.4°C maximum error, from −25°C to +75°C (100° span from −25°C), it can be satisfied by an M-grade device with no trims, a K-grade device with one trim, or an I-grade device with two trims.

I GRADE—MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	8.4	9.2	10.0	10.8	11.6	12.4	13.2	14.4
None	25	10.0	10.4	11.0	11.8	12.0	13.8	15.0	16.0
None	50	13.0	13.0	12.8	13.8	14.6	16.4	18.0	
None	100	15.2	16.0	16.6	17.4	18.8			
None	150	18.4	19.0	19.2					
None	205	20.0							
One	10	0.6	0.4	0.4	0.4	0.4	0.4	0.4	0.6
One	25	1.8	1.2	1.0	1.0	1.0	1.2	1.6	1.8
One	50	3.8	3.0	2.0	2.0	2.0	3.0	3.8	
One	100	4.8	4.5	4.2	4.2	5.0			
One	150	5.5	4.8	5.5					
One	205	5.8							
Two	10	0.3	0.2	0.1	<	<	0.1	0.2	0.3
Two	25	0.5	0.3	0.2	<	0.1	0.2	0.3	0.5
Two	50	1.2	0.6	0.4	0.2	0.2	0.3	0.7	
Two	100	1.8	1.4	1.0	2.0	2.5			
Two	150	2.6	2.0	2.8					
Two	205	3.0							

<: Less than 0.05°C.

J GRADE—MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	4.2	4.6	5.0	5.4	5.8	6.2	6.6	7.2
None	25	5.0	5.2	5.5	5.9	6.0	6.9	7.5	8.0
None	50	6.5	6.5	6.4	6.9	7.3	8.2	9.0	
None	100	7.7	8.0	8.3	8.7	9.4			
None	150	9.2	9.5	9.6					
None	205	10.0							
One	10	0.3	0.2	0.2	0.2	0.2	0.2	0.2	0.3
One	25	0.9	0.6	0.5	0.5	0.5	0.6	0.8	0.9
One	50	1.9	1.5	1.0	1.0	1.0	1.5	1.9	
One	100	2.3	2.2	2.0	2.0	2.3			
One	150	2.5	2.4	2.5					
One	205	3.0							
Two	10	0.1	<	<	<	<	<	<	0.1
Two	25	0.2	0.1	<	<	<	<	0.1	0.2
Two	50	0.4	0.2	0.1	<	<	0.1	0.2	<
Two	100	0.7	0.5	0.3	0.7	1.0			
Two	150	1.0	0.7	1.2					
Two	205	1.6							

<: Less than ±0.05°C.

K GRADE—MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	2.1	2.3	2.5	2.7	2.9	3.1	3.3	3.6
None	25	2.6	2.7	2.8	3.0	3.2	3.5	3.8	4.2
None	50	3.8	3.5	3.4	3.6	3.8	4.3	5.1	
None	100	4.2	4.3	4.4	4.6	5.1			
None	150	4.8	4.8	5.3					
None	205	5.5							
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.6	0.4	0.3	0.3	0.3	0.4	0.5	0.6
One	50	1.2	1.0	0.7	0.7	0.7	1.0	1.2	
One	100	1.5	1.4	1.3	1.3	1.5			
One	150	1.7	1.5	1.7					
One	205	2.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.2	0.1	*	*	*	*	0.1	0.2
Two	50	0.3	0.1	*	*	*	0.1	0.2	
Two	100	0.5	0.3	0.2	0.3	0.7			
Two	150	0.6	0.5	0.7					
Two	205	0.8							

* Less than ±0.05°C

5

L GRADE—MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	1.0	1.0	1.1	1.1	1.2	1.3	1.4	1.6
None	25	1.3	1.3	1.3	1.4	1.5	1.6	1.7	1.9
None	50	1.9	1.8	1.7	1.8	1.9	2.1	2.4	
None	100	2.4	2.4	2.4	2.4	2.7			
None	150	2.7	2.6	2.8					
None	205	3.0							
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.5	0.4	0.3	0.3	0.3	0.3	0.4	0.5
One	50	1.0	0.8	0.6	0.6	0.6	0.8	1.0	
One	100	1.3	1.2	1.1	1.1	1.3			
One	150	1.4	1.3	1.4					
One	205	1.6							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.1	*	*	*	*	*	*	0.1
Two	50	0.2	*	*	*	*	*	0.2	
Two	100	0.3	0.2	0.1	0.2	0.3			
Two	150	0.3	0.2	0.3					
Two	205	0.4							

* Less than ±0.05°C

M GRADE—MAXIMUM ERRORS, °C

NUMBER OF TRIMS	TEMPERATURE SPAN—°C	LOWEST TEMPERATURE IN SPAN—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	0.6	0.5	0.6	0.6	0.7	0.7	0.7	0.9
None	25	0.8	0.8	0.7	0.7	0.8	0.8	1.0	1.1
None	50	1.0	0.9	0.8	0.9	0.9	1.1	1.2	
None	100	1.3	1.4	1.3	1.4	1.5			
None	150	1.5	1.6	1.6					
None	205	1.7							
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.4	0.3	0.2	0.2	0.2	0.2	0.3	0.4
One	50	0.5	0.4	0.3	0.3	0.3	0.4	0.5	
One	100	0.8	0.8	0.7	0.7	0.8			
One	150	0.9	0.9	0.9					
One	205	1.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.1	*	*	*	*	*	*	0.1
Two	50	0.2	*	*	*	*	*	0.2	
Two	100	0.2	0.1	*	0.1	0.2			
Two	150	0.3	0.2	0.3					
Two	205	0.3							

* Less than ±0.05°C

5

NOTES

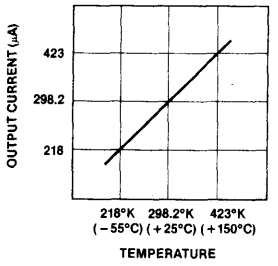
1. Maximum errors over all ranges are guaranteed based on the known behavior characteristic of the AD590.
2. For one-trim accuracy specifications, the 205°C span is assumed to be trimmed at +25°C; for all other spans, it is assumed that the device is trimmed at the midpoint.
3. For the 205°C span, it is assumed that the two-trim temperatures are in the vicinity of 0°C and +140°C; for all other spans, the specified trims are at the endpoints.
4. In precision applications, the actual errors encountered are usually dependent upon sources of error which are often overlooked in error budgets. These typically include:
   a. Trim error in the calibration technique used
   b. Repeatability error
   c. Long-term drift errors

Trim error is usually the largest error souce. This error arises from such causes as poor thermal coupling between the device to be calibrated and the reference sensor; reference sensor errors; lack of adequate time for the device being calibrated to settle to the final temperature; radically different thermal resistances between the case and the surroundings ($R_{\theta CA}$) when trimming and when applying the device.

Repeatability errors arise from a strain hysteresis of the package. The magnitude of this error is solely a function of the magnitude of the temperature span over which the device is used. For example, thermal shocks between 0°C and 100°C involve extremely low hysteresis and result in repeatability errors of less than ±0.05°C. When the thermal-shock excursion is widened to −55°C to +150°C, the device will typically exhibit a repeatability error of ±0.05°C (±0.10 guaranteed maximum).

Long-term drift errors are related to the average operating temperature and the magnitude of the thermal shocks experienced by the device. Extended use of the AD590 at temperatures above 100°C typically results in long-term drift of ±0.03°C per month; the guaranteed maximum is ±0.10°C per month. Continuous operation at temperatures below 100°C induces no measurable drifts in the device. Besides the effects of operating temperature, the severity of thermal shocks incurred will also affect absolute stability. For thermal-shock excursions less than 100°C, the drift is difficult to measure (<0.03°C). However, for 200°C excursions, the device may drift by as much as ±0.10°C after twenty such shocks. If severe, quick shocks are necessary in the application of the device, realistic simulated life tests are recommended for a thorough evaluation of the error introduced by such shocks.

TYPICAL APPLICATIONS



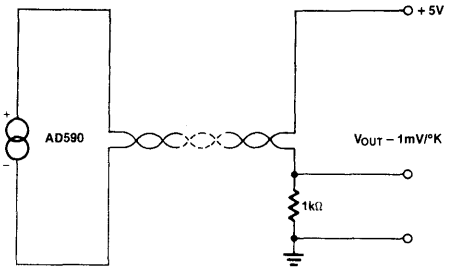


Figure 6. Simple connection. Output is proportional to absolute temperature.

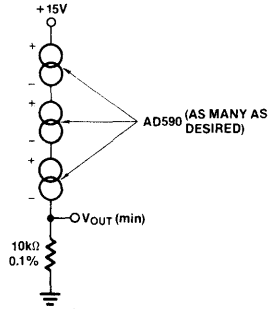


Figure 7. Lowest-temperature sensing scheme. Available current is that of the "coldest" sensor.

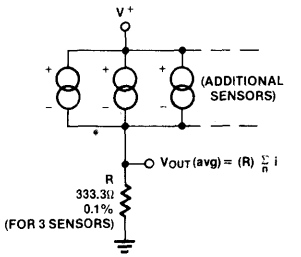


Figure 8. Average-temperature sensing scheme. The sum of the AD590 currents appears across R, which is chosen by the formula

$$R = \frac{10k\Omega}{n},$$

n being the number of sensors.

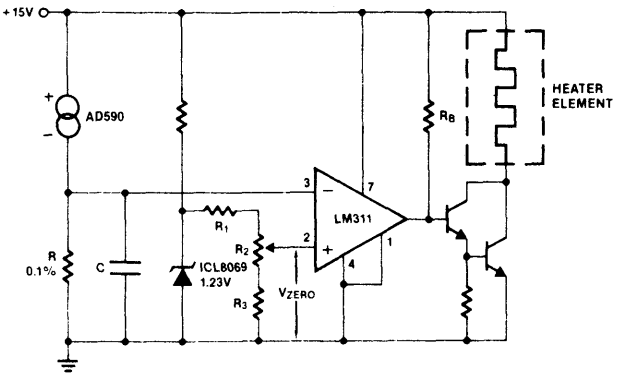


Figure 9. Single-setpoint temperature controller. The AD590 produces a temperature-dependent voltage across R (C is for filtering noise). Setting R_2 produces a scale-zero voltage. For the Celsius scale, make R = 1kΩ and V_{ZERO} = 0.273 volts. For Fahrenheit, R = 1.8kΩ and V_{ZERO} = 0.460 volts.

TYPICAL APPLICATIONS (Cont'd)

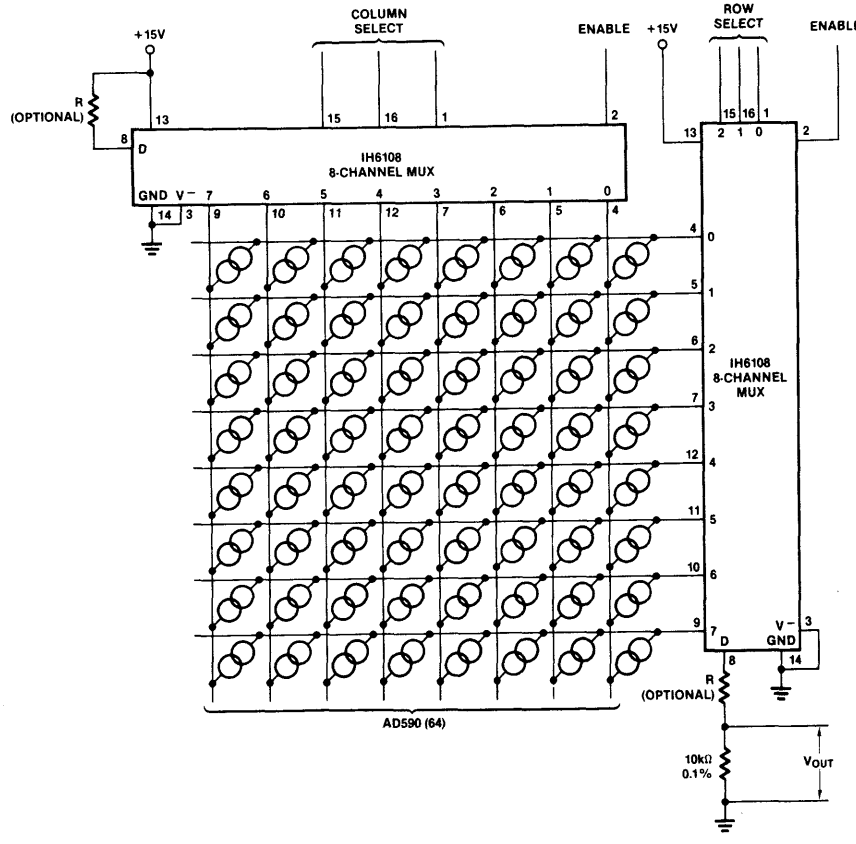


Figure 10. Multiplexing sensors. If shorted sensors are possible, a series resistor in series with the D line will limit the current (shown as R, above: only one is needed). A six-bit digital word will select one of 64 sensors.

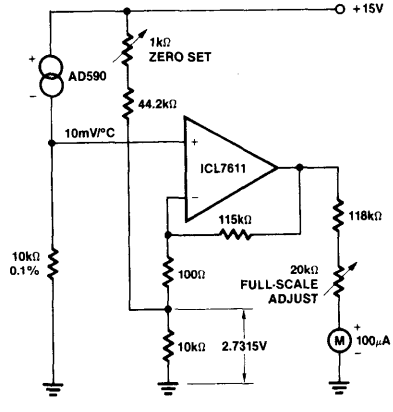


Figure 11. Centigrade thermometer (0°C–100°C). The ultra-low bias current of the ICL7611 allows the use of large-value gain-resistors, keeping meter-current error under 1/2%, and therefore saving the expense of an extra meter-driving amplifier.

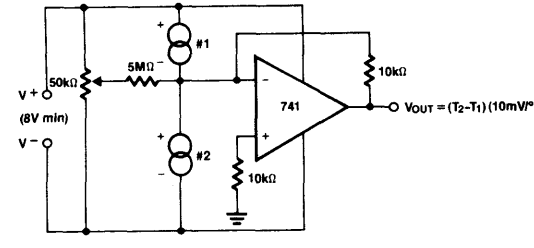


Figure 12. Differential thermometer. The 50kΩ pot trims offsets in the devices whether internal or external, so it can be used to set the size of the difference interval. This also makes it useful for liquid-level detection (where there will be a measurable temperature difference).

TYPICAL APPLICATIONS (Cont'd)

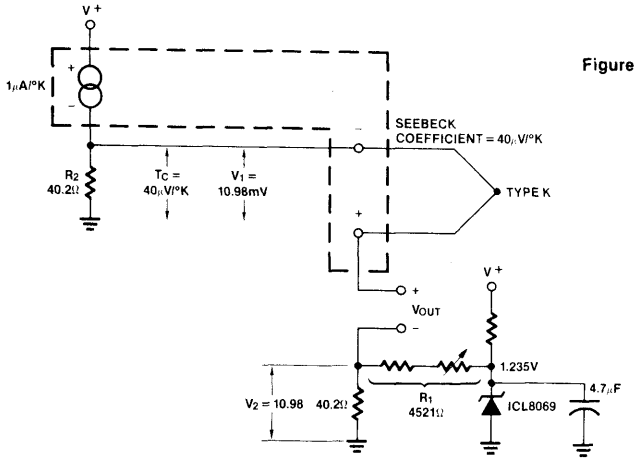


Figure 13. Cold-junction compensation for type K thermocouple. The reference junction(s) should be in close thermal contact with the AD590 case. V^+ must be at least 4V, while ICL8069 current should be set at 1 mA–2 mA. Calibration does not require shorting or removal of the thermocouple: set R_1 for $V_2 = 10.98$mV. If very precise measurements are needed, adjust R_2 to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V_1, and set R_1 to buck out this voltage (i.e., set $V_2 = V_1$). For other thermocouple types, adjust values to the appropriate Seebeck coefficient.

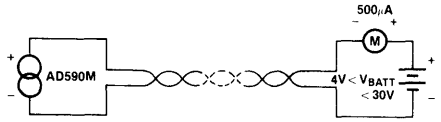
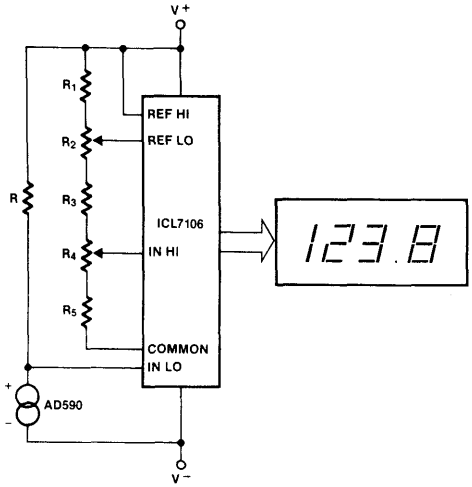


Figure 14. Simplest thermometer. Meter displays current output directly in degrees Kelvin. Using the AD590M, sensor output is within ± 1.7 degrees over the entire range, and less than ± 1 degree over the greater part of it.



	R	R_1	R_2	R_3	R_4	R_5
°F	9.00	4.02	2.0	12.4	10.0	0
°C	5.00	4.02	2.0	5.11	5.0	11.8

$$\sum_{1}^{5} R_n = 28k\Omega \text{ (nominal)}$$

All values in kΩ

The ICL7106 has a V_{IN} span of ± 2.0V, and a V_{CM} range of ($V^+ - 0.5$) Volts to ($V^- + 1$) Volts; R is scaled to bring each range within V_{CM} while not exceeding V_{IN}. V_{REF} for both scales is 500mV. Maximum reading on the Celsius range is 199.9°C, limited by the (short-term) maximum allowable sensor temperature. Maximum reading on the Fahrenheit range is 199.9°F (93.3°C), limited by the number of display digits. See also note below.

Figure 15. Basic digital thermometer, Celsius and Fahrenheit scales

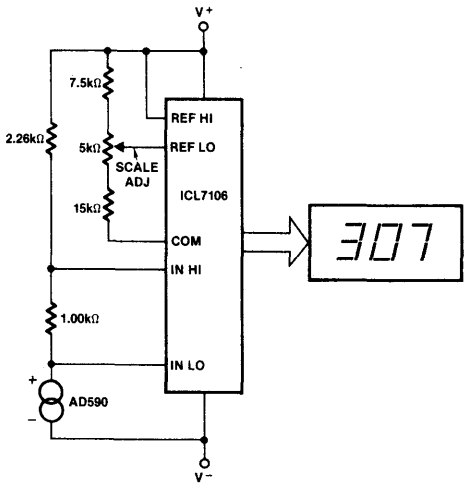


Figure 16. Basic digital thermometer, Kelvin scale. The Kelvin scale version reads from 0 to 1999°K theoretically, and from 223°K to 473°K actually. The 2.26kΩ resistor brings the input within the ICL7106 V_{CM} range: 2 general-purpose silicon diodes or an LED may be substituted.

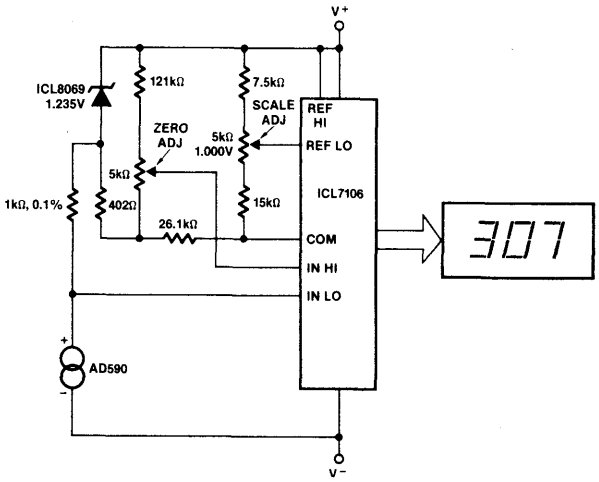


Figure 17. Basic digital thermometer, Kelvin scale with zero adjust. This circuit allows "zero adjustment" as well as slope adjustment. The ICL8069 brings the input within the common-mode range, while the 5kΩ pots trim any offset at 218°K (−55°C), and set scale factor.

Note on Figure 15, Figure 16 and Figure 17: Since all 3 scales have narrow V_{IN} spans, some optimization of ICL7106 components can be made to lower noise and preserve CMR. The table below shows the suggested values. Similar scaling can be used with the ICL7126/36.

Scale	V_{IN} Range (V)	R_{INT}(kΩ)	C_{AZ}(μF)
K	0.223 to 0.473	220	0.47
C	−0.25 to +1.0	220	0.1
F	−0.29 to +0.996	220	0.1

For all:

$C_{REF} = 0.1\mu F$ $C_{OSC} = 100pF$

$C_{INT} = 0.22\mu F$ $R_{OSC} = 100k\Omega$

NE/SE592
Video Amplifier

FEATURES

- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

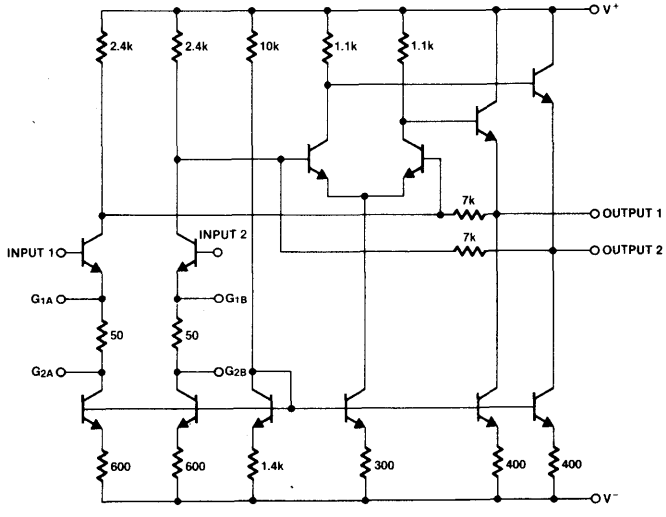
DESCRIPTION

The NE/SE592 is a monolithic, two stage, differential output, wideband video amplifier which offers fixed gains of 100 and 400 without external components and adjustable gains from 0 to 400 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The NE/SE592 is a pin-for-pin replacement for the μA733 in most applications.

ORDERING INFORMATION

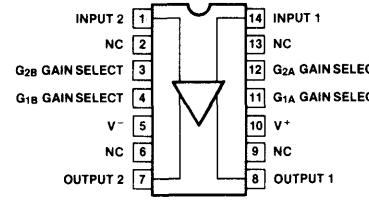
PART TYPE	TEMP RANGE	PACKAGE		
		14-Pin Plastic	14-Pin CERDIP	10-Pin TO-100
SE592	−55°C to +125°C	—	SE592F	SE592H
NE592	0°C to +70°C	NE592N	NE592F	NE592H

EQUIVALENT CIRCUIT (resistor values nominal only)



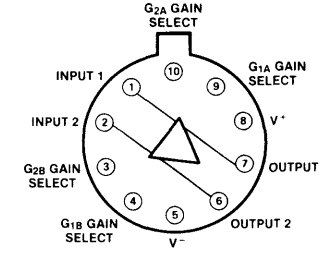
PIN CONFIGURATIONS

14-Pin DIP Package (JD, PD Package)



TOP VIEW

10-Pin TO-100 Package (H Package)



TOP VIEW

Note: Pin 5 connected to case

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise specified)

Supply Voltage ..... ±8V
Differential Input Voltage ..... ±5V
Common-Mode Input Voltage ..... ±6V
Output Current 10mA

Operating Temperature Range
SE592 ..... −55°C to +125°C
NE592 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

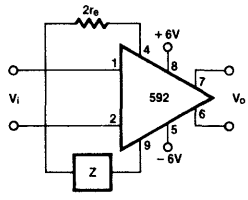
T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V

PARAMETER	SYMBOL	TEST CONDITIONS	NE592			SE592			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain Gain 1 (Note 1) Gain 2 (Note 2)	A_{VOL}	R_L = 2kΩ, V_{OUT} = 3Vp-p	 250 80	 400 100	 600 120	 300 90	 400 100	 500 110	V/V
Bandwidth Gain 1 (Note 1) Gain 2 (Note 2)	BW			 40 90			 40 90		MHz
Rise Time Gain 1 (Note 1) Gain 2 (Note 2)	t_r	V_{OUT} = 1Vp-p		 10.5 4.5	 12		 10.5 4.5	 10	ns
Propagation Delay Gain 1 (Note 1) Gain 2 (Note 2)	t_d	V_{OUT} = 1Vp-p		 7.5 6.0	 10		 7.5 6.0	 10	ns
Input Resistance Gain 1 (Note 1) Gain 2 (Note 2)	R_{IN}		 10	 4.0 30		 20	 4.0 30		kΩ
Input Capacitance (Note 2)	C_{IN}	Gain 2		2.0			2.0		pF
Input Offset Current	I_{OS}			0.4	5.0		0.4	3.0	μA
Input Bias Current	I_{BIAS}			9.0	30		9.0	20	μA
Input Noise Voltage	$\overline{e_n}$	BW = 1kHz to 10MHz		12			12		μVrms
Input Voltage Range	ΔV_{IN}				±1.0			±1.0	V
Common-Mode Rejection Ratio Gain 2 (Note 2) Gain 2 (Note 2)	CMRR	 V_{CM} ± 1V, F < 100kHz V_{CM} ± 1V, F = 5MHz	 60	 86 60		 60	 86 60		dB
Supply Voltage Rejection Ratio Gain 2 (Note 2)	PSRR	 ΔV_S = ±0.5V	 50	 70		 50	 70		dB
Output Offset Voltage Gain 2 (Note 2)	V_{OOS}	 R_L = ∞		 0.35	 0.75		 0.35	 0.75	V
Output Common-Mode Voltage	V_{OCM}	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing Differential	±V_o	R_L = 2kΩ	3.0	4.0		3.0	4.0		V
Output Resistance	R_o			20			20		Ω
Power Supply Current	I^+	R_L = ∞		18	24		18	24	mA

Note 1: Gain select pins G_{1A} and G_{1B} connected together.
Note 2: Gain select pins G_{2A} and G_{2B} connected together.

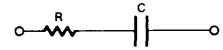
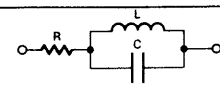
TYPICAL APPLICATIONS

Basic Configuration (see note)



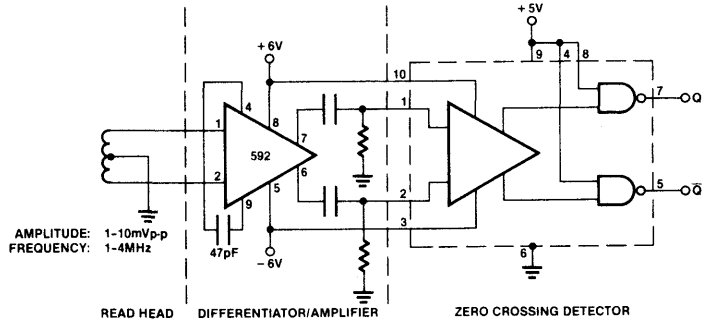
$$\frac{V_o(s)}{V_i(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Filter Networks

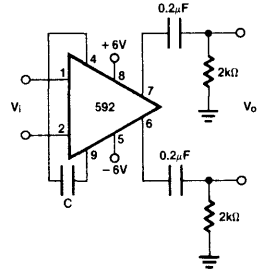
Z NETWORK	FILTER TYPE	$\frac{V_o(s)}{V_i(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

Note: In the networks above, the R value used is assumed to include the internal $2r_e$ of approximately 32Ω.

Disc/Tape Phase Modulated Readback Systems



Differentiation with High Common-Mode Noise Rejection



For frequency $F_1 << 1/2\,\pi\,(32)C$

$$V_o \cong 1.4 \times 10^4 C \frac{dV_i}{dT}$$

NE592-8
Video Amplifier

FEATURES

- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

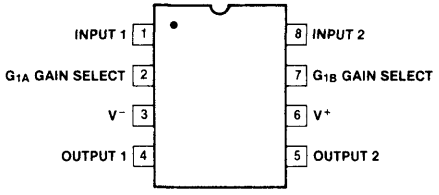
DESCRIPTION

The NE592-8 is a monolithic, two stage, differential output, wideband video amplifier which offers a fixed gain of 400 without external components and adjustable gains from 0 to 400 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The NE592-8 is a pin-for-pin replacement for the μA733 in most applications.

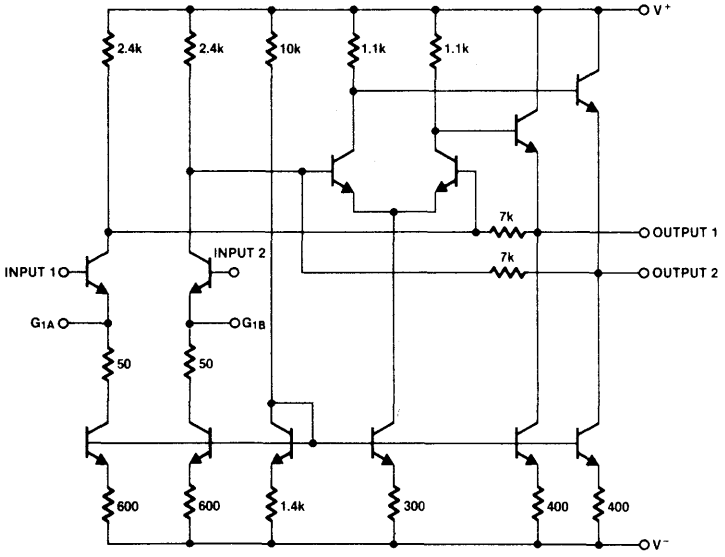
ORDERING INFORMATION

PART TYPE	TEMP RANGE	PACKAGE
NE592	0°C to +70°C	NE592N-8

PIN CONFIGURATION (outline dwg PA)



EQUIVALENT CIRCUIT (resistor values nominal only)



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise specified)

Supply Voltage	±8V	Operating Temperature Range	0°C to +70°C
Differential Input Voltage	±5V	Storage Temperature Range	−65°C to +150°C
Common-Mode Input Voltage	±6V	Power Dissipation	500mW
Output Current	10mA		

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

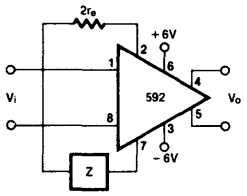
T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V

PARAMETER	SYMBOL	TEST CONDITIONS	NE592-8			UNIT
			MIN	TYP	MAX	
Differential Voltage Gain Gain 1 (Note 1)	A_{VOL}	R_L = 2kΩ, V_{OUT} = 3Vp-p	250	400	600	V/V
Bandwidth Gain 1 (Note 1)	BW			40		MHz
Rise Time Gain 1 (Note 1)	t_r	V_{OUT} = 1Vp-p		10.5		ns
Propagation Delay Gain 1 (Note 1)	t_d	V_{OUT} = 1Vp-p		7.5		ns
Input Resistance Gain 1 (Note 1)	R_{IN}			4.0		kΩ
Input Capacitance	C_{IN}			2.0		pF
Input Offset Current	I_{OS}			0.4	5.0	μA
Input Bias Current	I_{BIAS}			9.0	30	μA
Input Noise Voltage	$\overline{e}_n$	BW = 1kHz to 10MHz		12		μVrms
Input Voltage Range	ΔV_{IN}				±1.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} ±1V, F < 100kHz V_{CM} ±1V, F = 5MHz	60	86 60		dB
Supply Voltage Rejection Ratio	PSRR	ΔV_S = ±0.5V	50	70		dB
Output Offset Voltage	V_{OOS}	R_L = ∞		0.35	0.75	V
Output Common-Mode Voltage	V_{OCM}	R_L = ∞	2.4	2.9	3.4	V
Output Voltage Swing Differential	$\pm V_o$	R_L = 2kΩ	3.0	4.0		V
Output Resistance	R_o			20		Ω
Power Supply Current	I^+	R_L = ∞		18	24	mA

Note 1: Gain select pins G_{1A} and G_{1B} connected together.

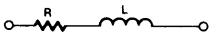
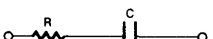
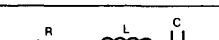
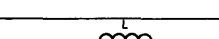
TYPICAL APPLICATIONS

Basic Configuration (see note)



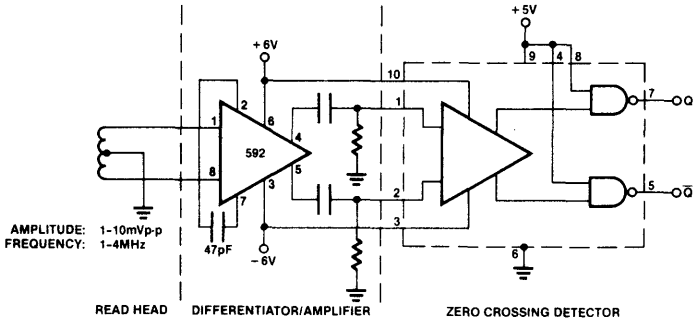
$$\frac{V_o(s)}{V_i(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Filter Networks

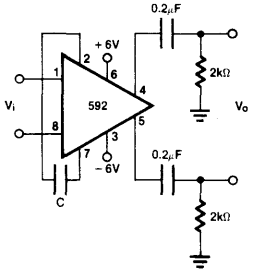
Z NETWORK	FILTER TYPE	$\frac{V_o(s)}{V_i(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

Note: In the networks above, the R value used is assumed to include the internal $2r_e$ of approximately 32Ω.

Disc/Tape Phase Modulated Readback Systems



Differentiation with High Common-Mode Noise Rejection



For frequency $F_1 << 1/2\,\pi\,(32)C$

$V_o \cong 1.4 \times 10^4 C \frac{dV_i}{dT}$

ICL741HS
High Speed 741 Operational Amplifier

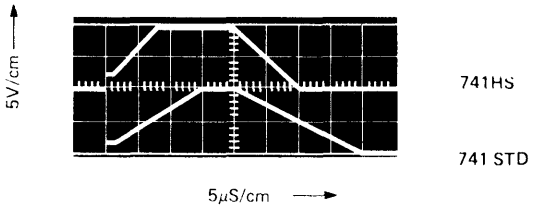
FEATURES

- Pin For Pin and Electrically Equivalent to μA741
- Guaranteed Slew Rate – 0.7V/μs Min.
- Low Cost
- Short Circuit Protection
- Large Common-Mode Input Range
- Guaranteed Drift Characteristics
- No Latch Up
- Internal Frequency Compensation

GENERAL DESCRIPTION

The 741HS high slew rate version of the 741 general purpose operational amplifier is intended for applications where slew rate performance greater than 0.3V/μsec is required. Typical applications are oscillators, active filters, sample and hold and other large signal applications. This device has a guaranteed minimum slew rate of 0.7V/μsec and is identical and equivalent to the standard 741 operational amplifier. It will fill the application void between the 741 and 101A type amplifiers (slew rate = 0.3V/μsec) and the more costly high-speed amplifiers (slew rate = 30V/μsec).

HIGH-SPEED 741 OPERATIONAL AMPLIFIER



ORDERING INFORMATION

8 Pin Plastic DIP	14 Pin CERDIP	TO-99 Can
ICL741CHSPA	ICL741MHSJD	ICL741CHSTY ICL741MHSTY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage (Note 2) . . . . . ±15V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering at 60 sec.) . . . . . 300°C
Output Short-Circuit Duration (Note 3) . . . . . Indefinite

NOTE 1: The maximum junction temperature of the 741HS is 150°C, while that of the 741CHS is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

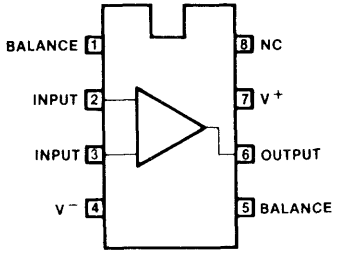
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage. T_A = 25°C unless otherwise specified.

NOTE 3: Short circuit may be to ground or either supply.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

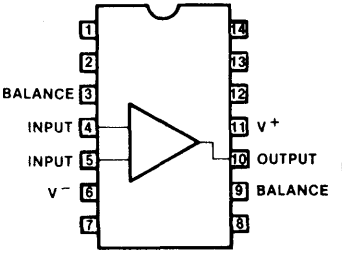
PIN CONFIGURATIONS

NOTE: AVAILABLE IN COMMERCIAL TEMP RANGE ONLY

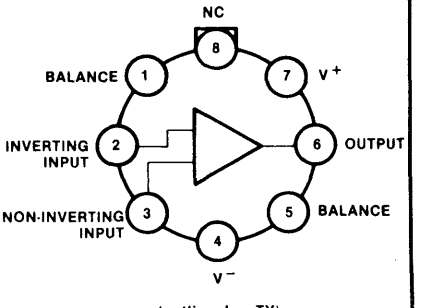


(outline dwg PA)

NOTE: AVAILABLE IN MILITARY TEMP RANGE ONLY



(outline dwg JD)



(outline dwg TY)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	741CHS MIN	741CHS TYP	741CHS MAX	741MHS MIN	741MHS TYP	741MHS MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		2	6.0		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		20	200		20	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	2.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	25	160		50	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			7.5			6	mV
Slew Rate	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$ $C_L = 50pF$	0.7	1.0		0.7	1.0		V/μsec
Input Offset Current	$T_A = 25°C$			300			500	nA
Input Bias Current				0.8			1.5	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	77	96		77	96		dB

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT OFFSET CURRENT: The difference in the currents into the two input terminals when the output is at zero.

INPUT VOLTAGE RANGE: The range of voltages on the input terminals for which the offset specifications apply.

INPUT BIAS CURRENT: The average of the two input currents.

COMMON MODE REJECTION RATIO: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT RESISTANCE: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

SLEW RATE: A measure of the large signal capability of amplifier output to follow the amplifier input. Slew Rate = $2\pi BW_{Large\ Signal} V_{O\text{-}Peak}$.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier with no load and the output at zero.

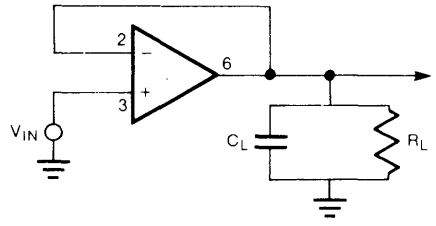
OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without clipping.

LARGE-SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

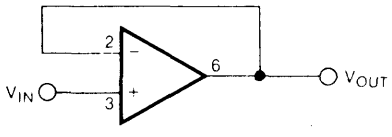
POWER SUPPLY REJECTION: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

TEST CIRCUITS

TRANSIENT RESPONSE TEST CIRCUIT



FAST VOLTAGE FOLLOWER



Power Bandwidth: 1.5kHz
Slew Rate: 1V/μs

ICL741LN, ICL741CLN, ICL101ALN ICL301ALN, ICL108LN, ICL308LN

Low Noise Operational Amplifiers

FEATURES

- Guaranteed Noise Specifications
- Complete Electrical Specifications

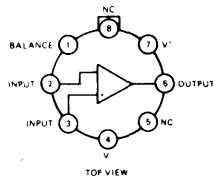
GENERAL DESCRIPTION

These low noise amplifiers are suitable for all applications where low level signals are encountered. The three important noise parameters, input referred voltage noise, input referred current noise, and popcorn noise, are all 100% screened and guaranteed.

5

PIN CONFIGURATIONS

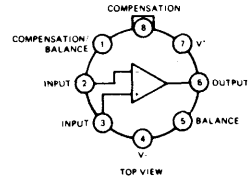
741/741C



(outline dwg TY)

NOTE: PIN 4 CONNECTED TO CASE.

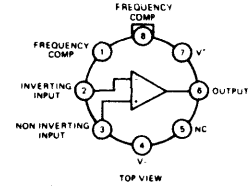
101A/301A



(outline dwg TY)

NOTE: PIN 4 CONNECTED TO CASE.

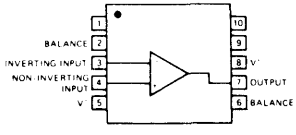
108/308



(outline dwg TY)

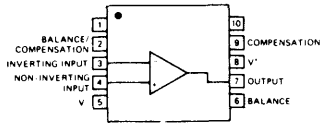
NOTE: PIN 4 CONNECTED TO CASE.

741



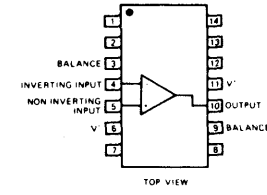
(outline dwg FB-1)

101A



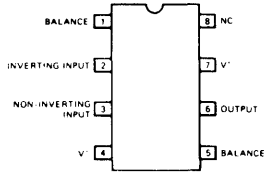
(outline dwg FB)

741



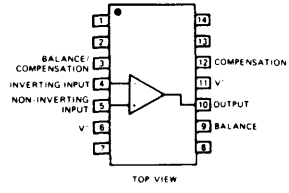
(outline dwg JD)

741C



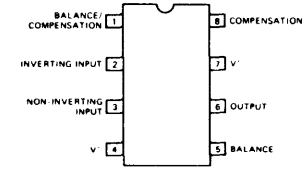
(outline dwg PA)

101A



(outline dwg JD)

301A



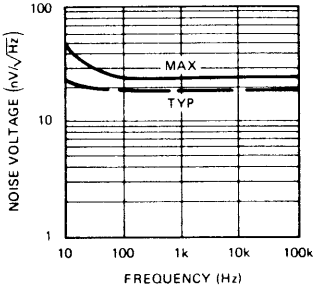
(outline dwg PA)

GUARANTEED NOISE SPECIFICATIONS (T_A = 25°C)

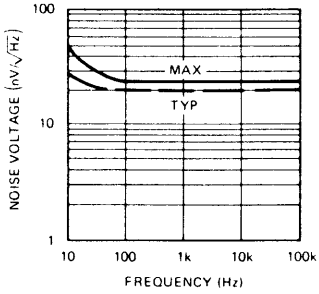
	741	741C	101A	301A	108	308	UNITS
Input Referred Voltage Noise @ 10 Hz (Max)	50	50	50	50	70	70	$nV/\sqrt{Hz}$
Input Referred Current Noise @ 10 Hz (Max)	0.4	0.4	0.7	0.7	0.2	0.2	$pA/\sqrt{Hz}$
Popcorn Noise Transition Amplitude for R_S = 100k (Max)	25	25	25	25	25	25	μV

For other electrical specifications see standard data sheets.

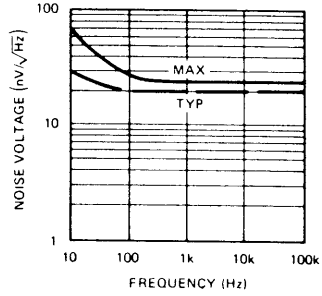
741 INPUT REFERRED VOLTAGE NOISE



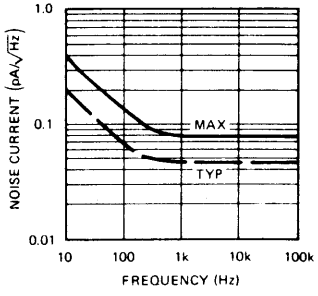
101A/301A INPUT REFERRED VOLTAGE NOISE



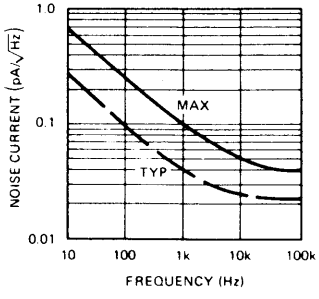
108/308 INPUT REFERRED VOLTAGE NOISE



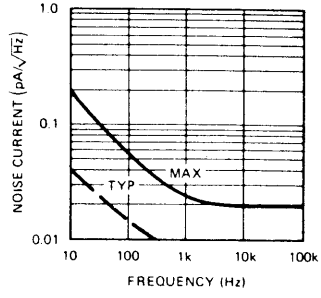
741 INPUT REFERRED CURRENT NOISE



101A/301A INPUT REFERRED CURRENT NOISE



108/308 INPUT REFERRED CURRENT NOISE



ORDERING INFORMATION

PART NUMBER	TYPE	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
741-LN	MIL	TO-99	-55°C to +125°C	ICL741LNTY
741C-LN	COM	TO-99	0°C to + 70°C	ICL741CLNTY
741-LN	MIL	14 Lead DIP	-55°C to +125°C	ICL741LNJD
741C-LN	COM	8 Lead DIP	0°C to + 70°C	ICL741CLNPA
741-LN	MIL	FLAT PACK	-55°C to +125°C	ICL741LNFB
101A-LN	MIL	TO-99	-55°C to +125°C	ICL101ALNTY
301A-LN	COM	TO-99	0°C to + 70°C	ICL301ALNTY
101A-LN	MIL	14 Lead DIP	-55°C to +125°C	ICL101ALNJD
301A-LN	COM	8 Lead DIP	0°C to + 70°C	ICL301ALNPA
101A-LN	MIL	FLAT PACK	-55°C to +125°C	ICL101ALNFB
108-LN	MIL	TO-99	-55°C to +125°C	ICL108LNTY
308-LN	COM	TO-99	0°C to + 70°C	ICL308LNTY

NOISE IN OPERATIONAL AMPLIFIERS

VOLTAGE NOISE: The noise due to the equivalent input voltage generator is measured using the circuit shown in Figure 1. It is expressed in $nV/\sqrt{Hz}$.

CURRENT NOISE: The noise due to the equivalent input current generator is measured using the circuit in Figure 2. It is expressed in $pA/\sqrt{Hz}$. Popcorn noise cannot be effectively screened using this test due to its erratic nature and very low frequency.

POPCORN NOISE: Popcorn noise, sometimes referred to as burst noise, is a low frequency noise phenomenon in which the output of the amplifier appears to jump erratically between two or more stable states. It is most noticeable when operating at high source impedances and is expressed as a transition amplitude, in μV, for a given source resistance. The test circuit of Figure 3 is used.

The noise of an amplifier may be expressed in terms of an input referred voltage generator (e_n) and an input referred current generator (i_n), see Figure 4. The total noise of an amplifier in a typical application contains contributions from both these generators, together with a contribution from the source resistance. The total mean square noise for a bandwidth of 1 Hz is given by:

$$e^2_T = e^2_n + i^2_n R^2_S + 4kTR_S \qquad (1)$$

Since both e_n and i_n are frequency dependent, the total mean square noise for a given bandwidth $\Delta f = f_2 - f_1$ is given by:

$$e^2_T = \int_{f_1}^{f_2} e^2_n \, df + R^2_S \int_{f_1}^{f_2} i^2_n \, df + 4kTR_S \Delta f \qquad (2)$$

With most amplifiers, the voltage noise term dominates for low source impedances. The current noise term is dominant at higher source impedances.

To specify operational amplifier noise performance one of two methods is used. One is to specify the total input referred noise for a given bandwidth and source impedance. This is defined as e_T from equation 1 above. The test circuit in Figure 5 is used. The typical broadband noise of the 741 and 101A type amplifier is shown in Figure 5.

The second method is to guarantee specific values of e_n and i_n (in equation 2) at various frequencies. A Noise Analyzer is used for this measurement (Figure 3). The values of e_n and i_n (for Δf = 1 Hz) are measured at 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz. The recorded values may be plotted graphically, as shown on page 1. The noise information obtained from these measurements is considerably more general than that obtained from the first method, since the noise for any source impedance and bandwidth may be calculated from equation 2. (Graphical integration can determine the area under each curve.)

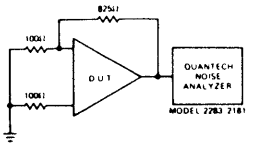


FIGURE 1.

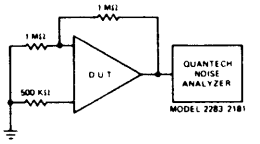


FIGURE 2.

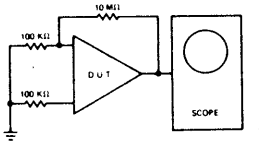


FIGURE 3.

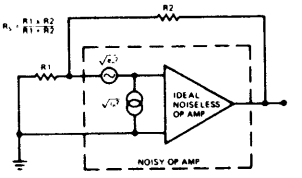


FIGURE 4.

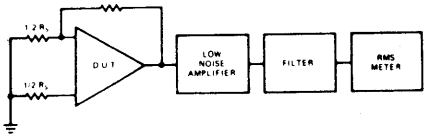


FIGURE 5.

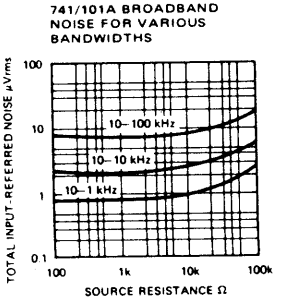


FIGURE 6.

μA777
Precision Operational Amplifier

FEATURES

- **Low offset voltage and offset current**
- **Low offset voltage and current drift**
- **Low input bias current**
- **Low input noise voltage**
- **Large common mode and differential voltage ranges**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1)
Metal Can 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range (HC) ..... 0°C to 70°C
(HM) .. −55°C to +125°C
Lead Temperature (Soldering, 10s) ..... 300°C
..... 260°C
Output Short Circuit Duration (Note 3) ..... Indefinite

Note 1: Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for the DIP, and 5.6mW/°C for the Mini DIP.

Note 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3. Short Circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30\mu A$.

ORDERING INFORMATION

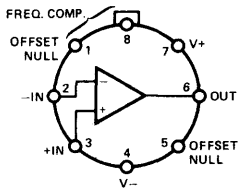
	Dice	TO-99 Can
μA777C	μA777C/D	μA777HC
μA777M	μA777M/D	μA777MC

GENERAL DESCRIPTION

The μA777 is a monolithic Precision Operational Amplifier. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777 maintains full ±30V differential voltage range. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easily used.

PIN CONFIGURATION

8-LEAD METAL CAN
(TOP VIEW)



(outline dwg TY)

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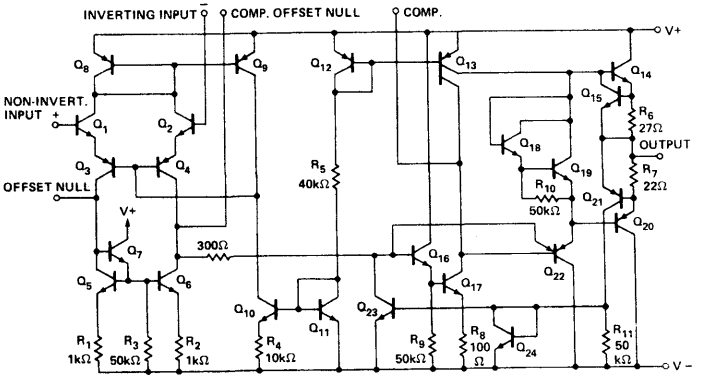
ELECTRICAL CHARACTERISTICS FOR μA777 (V_S = ±15V, T_A = 25°C, C_C = 30pF unless otherwise specified)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50k\Omega$		0.7	5.0	mV
Input Offset Current				0.7	20.0	nA
Input Bias Current				25	100	nA
Input Resistance			1.0	2.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20mV, C_C = 30pF R_L = 2kΩ, $C_L \leq$ 100pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2k\Omega$		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20mV, C_C = 3.5pF R_L = 2kΩ, $C_L \leq$ 100pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \leq 2k\Omega$, C_C = 3.5pF		5.5		V/μs
The following specifications apply over operating temperature range.						
Input Offset Voltage		$R_S \leq 50k\Omega$		0.8	5.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50k\Omega$		4.0	30	μV/°C
Input Offset Current					40	nA
Average Input Offset Current Drift		25°C ≤ T_A ≤ +70°C 0°C ≤ T_A ≤ +25°C		0.01 0.02	10.3 0.6	nA/°C nA/°C
Input Bias Current					200	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50k\Omega$	70	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50k\Omega$		15	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15,000			V/V
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Power Consumption				60	100	mW

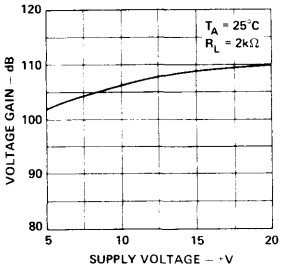
5

EQUIVALENT CIRCUIT

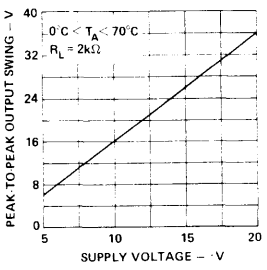


TYPICAL PERFORMANCE CURVES

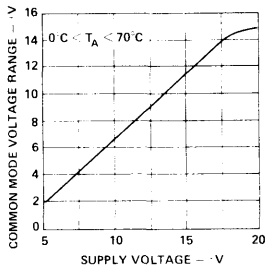
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



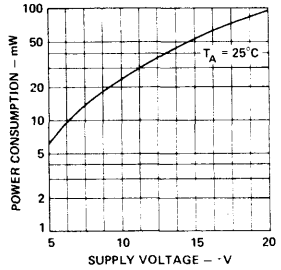
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



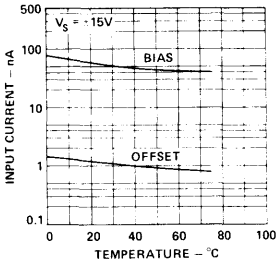
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



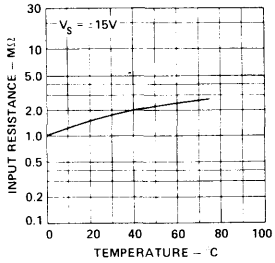
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



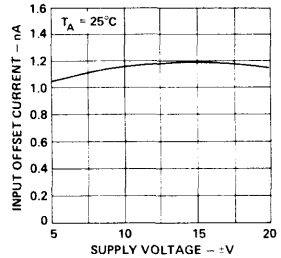
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



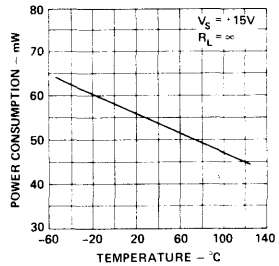
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



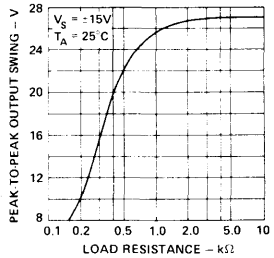
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



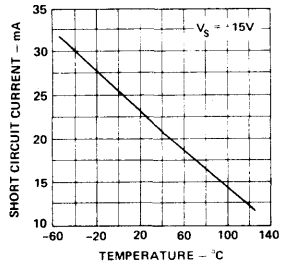
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



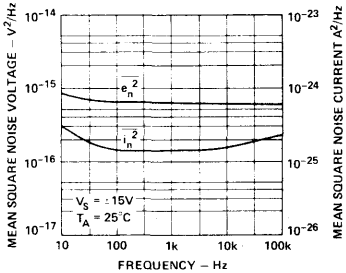
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

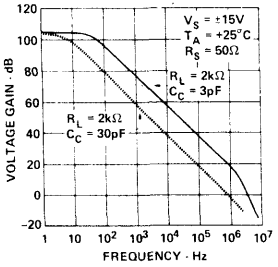


INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

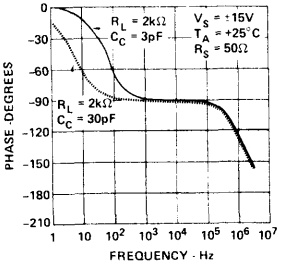


TYPICAL PERFORMANCE CURVES

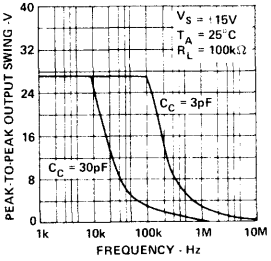
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



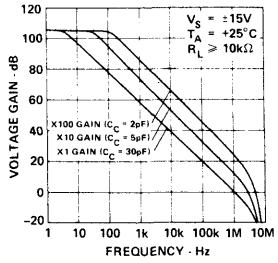
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



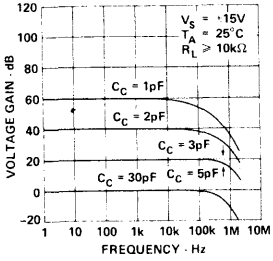
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



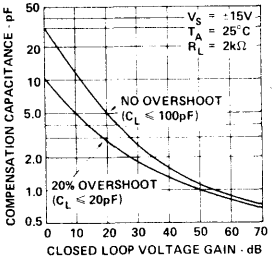
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



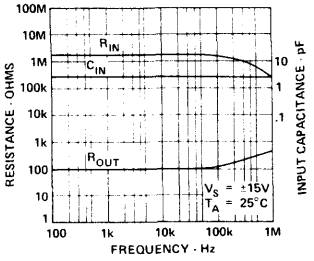
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



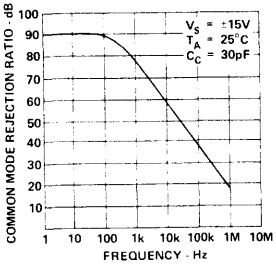
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



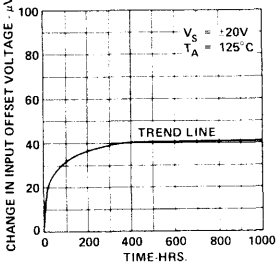
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



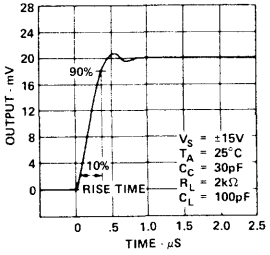
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



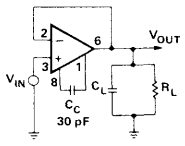
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



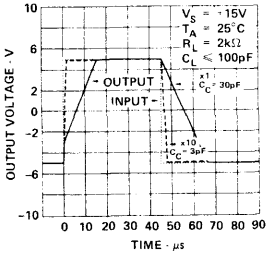
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

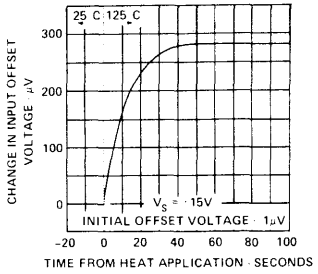


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

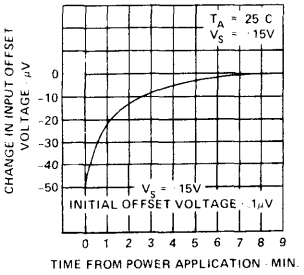


TYPICAL PERFORMANCE CURVES

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

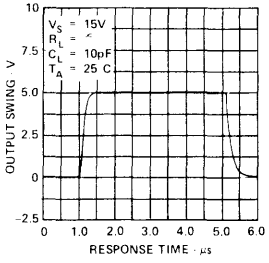


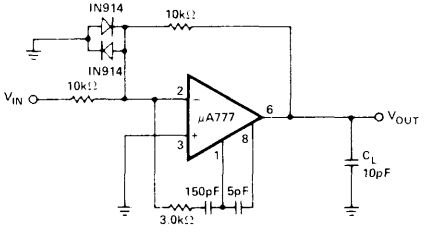
STABILIZATION TIME OF INPUT OFF—SET VOLTAGE FROM POWER TURN-ON



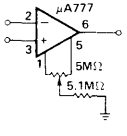
FEED FORWARD COMPENSATION

LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE

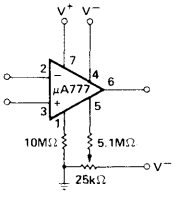




VOLTAGE OFFSET NULL CIRCUIT

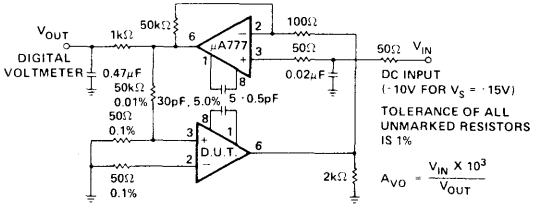


SUGGESTED



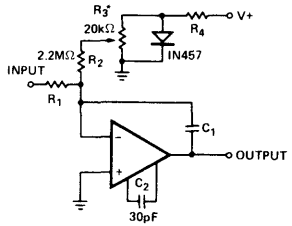
ALTERNATE

GAIN TEST CIRCUIT



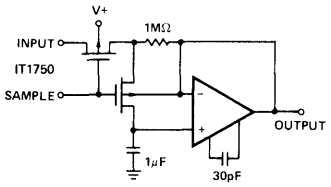
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

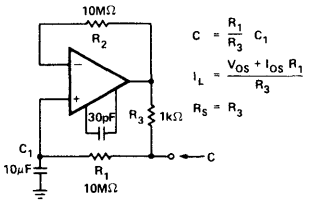


*ADJUST R_3 FOR MINIMUM INTEGRATOR DRIFT

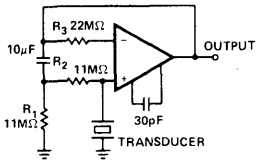
SAMPLE AND HOLD



CAPACITANCE MULTIPLIER

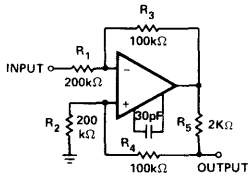


AMPLIFIER FOR CAPACITANCE TRANSDUCERS



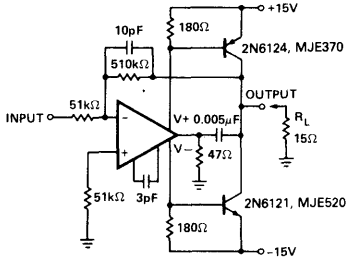
LOW FREQUENCY CUTOFF $R_1 \times C_1$

BILATERAL CURRENT SOURCE

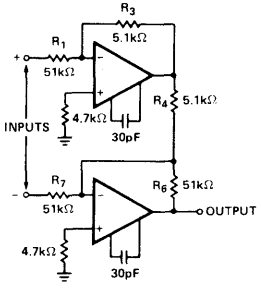


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \; ; R_1 = R_2; R_3 = R_4 + R_5$$

HIGH SLEW RATE POWER AMPLIFIER



±100V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER



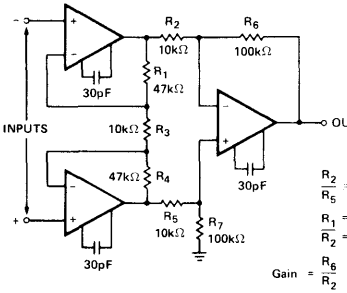
$\frac{R_1}{R_7} = \frac{R_3}{R_4}$ for best CMRR

$R_3 = R_4$

$R_1 = R_6 = 10R_3$

$\text{Gain} = \frac{R_7}{R_6}$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$\frac{R_2}{R_5} = \frac{R_6}{R_7}$ for best CMRR

$\frac{R_1}{R_2} = \frac{R_4}{R_5}$

$\text{Gain} = \frac{R_6}{R_2}\left(1 + \frac{2R_1}{R_3}\right)$

LH2108/2308
Dual Super Beta Op Amp

FEATURES

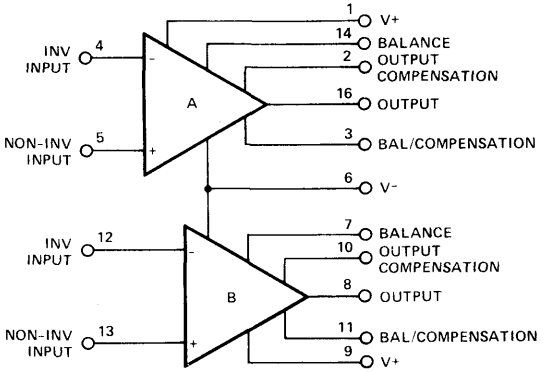
- **Low offset current - 50 pA**
- **Low offset voltage - 0.7 mV**
- **Low offset voltage - LH2108A: 0.3 mV**
  LH2108: 0.7 mV
- **Wide input voltage range - ±15V**
- **Wide operating supply range - ±3V to ±20V**

GENERAL DESCRIPTION

The LH2108A/LH2308A and LH2108/LH2308 series of dual operational amplifiers consist of two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, and reduced insertion cost.

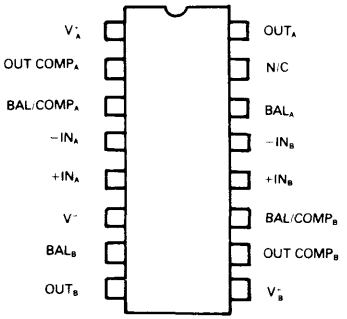
The LH2108A/LH2108 is specified for operation over the −55°C to +125°C military temperature range, and the LH2308A/LH2308 is specified for operation from 0°C to +70°C.

CONNECTION DIAGRAM



ORDER NUMBER LH2108AD, LH2408AD, LH2108D, OR LH2408D

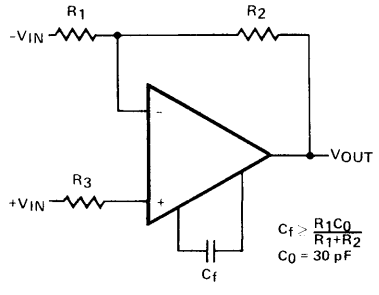
PIN CONFIGURATION



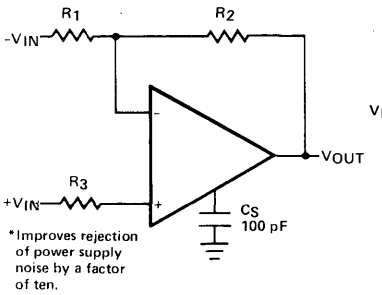
(outline dwg DE)

AUXILIARY CIRCUITS

STANDARD COMPENSATION CIRCUIT

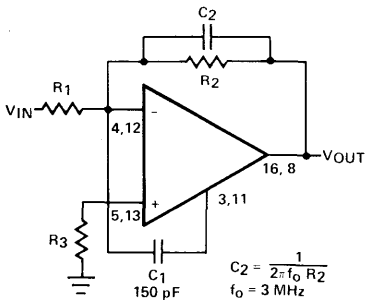


ALTERNATE* FREQUENCY COMPENSATION



*Improves rejection of power supply noise by a factor of ten.

FEEDFORWARD COMPENSATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Power Dissipation (Note 1) ..... 500 mW
Differential Input Current (Note 2) ..... ±10mA
Input Voltage (Note 3) ..... ±15V
Output Short Circuit Duration ..... Continuous
Operating Temperature Range
LH2108A/LH2108 ..... −55°C to +125°C
LH2308A/LH2408 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS Each side (Note 4)

PARAMETER	CONDITIONS	LIMITS LH2108	LIMITS LH2308	UNITS
Input Offset Voltage	$T_A = 25°C$	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	7.0	
Input Resistance	$T_A = 25°C$	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10\ k\Omega$	50	25	V/mV Min
Input Offset Voltage		3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	30	μV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	—	mA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10\ k\Omega$	25	15	V/mV Min
Output Voltage Swing	$V_S = ±15V$, $R_L = 10\ k\Omega$	±13	±13	V Min
Input Voltage Range	$V_S = ±15V$	±13.5	±14	
Common Mode Rejection Ratio		85	80	dB Min
Supply Voltage Rejection Ratio		80	80	

PARAMETER	CONDITIONS	LIMITS LH2108A	LIMITS LH2308A	UNITS
Input Offset Voltage	$T_A = 25°C$	0.5	0.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	7.0	
Input Resistance	$T_A = 25°C$	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10\ k\Omega$	80	80	V/mV Min
Input Offset Voltage		1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	μV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	-	mA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10\ k\Omega$	40	60	V/mV Min
Output Voltage Swing	$V_S = ±15V$, $R_L = 10\ k\Omega$	±13	±13	V Min
Input Voltage Range	$V_S = ±15V$	±13.5	±14	
Common Mode Rejection Ratio		96	96	dB Min
Supply Voltage Rejection Ratio		96	96	

Note 1: The maximum junction temperature of the LH2108/A is 150°C, and that of the LH2308/A is 85°C. The thermal resistance of the packages is 100°C/W, junction to ambient.
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 4: These specifications apply for $±5V \leq V_S \leq ±20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified, and the LH2308A/LH2308 for $±5V \leq V_S \leq 15V$ and $0°C \leq T_A \leq 70°C$.

IH5110 — IH5115
General Purpose Sample & Hold

FEATURES

- **Low cost**
- **Military and industrial temperature ranges**
- **±10V input voltage range**
- **0.5mV/sec drift typical @ C_S = 0.01μF**
- **TTL, DTL and CMOS compatible**
- **Short circuit protected**
- **Input offset voltage adjustable to < 100μV using a 20k potentiometer**
- **0.1% guaranteed sample accuracy with 10V signals and C_S = 0.01μF**
- **Sample to hold offset is 5mV max**

SCHEMATIC DIAGRAM

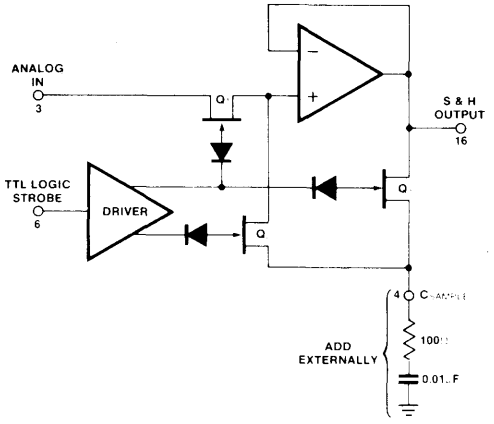


FIGURE 1

GENERAL DESCRIPTION

Each of the 5110 family is a complete Sample and Hold circuit, (except for sampling capacitor) including input buffer amplifier, output buffer amplifier and CMOS logic switching. The devices are designed to operate from ±15V and +5V supplies. The input logic is designed to "Sample" and "Hold" from standard TTL logic levels.

The design is such that the input and output buffering is performed by only one operational amplifier, by switching the sampling capacitor from the output back to input. Switches Q_1, Q_2, and Q_3 (see Fig. 1) accomplish this switching. In the sampling mode Q_1 and Q_3 are shorted and Q_2 is open; thus the op. amp. charges up the sampling capacitor. In the hold mode Q_1 and Q_3 are open and Q_2 is shorted; thus the sampling cap. is switched back to the non-inverting input of the op. amp.

This structure provides a very accurate d.c. gain of 1 with very fast settling times (i.e. 5μs); additionally the design has *internal feedback to cancel charge injection effects* (sample to hold offsets). Q_1 and Q_2 are driven 180 degrees out of phase to accomplish this charge nulling.

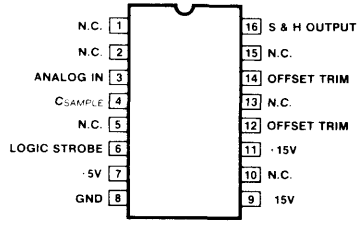
5

ORDERING INFORMATION

IH5110 M JE

- JE: Package
  - JE = 16 pin CERDIP
  - DE = 16 pin ceramic DIP (special order only)
- M: Temperature Range
  - M = Military (-55°C to +125°C)
  - I = Industrial (-20°C to +85°C)
- IH5110: Device Chip Type

PIN CONFIGURATION



(outline dwg DE, JE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±16V
Power Dissipation 500mW
Operating Temperature ..... −25°C to 85°C
−55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

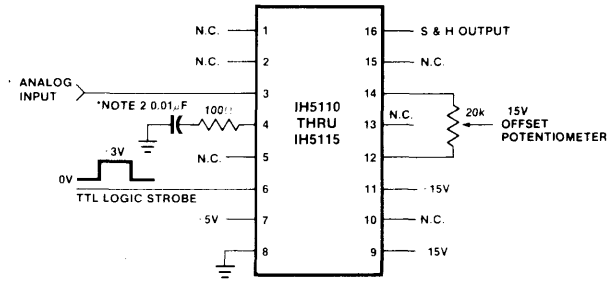
ELECTRICAL CHARACTERISTICS (Pin 7 = 5V, Pin 8 = GND, Pin 9 = −15V, Pin 11 = 15V, T_A = 25°C) Note 3

SYMBOL	CHARACTERISTIC	IH5110, 5112, 5114			IH5111, 5113, 5115			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Close	Aperature Time		120	200		120	200	ns
$t_{acq.}$	Acquisition Time for Max Analog Voltage Step C_S = 0.1μF (0.1% Accur.) C_S = 0.01μF (0.1% Accur.) C_S = 0.001μF (0.1% Accur.) See fig. 4		 25 4 4	 35 6 6		 25 4 4	 35 6 6	μs
V_{drift}	Drift Rate C_S = 0.1μF C_S = 0.01μF C_S = 0.001μF See fig. 2		 0.3 0.5 2.0	 2.5 5 10		 0.3 0.5 2.0	 2.5 5 10	mV/sec
V_{inject}	Charge Injection or Sample to Hold Offsets C_S = 0.1μF C_S = 0.01μF C_S = 0.001μF See Note 1 & fig. 3		 <1 <1 12	 5 5 25		 <1 <1 12	 5 5 25	mV_{p-p}
V_{switch}	Switching Transients or Spikes (Duration Less than 2μs) C_S = 0.1μF C_S = 0.01μF C_S = 0.001μF See fig. 3		 0.1 0.1 0.2	 0.5 0.5 0.5		 0.1 0.1 0.2	 0.5 0.5 0.5	V_p
V_{couple}	A.C. Feedthrough Coupled to Output			5			5	mV_{p-p}
V_{offset}	D.C. Offset When in Sample Mode (Trimmable to 0m V With Ext. 20kΩ Potentiometer See fig. 2 5110 5111 5112 5113 5114 5115		 	 40 10 5		 	 40 10 5	mV
R_{in}	Input Impedance in Hold or Sample Mode (f ≤ 10Hz)		100			100		MegΩ
$I_{±15V}$	Plus or Minus 15V Supply Quiescent Current		3.4	6		3.4	6	mA
I_{5V}	5V Supply Quiescent Current		0.3	10		0.3	10	A
V_{analog}	D.C. Input Voltage Range			±7.5			±10	
$V_{A.C. range}$	A.C. Input Voltage Range See Note 2 & fig. 5	15			20			V
I_{strobe}	TTL Logic Strobe Input Current in Either Hold or Sample Mode		0.1	10		0.1	10	μA

NOTES:
1. Offset voltage of op. amp. must be adjusted to 0mV (using 20kΩ potentiometer) before charge injection is measured.
2. The A.C. input voltage range differs from the D.C. input voltage range. All versions will handle any analog input within the range of plus 10V to minus 10V; however the IH5110, 5112, 5114 has the added restriction that the peak to peak swing should be less than $15V_{p-p}$ i.e. ±7.5 Vac.
3. All of the electrical characteristics specs, are guaranteed with C_S = 0.01μF in series with 100Ω as per Fig. 2, C_S = 0.1μF & C_S = 0.001μF are for design aid only.
4. If supplies are reduced to ±12VDC, analog signal range will be reduced to ±7Vp-p.

APPLICATIONS INFORMATION

I. Typical Connection Diagram

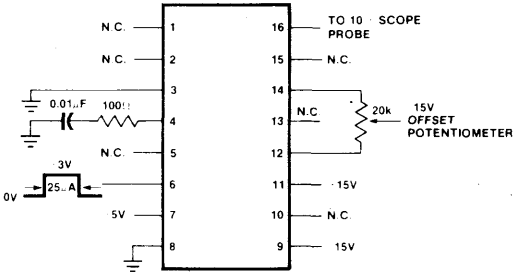


NOTES: 1. To trim output offset to 0mV, set strobe input to sample mode (3V), set analog input to GND, adjust potentiometer until S & H output is 0mV.
2. Use a low dielectric absorption capacitor such as polystyrene.

SAMPLE MODE occurs when logic input is greater than 2.4V.
HOLD MODE occurs when logic input is less than 0.8V.

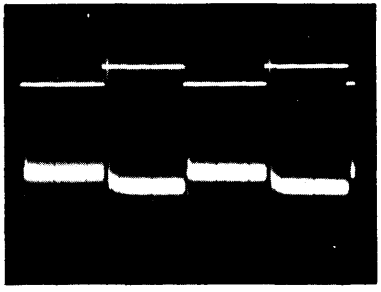
FIGURE 2

II. Charge Injection (sample to hold offset) measurement circuit; also switching transients test circuit.



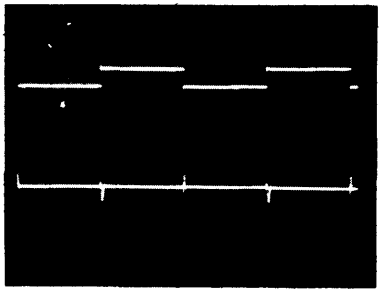
Adjust offset to 0mV before testing for charge injection. See note 1.

CHARGE INJECTION



V_A = GND
LOGIC INPUT
C_S = 0.01μF
3V
0V
UPPER TRACE
LOWER TRACE = 5mV/DIV.
TIME = 10μs/cm
5V/DIV.
+3V
0V

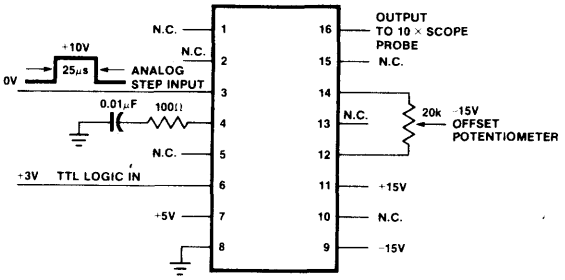
SWITCHING TRANSIENTS



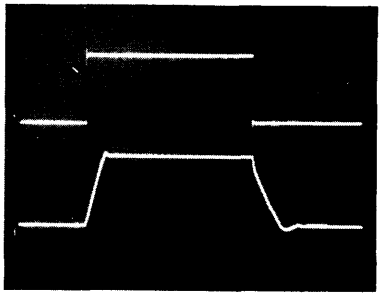
V_A = GND
LOGIC INPUT
C_S = 0.01μs
3V
0V
UPPER TRACE =
LOWER TRACE = 500mV/DIV.
TIME = 10μs/cm
5V/DIV.
+3V
0V

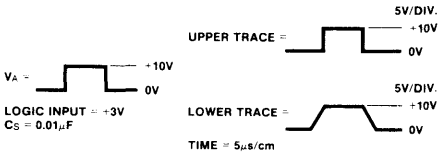
FIGURE 3

III. Typical Circuit for measurement of A.C. signal handling capability.



ACQUISITION TIME





NOTE: The acquisition time is actually a settling time spec. since the reading is only taken when the output has settled within 1% of its final value. The 6μs spec. (IH5111, 5113 & 5115 is the worst reading of the t_{on} or t_{off} settling time shown above. The above test can be performed with a 0 to +7.5V or 0 to −7.5V step for the IH5110, 5112, 5114.

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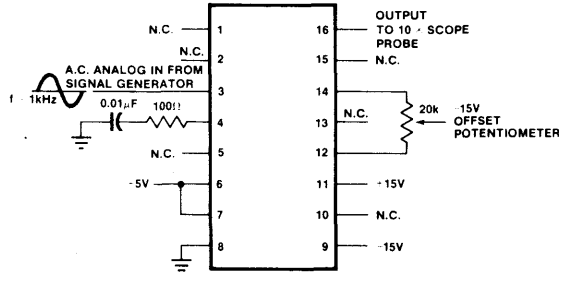
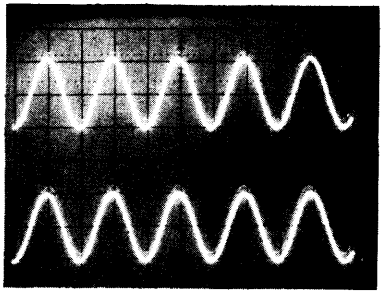
FIGURE 4

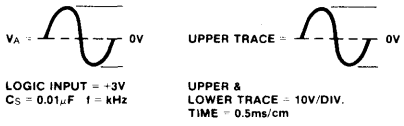
IV. Typical Circuit for measurement of A.C. peak to peak signal handling capability.



A.C. PEAK TO PEAK



TYP. IH5111



To test this parameter, increase the amplitude of the signal generator until the output starts to distort (it will always show up on the positive excursion of the sine wave first); then back off until all distortion is gone. The resultant peak to peak swing must be greater than 15Vpp for the IH5110, 5112, 5114 and greater than 20Vpp for the IH5111, 5113, 5115.

FIGURE 5

V. Application Tips:

If you are undecided as to which sample and hold to use within the family, the following will give you a pretty good idea of the outstanding differences between the six models.

First, determine the voltage range you need to sample and hold.

The even numbered parts are designed to switch smaller a.c. signal amplitudes with the goal being to minimize the charge injection effects (sample to hold offsets). This charge injection error is shown in Fig. 3. Once the voltage offset is zeroed, the 5110 has typical error amplitudes of 1 to 2mVp-p (corresponds to 10pc to 20pc of charge). Thus one could sample very low level d.c. signals with extreme accuracy. If very low level a.c. signals are being sampled, voltage offset potentiometer can be adjusted for a zero charge injection effect. Once the potentiometer has been adjusted, there will be a zero error going from sample to hold; however there will be a d.c. error caused by adjusting the potentiometer for zero charge injection and not for zero voltage offset. In general, this d.c. error will be in the area of 2mV to 5mV.

The odd numbered parts are primarily designed to handle any input in the plus or minus 10V range, regardless of whether it is a.c. or d.c.; to obtain this, the charge injection is about a factor of 2 higher than the even numbered parts.

The use of Varafet switching elements similar to Intersil's IH401/401A leads to a trade-off between AC signal swing and charge injection.

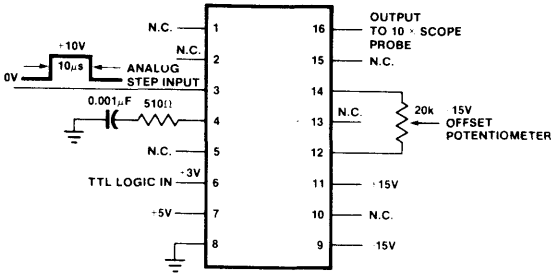
After the voltage range and charge injection requirements have been determined, all that remains is to determine the input offset voltage the system can tolerate. By using the higher numbered parts, it is possible to eliminate the offset potentiometer if system accuracy will allow 5mV (5114, 5115) or 10mV (5112, 5113) due to the low input offset voltage on these devices.

The drift rate is specified at 10mV/sec. Max. for all models: this corresponds to approximately 100pA total leakage into a 0.01μF sampling capacitor (C_S). While the 10mV/sec. is the Max. encountered, a more typical reading is less than 1mV/sec. (true for any input between −10V and +10V); thus the IH5110 family is ideal for applications requiring very low drift or droop rates.

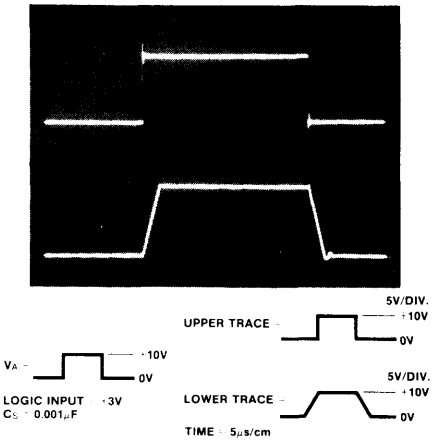
The aperture time is spec'd at 200ns Max. for all models, but a more typical value is 150ns; this is basically the off time of switch Q_1. The way this aperture time affects system accuracy is shown below:

Assume the input signal to the Sample and Hold is an a.c. signal of peak amplitude A (peak to peak swing is 2A) and frequency $2\pi f = w$, then $V_{input} = Ae^{jwt}$ then $dV/dt = Ae^{jwt}$. This means the slope of input signal = dV/dt; this slope is a maximum at t (time) = 0, this maximum value is wA (in amplitude). (i.e.) input frequency is 10kc, therefore dV/dt = $wA = 6.28 \times 10^4 \times 10V = 6.3 \times 10^5$V/sec. A = 10V, then slope or dV/dt = 0.63V/μs. Now if we wish error to be a Max. of say 1% of full scale 10V, we see that 100mV (1%/aperture time = 0.63V/μs. Solving this equation we see that aperture time must be 160ns or less to get 1% holding accuracy. Since our aperture time is 150ns typical, we have 1% accuracy in holding 10kHz varying signals; for signal frequencies 1kHz and less, Max. error is 0.1%. The simple interpretation of just how the off time of the switch causes this system error is due to the fact a finite time is required for the switch to react to a hold command; this reaction time manifests itself with a system voltage error because the time varying input signal is changing to a new value before the switch has actually turned off. (i.e.) in the above example off = 10kHz and A = 10V, suppose we gave the hold command (thru TTL logic) at t = 0 (a.c. signal goes thru zero pt.) At this point we have calculated the slope to be a Max. and equal to 0.63V/μs. If there were no aperture time error, we would read 0V at output of Sample and Hold; however because of finite time for switch to respond to hold command, 150ns passes before switch goes off. During this 150ns, the input signal has gone to 100mV above or below 0V, thus the stored value of signal will be 100mV and that is the reading at the output of the Sample and Hold. If the input frequency were 1kHz, the "error voltage" would be 10mV.

VI. Connection for Hi-Speed Sample and Hold with following typical performance: w/C_S = 0.001
  a. 2μs settling time (acquisition time) to 1% accuracy
  b. 25mV charge injection amplitude
  c. 10mV/sec drift rate



HI-SPEED SAMPLE AND HOLD



NOTE: Typical times for the Sample and Hold to acquire the input are 2μs for turn on (output) goes to +10V and 3μs for turn off (output goes down to 0V). As a general note, all the electrical specifications are guaranteed with a sampling capacitor equal to 0.01μf. As the above application (Fig. 6) shows, other values of sampling capacitors can be used but the best combinations of S & H specs may not result with values other than 0.01μF. The only advantage of using a 0.001μF for C_S is the acquisition time is 2μs typical instead of 5μs typical (with 0.01μF; however the drift rate would be worse and charge injection would be affected). To minimize drift rate, use a 0.1μF capacitor; this should produce a 0.1mV/sec rate of change and a charge injection amplitude of 0.2mVp-p. Of course the acquisition time will be slowed down to the 25μs area. Also use a 0.1μs system for slow speed changes (i.e., input frequency is less than 1kHz. The series resistor should be about 100Ω-200Ω to stabilize the system.

FIGURE 6

DEFINITION OF TERMS

Aperture Time: The time it takes to switch from sample mode to hold mode and the actual opening of switch.

Charge Injection: The amount of charge coupled across the switch with no input voltage.

Drift Rate: The amount of drift of output voltage at a rate caused by current flow through the storage capacitor.

$\left(\frac{dV}{dt} = \frac{i}{c}\right)$ This current is the leakage across the switch and the amplifier's bias current.

Feed Through: The amount of input signal that appears at the output when in the hold mode. Normally caused by capacitance across the switch.

Offset Voltage: Voltage measured at output with no input voltage and circuit in sample mode.

Acquisition Time: The time it takes amplifier to reach full scale output either plus or minus.

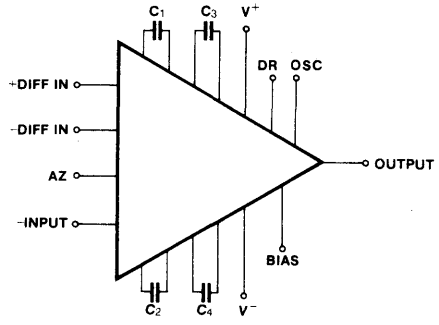
ICL7605/ICL7606

Commutating Auto-Zero (CAZ) Instrumentation Amplifier

FEATURES

- **Exceptionally low input offset voltage — 2μV**
- **Low long term input offset voltage drift — 0.2μV/year**
- **Low input offset voltage temperature drift — 0.05μV/°C**
- **Wide common mode input voltage range — 0.3V above supply rail**
- **High common mode rejection ratio — 100 dB**
- **Operates at supply voltages as low as ±2V**
- **Short circuit protection on outputs for ±5V operation**
- **Static-protected inputs — no special handling required**
- **Fabricated using proprietary MAXCMOS™ process technology**
- **Compensated (ICL7605) or uncompensated (ICL7606) versions**

SYMBOL



GENERAL DESCRIPTION

The ICL7605/ICL7606 commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10 Hz. This is made possible by the unique construction of this new Intersil device, which takes an entirely new design approach to low frequency amplifiers.

Unlike conventional amplifier designs, which employ three op amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long term drift phenomena and temperature effects, and a flying capacitor input.

The ICL7605/ICL7606 is a monolithic CMOS chip which consists of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauges, which require voltage gains from 1 to 1000 and bandwidths from DC to 10 Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. The no-adjustment feature, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

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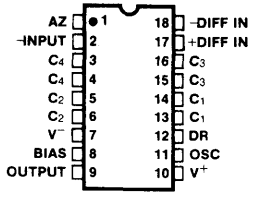
PIN CONFIGURATION



(outline dwg JN)

ORDERING INFORMATION

Order parts by the following part numbers:

Compensated	Uncompensated	Package	Temperature Range
ICL7605CJN	ICL7606CJN	CERDIP	0°C to +70°C
ICL7605IJN	ICL7606IJN	CERDIP	-25°C to +85°C
ICL7605MJN	ICL7606MJN	CERDIP	-55°C to +125°C

Order dice by the following part numbers:

ICL7605/D
ICL7606/D

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (sum of both positive and negative supply voltages V^+ to V^-) ..... 18 Volts
DR Input Voltage ..... (V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, C_3, C_4 +DIFF IN, −DIFF IN, −INPUT, BIAS, OSC) (Note 1) ..... (V^+ +0.3) to (V^- −0.3) Volts
Differential Input Voltage (+DIFF IN to −DIFF IN) (Note 2) ..... +(V^+ +0.3) to (V^- −0.3) Volts
Duration of Output Short Circuit (Note 3) ..... Unlimited

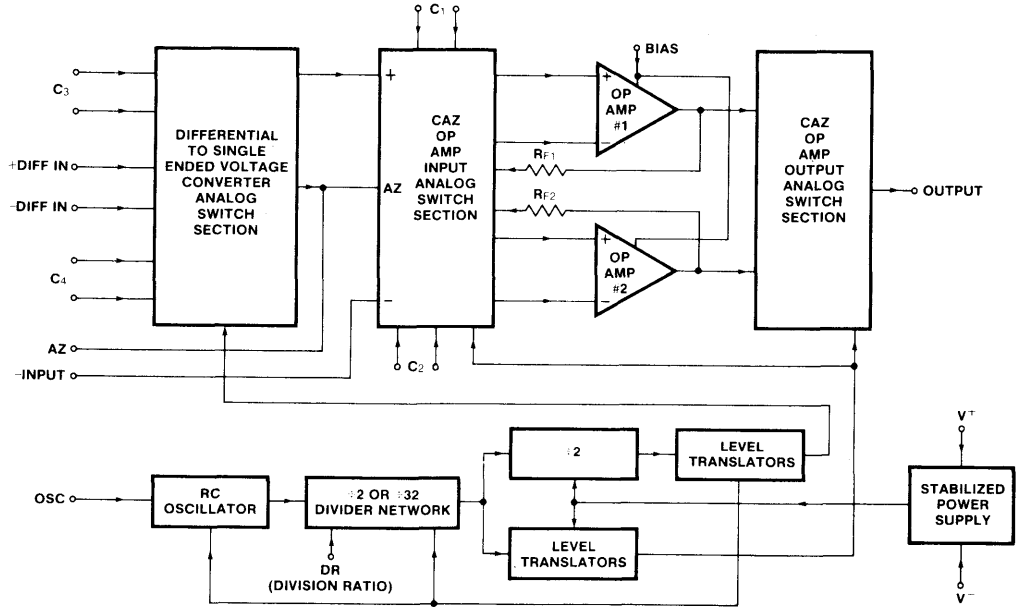
Continuous Total Power Dissipation (at or below 25°C free-air temperature) (Note 4) ..... 500 mW
Operating Temperature Range:
ICL7605/ICL7606CJN ..... 0 to +70°C
ICL7605/ICL7606IJN ..... −25°C to +85°C
ICL7605/ICL7606MJN ..... −55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering 60 seconds) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latchup. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.
Note 2: No restrictions are placed on the differential input voltages on either the +DIFF IN or −DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.
Note 3: The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.
Note 4: For operation above 25°C free-air temperature, derate 4mW/°C from 500 mW above 25°C.

5

BLOCK DIAGRAM



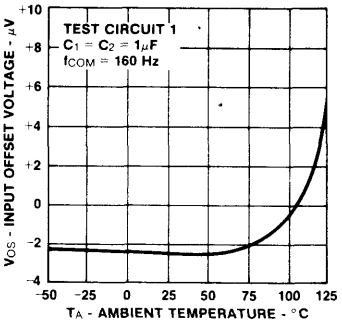
OPERATING CHARACTERISTICS

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

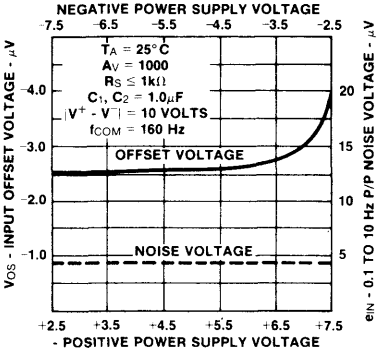
PARAMETER	SYMBOL	CONDITIONS		VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
			Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±20	μV
Average Input Offset Voltage Temperature Coefficient	$\Delta V_{OS}/\Delta T$	Low or Med Bias Settings	−55°C > T_A > +25°C		0.01	0.2	μV/°C
			+25°C > T_A > +85°C		0.01	0.2	μV/°C
			+25°C > T_A > +125°C		0.05	0.2	μV/°C
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	Low or Med Bias Settings			0.5		μV/Year
Common Mode Input Range	CMVR			−5.3		+5.3	V
Common Mode Rejection Ratio	CMRR	C_{OSC} = 0, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
Power Supply Rejection Ratio	PSRR				110		dB
-INPUT Bias Current	$-I_{BIAS}$	Any bias setting, f_C = 160Hz (Includes charge injection currents)			0.15	1.5	nA
Equivalent Input Noise Voltage peak-to-peak	$\bar{e}_{np-p}$		Low Bias Mode		4.0		μV
		Band Width	Med Bias Mode		4.0		μV
		0.1 to 10Hz	High Bias Mode		5.0		μV
Equivalent Input Noise Voltage	$\bar{e}_n$	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		μV
Voltage Gain	A_V	R_L = 100kΩ	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
Maximum Output Voltage Swing	$\pm V_O$	R_L = 1MΩ			±4.9		V
		R_L = 100kΩ			±4.8		V
		R_L = 10kΩ	Positive Swing	+4.4			V
			Negative Swing			−4.5	V
Band Width of Input Voltage Translator	GBW	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
Nominal Commutation Frequency	f_{COM}	C_{OSC} = 0pF	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
Nominal Input Converter Commutation Frequency	f_{COM1}	C_{OSC} = 0pF	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
Bias Voltage to define Current Modes	V_{BA}	Low Bias Setting		V^+−0.3	V^+	V^++0.3	V
	V_{BM}	Med Bias Setting		V^-+1.4	GND	V^+−1.4	V
	V_{BL}	High Bias Setting		V^-−0.3	V^-	V^-+0.3	V
Bias (Pin 8) Input Current	I_{BIAS}				±30		pA
Division Ratio Input Current	I_{DR}	$V^+ - 8.0 \leq V_{DR} \leq V^+ + 0.3$ volt			±30		pA
DR Voltage to define Oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32		V^+−0.3		V^++0.3	V
	V_{DRL}	Internal oscillator division ratio 2		V^+−8		V^+−1.4	V
Effective Impedance of Voltage Translator Analog Switches	R_{AS}				30		kΩ
Supply Current	I_{SUPP}	High Bias Setting			7	15	mA
		Med Bias Setting			1.7	5	mA
		Low Bias Setting			0.6	1.5	mA
Operating Supply Voltage Range	V^+-V^-	High Bias Setting		5		10	V
		Med or Low Bias Setting		4		10	V

INTERSIL

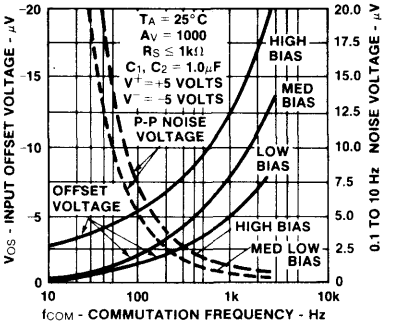
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



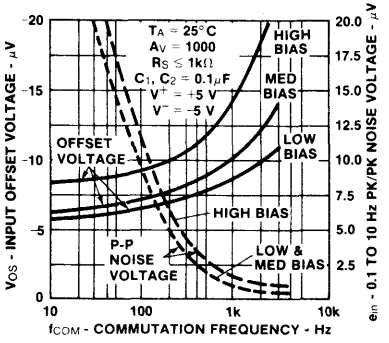
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



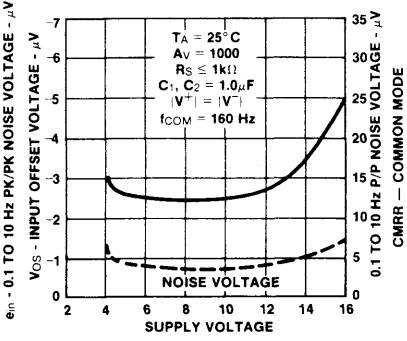
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1μF)



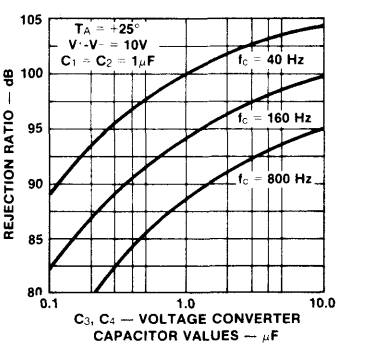
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1 μF)



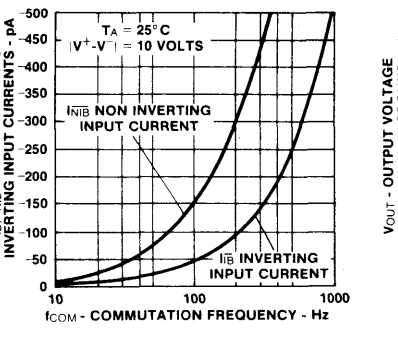
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)



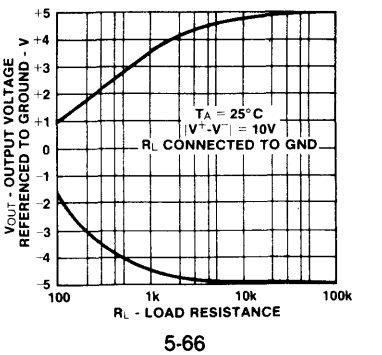
COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



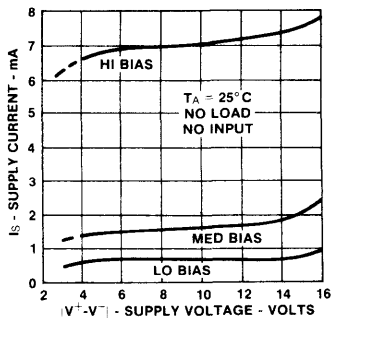
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



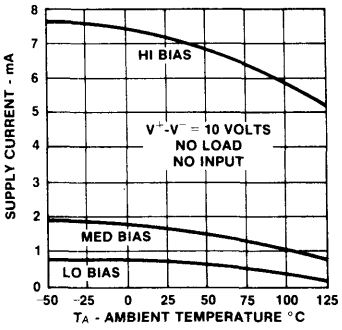
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



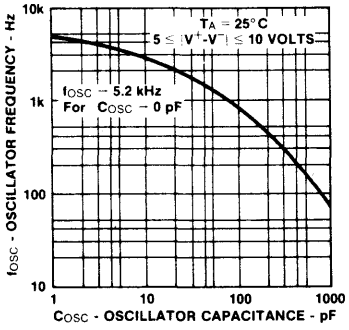
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



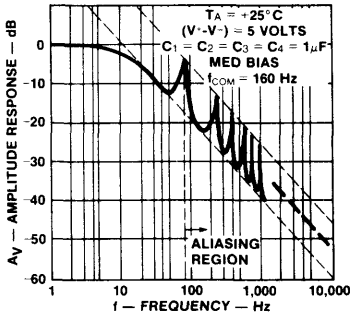
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



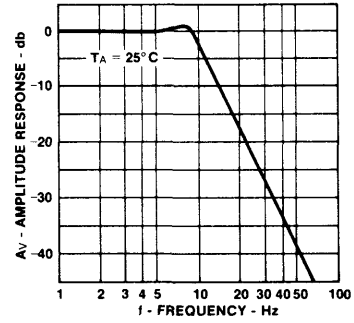
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

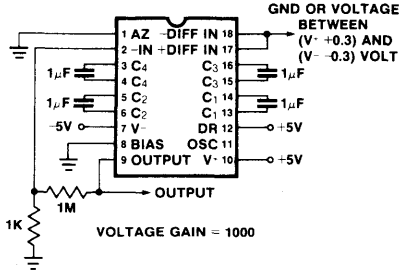


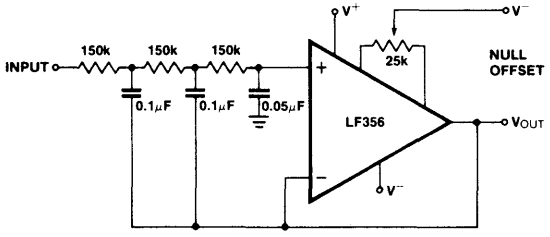
AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).







TEST CIRCUIT 1: USE TO MEASURE:

a) INPUT OFFSET VOLTAGE $\left(\frac{V_{OUT}}{1000}\right)$

b) INPUT EQUIV NOISE VOLTAGE

c) SUPPLY CURRENT

d) CMRR

e) PSRR

TEST CIRCUIT 2: DC to 10Hz (1Hz) Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation for internal error voltages, whether they are derived from steady-state conditions, temperature, supply voltage fluctuations, or are variable over a long term.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 1.

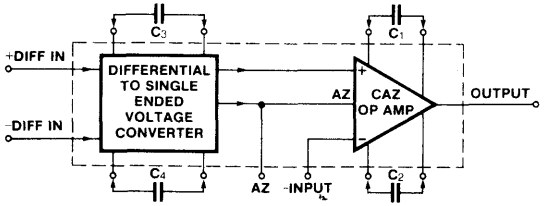


Figure 1: Simplified Block Diagram

The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20 Hz maximum). However in many applications speed is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ amp section of the ICL7605/ICL7606 instrumentation amplifier is best illustrated by referring to Figure 2. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and

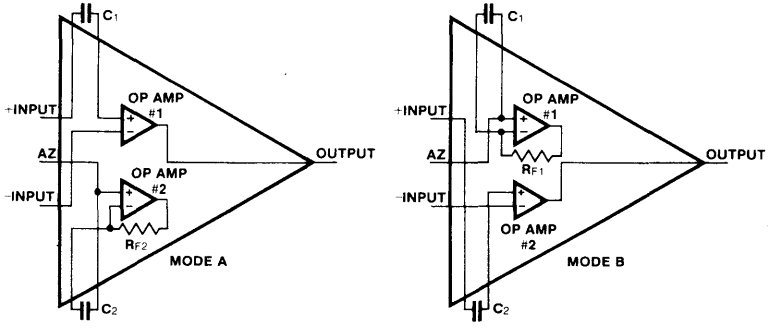


Figure 2: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

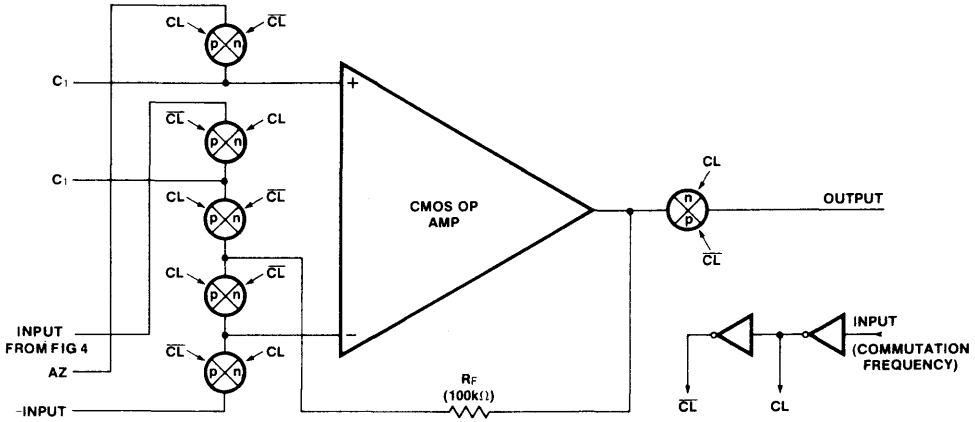


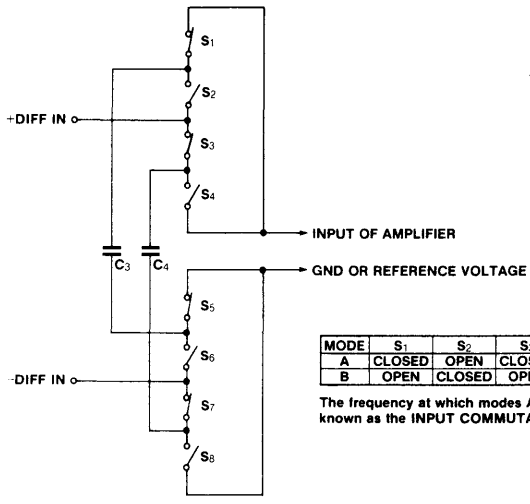
Figure 3: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. CMOS structure provides the CAZ amp with open-loop gains of greater than 100 dB, typical input offset voltages of ±5 mV, and ultra-low leakage currents, typically 1 pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 3. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of a voltage converter block is shown in Figure 4. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 5, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, commutation and noise voltages are added. Sampling theory states that to preserve the integrity of the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency of the signal being



MODE	S1	S2	S3	S4	S5	S6	S7	S8
A	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED

The frequency at which modes A & B are cycled is known as the INPUT COMMUTATION FREQUENCY

Figure 4: *Schematic of the differential to single ended voltage converter*

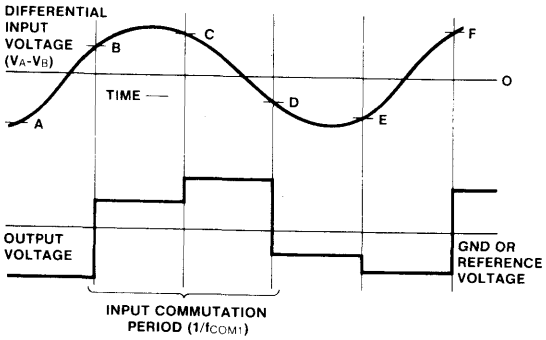


Figure 5: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is transferred to a lower frequency. This phenomenon is known as aliasing. Although the output responds above the commutation frequency, the frequencies of the output responses have been aliased down to frequencies below the commutation frequency.

The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_0 and C_0 must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is approximately 3 dB at 10 Hz.

APPLICATIONS

USING THE ICL7605/ICL7606 TO BUILD A DIGITAL READOUT TORQUE WRENCH

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting this voltage to a single-ended voltage reference to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter chip for LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of the A/D. In order to set the full-scale reading, it is required that, given a certain strain gauge bridge with a defined pressure voltage sensitivity, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2 mA. The accuracy is limited only by resistor ratios and the transducer.

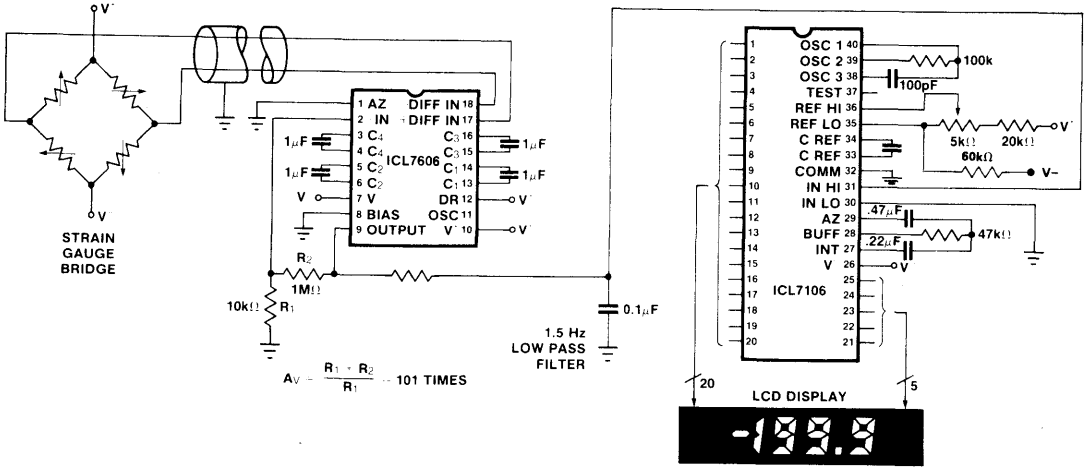


Figure 6: 3-1/2 Digit Digital Readout Torque Wrench

SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Test Circuits #1 and #2 provide convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5 Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be of a high-input impedance type—(not simply a capacitor across the feedback resistor R_2) at about 100kΩ and 1.0μF so that the output dynamic loading on the CAZ instrumentation is about 100kΩ.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606 instrumentation op amp. For this reason, the internal op amps have externally-programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^- for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of power supply versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20 dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output load of 100kΩ or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked, and that is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

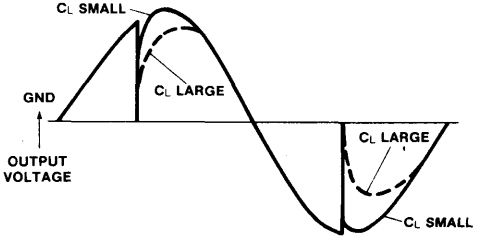
In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 7. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5 Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1 MΩ resistor and an 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160 Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2 kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 8) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar voltage supply. The



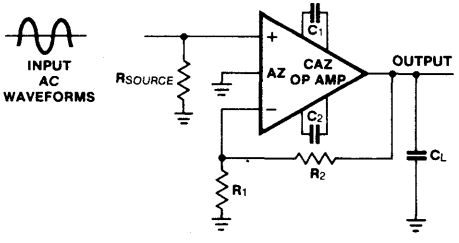


Figure 7: Effect of a load capacitor on output voltage waveforms.

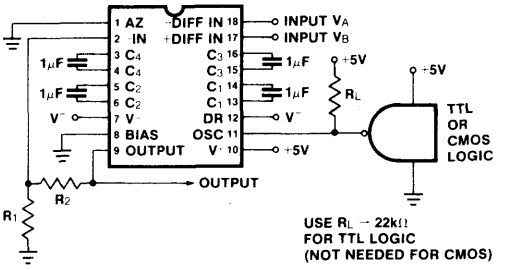


Figure 8: ICL7605 being clocked from external logic into the oscillator terminal.

reason for this requirement is that the logic section (including the oscillator) operates from an internal –5V supply, referenced to V^+ supply, which is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep well away from equipment which dissipates heat.

Component Selection

The four capacitors (C_1 thru C_4) should each be about 1.0μF. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene are the best for C_3 and C_4, though Mylar may be adequate for C_1 and C_2.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10 Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000 x 10 pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0 pA at an ambient temperature of 25°C.

The output waveform in Test Circuit #1 (with no input signal) is shown in Figure 9. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7 mV are not amplified by 1000.

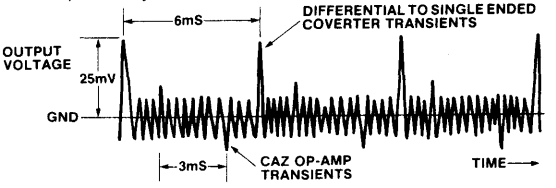


Figure 9: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board, particularly the capacitors C_1, C_2, C_3 and C_4, all of which must be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

ICL761X/ 762X/763X/764X Low Power CMOS™ Operational Amplifiers

FEATURES

- **Wide operating voltage range ±1.0V to ±8V**
- **High input impedance — $10^{12}\Omega$**
- **Programmable power consumption — as low as 20μW**
- **Input current lower than BIFETs — typ 1pA**
- **Available as singles, duals, triples, and quads**
- **Output voltage swing ranges to within millivolts of V⁻ to V+**
- **Low power replacement for many standard op amps**
- **Compensated and uncompensated versions**

APPLICATIONS

- **Portable instruments**
- **Telephone headsets**
- **Hearing aid/microphone amplifiers**
- **Meter amplifiers**
- **Medical instruments**
- **High impedance buffers**

A number of special options are available. They include:

- Single, dual, triple, and quad configurations
- Internally compensated and uncompensated versions
- Inputs protected to ±200V (ICL7613/15)
- Input common mode voltage range greater than supply rails (ICL7612)

Note: See page 2 for table of options.

SCHEMATIC

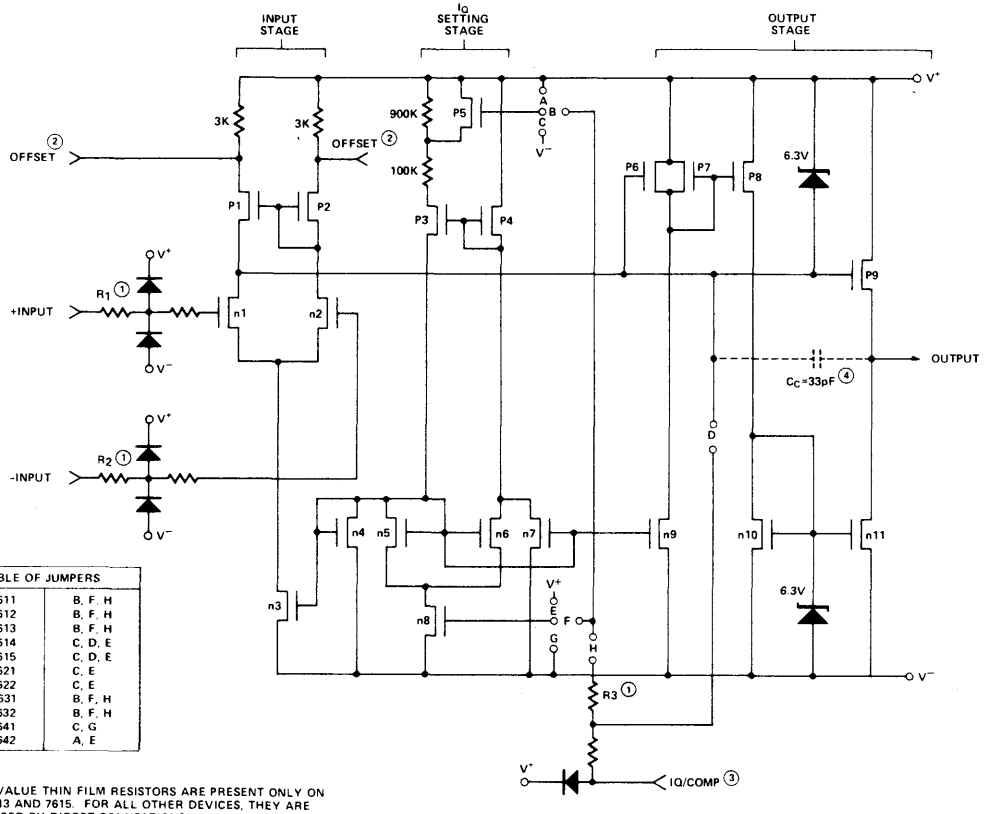


TABLE OF JUMPERS	
ICL7611	B, F, H
ICL7612	B, F, H
ICL7613	B, F, H
ICL7614	C, D, E
ICL7615	C, D, E
ICL7621	C, E
ICL7622	C, E
ICL7631	B, F, H
ICL7632	B, F, H
ICL7641	C, G
ICL7642	A, E

NOTES:
1. HIGH VALUE THIN FILM RESISTORS ARE PRESENT ONLY ON ICL7613 AND 7615. FOR ALL OTHER DEVICES, THEY ARE REPLACED BY DIRECT CONNECTIONS.
2. OFFSET NULLING PINS ARE NOT AVAILABLE ON TRIPLE (ICL763X) AND QUIAD (ICL764X) VERSIONS.
3. I_Q AND COMP TERMINALS ARE METAL MASK OPTIONS OF THE SAME BONDING PAD; ONLY ONE OF THESE FUNCTIONS IS AVAILABLE IN A GIVEN DEVICE.
4. FOR INTERNALLY COMPENSATED VERSIONS ONLY. THIS CAPACITOR IS ABSENT FOR ALL OTHER DEVICES.

GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS op amps. These amplifiers provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power drain are essential.

The basic amplifier will operate at supply voltages ranging from ±1.0V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1 mA, 100 μA, or 10 μA, with no external components. This results in power drain as low as 20 μW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1 pA) input current, input noise current of .01 pA/ √Hz, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

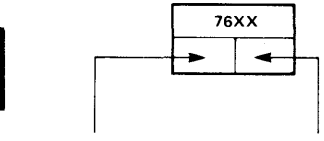
The inputs are internally protected and require no special handling procedures. Outputs are fully protected against shorts to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1 MHz at I_Q= 1 mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

SELECTION GUIDE

BASIC TYPE



OFFSET NULL CAPABILITY
Y = YES
N = NO

I_Q SETTING
L = 10μA FIXED
M = 100μA FIXED
H = 1mA FIXED
P = PROGRAMMABLE

ORDERING INFORMATION [2]

ICL76XX M N O P

V_{OS} SELECTION
A = 2mV
B = 5mV
C = 10mV
D = 15mV
E = 20mV

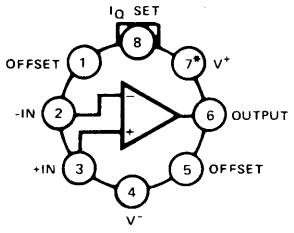
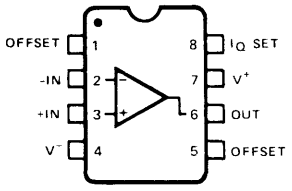
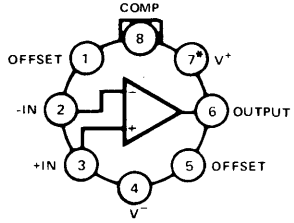
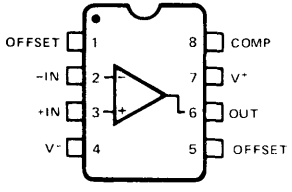
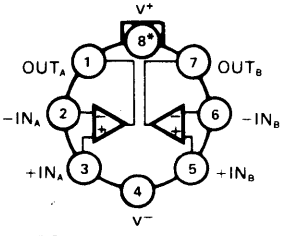
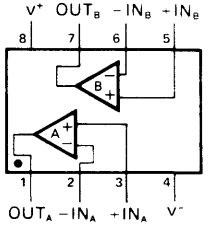
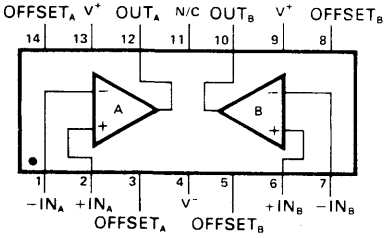
TEMP. RANGE
C = 0°C TO 70°C
M = -55°C TO +125°C

PACKAGE CODE
TV – TO-99, 8 PIN
PA – PLASTIC 8 PIN MINIDIP
PD – 14 PIN PLASTIC
PE – 16 PIN PLASTIC
JD – 14 PIN CERDIP
JE – 16 PIN CERDIP

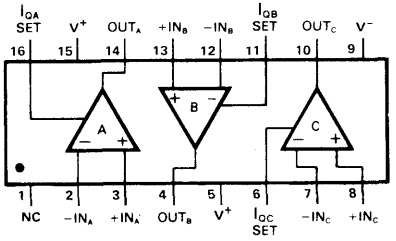
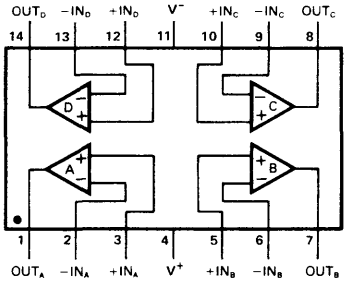
BASIC TYPE							ORDER SUFFIX							
							TO-99		MINI DIP	PLASTIC DIP[1]	CERAMIC DIP[1]		DIE	
	COMPENSATED	EXTERNALLY COMPENSATED	COMPENSATED/ INPUT PROTECTED	EXTERNALLY COMPENSATED INPUT PROTECTED	EXTENDED CMVR		0°C to +70°C	55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	55°C to +125°C	0°C to +70°C	55°C to +125°C
SINGLE	7611 Y P	7614 Y M	7613 Y P	7615 Y M	7612 Y P		ACTV BCTV DCTV	AMTV BMTV —	ACPA BCPA DCPA				DC/D	
DUAL 1458 PINOUT	7621 N M						ACTV BCTV DCTV	AMTV BMTV —	ACPA BCPA DCPA				DC/D	
DUAL 747 PINOUT	7622 Y M									ACPD BCPD DCPD	ACJD BCJD DCJD	AMJD BMJD —	DC/D	
TRIPLE	7631 N P	[3] 7632 N P								BCPE CCPE ECPE	BCJE CCJE ECJE	BMJE CMJE —	EC/D	
QUAD High I_Q	7641 N H									BCPD CCPD ECPD	BCJD CCJD ECPD	BMJD CMJD —	EC/D	
QUAD Low I_Q	7642 N L									BCPD CCPD ECPD	BCJD CCJD ECJD	BMJD CMJD —	EC/D	

NOTES: 1. Duals and quads are available in 14 pin DIP packages, triples in 16 pin only.
2. Ordering code must consist of basic device and order suffix, e.g., ICL7611BCPA.
3. ICL7632 is not compensatable. Recommended for use in high gain circuits only.

PIN CONFIGURATIONS

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7611XCPA ICL7611XCTV ICL7611XMTV ICL7612XCPA ICL7612XCTV ICL7612XMTV ICL7613XCPA ICL7613XCTV ICL7613XMTV	Internal compensation, plus offset null capability and external I_Q control.	**TO-99** (TOP VIEW) (outline dwg TV)  **8 PIN DIP** (TOP VIEW) (outline dwg PA)  *Pin 7 connected to case.
ICL7614XCPA ICL7614XCTV ICL7614XMTV ICL7615XCPA ICL7615XCTV ICL7615XMTV	Fixed I_Q (100μA), external compensation, and offset null capability.	**TO-99** (TOP VIEW) (outline dwg TV)  **8 PIN DIP** (TOP VIEW) (outline dwg PA)  * Pin 7 connected to case.
ICL7621XCPA ICL7621XCTV ICL7621XMTV	Dual op amps with internal compensation; I_Q fixed at 100μA Pin compatible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	**TO-99** (TOP VIEW) (outline dwg TV)  **8 PIN DIP** (TOP VIEW) (outline dwg PA)  * Pin 8 connected to case.
ICL7622XCPD	Dual op amps with internal compensation and offset null capability; I_Q fixed at 100μA Pin compatible with Texas Inst. TL083 Fairchild μA747	**14 PIN DIP** (TOP VIEW) (outline dwgs JD, PD)  Note: Pins 9 and 13 are internally connected.

PIN CONFIGURATIONS (Cont.)

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7631XCPE ICL7632XCPE	Triple op amps with internal compensation (ICL7631) and no compensation (ICL7632). Adjustable I_Q Same pin configuration as ICL8023.	16 PIN DIP (TOP VIEW) (outline dwgs JE, PE)  Note: Pins 5 and 15 are internally connected.
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at 10μA (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	14 PIN DIP (TOP VIEW) (outline dwg JD, PD) 

5

GENERAL INFORMATION

STATIC PROTECTION

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

LATCHUP AVOIDANCE

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. (An exception to this rule concerns the inputs of the ICL7613 and ICL7615, which are protected to ±200V.) In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2 mA to prevent latchup.

CHOOSING THE PROPER I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10 μA, 100 μA or 1 mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12/13 and ICL7631/32 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The ICL7614/15, 7621/22, and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

I_Q = 10μA — I_Q pin to V^+

I_Q = 100μA — I_Q pin to ground. If this is not possible, any voltage from V^+ -0.8 to V^- +0.8 can be used.

I_Q = 1mA — I_Q pin to V^-

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p ouput voltage swings into low impedance loads, I_Q of 1 mA should be selected.

OUTPUT STAGE AND LOAD DRIVING CONSIDERATIONS

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1M, 100K, and 10K, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB, which can supply

higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10K, 100K, and 1M are used.

INPUT OFFSET NULLING

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1 mA and 100 μA, the nulling range provided is adequate for all V_{OS} selections; however with $I_Q = 10\ \mu A$, nulling may not be possible with higher values of V_{OS}.

FREQUENCY COMPENSATION

The ICL7611/12/13, 7621/22, 7631, 7641/42 are internally compensated, and are stable for closed loop gains as low as unity for capacitive loads up to 100pF

The ICL7614 and 15 are externally compensated by connecting a capacitor between the COMP and OUT pins. A 39pF capacitor is required for unity gain compensation; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor.

Since the g_m of the first stage is proportional to $\sqrt{I_Q}$, greatest compensation is required when $I_Q = 1$mA. The ICL7632 is not compensated internally, nor can it be compensated externally. The device is stable when used as follows:

I_Q of 1 mA for gains ≥ 20
I_Q of 100 μA for gains ≥ 10
I_Q of 10 μA for gains ≥ 5

HIGH VOLTAGE INPUT PROTECTION

The ICL7613 and 7615 include on-chip thin film resisitors and clamping diodes which allow voltages of up to ± 200 to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages, or high transients may be experienced. Such conditions may be found when interfacing separate systems with separate supplies. Unity gain stability is somewhat degraded with capacitive loads because of the high value of input resistors.

EXTENDED COMMON MODE INPUT RANGE

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$, the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for $V_{SUPP} = \pm 1.0V$, the input CMVR would be + 0.6 volts to -1.1 volts).

OPERATION AT $V_{SUPP} = \pm 1.0$ VOLTS

Operation at $V_{SUPP} = \pm 1.0V$ is guaranteed at $I_Q = 10\mu A$ only. This applies to these devices with selectable I_Q, and those devices are set internally to $I_Q = 10\mu A$ (i.e., ICL7611 , 7612, 7613, 7631, 7632, 7642).

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1$ MegΩ. Guaranteed input CMVR is $\pm 0.6V$ minimum and typically +0.9V to -0.7 at $V_{SUPP} = \pm 1.0V$. For applications where greater common mode range is desirable, refer to description of ICL7612 above.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

ABSOLUTE MAXIMUM RATINGS [1]

Total Supply Voltage V^+ to V^- 18V
Input Voltage ..... $V^+ + 0.3$ to $V^- - 0.3V$
Input Voltage ICL7613/15 Only .... $V^+ + 200$ to $V^- - 200V$
Differential Input Voltage [2] ... $\pm (V^+ + 0.3 - (V^- - 0.3))V$
Differential Input Voltage [2]
ICL7613/15 Only ..... $\pm (V^+ + 200 - (V^- - 200))V$
Duration of Output Short Circuit [3] ..... Unlimited

Continuous Power Dissipation @ 25°C		Above 25°C derate as follows:
TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range
M Series ..... -55°C to +125°C
C Series ..... 0°C to +70°C
Lead Temperature Soldering, 10 sec ..... 300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

INTERSIL

ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm5.0V$, $T_A = 25°C$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			2 3			5 7			15 20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		10			15			25		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$ [2] $\Delta T_A=M$ [2]		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	$I_Q=10\mu A$ [1] $I_Q=100\mu A$ $I_Q=1mA$ [1]	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	$I_Q=10\mu A$	±5.3			±5.3			±5.3			V
		$I_Q=100\mu A$	+5.3 -5.1			+5.3 -5.1			+5.3 -5.1			
		$I_Q=1mA$	+5.3 -4.5			+5.3 -4.5			+5.3 -4.5			
Output Voltage Swing	V_{OUT}	(1) $I_Q = 10\mu A$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	± 4.9 ± 4.8 ± 4.7			± 4.9 ± 4.8 ± 4.7			± 4.9 ± 4.8 ± 4.7			V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	± 4.9 ± 4.8 ± 4.5			± 4.9 ± 4.8 ± 4.5			± 4.9 ± 4.8 ± 4.5			
		(1) $I_Q = 1mA$, $R_L = 10k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	± 4.5 ± 4.3 ± 4.0			± 4.5 ± 4.3 ± 4.0			± 4.5 ± 4.3 ± 4.0			
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm4.0V$, $R_L=1M\Omega$ $I_Q=10\mu A$ [1], $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$	86 80 74	104		80 75 68	104		80 75 68	104		dB
		$V_O=\pm4.0V$, $R_L=100k\Omega$ $I_Q=100\mu A$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$	86 80 74	102		80 75 68	102		80 75 68	102		
		$V_O=\pm4.0V$, $R_L=10k\Omega$ $I_Q=1mA$ [1], $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$	80 76 72	83		76 72 68	83		76 72 68	83		
Unity Gain Bandwidth	G_{BW}	$I_Q=10\mu A$ [1] $I_Q=100\mu A$ $I_Q=1mA$ [1]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$, $I_Q=10\mu A$ [1] $R_S \le 100K\Omega$, $I_Q=100\mu A$ $R_S \le 100K\Omega$, $I_Q=1mA$ [1]	76 76 66	96 91 87		70 70 60	96 91 87		70 70 60	96 91 87		dB
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$, $I_Q=10\mu A$ [1] $R_S \le 100K\Omega$, $I_Q=100\mu A$ $R_S \le 100K\Omega$, $I_Q=1mA$ [1]	80 80 70	94 86 77		80 80 70	94 86 77		80 80 70	94 86 77		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load $I_Q=10\mu A$ [1] $I_Q=100\mu A$ $I_Q=1mA$ [1]		0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL}=100$		120			120			120		dB
Slew Rate [3]	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN} = 8V_{p-p}$ $I_Q=10\mu A$ [1], $R_L=1M\Omega$ $I_Q=100\mu A$, $R_L=100K\Omega$ $I_Q=1mA$ [1], $R_L=10K\Omega$		0.016 0.16 1.6			0.016 0.16 1.6			0.016 0.16 1.6		V/μs
Rise Time [3]	t_r	$V_{IN}=50mV$, $C_L=100pF$ $I_Q=10\mu A$ [1], $R_L=1M\Omega$ $I_Q=100\mu A$, $R_L=100K\Omega$ $I_Q=1mA$ [1], $R_L=10K\Omega$		20 2 0.9			20 2 0.9			20 2 0.9		μs
Overshoot Factor [3]		$V_{IN}=50mV$, $C_L=100pF$ $I_Q=10\mu A$ [1], $R_L=1M\Omega$ $I_Q=100\mu A$, $R_L=100K\Omega$ $I_Q=1mA$ [1], $R_L=10K\Omega$		5 10 40			5 10 40			5 10 40		%

Note: 1. ICL7611, 7612, 7613 only.
2. C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C
3. ICL7614/15; 39pF from pin 6 to pin 8

ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified. Specs apply to ICL7611/7612/7613 only.

PARAMETER	SYMBOL	CONDITIONS	76XXA			76XXB			UNITS
			MIN.	TYP.	MAX.	MIN	TYP.	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100K\Omega$, $T_A=25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100K\Omega$		10			15		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ ΔT_A=C		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ ΔT_A=C		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		±0 .6			±0 .6			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		+0.6 to -1.1			+0.6 to -1.1			V
Output Voltage Swing	V_{OUT}	$R_L=1M\Omega$, $T_A=25°C$ ΔT_A=C		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm 0.1V$, $R_L=1M\Omega$ $T_A=25°C$ ΔT_A=C		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100K\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 100K\Omega$		80			80		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Slew Rate	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN}=0.2Vp\text{-}p$ $R_L=1M\Omega$		0.016			0.016		$V/\mu s$
Rise Time	t_r	$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		5			5		%

Note: C = Commercial Temperature Range (0°C to +70°C); M = Military Temperature Range (-55°C to +125°C).

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ELECTRICAL CHARACTERISTICS V_{SUPP}= ±5.0V, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, T_A=25°C $T_{MIN} \le T_A \le T_{MAX}$			5 7			10 15			20 25	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		15			20			30		µV/°C
Input Offset Current	I_{OS}	T_A=25°C ΔT_A=C ΔT_A=M		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	T_A=25°C ΔT_A=C ΔT_A=M		1.0	50 500 4000		1.0	50 500 4000		1.0	50 500 4000	pA
Common Mode Voltage Range	V_{CMR}	I_Q=10µA [1] I_Q=100µA [3] I_Q=1mA [2]	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
Output Voltage Swing	V_{OUT}	(1) I_Q = 10µA, R_L = 1MΩ T_A = 25°C ΔT_A = C ΔT_A = M	± 4.9 ± 4.8 ± 4.7			± 4.9 ± 4.8 ± 4.7			± 4.9 ± 4.8 ± 4.7			V
		I_Q = 100µA, R_L = 100kΩ (3) T_A = 25°C ΔT_A = C ΔT_A = M	± 4.9 ± 4.8 ± 4.5			± 4.9 ± 4.8 ± 4.5			± 4.9 ± 4.8 ± 4.5			
		(2) I_Q = 1mA, R_L = 10kΩ T_A = 25°C ΔT_A = C ΔT_A = M	± 4.5 ± 4.3 ± 4.0			± 4.5 ± 4.3 ± 4.0			± 4.5 ± 4.3 ± 4.0			
Large Signal Voltage Gain	A_{VOL}	V_O=±4.0V, R_L=1MΩ [1] I_Q=10µA [1], T_A=25°C ΔT_A=C ΔT_A=M	86 80 74	104		80 75 68	104		80 75 68	104		dB
		V_O=±4.0V, R_L=100kΩ [3] I_Q=100µA, T_A=25°C ΔT_A=C ΔT_A=M	86 80 74	102		80 75 68	102		80 75 68	102		
		V_O=±4.0V, R_L=10kΩ [2] I_Q=1mA [1], T_A=25°C ΔT_A=C ΔT_A=M	86 80 74	98		80 75 68	98		80 75 68	98		
Unity Gain Bandwidth	G_{BW}	I_Q=10µA [1] I_Q=100µA [3] I_Q=1mA [2]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$, I_Q=10µA [1] $R_S \le 100K\Omega$, I_Q=100µA $R_S \le 100K\Omega$, I_Q=1mA [2]	76 76 66	96 91 87		70 70 60	96 91 87		70 70 60	96 91 87		dB
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$, I_Q=10µA [1] $R_S \le 100K\Omega$, I_Q=100µA $R_S \le 100K\Omega$, I_Q=1mA [2]	80 80 70	94 86 77		80 80 70	94 86 77		80 80 70	94 86 77		dB
Input Referred Noise Voltage	e_n	R_S=100Ω, f=1KHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	R_S=100Ω, f=1KHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current Per Amplifier	I_{SUPP}	No Signal, No Load I_Q=10µA [1] I_Q=100µA I_Q=1mA [2]		0.01 0.1 1.0	0.022 0.25 2.5		0.01 0.1 1.0	0.022 0.25 2.5		0.01 0.1 1.0	0.022 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_{VOL}=100		120			120			120		dB
Slew Rate [4]	SR	A_{VOL}=1, C_L=100pF, V_{IN} = 8V_{p-p} I_Q=10µA [1], R_L=1MΩ I_Q=100µA, R_L=100KΩ I_Q=1mA [1], R_L=10KΩ [2]		0.016 0.16 1.6			0.016 0.16 1.6			0.016 0.16 1.6		V/µs
Rise Time [4]	t_r	V_{IN}=50mV, C_L=100pF I_Q=10µA [1], R_L=1MΩ I_Q=100µA, R_L=100KΩ I_Q=1mA [2], R_L=10KΩ		20 2 0.9			20 2 0.9			20 2 0.9		µs
Overshoot Factor [4]		V_{IN}=50mV, C_L=100pF I_Q=10µA [1], R_L=1MΩ I_Q=100µA, R_L=100KΩ I_Q=1mA [2], R_L=10KΩ		5 10 40			5 10 40			5 10 40		%

Note: 1. Does not apply to 7641.
2. Does not apply to 7642.
C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C
3. ICL7631/32 only.
4. Does not apply to 7632.

ELECTRICAL CHARACTERISTICS V_{SUPP} = ±1.0V, I_Q = 10μA, T_A = 25°C, unless otherwise specified. Specs apply to ICL7631/7632/7642 only.

PARAMETER	SYMBOL	CONDITIONS	76XXB			76XXC			UNITS
			MIN.	TYP.	MAX.	MIN	TYP.	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100K\Omega$, T_A=25°C $T_{MIN} \leq T_A \leq T_{MAX}$			5 7			10 12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100K\Omega$		15			20		μV/°C
Input Offset Current	I_{OS}	T_A=25°C ΔT_A=C		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	T_A=25°C ΔT_A=C		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range	V_{CMR}		±0 .6			±0 .6			V
Output Voltage Swing	V_{OUT}	R_L=1MΩ, T_A=25°C ΔT_A=C		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	V_O=±0.1V, R_L=1MΩ T_A=25°C ΔT_A=C		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100K\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR			80			80		dB
Input Referred Noise Voltage	e_n	R_S=100Ω, f=1KHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	R_S=100Ω, f=1KHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Channel Separation	$V_{O1/VO2}$	A_{VOL}=100		120			120		dB
Slew Rate	SR	A_{VOL}=1, C_L=100pF, V_{IN}=0.2Vp-p R_L=1MΩ		0.016			0.016		V/μs
Rise Time	t_r	V_{IN}=50mV, C_L=100pF R_L=1MΩ		20			20		μs
Overshoot Factor		V_{IN}=50mV, C_L=100pF R_L=1MΩ		5			5		%

Note: C = Commercial Temperature Range (0°C to +70°C)

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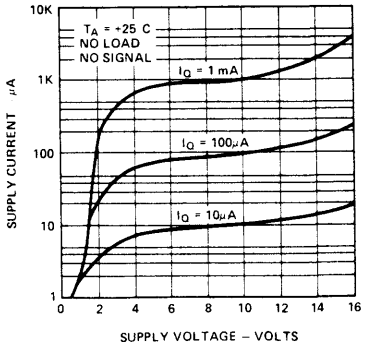
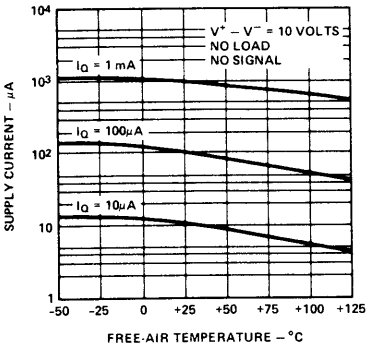
INTERSIL

TYPICAL PERFORMANCE CHARACTERISTICS

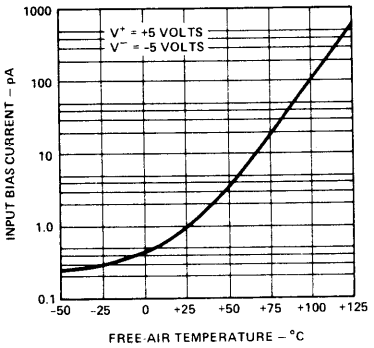
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



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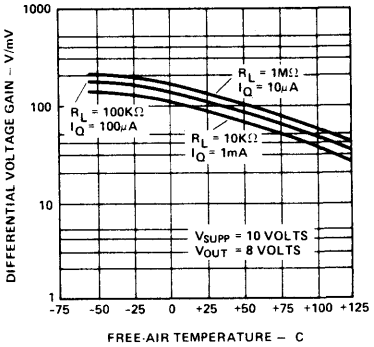
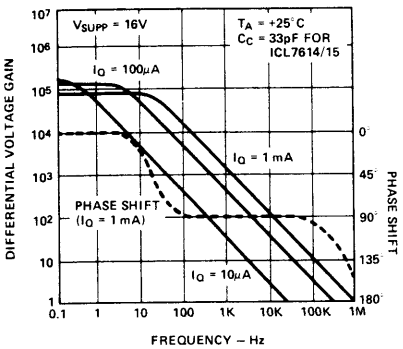
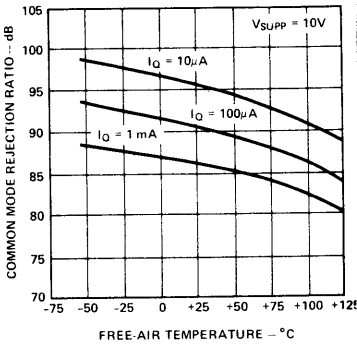
LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE



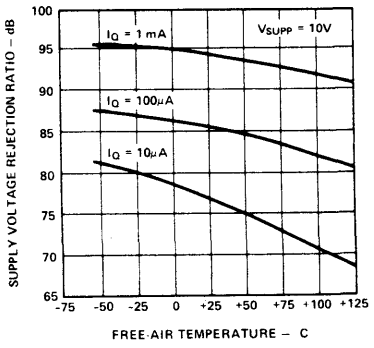
LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY



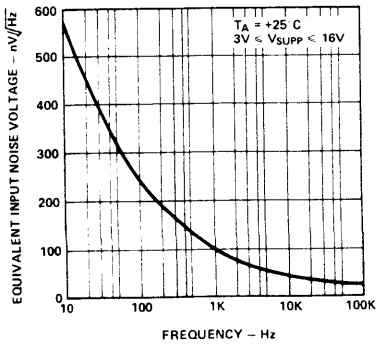
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



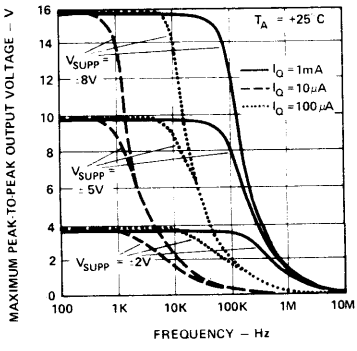
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

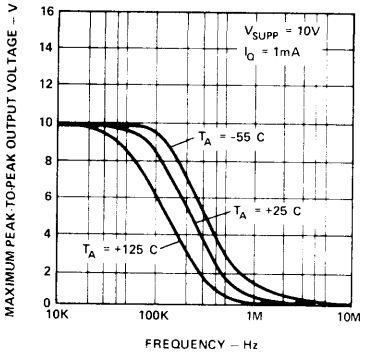


PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

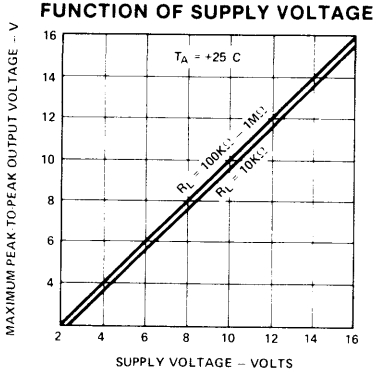


TYPICAL PERFORMANCE CHARACTERISTICS

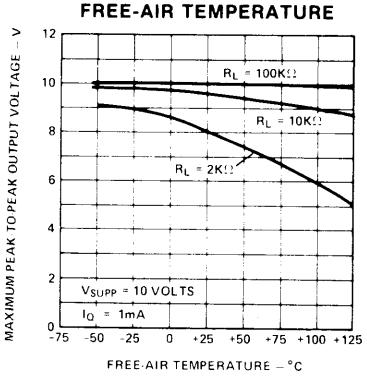
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



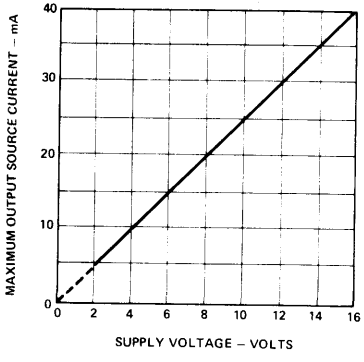
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



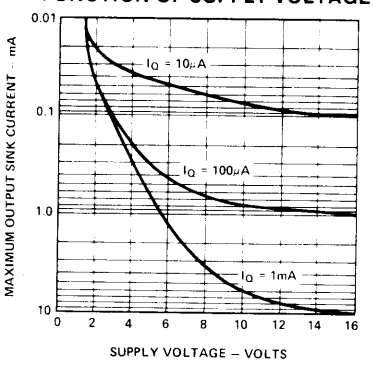
MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



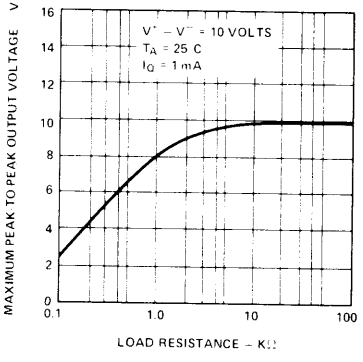
MAXIMUM OUTPUT/SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



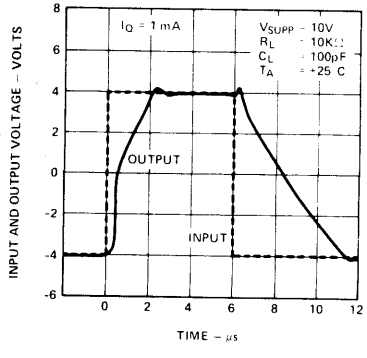
MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



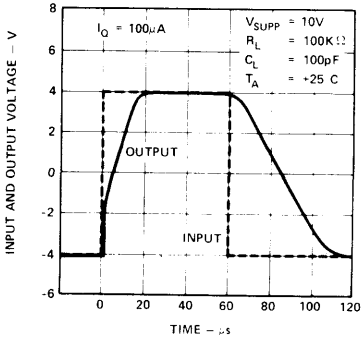
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



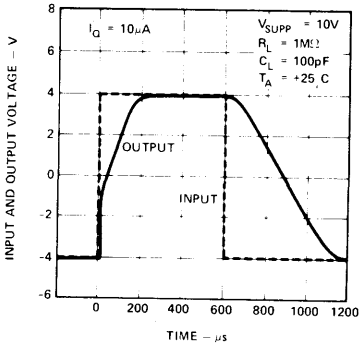
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



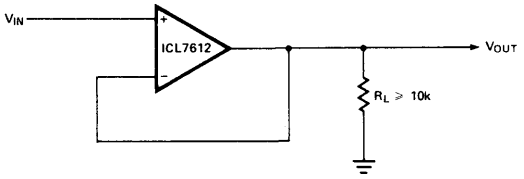
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



APPLICATIONS

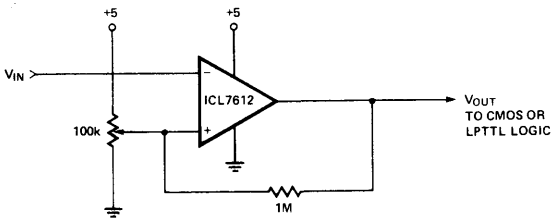
Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

SIMPLE FOLLOWER*



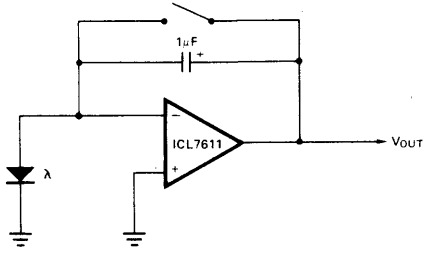
LEVEL DETECTOR*

*By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.



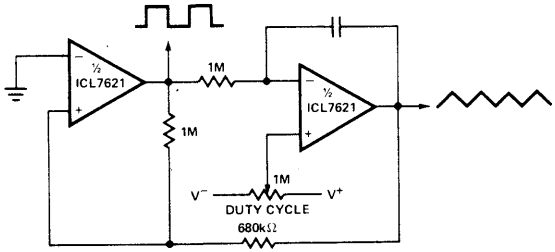
PHOTOCURRENT INTEGRATOR

Low leakage currents allow integration times up to several hours.



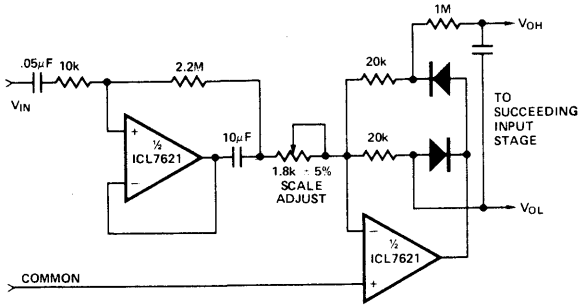
PRECISE TRIANGLE/SQUARE WAVE GENERATOR

Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.



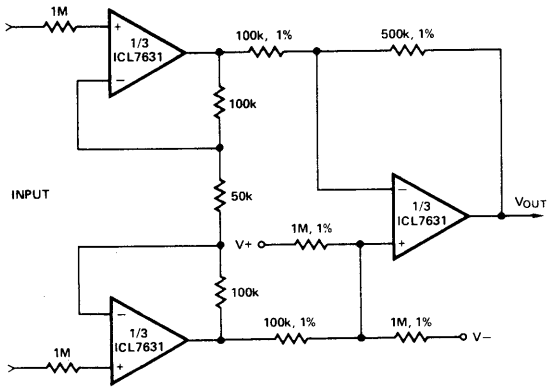
WAVEFORM GENERATOR

AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, 7107, 7109, 7116, 7117.



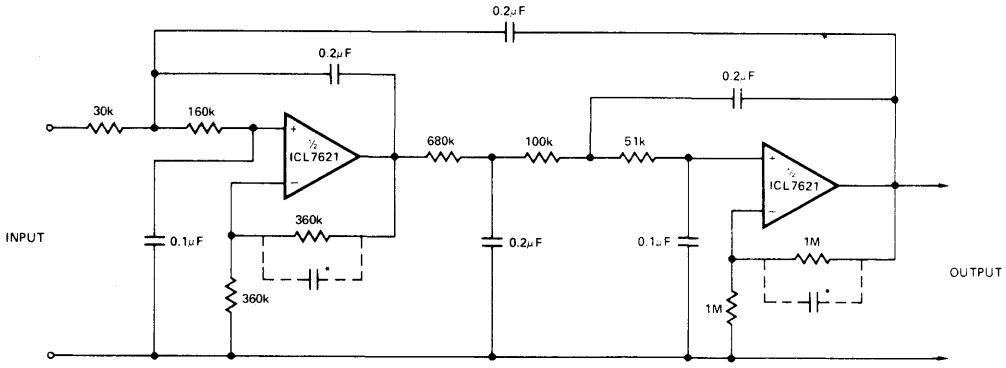
MEDICAL INSTRUMENT PREAMP

Note that A_{VOL} = 25; single Ni-cad battery operation. Input current (from sensors connected to patient) limited to < 5μA under fault conditions.



FIFTH ORDER CHEBYSHEV MULTIPLE FEEDBACK LOW PASS FILTER

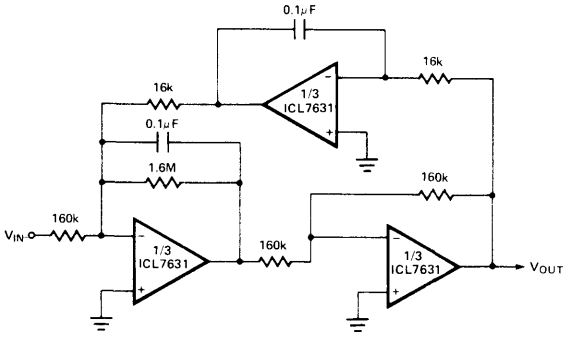
The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. $f_C = 10Hz$, $A_{VOL} = 4$, Passband ripple = 0.1 dB.



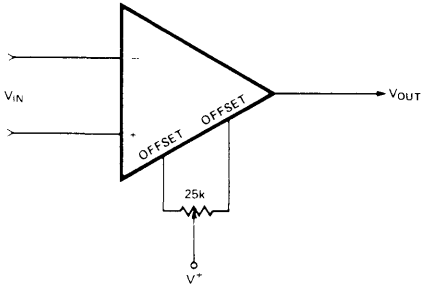
*Note that small capacitors (25-50pF) may be needed for stability in some cases.

SECOND ORDER BIQUAD BANDPASS FILTER

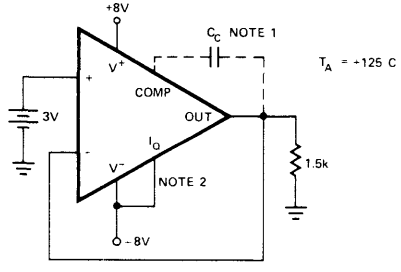
Note that I_Q on each amplifier may be different.
$A_{VOL} = 10$, $Q = 100$, $f_o = 100Hz$.



VOS NULL CIRCUIT

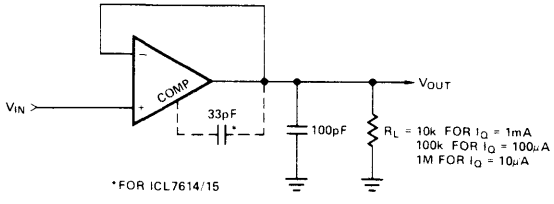


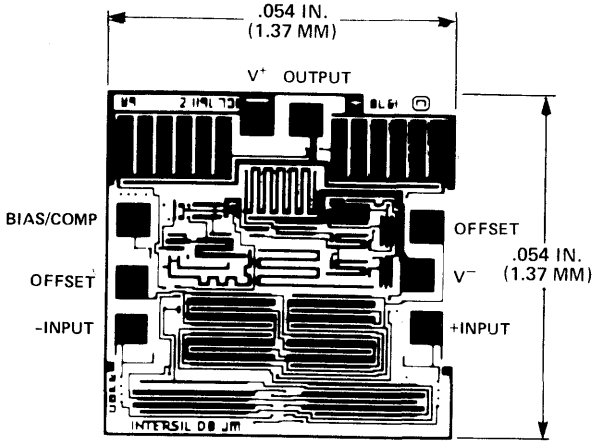
BURN—IN AND LIFE TEST CIRCUIT



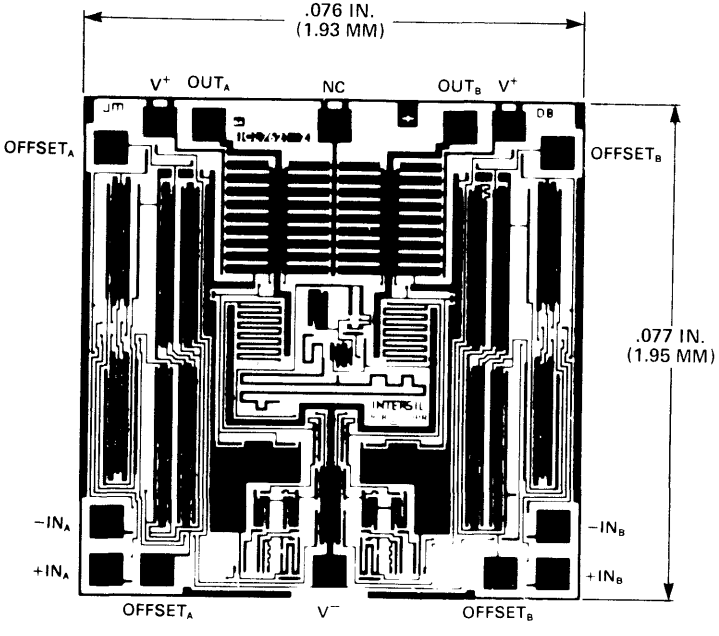
NOTES:
1. FOR DEVICES WITH EXTERNAL COMPENSATION, USE 33pF.
2. FOR DEVICES WITH PROGRAMMABLE STANDBY CURRENT, CONNECT I_Q PIN TO V^- (I_Q = 1mA MODE).

UNITY GAIN FREQUENCY COMPENSATION



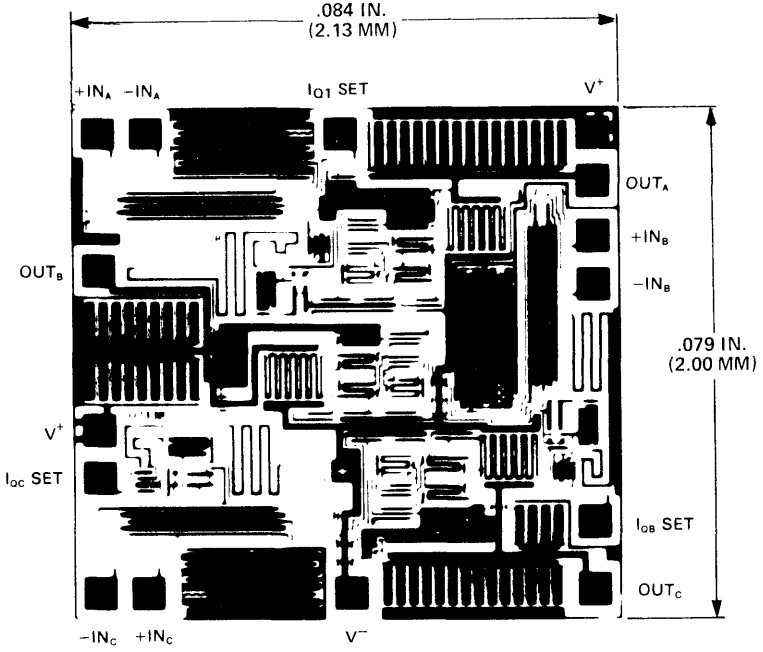

.054 IN.
(1.37 MM)
V+ OUTPUT
BIAS/COMP
OFFSET
-INPUT
OFFSET
V−
+INPUT
.054 IN.
(1.37 MM)
INTERSIL DB JM

761X

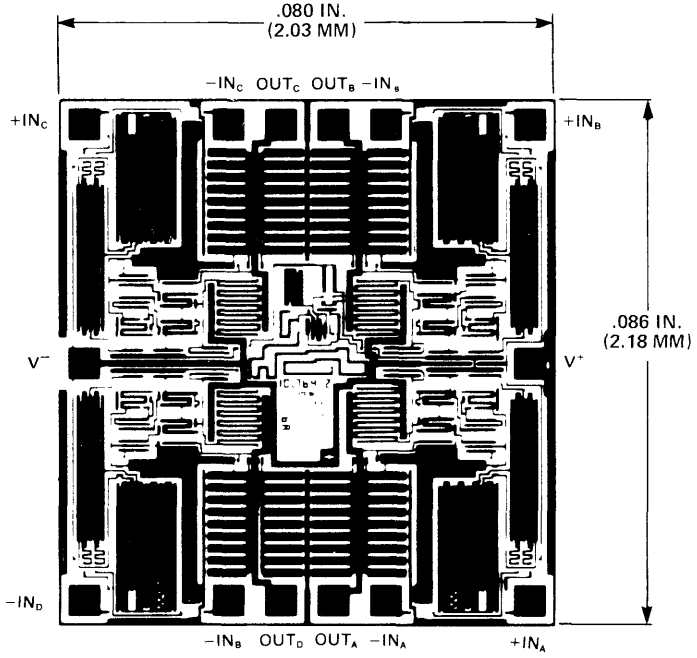

.076 IN.
(1.93 MM)
V+ OUTA
NC
OUTB V+
OFFSETA
OFFSETB
.077 IN.
(1.95 MM)
−INA
+INA
−INB
+INB
OFFSETA
V−
OFFSETB

762X

CHIP TOPOGRAPHY (Cont.)



763X



764X

ICL7650
Chopper Stabilized Operational Amplifier

FEATURES

- **Extremely low input offset voltage – 1μV over temperature range**
- **Low long-term and temperature drifts of input offset voltage**
- **Low DC input bias current – 10pA**
- **Extremely high gain, CMRR and PSRR – min 120dB**
- **High slew rate – 2.5V/μs**
- **Wide bandwidth – 2MHz**
- **Internally compensated for unity-gain operation**
- **Very low intermodulation effects (open loop phase shift < 10° @ chopper frequency)**
- **Clamp circuit to avoid overload recovery problems and allow comparator use**
- **Extremely low chopping spikes at input and output**

5

GENERAL DESCRIPTION

The ICL7650 chopper-stabilized amplifier is a high-performance device which offers exceptionally low offset voltage and input-bias parameters, combined with excellent bandwidth and speed characteristics. Intersil's unique CMOS approach to chopper-stabilized amplifier design yields a versatile precision component which can replace more expensive hybrid or modular parts, while at the same time out-performing them and other monolithic devices.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650 is internally compensated for unity-gain operation.

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICL 7650 CPA	0° - 70°C	8-Pin Plastic
ICL 7650 CPD	0° - 70°C	14-Pin Plastic
ICL 7650 CTV	0° - 70°C	8-Pin TO-99
ICL 7650 IJA	– 20°C - 85°C	8-Pin Cerdip
ICL 7650 IJD	– 20°C - 85°C	14-Pin Cerdip
ICL 7650 ITV	– 20°C - 85°C	8-Pin TO-99
ICL 7650 MJD	– 55°C - 125°C	14-Pin Cerdip
ICL 7650 MTV	– 55°C - 125°C	8-Pin TO-99
ICL 7650 CPA-1	0° - 70°C	8-Pin Plastic
ICL 7650 CTV-1	0° - 70°C	8-Pin TO-99
ICL 7650 IJD-1	– 20°C - 85°C	8-Pin Cerdip
ICL 7650 ITV-1	– 20°C - 85°C	8-Pin TO-99
ICL 7650 MTV-1	– 55°C - 125°C	8-Pin TO-99

NOTE: By using the ICL 7650-1 versions and connecting C_{RETN}, better noise performance can be attained.

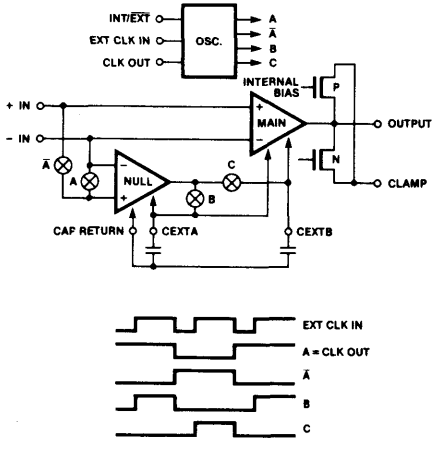
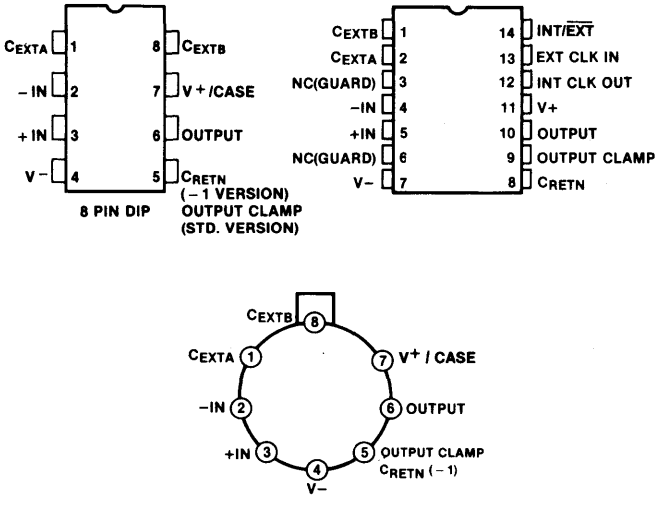


FIG. 1 BLOCK DIAGRAM

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... 18 Volts
Input Voltage ..... ($V^+ + 0.3$) to ($V^- - 0.3$) Volts
Storage Temp. Range ..... −55°C to 150°C
Operating Temp. Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on oscillator control pins ..... V^+ to V^-
except EXT CLOCK IN: .($V^+ + 0.3$) to ($V^+ - 6.0$) Volts
Duration of Output short circuit ..... Indefinite
Current into any pin 10mA
— while operating (Note 4) ..... 100 μA

Cont. Total Power Dissipn (T_A =25°C)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW
TO-99 ..... 250 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

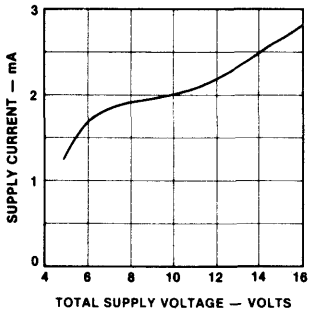
OPERATING CHARACTERISTICS: Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, Test Ckt (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	LIMITS TYP.	MAX.	UNIT
Input Offset Voltage	V_{OS}	$T_A = +25°C$ $-55°C < T_A < +85°C$ $-55°C < T_A < +125°C$		±0.7 ±1.0	±5 5.0	μV
Average Temp. Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	$-20°C < T_A < +85°C$		0.01 50	0.05	μV/°C
Input Bias Current (doubles every 10°C)	I_{BIAS}	$T_A = +25°C$ $0°C < T_A < +70°C$ $-20°C < T_A < +85°C$		1.5 35 100	10	pA
Input Offset Current	I_{OS}	$T_A = 25°C$		0.5		pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	$R_L = 10kΩ$	$1x10^6$	$5x10^6$		V/V
Output Voltage Swing (Note 3)	V_{OUT}	$R_L = 10kΩ$ $R_L = 100kΩ$	±4.7	±4.85 ±4.95		V
Common Mode Voltage Range	CMVR		−5.0	−5.2 to +2.0	1.6	V
Common Mode Rejection Ratio	CMRR	CMVR = −5V to +1.6	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	120	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	$R_S = 100Ω$ 0 to 10Hz		2		μVp-p
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	$C_L = 50pF$, $R_L = 10kΩ$		2.5		V/μs
Rise Time	t_r			0.2		μs
Overshoot				20		%
Operating Supply Range	V+ to V−		4.5		16	V
Supply Current	I_{SUPP}	no load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	pins 12-14 open (DIP)	120	200	375	Hz
Clamp ON Current (note 2)		$R_L = 100kΩ$	25	70	200	μA
Clamp OFF Current (note 2)		$-4.0V < V_{OUT} < +4.0V$		1		pA
Offset Voltage vs Time				100		nV/√month

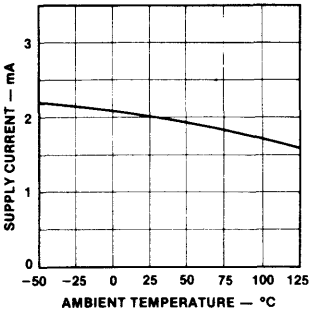
NOTE 1: Operating temperature range for M series parts is −55°C to +125°C, for I series is −20°C to +85°C, for C series is 0°C to +70°C
NOTE 2: See *OUTPUT CLAMP under detailed description.*
NOTE 3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
NOTE 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
NOTE 5: $I_{OS} = 2 \bullet I_{BIAS}$

TYPICAL OPERATING CHARACTERISTICS

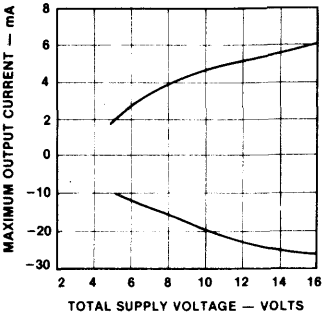
SUPPLY CURRENT vs. SUPPLY VOLTAGE



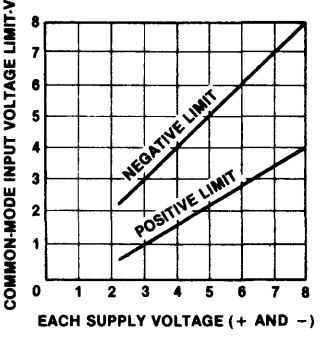
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



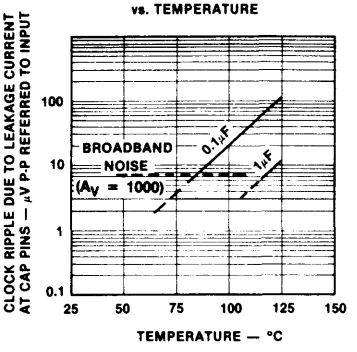
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



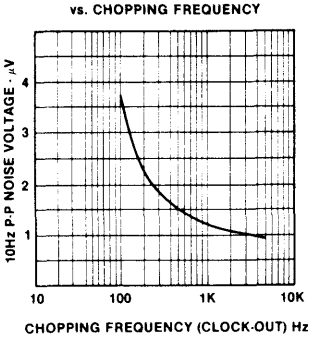
COMMON-MODE INPUT-VOLTAGE RANGE vs SUPPLY VOLTAGE



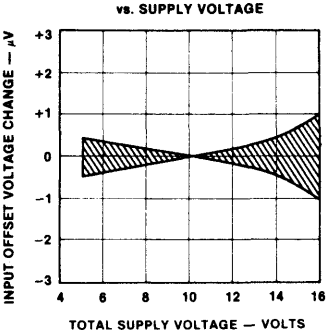
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



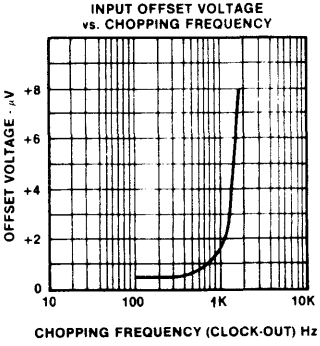
10Hz P-P NOISE VOLTAGE vs. CHOPPING FREQUENCY



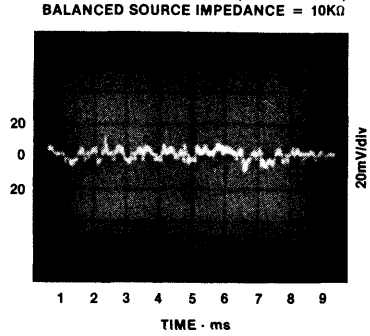
INPUT OFFSET VOLTAGE CHANGE vs. SUPPLY VOLTAGE



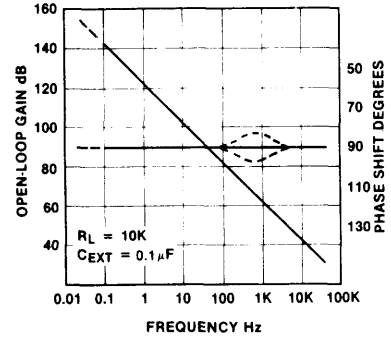
INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



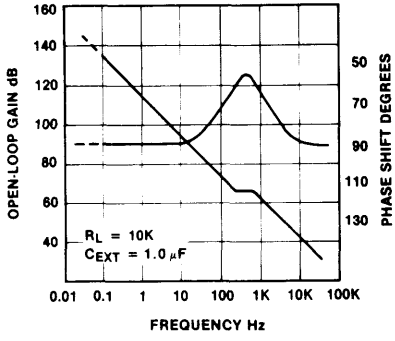
OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10KΩ



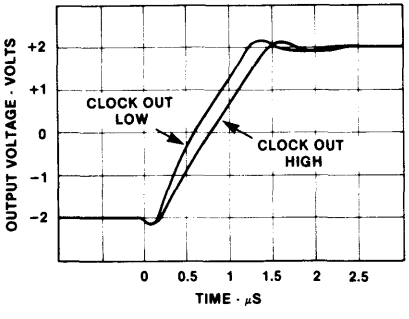
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



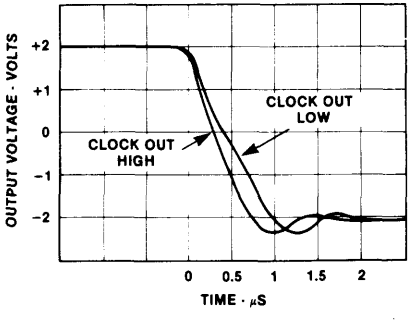
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE *

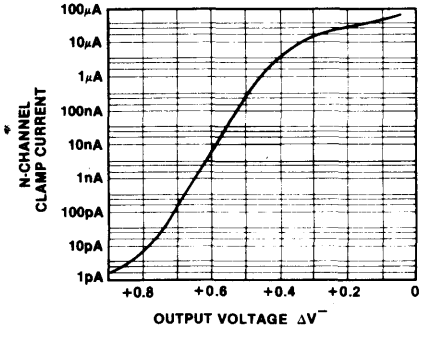


VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE *

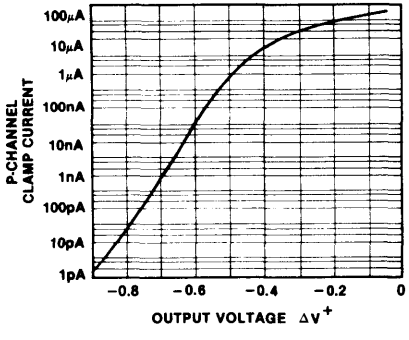


* THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

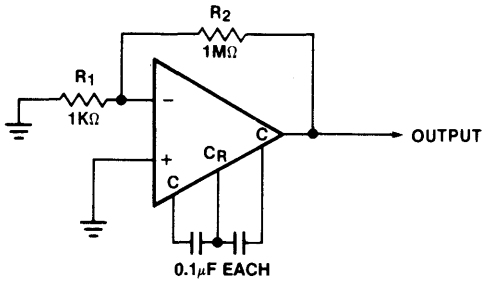
N-CHANNEL CLAMP CURRENT
vs. OUTPUT VOLTAGE



P-CHANNEL CLAMP CURRENT
vs. OUTPUT VOLTAGE



TEST CIRCUIT



DETAILED DESCRIPTION

AMPLIFIER

The block diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output, while the nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET back gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

INTERMODULATION

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are sustantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

CAPACITOR CONNECTION

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (in the case of 14-pin devices) or the V^- pin (in the case of the 8-pin devices). This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} (or V^-).

OUTPUT CLAMP

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

CLOCK

The ICL7650 has an internal oscillator giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies, the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50-80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V^+ and GROUND for power supplies up to ±6V, and between V^+ and V^+ −6V for higher supply voltages. Note that a signal of about 400Hz will be present at the EXT CLK IN pin with INT/$\overline{EXT}$ high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

COMPONENT SELECTION

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorbtion capacitors (such as poly propylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

STATIC PROTECTION

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

LATCH-UP AVOIDANCE

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

OUTPUT STAGE/LOAD DRIVING

The output circuit is a high-impedance stage (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1KΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10K or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

THERMO-ELECTRIC EFFECTS

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

GUARDING

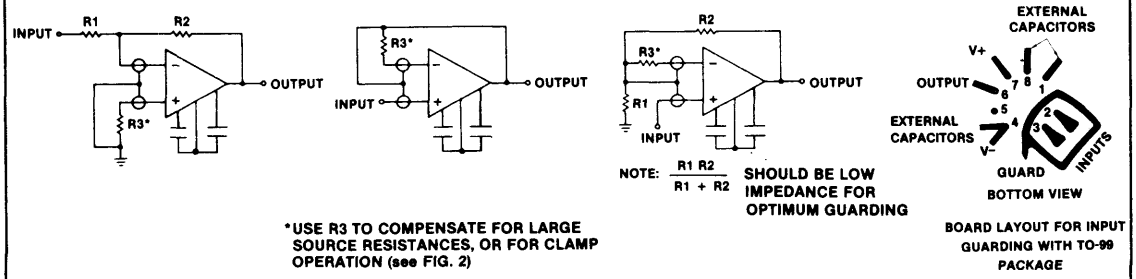
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

5

CONNECTION OF INPUT GUARDS



PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to V−, will provide easy compatibility. As for the LM108, replacement the compensation capacitor between pins 1 and 8 by the two capacitors to V− is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7650.

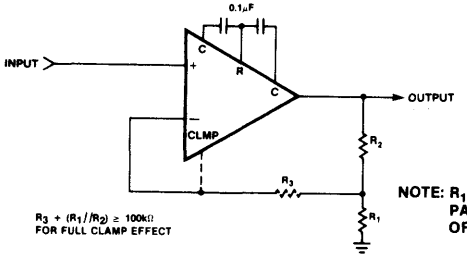
TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op. amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figs. 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op. amps by the ICL7650 are the supply voltage (± 8V max.) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Fig. 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

Fig. 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ≈ V_{IN}/R without disturbing other portions of the system.

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Fig. 6. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps. to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

Mixing the ICL7650 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be met fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit 'backwards'. A suitable connection is shown in Fig. 7.



NOTE: $R_1//R_2$ INDICATES THE PARALLEL COMBINATION OF R_1 AND R_2

FIG. 2 NON INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

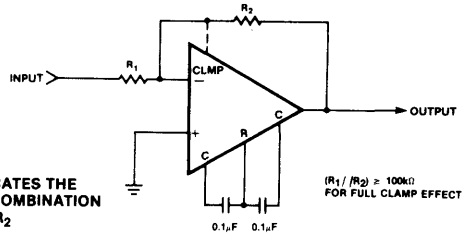


FIG. 3 INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

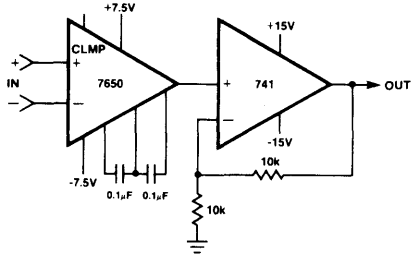


FIG. 4 USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

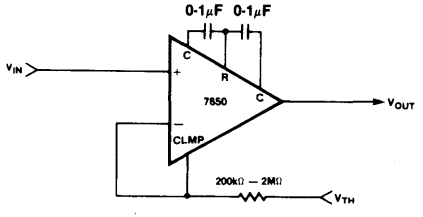


FIG. 5 LOW OFFSET COMPARATOR

TYPICAL APPLICATIONS (Continued)

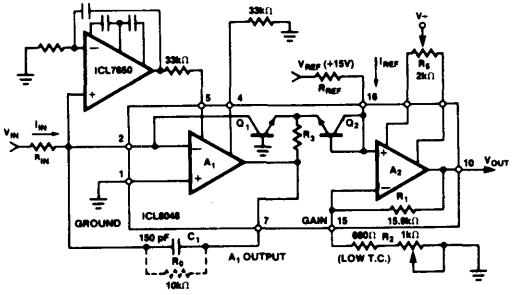


FIG. 6 ICL8048 OFFSET NULLED BY ICL7650

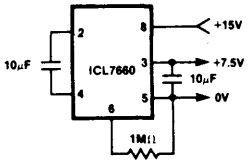


FIG. 7 SPLITTING +15V WITH ICL7660. SAME FOR −15V. >95% EFF.

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

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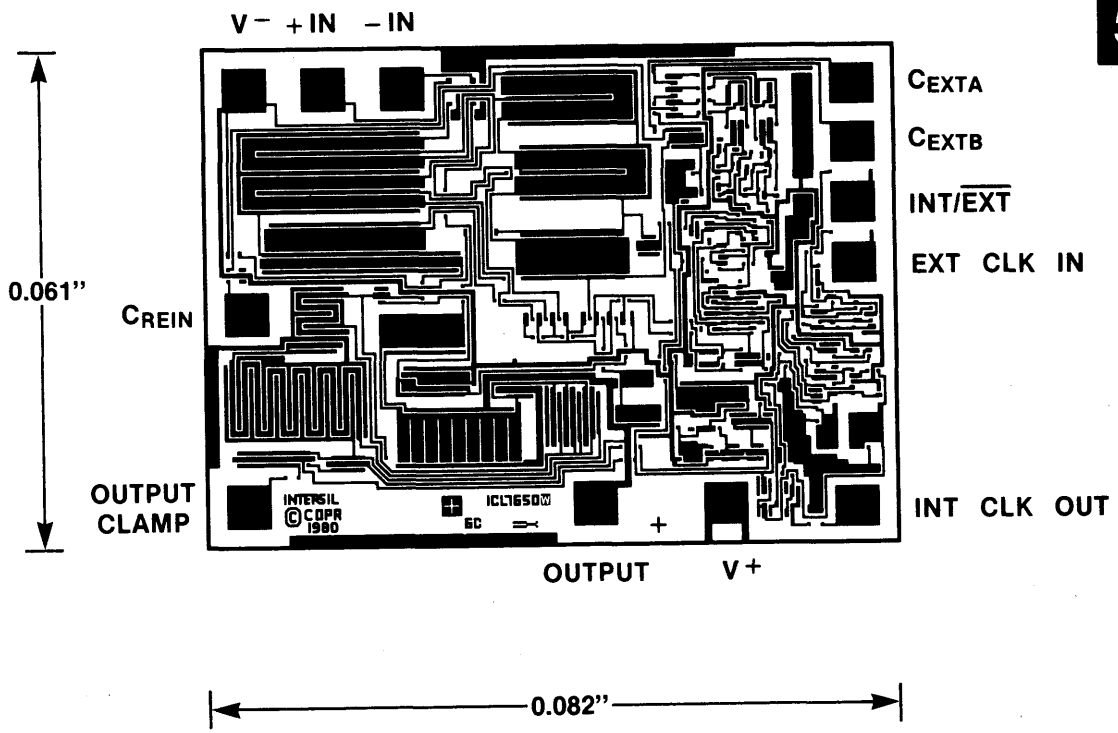


ICL7652

Chopper-Stabilized Operational Amplifier

FEATURES

- **Extremely low input offset voltage—1μV over temperature range**
- **Ultra low long-term and temperature drifts of input offset voltage (100nV/√month, 10nV/°C)**
- **Low DC input bias current—15pA**
- **Extremely high gain, CMRR and PSRR—min 110dB**
- **Low input noise voltage—0.2μVp-p (DC—1Hz)**
- **Internally compensated for unity-gain operation**
- **Very low intermodulation effects (open-loop phase shift < 2° @ chopper frequency)**
- **Clamp circuit to avoid overload recovery problems and allow comparator use**
- **Extremely low chopping spikes at input and output**

GENERAL DESCRIPTION

The ICL7652 chopper-stabilized amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is similar to INTERSIL's ICL7650 but offers improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are reduced slightly.

INTERSIL's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652 is internally compensated for unity-gain operation.

5

ORDERING INFORMATION

TEMP RANGE	PACKAGE	ORDER#
0°C to +70°C	14-pin plastic	ICL7652CPD
−20°C to +85°C	14-pin CERDIP	ICL7652IJD
0°C to +70°C	8-pin TO-99	ICL7652CTV
−20°C to +85°C	8-pin TO-99	ICL7652ITV

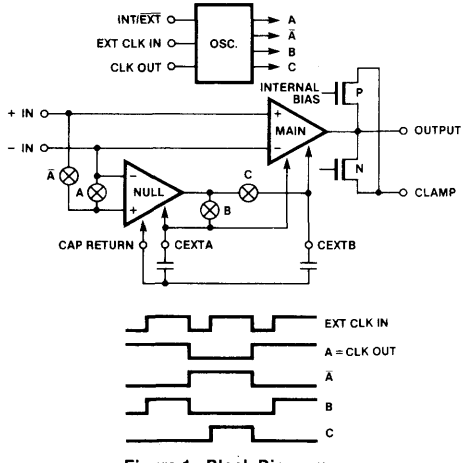
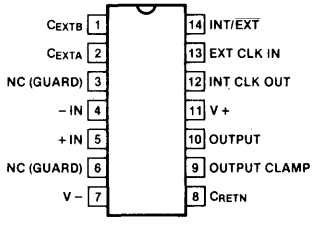
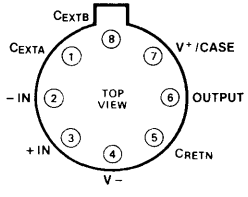


Figure 1. Block Diagram

PIN CONFIGURATIONS



14 Lead



TO-99

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... ($V^+ + 0.3$) to ($V^- - 0.3$) V
Storage Temperature Range ..... −55°C to 150°C
Operating Temperature Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite

Current into Any Pin 10mA
—while operating (Note 4) 100μA
Continuous Total Power Dissipation ($T_A = 25°C$)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 ..... 250mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

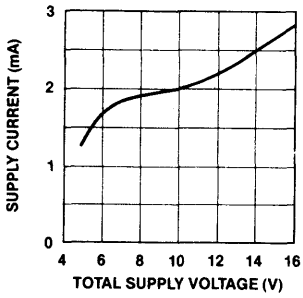
OPERATING CHARACTERISTICS: Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, Test Circuit (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$T_A = +25°C$		±0.7	±5	μV
		Over Operating Temperature Range (Note 1)		±1.0		
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Operating Temperature Range (Note 1)		0.01	0.05	μV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_{BIAS}	$T_A = +25°C$		15	30	pA
		$0°C < T_A < +70°C$		35		
		$-20°C < T_A < +85°C$		100		
Input Offset Current	I_{OS}	$T_A = +25°C$		25	60	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	$R_L = 10kΩ$, $V_{OUT} = ±4V$	120	150		dB
Output Voltage Swing (Note 3)	V_{OUT}	$R_L = 10kΩ$	±4.7	±4.85		V
		$R_L = 100kΩ$		±4.95		
Common-Mode Voltage Range	CMVR		−4.3	−4.8 to +4.0	3.5	V
Common-Mode Rejection Ratio	CMRR	CMVR = −4.3V to +3.5V	110	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	110	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	$R_S = 100Ω$, DC to 1Hz		0.2		μVp-p
		DC to 10Hz		0.7		
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	$C_L = 50pF$, $R_L = 10kΩ$		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	I_{SUPP}	No Load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		$R_L = 100kΩ$	25	100		μA
Clamp OFF Current (Note 2)		$-4.0V < V_{OUT} < +4.0V$		1		pA
Offset Voltage vs Time				100		nV/√month

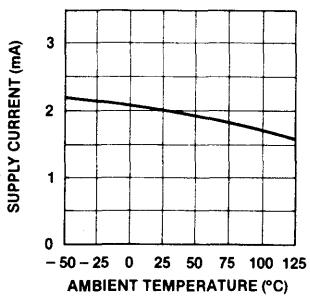
Note 1: Operating temperature range for I series parts is −20°C to +85°C, for C series is 0°C to +70°C.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.

TYPICAL OPERATING CHARACTERISTICS

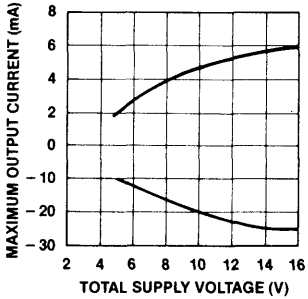
Supply Current vs Supply Voltage



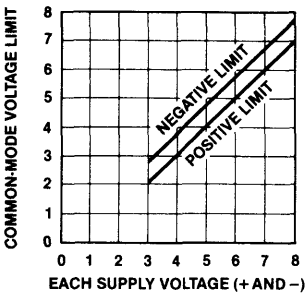
Supply Current vs Ambient Temperature



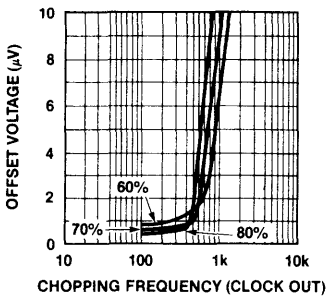
Maximum Output Current vs Supply Voltage



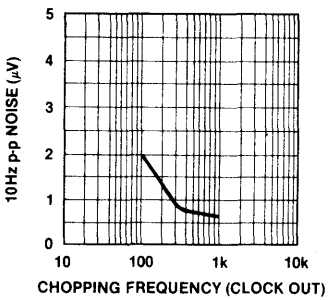
Common-Mode Input Voltage Range vs Supply Voltage



Input Offset Voltage vs Chopping Frequency

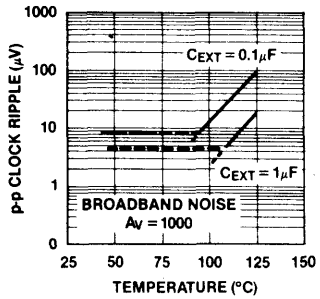


10Hz P-P Noise Voltage Voltage vs Chopping Frequency

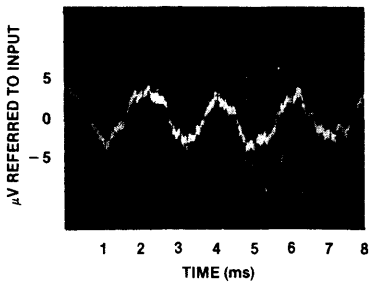


% parameter is EXT CLK in duty cycle

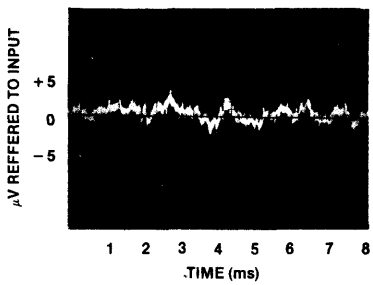
Clock Ripple Referred to the Input vs Temperature



Broadband Noise Balanced
Source Impedance = 1kΩ
Gain = 1000
C_{EXT} = 0.1μF

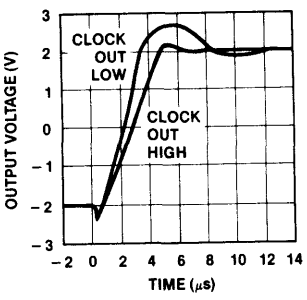


Broadband Noise Balanced
Source Impedance = 1kΩ
Gain = 1000
C_{EXT} = 1.0μF

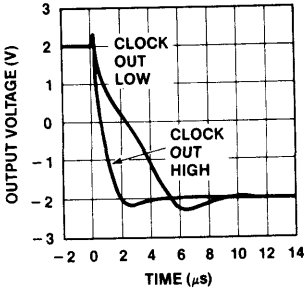


TYPICAL OPERATING CHARACTERISTICS (Continued)

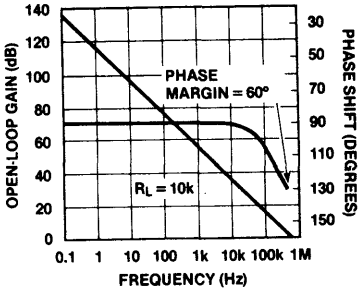
Voltage Follower Large Signal Pulse Response*



Voltage Follower Large Signal Pulse Response*

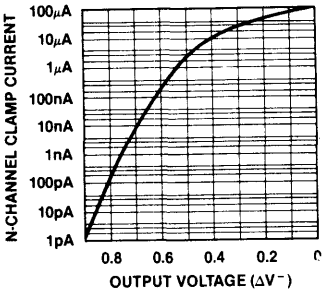


Open-Loop Gain and Phase Shift vs Frequency

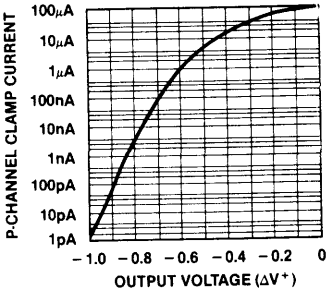


*The two different responses correspond to the two phases of the clock.

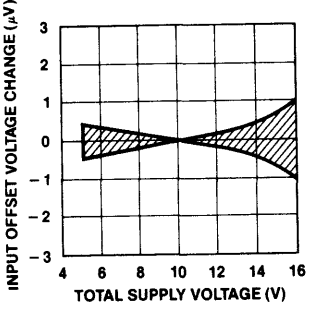
N-Channel Clamp Current vs Output Voltage



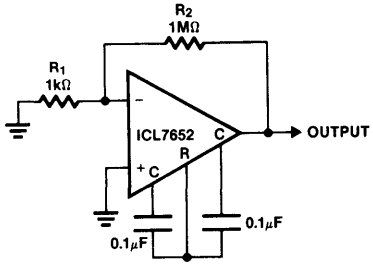
P-Channel Clamp Current vs Output Voltage



Input Offset Voltage Change vs Supply Voltage



TEST CIRCUIT



DETAILED DESCRIPTION

Amplifier

The Block Diagram shows the major elements of the ICL7652. There are two amplifiers, the main amplifier, and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output, while the nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET back gates, are inherently high-impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, together with the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7652, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (in the case of 14-pin devices) or the V^- pin (in the case of 8-pin devices). This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} (or V^-).

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7652 has an internal oscillator, giving a chopping frequency of 400Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%-80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^-. The logic threshold will be at about 2.5V below V^+. Note also that a signal of about 800Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The required capacitors, C_{EXTA} and C_{EXTB}, are normally in the range of 0.1μF to 1.0μF. A 1.0μF capacitor should be used in broad bandwidth circuits if minimum clock ripple noise is desired. For limited bandwidth applications where clock ripple is filtered out, using a 0.1μF capacitor results in slightly lower offset voltage. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as poly-propylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics which may result in increased input-leakage currents.

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be trigerred into a low-impedance state, resulting in excessive supply current. To avoid this condition no voltage

greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latch-up, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

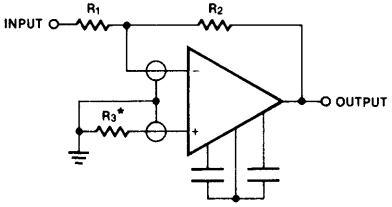
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7652. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 lead TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

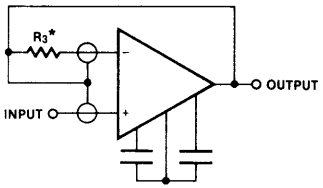
The pin configuration of the 14-pin dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

5

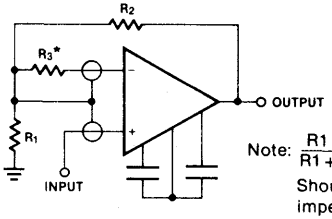
CONNECTION OF INPUT GUARDS



Inverting Amplifier



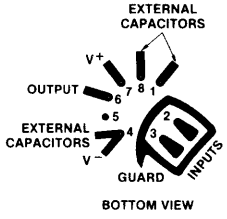
Follower



Note: $\frac{R1\ R2}{R1 + R2}$

Should be low impedance for optimum guarding

Non-Inverting Amplifier



Board Layout for Input Guarding with TO-99 Package

*Use R3 to compensate for large source resistances, or for clamp operation (see Figure 2)

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset-null or compensation capacitors, or simply not connected. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V^+, by two capacitors from those pins to V^-, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V^- is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7652.

TYPICAL APPLICATIONS

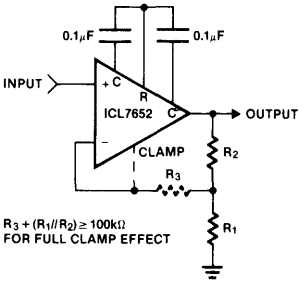
5

Clearly the applications of the ICL7652 will mirror those of other op-amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7652 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op-amps by the ICL7652 are the supply voltage (±8V max) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7652. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

Figure 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper-stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.

It is possible to use the ICL7652 to offset-null such high slew rate and bandwidth amplifiers as the HA2500 and HA2600 series, as shown in Figure 6. The same basic idea can be used with low-noise bipolar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced. More details on these and other ideas are explained in application note A053.

Mixing the ICL7652 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit "backwards". A suitable connection is shown in Figure 7.



Note: $R_1//R_2$ indicates the parallel combination of R_1 and R_2

Figure 2. Non-Inverting Amplifier with (Optional) Clamp

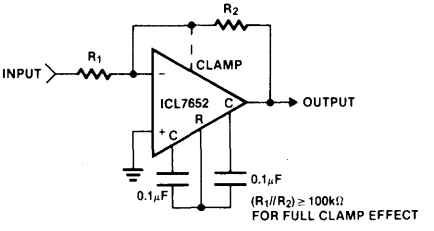


Figure 3. Inverting Amplifier with (Optional) Clamp

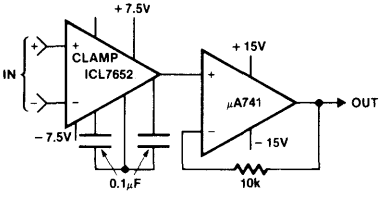


Figure 4. Using 741 to Boost Output Drive Capability

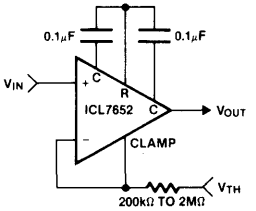


Figure 5. Low Offset Comparator

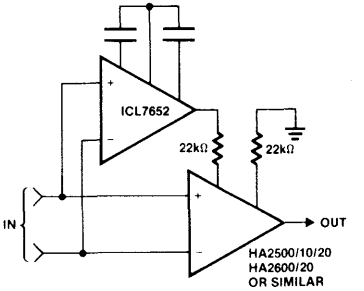


Figure 6. HA2500 or 2600 Offset-Nulled by ICL7652

TYPICAL APPLICATIONS (Continued)

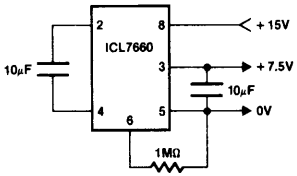
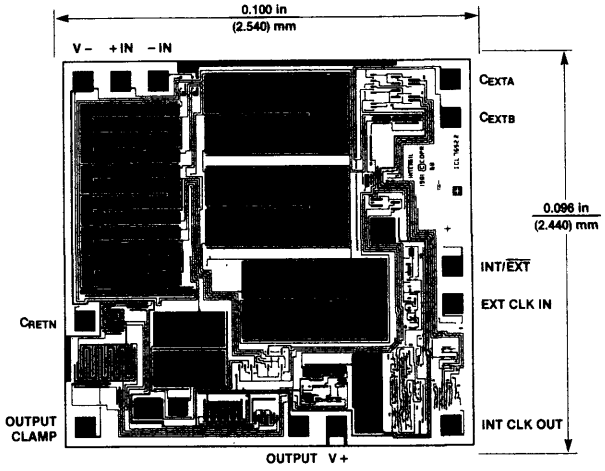


Figure 7. Splitting +15V with ICL7660 at >95% efficiency. Same for −15V.

For further applications assistance, see A053 and R017

CHIP TOPOGRAPHY



ICL7660

Monolithic MAXCMOS™ Voltage Converter

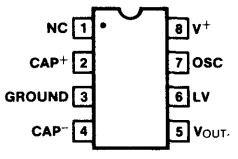
FEATURES

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication (V_{OUT} = (−) nV_{IN})**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to use - Requires only 2 External Non-Critical Passive Components**

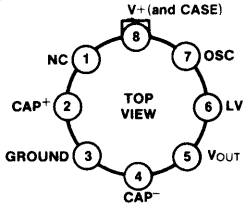
APPLICATIONS

- On Board Negative Supply for up to 64 Dynamic RAMs.
- Localized μ-Processor (8080 type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

PIN CONFIGURATIONS



(outline dwg PA)



(outline dwg TV)

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7660CTV	−20° to +70°C	TO-99
ICL7660CPA	−20° to +70°C	8 PIN MINI DIP
ICL7660MTV	−55° to +125°C	TO-99
ICL7660/D		DICE

GENERAL DESCRIPTION

The Intersil ICL7660 is a monolithic MAXCMOS™ power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for V_{SUPPLY} >6.5V.

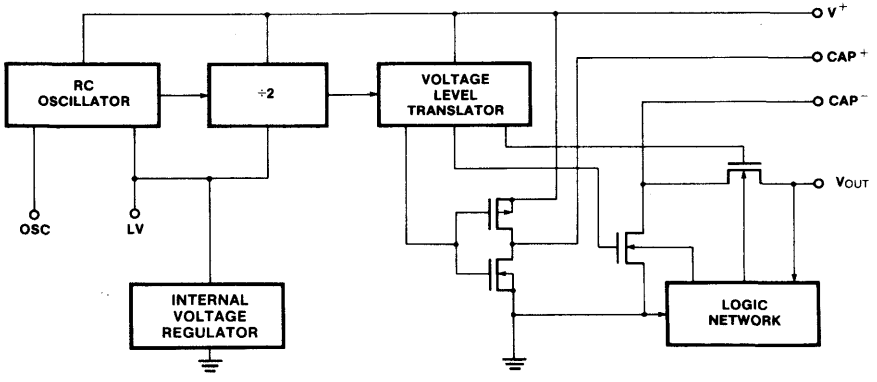
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the ICL7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The ICL7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
LV and OSC Input Voltage
(Note 1) ..... -0.3V to (V^+ +0.3V) for $V^+ < 5.5V$
(V^+ -5.5V) to (V^+ +0.3V) for $V^+ > 5.5V$
Current into LV (Note 1) ..... 20μA for $V^+ > 3.5V$
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) .... Continuous
Power Dissipation (Note 2)
ICL7660CTV 500mW
ICL7660CPA 300mW
ICL7660MTV 500mW

Operating Temperature Range
ICL7660M ..... -55°C to +125°C
ICL7660C ..... 0°C to 70°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature
(Soldering, 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

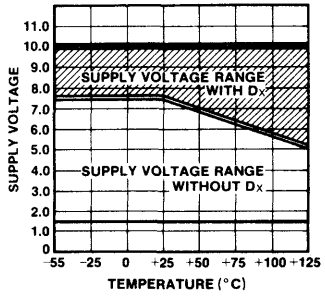
OPERATING CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 1 (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I^+	Supply Current		170	500	μA	$R_L = \infty$
V^+_{H1}	Supply Voltage Range - Hi	3.0		6.5	V	$0°C \leq T_A \leq 70°C$, $R_L = 10k\Omega$, LV Open
	(D_X out of circuit) (Note 3)	3.0		5.0	V	$-55°C \leq T_A \leq 125°C$, $R_L = 10k\Omega$, LV Open
V^+_{L1}	Supply Voltage Range - Lo (D_X out of circuit)	1.5		3.5	V	$MIN \leq T_A \leq MAX$, $R_L = 10k\Omega$, LV to GROUND
V^+_{H2}	Supply Voltage Range - Hi (D_X in circuit)	3.0		10.0	V	$MIN \leq T_A \leq MAX$, $R_L = 10k\Omega$, LV Open
V^+_{L2}	Supply Voltage Range - Lo (D_X in circuit)	1.5		3.5	V	$MIN \leq T_A \leq MAX$, $R_L = 10k\Omega$, LV to GROUND
R_{OUT}	Output Source Resistance		55	100	Ω	$I_{OUT} = 20mA$, $T_A = 25°C$
				120	Ω	$I_{OUT} = 20mA$, $-20°C \leq T_A \leq +70°C$
				150	Ω	$I_{OUT} = 20mA$, $-55°C \leq T_A \leq +125°C$ (Note 3)
				300	Ω	$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $-20°C \leq T_A \leq +70°C$
				400	Ω	$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $-55°C \leq T_A \leq +125°C$, D_X in circuit (Note 3)
f_{OSC}	Oscillator Frequency		10		kHz	
P_{Ef}	Power Efficiency	95	98		%	$R_L = 5k\Omega$
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	97	99.9		%	$R_L = \infty$
Z_{OSC}	Oscillator Impedance		1.0		MΩ	$V^+ = 2$ Volts
			100		kΩ	V = 5 Volts

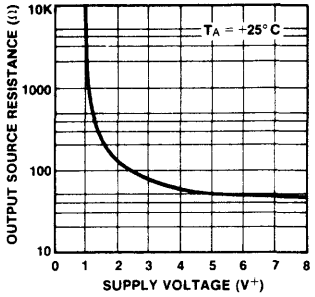
Notes: 1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.
2. Derate linearly above 50°C by 5.5mW/°C.
3. ICL7660M only.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 1)

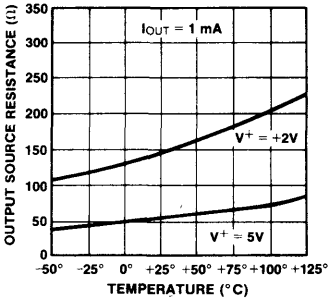
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



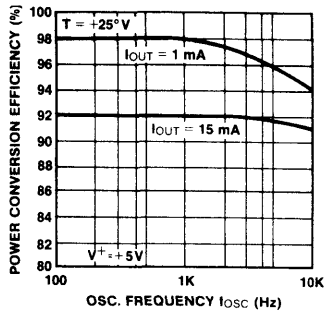
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



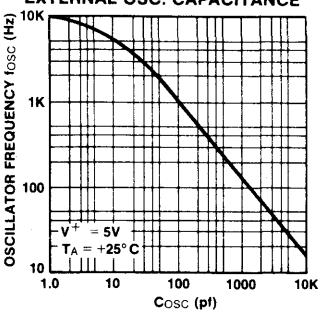
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



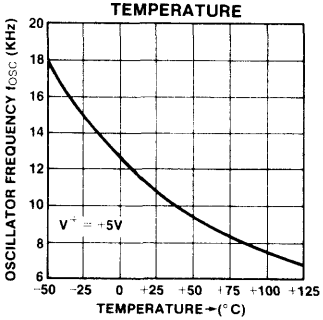
POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



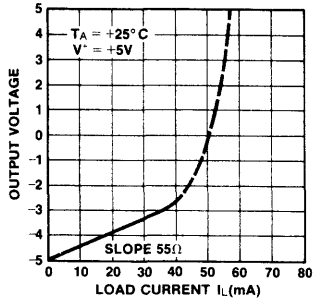
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



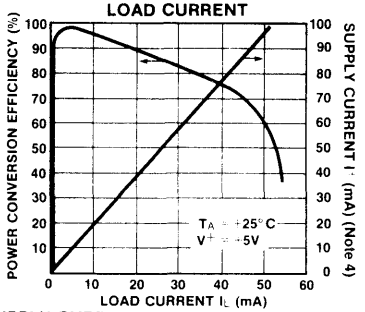
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



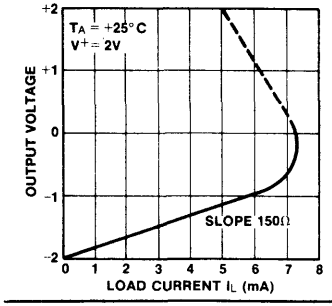
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



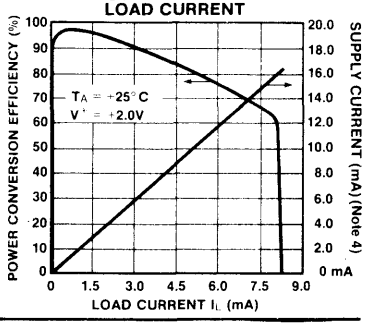
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

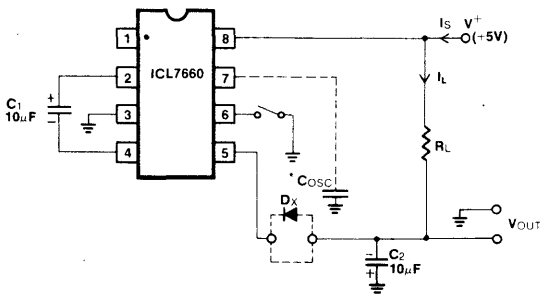


NOTE 4.

Note that the curves on the right include in the supply current that current fed directly into the load (R_L) from V^+ (see Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \approx 2\ V_{IN}$, $I_S \approx 2\ I_L$, so $V_{IN} \cdot I_S \approx V_{OUT} \cdot I_L$.

SUPPLY CURRENT POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT





NOTES: 1. For large value of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100μF.

2. D_X is required for supply voltages greater than 6.5V @ −55° ≤ T_A ≤ +70°C; refer to performance curves for additional information.

Figure 1: ICL7660 Test Circuit

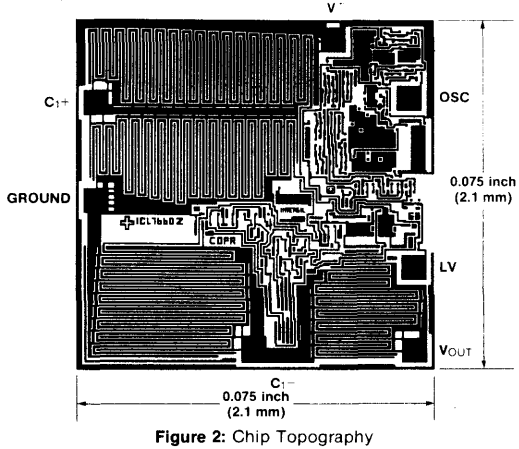


Figure 2: Chip Topography

CIRCUIT DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660, the 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

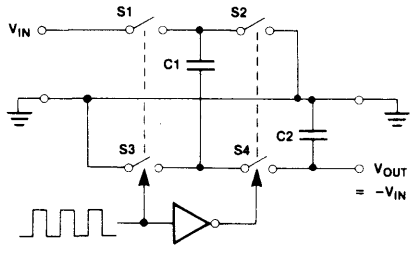


Figure 3. Idealized Voltage Doubler

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however it's inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power
B The output switches have extremely low ON resistance and virtually no offset.
C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Fig. 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1 Do not exceed maximum supply voltages.
2 Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3 Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4 When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5 Add diode D_X as shown in Fig. 1 for hi-voltage, elevated temperature applications.

CONSIDERATIONS FOR HI VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (storage & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latch-up of the ICL7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the ICL7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

TYPICAL APPLICATIONS

1. Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10.0 volts, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of −10mA and a supply voltage of +5 volts, the output voltage will be −4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$ where

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\mu F$ and $f_{OSC} = 5kHz$ (1/2 of oscillator frequency)

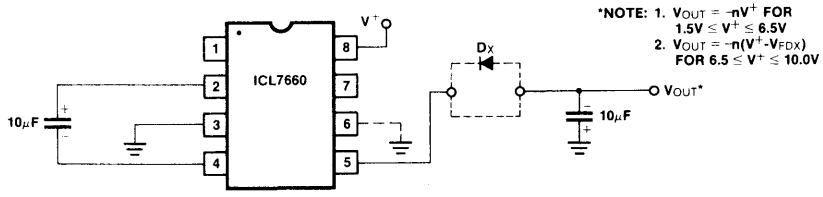


Figure 4: Simple Negative Converter

2. Paralleling Devices

Any number of ICL7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

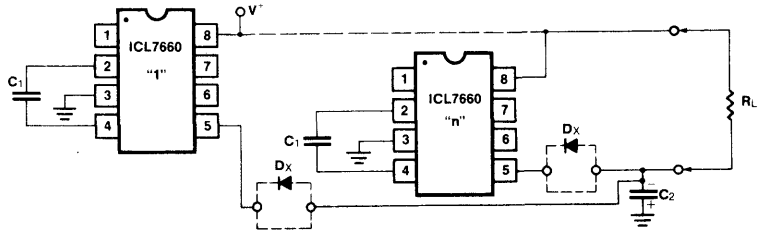


Figure 5: Paralleling Devices

3. Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

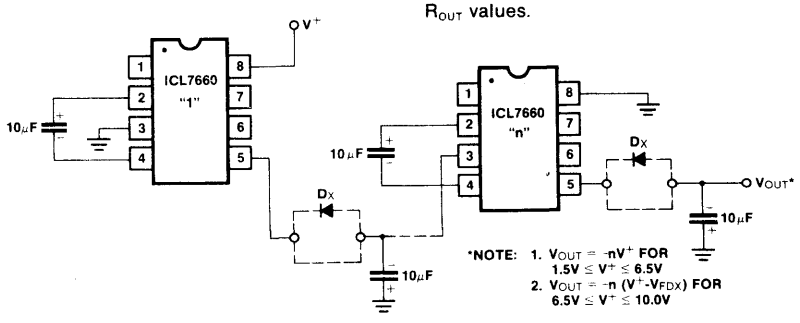


Figure 6: Cascading Devices for Increased Output Voltage

4. Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

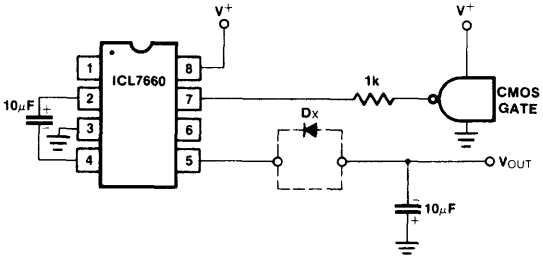


Figure 7: External Clocking

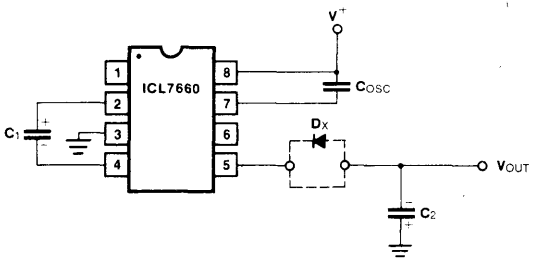


Figure 8: Lowering Oscillator Frequency

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5. Positive Voltage Multiplication

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

6. Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

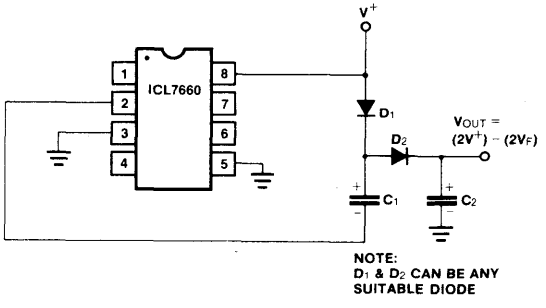


Figure 9: Positive Voltage Multiplier

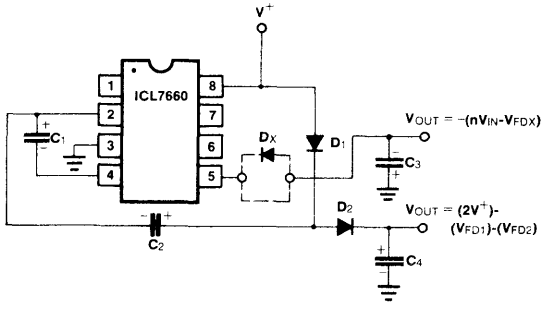


Figure 10: Combined Negative Converter and Positive Multiplier

7. Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, + 15V can be converted (via + 7.5, and − 7.5) to a nominal − 15V, though with rather high series resistance (~250Ω).

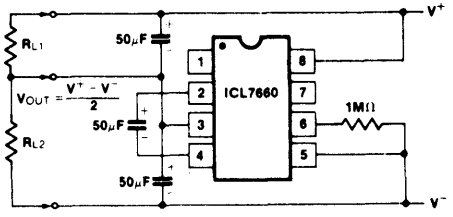


Figure 11: Splitting a Supply in Half.

ICL7660's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

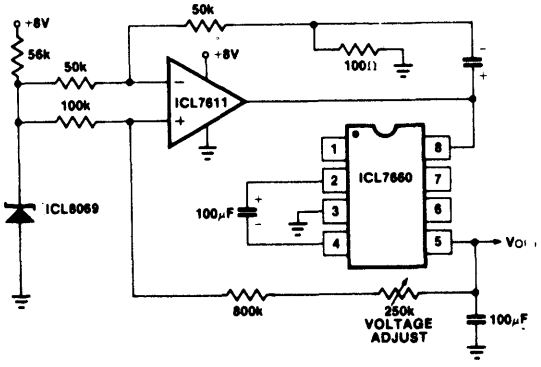


Figure 12: Regulating the Output Voltage

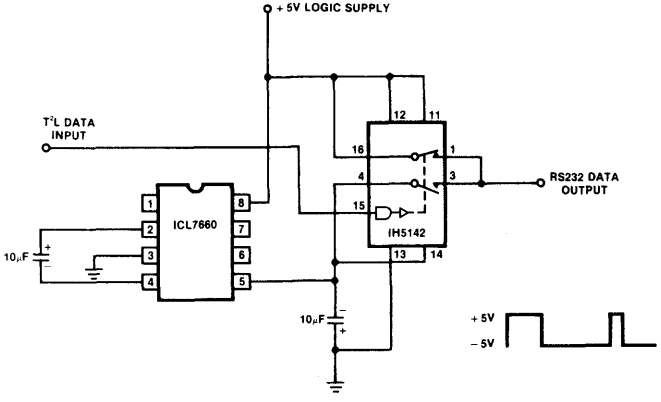


Figure 13: RS232 Levels from a Single 5V Supply

8. Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter" by Peter Bradshaw and Dave Bingham.

ICL7663/7664

CMOS Programmable Micropower Voltage Regulators

FEATURES

- **Ideal for battery-operated systems: less than 4μA typical current drain**
- **Will handle input voltages from 1.6V to 16V**
- **Very low input-output differential voltage**
- **1.3V bandgap voltage reference**
- **Up to 40mA output current**
- **Output shutdown via current-limit sensing or external logic signal**
- **Output voltages programmable from 1.3V to 16V**
- **Output voltages with programmable negative temperature coefficients (ICL7663 only)**

GENERAL DESCRIPTION

The ICL7663 (positive) and ICL7664 (negative) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 16V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4μA, regardless of load.

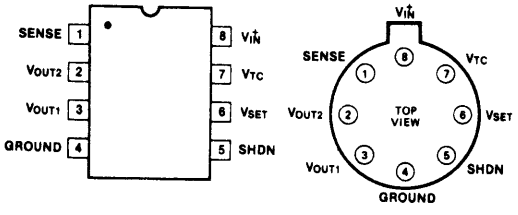
Output current sensing and remote shutdown are available on both devices, thereby providing protection for the regulators and the circuits they power. A unique feature, on the ICL7663 only, is a negative temperature coefficient output. This can be used, for example, to efficiently tailor the voltage applied to a multiplexed LCD through the driver (e.g., ICM7231/2/3/4) so as to extend the display operating temperature range many times.

The ICL7663 and ICL7664 are available in either an 8-pin plastic minidip package or a TO-99 can.

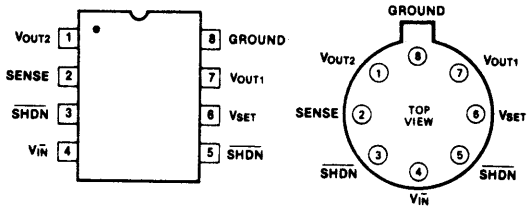
5

PIN CONFIGURATIONS (outline dwgs PA, TV)

ICL7663 Positive Regulator



ICL7664 Negative Regulator



ORDERING INFORMATION

Positive Regulator		
ICL7663CPA	0°C to +70°C	8-pin minidip
ICL7663CTV	0°C to +70°C	TO-99
ICL7663/D		DICE

Negative Regulator		
ICL7664CPA	0°C to +70°C	8-pin minidip
ICL7664CTV	0°C to +70°C	TO-99
ICL7664/D		DICE

ABSOLUTE MAXIMUM RATINGS, ICL7663 POSITIVE REGULATOR

Input Supply Voltage ..... +18V
Any Input or Output Voltage (Note 1) (GND – 0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) ..... (V_{IN}^+ + 0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current (Terminal 7) ..... –10mA
Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $V_{IN}^+ = 9V$, $V_{OUT} = 5V$, $T_A = +25°C$, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Voltage	V_{IN}^+	$T_A = +25°C$ $20°C \le T_A \le +70°C$	1.5 1.6		16.0 16.0	V
Quiescent Current	I_Q	$R_L = \infty$, $1.4V \le V_{OUT} \le 8.5V$ $V_{IN}^+ = 16V$ $V_{IN}^+ = 9V$		4.0 3.5	12 10	μA
Reference Voltage	V_{SET}		1.2	1.3	1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	$8.5V < V_{IN}^+ < 9V$		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	$2V < V_{IN}^+ < 15V$		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	1.4		0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	$V_{IN}^+ = 2V$ $V_{IN}^+ = 9V$ $V_{IN}^+ = 15V$		200 70 50		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	$\Delta I_{OUT1} = 100\mu A$ @ $V_{OUT1} = 5V$ $\Delta I_{OUT2} = 10mA$ @ $V_{OUT2} = 5V$		2.0 1.0		Ω
Available Output Current (V_{OUT2})	I_{OUT2}	$V_{IN}^+ = 3V$ $V_{OUT} = V_{SET}$ $V_{IN}^+ = 9V$ $V_{OUT} = 5V$ $V_{IN}^+ = 15V$ $V_{OUT} = 5V$	10 25 40			mA
Negative-Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	(Includes V_{SET} Divider)			1.0	μA

Note 1: Connecting any terminal to voltages greater than (V_{IN}^+ + 0.3V) or less than (GND – 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

ABSOLUTE MAXIMUM RATINGS, ICL7664 NEGATIVE REGULATOR

Input Supply Voltage ..... −18V
Any Input or Output Voltage (Note 1) (GND + 0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) ..... ($V_{\overline{IN}}$ − 0.3V)
Output Sink Current
(Terminals 1, 7) ..... −25mA

Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $V_{\overline{IN}} = -9V$, $V_{OUT} = -5V$, $T_A = +25°C$, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Voltage	$V_{\overline{IN}}$	$T_A = +25°C$ $0°C \le T_A \le +70°C$	−1.5 −1.6		−16.0 −16.0	V
Quiescent Current	I_Q	$R_L = \infty$, $-1.4V \le V_{OUT} \le -8.5V$		4.0 3.5	12 10	µA
						$V_{\overline{IN}} = 16V$ $V_{\overline{IN}} = 9V$
Reference Voltage	V_{SET}		−1.2	−1.3	−1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	$-8.5V < V_{\overline{IN}} < -9V$		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	$-2V < V_{\overline{IN}} < -15V$		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	$I_{\overline{SHDN}}$			±0.01	10	nA
Shutdown Input Voltage	$V_{\overline{SHDN}}$	$V_{\overline{SHDN}}$HI: Both V_{OUT} Enabled $V_{\overline{SHDN}}$LO: Both V_{OUT} Disabled	−0.3		−1.4	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		−0.35		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	$V_{\overline{IN}} = 2V$ $V_{\overline{IN}} = 9V$ $V_{\overline{IN}} = 15V$		150 40 30		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	$\Delta I_{OUT} = 100\mu A$ @ $V_{OUT} = -5V$		2.0		Ω
Output Current, V_{OUT1} or V_{OUT2}	I_{OUT}	$V_{\overline{IN}} = 3V$ $V_{OUT} = V_{SET}$ $V_{\overline{IN}} = 9V$ $V_{OUT} = -5V$ $V_{\overline{IN}} = 15V$ $V_{OUT} = -5V$		−2 −20 −40		mA
Minimum Load Current (Includes V_{SET} Divider)	$I_{L(min)}$				1.0	µA

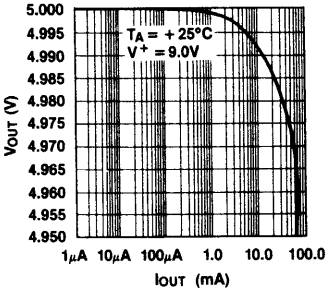
Note 1: Connecting any terminal to voltages greater than (GND + 0.3V) or less than ($V_{\overline{IN}}$ − 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

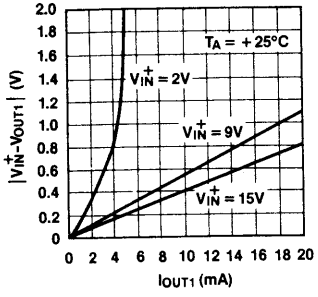
Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

TYPICAL CHARACTERISTICS

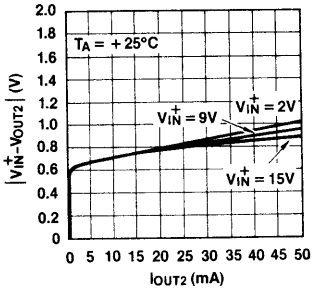
ICL7663
Output Voltage as a
Function of Output Current



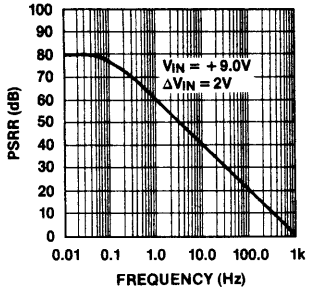
ICL7663
V_{OUT1} Input-Output Differential
vs Output Current



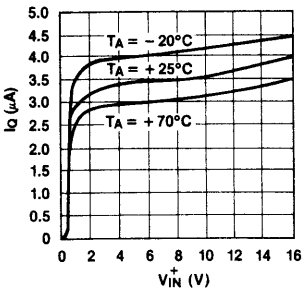
ICL7663
V_{OUT2} Input-Output Differential
vs Output Current



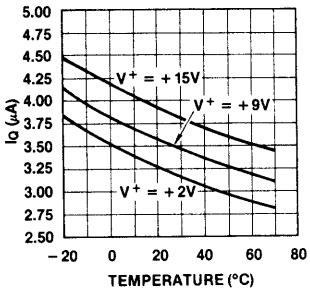
ICL7663
Input Power Supply
Rejection Ratio



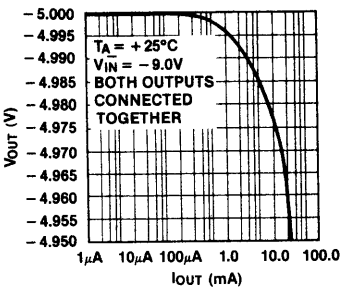
ICL7663
Quiescent Current as a
Function of Input Voltage



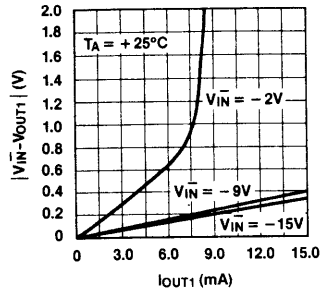
ICL7663
Quiescent Current as a
Function of Temperature



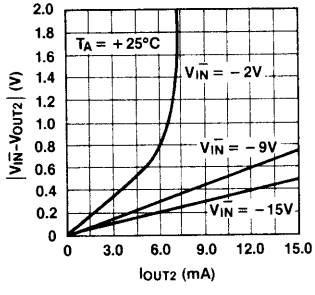
ICL7664
Output Voltage as a
Function of Output Current



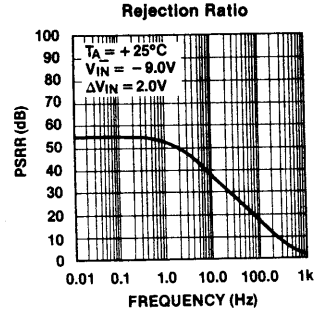
ICL7664
V_{OUT1} Input-Output Differential
vs Output Current



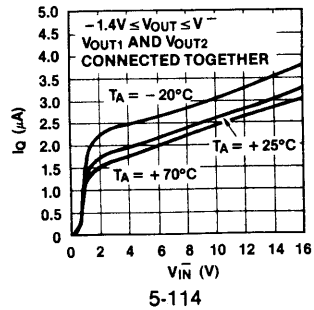
ICL7664
V_{OUT2} Input-Output Differential
vs Output Current



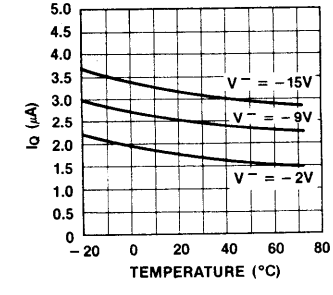
ICL7664
Input Power Supply
Rejection Ratio



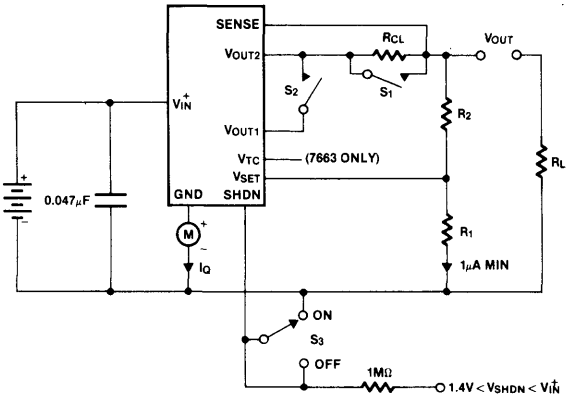
ICL7664
Quiescent Current as a
Function of Input Voltage



ICL7664
Quiescent Current as a
Function of Temperature



TEST CIRCUIT



Note 1: S_1 when closed, disables output current limiting
Note 2: For ICL7664, exchange V_{OUT1} and V_{OUT2}. S_2 action differs, as follows:

Device	S_2 Closed	S_2 Open
ICL7663	V_{OUT1}	V_{OUT2}
ICL7664	$V_{OUT1} + V_{OUT2}$	V_{OUT1}

Note 3: $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$

Note 4: I_Q quiescent current is measured at GND pin by meter M
Note 5: S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}

Test Circuit for ICL7663/64 (Polarities shown are for ICL7663. Reverse for ICL7664)

DETAILED DESCRIPTION

The ICL7663 and ICL7664 are CMOS integrated circuits which contain all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the block diagrams (Figures 1 and 2), each contains a bandgap-type voltage reference of 1.3 Volts; this voltage, therefore, is the lowest output voltage the regulators can control (−1.3V for the ICL7664). Error amplifier A drives either a P-channel (ICL7663) or an N-channel (ICL7664) pass transistor which is sufficient for low (under about 5mA) currents; this transistor is augmented by a duplicate in the ICL7664, which permits higher current outputs. In the ICL7663, the high current output is formed by an NPN transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via an MOS transistor of the appropriate polarity. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} line on each chip. Finally, the positive regulator (ICL7663 only) has an output (V_{TC}) from a buffer amplifier (B), which can be used to generate programmable-temperature-coefficient output voltages.

The amplifiers, reference and comparator circuitry all operate at bias levels well below 1μA to achieve the extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

BASIC OPERATION

The ICL7663 and ICL7664 are designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 15V supply regulated down to 5V with a load current of 30mA clearly exceeds the power dissipation rating of the minidip: (15-5) (30) $(10^{-3}) = 300$mW. The test circuit illustrates proper use of the devices. Although the following discussion refers to the ICL7663, it applies as well to the parallel features of the ICL7664 as long as the appropriate polarities are reversed. Individual features and precautions will be discussed where appropriate.

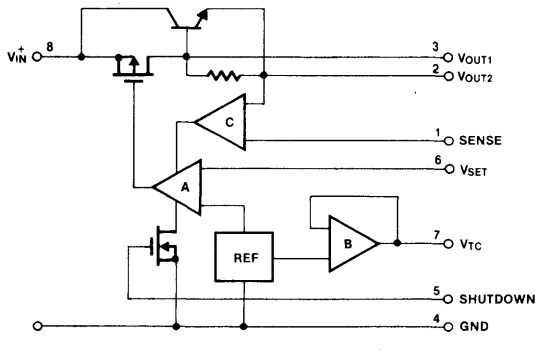


Figure 1. Block Diagram of the ICL7663

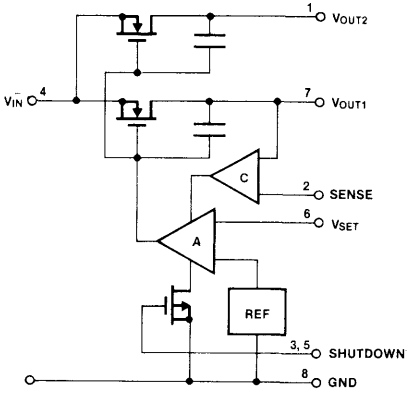


Figure 2. Block Diagram of the ICL7664

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or non-operation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Input Voltages—These regulators accept working inputs of about 1.4V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047μF capacitor on the device side of the switch will limit inputs to a safe level around 2V/μs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output Voltages—The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\ V_{SET}$. In the ICL7664, $V_{\overline{IN}}$ and V_{SET} are negative, so V_{OUT} will be also. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. Because of the low leakage current of the V_{SET} terminal, these resistors can be tens of megohms for minimum additional quiescent drain current. However, *some* load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1μA. This can include the current for R_2 and R_1.

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal.

Output Currents—For the ICL7663, low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Either output may be used on the ICL7664, with the unused output connected to $V_{\overline{IN}}$. Where higher currents are needed, use V_{OUT2} on the ICL7663 (V_{OUT1} should be left open in this case) and parallel V_{OUT1} and V_{OUT2} on the ICL7664.

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing—The on-chip comparator (C in the block diagrams) permits shutdown of the regulator output in the event of excessive current drain. As the test circuits show, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2}, and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.7V for ICL7663, 0.35V for ICL7664) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.

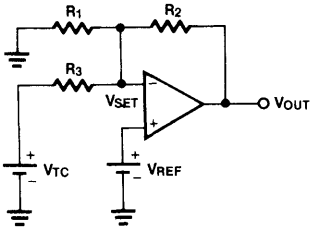
Logic-Controllable Shutdown—When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it *is* required. This usually means switches, with their unreliable contacts. Instead, the ICL7663 and ICL7664 can be shut down by a logic signal, leaving only I_Q (under 4μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663, and greater than −0.3V for the ICL7664 will keep the regulator ON, and a voltage level of more than 1.4V but less than V_{IN}^{+} for the ICL7663, and less than −1.4V but not less than $V_{\overline{IN}}$ for the ICL7664 control will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V_{IN}^{+} or $V_{\overline{IN}}$), the current from this signal should be limited to 100μA maximum by a high-value (1MΩ) series resistor. This situation may occur when the logic signal originates from a separately-powered system from that of the regulator.

Additional Circuit Precautions—These regulators have poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

$$I = C\frac{\Delta V}{\Delta t},\ C = I_{OUT}\frac{(20\times10^{-3})}{0.9V_{OUT}} = 0.022\frac{I_{OUT}}{V_{OUT}}.$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see **"Current-Limit Sensing"**).

Producing Output Voltages With Negative Temperature Coefficients—The ICL7663 has an additional output (not present on the ICL7664) which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 3 and its design equations).



EQ. 1: $V_{OUT} = V_{SET}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$

EQ. 2: $TC\,V_{OUT} = -\frac{R_2}{R_3}\ (TC\,V_{TC})$ in mV/°C

WHERE: $V_{SET} = 1.3V$
$V_{TC} = 0.9V$
$TCV_{TC} = +2.5mV/°C$

Figure 3. Generating Negative Temperature Coefficients

APPLICATIONS

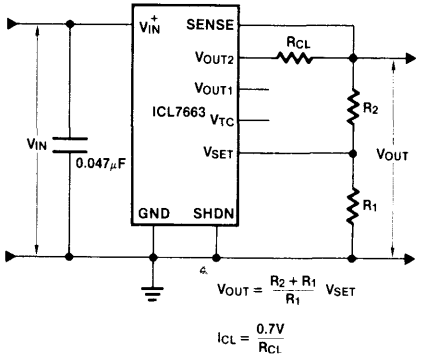


Figure 4. **Basic Application of ICL7663 as Positive Regulator with Current Limit**

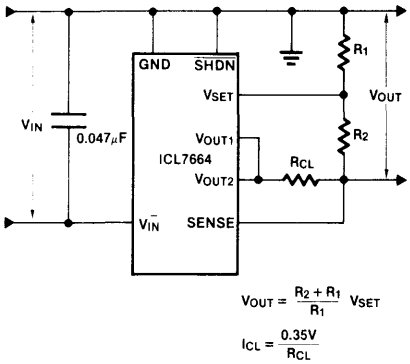
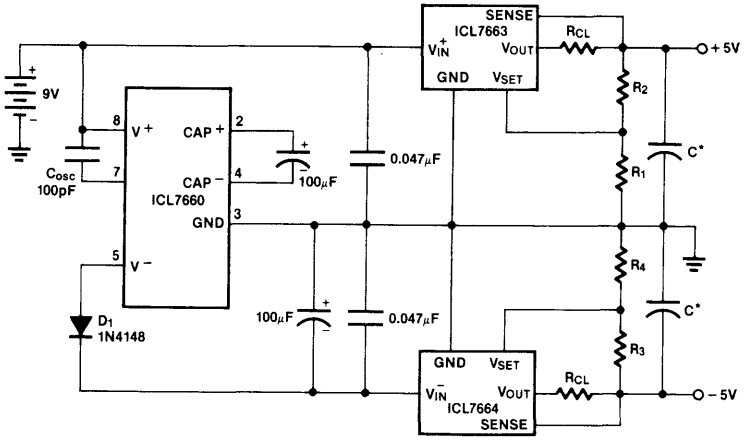


Figure 5. **Basic Application of ICL7664 as Negative Regulator with Current Limit**



*Values depend on load characteristics

Figure 6. Generating regulated split supplies from a single supply. The oscillation frequency of the ICL7660 is reduced by the external oscillator capacitor, so that it inverts the battery voltage more efficiently.

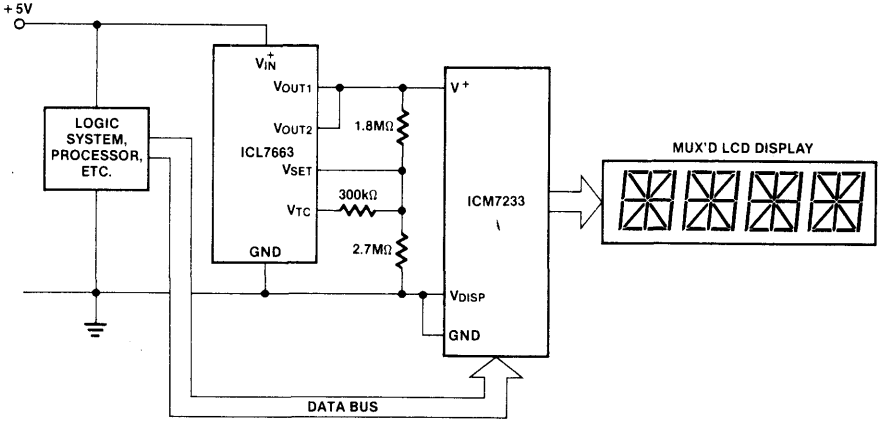


Figure 7. Driving a Multiplexed LCD Display. The negative temperature coefficient drive voltage to the displays allows consistent operation over more than 40°C temperature span, as opposed to about 10°C with a fixed drive voltage. Values based on EPSON LDB-728 display or similar.

APPLICATIONS (Continued)

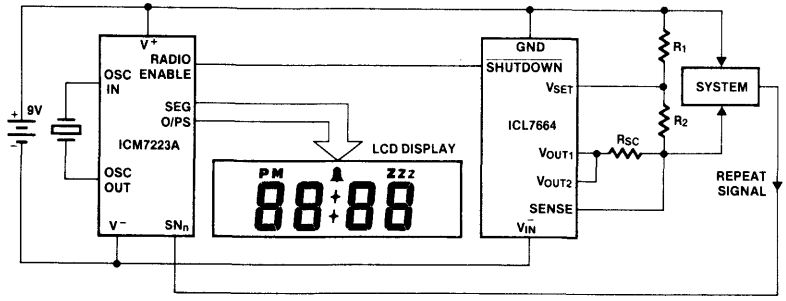
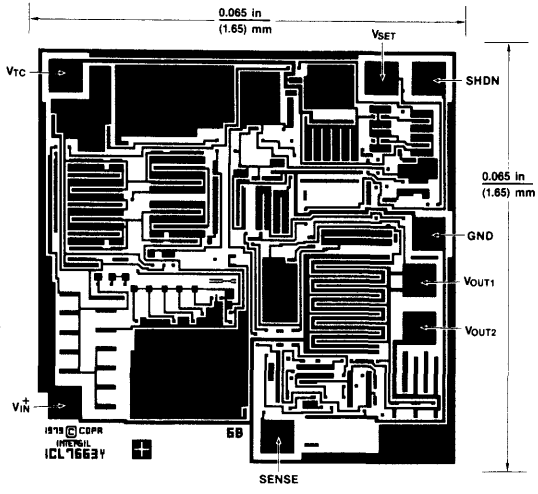
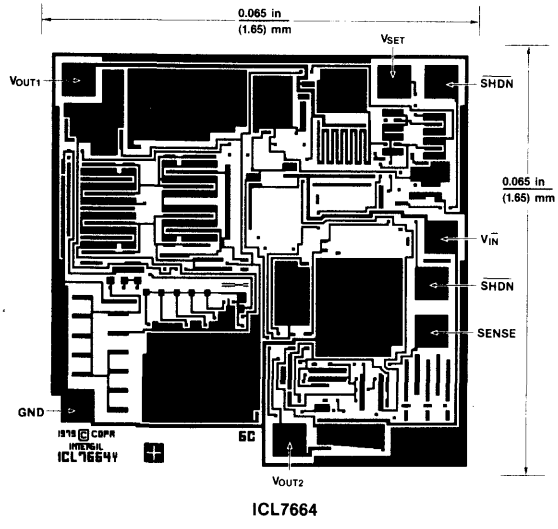


Figure 8. Once a Day System. This circuit will turn on a regulated supply to a system for one minute every day, via the $\overline{\text{SHUTDOWN}}$ pin on the ICL7664, and under control of the ICM7223A Alarm Clock circuit. If the system decides it needs another one minute activation, pulling the REPEAT line to V^+ (GND) during one activation will trigger a subsequent activation after a **snooze** interval set by the choice of SN pins (2 mins shown). Alternatively, activation of the **Sleep** timer, without pause, can be achieved. See ICM7223A data sheet for details.

CHIP TOPOGRAPHIES





ICL7663B/4B ADDENDUM TO THE ICL7663/4 DATASHEET

INTERSIL

This Addendum to the standard ICL7663/4 datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7663B/ICL7664B devices. The following table indicates those limits to which the ICL7663B/ICL7664B is tested and/or guaranteed operational.

ICL7663B POSITIVE REGULATOR ORDERING INFORMATION

Positive Regulator		
ICL7664BCPA	0 to +70°C	8-pin MiniDIP
ICL7664BCTV	0 to +70°C	TO-99
ICL7664BC/D	0 to +70°C	DICE

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... +12V
Any Input or Output Voltage (Note 1) (GND −0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) ..... (V_{IN}^{+} +0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current (Terminal 7) ..... −10mA
Power Dissipation (Note 2)
MiniDIP 200mW
TO-99 Can 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7663B OPERATING CHARACTERISTICS V_{IN}^{+} = 9V, V_{OUT} = 5V, T_A = +25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Voltage	V_{IN}^{+}	T_A = +25°C 20°C ≤ T_A ≤ +70°C	1.5 1.6		10 10	V
Quiescent Current	I_Q	{$R_L = \infty$ 1.4V ≤ V_{OUT} ≤ 8.5V}		3.5	10	µA
Reference Voltage	V_{SET}		1.2	1.3	1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	8.5V < V_{IN}^{+} < 9V		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	2V < V_{IN}^{+} < 9V		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	1.4		0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	V_{IN}^{+} = 2V V_{IN}^{+} = 9V		200 70		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT1} = 100µA @ V_{OUT1} = 5V ΔI_{OUT2} = 10mA @ V_{OUT2} = 5V		2 1		Ω
Available Output Current (V_{OUT2})	I_{OUT2}	V_{IN}^{+} = 3V V_{OUT} = V_{SET} V_{IN}^{+} = 9V V_{OUT} = 5V	10 25			mA
Negative-Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	(Includes V_{SET} Divider)			1	µA

Note 1: Connecting any terminal to voltages greater than (V_{IN}^{+} +0.3V) or less than (GND −0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663B power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

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INTERSIL

ORDERING INFORMATION

Negative Regulator		
ICL7664BCPA	0 to +70°C	8-pin MiniDIP
ICL7664BCTV	0 to +70°C	TO-99
ICL7664BC/D	0 to +70°C	DICE

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... −12V
Any Input or Output Voltage (Note 1) (GND +0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) ..... ($V_{\overline{IN}}$ −0.3V)
Output Source Current
(Terminal 1, 7) ..... −25mA
Power Dissipation (Note 2)
MiniDIP 200mW
TO-99 Can 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7664B OPERATING CHARACTERISTICS

$V_{\overline{IN}}$ = 9V, V_{OUT} = −5V, T_A = +25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Voltage	$V_{\overline{IN}}$	T_A = +25°C 0 ≤ T_A ≤ +70°C	−1.5 −1.6		−10 −10	V
Quiescent Current	I_Q	$R_L = \infty$ −1.4V ≤ V_{OUT} ≤ −8.5V		3.5	10	μA
Reference Voltage	V_{SET}		−1.2	−1.3	−1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	−8.5V < $V_{\overline{IN}}$ < −9V		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	−2V < $V_{\overline{IN}}$ < −9V		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	−0.3		−1.4	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	V_{CL} = V_{OUT2} − V_{SENSE} (Current-Limit Threshold)		−0.35		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	$V_{\overline{IN}}$ = 2V $V_{\overline{IN}}$ = 9V		150 40		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT1} = 100μA @ ΔI_{OUT} = −5V		2		Ω
Output Current V_{OUT1} or V_{OUT2}	I_{OUT}	$V_{\overline{IN}}$ = 3V V_{OUT} = V_{SET} $V_{\overline{IN}}$ = 9V V_{OUT} = −5V		−2 −20		mA
Minimum Load Current (Includes V_{SET} Divider)	$I_{L(min)}$				1	μA

Note 1: Connecting any terminal to voltages greater than (GND +0.3V) or less than ($V_{\overline{IN}}$ −0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664B power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

ICL7665

Micropower Under-/ Over-Voltage Detector

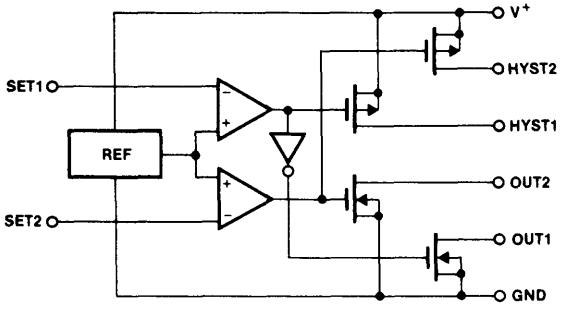
FEATURES

- **Exceptionally low supply current (<3μA typ)**
- **Individually programmable upper and lower trip voltages and hysteresis levels**
- **Accurate on-chip bandgap reference, used by both detectors**
- **Up to 20mA output current sinking ability**
- **Wide supply voltage range**

GENERAL DESCRIPTION

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only ~3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. Typical applications are battery-backup computer memories, battery-operated medical devices, radiation dosimeters, pocket pagers, portable calibrators and test instruments, and charging systems.

BLOCK DIAGRAM



Conditions*

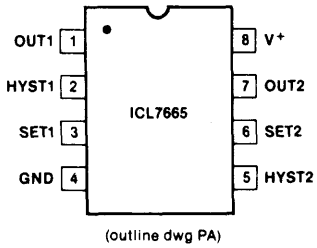
V_{SET1} > 1.3V, OUT1 switch ON	HYST1 switch ON
V_{SET1} < 1.3V, OUT1 switch OFF	HYST1 switch OFF
V_{SET2} > 1.3V, OUT2 switch OFF	HYST2 switch ON
V_{SET2} < 1.3V, OUT2 switch ON	HYST2 switch OFF

*See Operating Characteristics for exact thresholds.

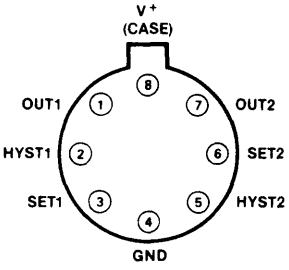
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665PA	– 20°C to + 70°C	8 Lead MiniDIP
ICL7665TV	– 20°C to + 70°C	8 Lead TO-99
ICL7665/D	—	DICE Only

PIN CONFIGURATIONS



(outline dwg PA)



(outline dwg TV)

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... −0.3V to +18V
Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2) ..... −0.3V to +18V
Output Voltages HYST1 and HYST2 (with respect to V^+) (Note 2) ..... +0.3V to −18V
Input Voltages SET1 and SET2 (Note 2) ..... (GND − 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current OUT1 and OUT2 ..... 25mA
Maximum Source Output Current HYST1 and HYST2 ..... −25mA
Power Dissipation (Note 1) 200mW
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ + 0.3V) or less than (GND − 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

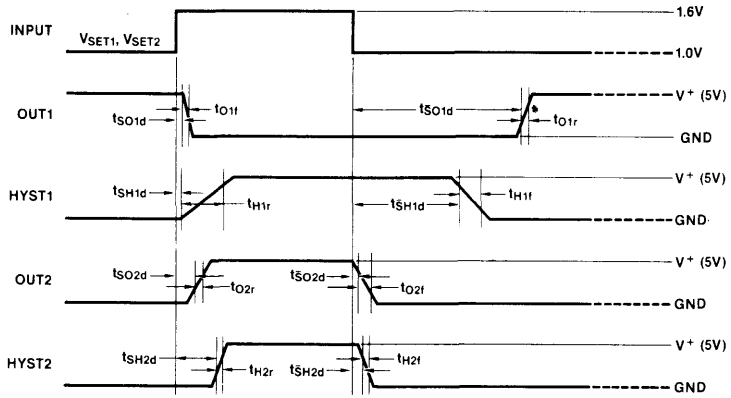
DC OPERATING CHARACTERISTICS (V^+ = 5V, T_A = +25°C, test circuit unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C −20°C ≤ T_A ≤ +70°C	1.6 1.8		16.0 16.0	V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V V^+ = 15V		 2.5 2.6 2.9	 10 10 15	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} ≈ 1 MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10 −10	200 −100	nA
	I_{OLK} I_{HLK}	V^+ = 15V, T_A = 70°C V^+ = 15V, T_A = 70°C			2000 −500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 15V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.2	V
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15 −0.05 −0.02	−0.3 −0.15 −0.10	
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.25	
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.25 −0.43 −0.35	−0.8 −1.0 −0.8	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	$V_{SET1} - V_{SET2}$	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

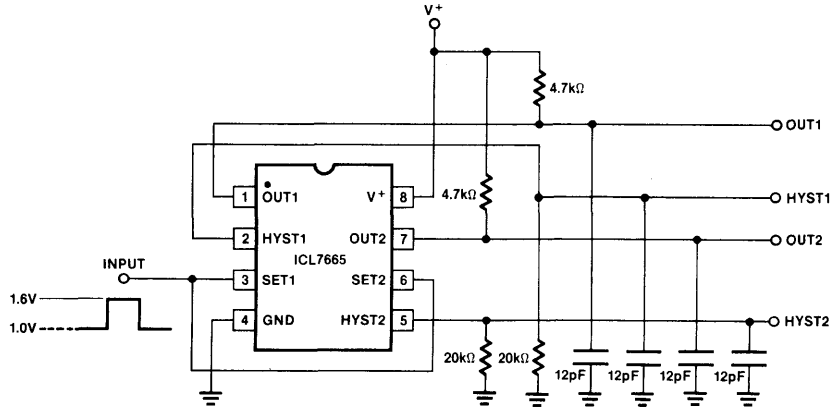
AC OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Output Delay Times Input Going HI	t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	V_{SET} Switched from 1.0V to 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		70 80 120 230		μs
Input Going LO	$t_{\overline{SO}1d}$ $t_{\overline{SH}1d}$ $t_{\overline{SO}2d}$ $t_{\overline{SH}2d}$	V_{SET} Switched from 1.6V to 1.0V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		1040 610 70 30		μs
Output Rise Times	t_{O1r} t_{O2r} t_{H1r} t_{H2r}	V_{SET} Switched between 1.0V and 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		120 80 330 25		μs
Output Fall Times	t_{O1f} t_{O2f} t_{H1f} t_{H2f}	V_{SET} Switched between 1.0V and 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		30 60 180 30		μs

SWITCHING WAVEFORMS

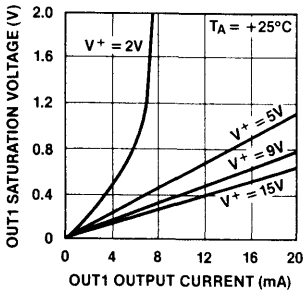


TEST CIRCUIT (Switching Response)

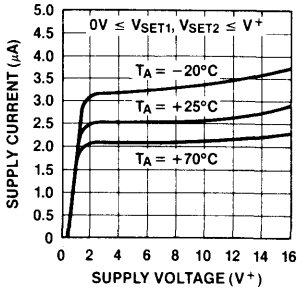


TYPICAL OPERATING CHARACTERISTICS

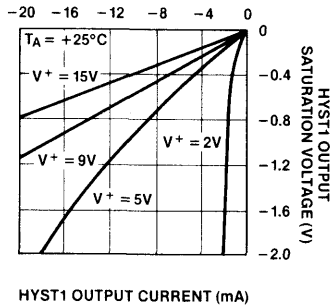
OUT1 Saturation Voltage as a Function of Output Current



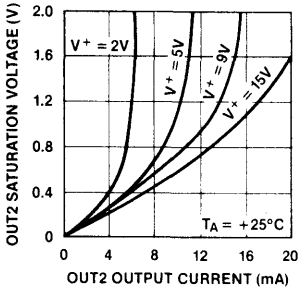
Supply Current as a Function of Supply Voltage



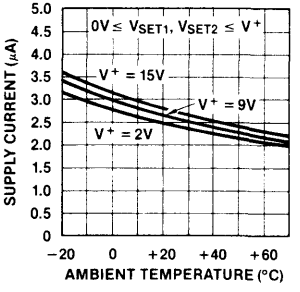
HYST1 Output Saturation Voltage vs HYST1 Output Current



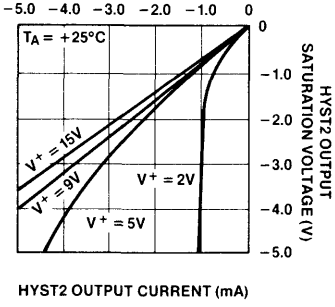
OUT2 Saturation Voltage as a Function of Output Current



Supply Current as a Function of Ambient Temperature



HYST2 Output Saturation Voltage vs HYST2 Output Current



5

DESCRIPTION

As shown in the Block Diagram, the ICL7665 consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal, so V_{SET1} will generally not quite equal V_{SET2}.

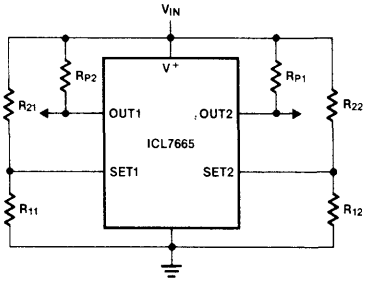
The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

PRECAUTIONS

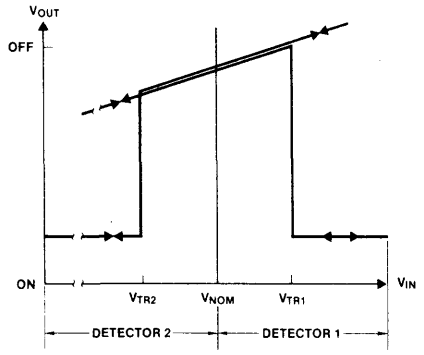
Junction-isolated CMOS devices like the ICL7665 have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low-current analog circuits, such as the ICL7665, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/μs in such a circuit. A low-impedance capacitor (e.g. 0.05μF disc ceramic) between the V^+ and GrouND pins of the ICL7665 can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V^+, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

APPLICATIONS



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 1. Simple Threshold Detector

Figure 1 shows the simplest connection of the ICL7665 for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are, from Figure 1(a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})} \qquad V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value of V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1 and}$$

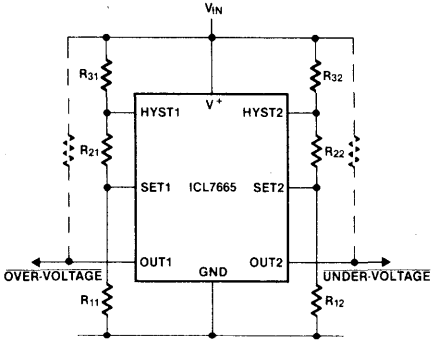
$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2.}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

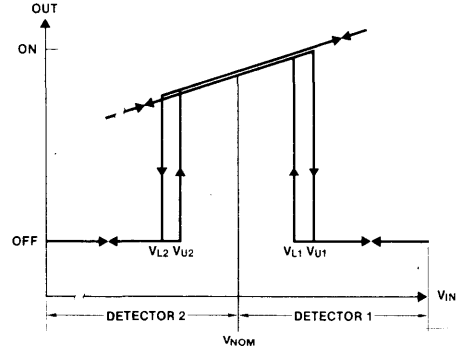
When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Figure 2(a) shows how to set up such hysteresis, while Figure 2(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n}, R_{2n} and R_{3n}, until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 3. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 2. Threshold Detector with Hysteresis

APPLICATIONS (Continued)

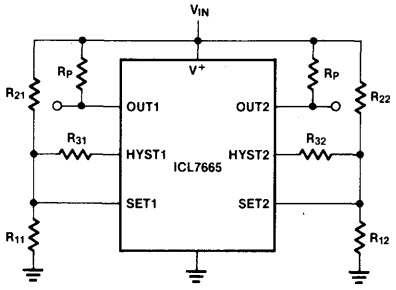
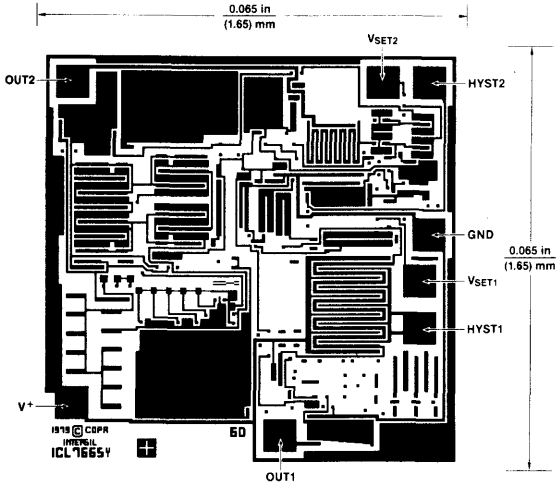


Figure 3. An Alternative Hysteresis Circuit

CHIP TOPOGRAPHY



ICL7665

Table 1. Set-Point Equations

a) NO HYSTERESIS

Over-Voltage $V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$

Under-Voltage $V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$

b) HYSTERESIS PER FIGURE 2A

Over-Voltage V_{TRIP}

$$V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$$

$$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

Under-Voltage V_{TRIP}

$$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$$

$$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

c) HYSTERESIS PER FIGURE 3

Over-Voltage V_{TRIP}

$$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$V_{L1} = \frac{R_{11} + \frac{R_{21}\,R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$$

Under-Voltage V_{TRIP}

$$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

$$V_{L1} = \frac{R_{12} + \frac{R_{22}\,R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$$

ICL7665B ADDENDUM TO THE ICL7665 DATASHEET

INTERSIL

This Addendum to the standard ICL7665 datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7665B device. The following table indicates those limits to which the ICL7665B is tested and/or guaranteed operational.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665BCPA	0 to +70°C	8 Lead MiniDIP
ICL7665BCTV	0 to +70°C	8 Lead TO-99
ICL7665BC/D	0 to +70°C	DICE Only

ABSOLUTE MAXIMUM RATINGS, ICL7665B

Supply Voltage ..... −0.3V to +12V
Output Voltages OUT1 and OUT2
(with respect to GND)(Note 2) ..... −0.3V to +12V
Output Voltages HYST1 and HYST2
(with respect to V^+)(Note 2) ..... +0.3V to −12V
Input Voltages SET1 and SET2
(Note 2) ..... (GND −0.3V) to (V^+ +0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... −25mA
Power Dissipation(Note 1) 200mW
Operating Temperature Range ..... 0 to +70°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS $V^+ = 5V, T_A = +25°C$, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	$T_A = +25°C$ $0 \leq T_A \leq +70°C$	1.6 1.8		10 10	V
Supply Current	I^+	$GND \leq V_{SET1}, V_{SET2} \leq V^+$ All Outputs Open Circuit $V^+ = 2V$ $V^+ = 9V$		 2.5 2.6	 10 10	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			± 200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	$R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1M\Omega$		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	$V_{SET} = 0V$ or $V_{SET} \geq 2V$		10 −10	200 −100	nA
	I_{OLK} I_{HLK}	$V^+ = 9V, T_A = 70°C$ $V^+ = 9V, T_A = 70°C$			2000 −500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	$V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA$ $V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA$ $V^+ = 9V, V_{SET1} = 2V, I_{OUT1} = 2mA$		0.2 0.1 0.06	0.5 0.3 0.25	V
	V_{HYST1} V_{HYST1} V_{HYST1}	$V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = -0.5mA$ $V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = -0.5mA$ $V^+ = 9V, V_{SET1} = 2V, I_{HYST1} = -0.5mA$		−0.15 −0.05 −0.02	−0.3 −0.15 −0.15	
	V_{OUT2} V_{OUT2} V_{OUT2}	$V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA$ $V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA$ $V^+ = 9V, V_{SET2} = 0V, I_{OUT2} = 2mA$		0.2 0.15 0.11	0.5 0.3 0.3	
	V_{HYST2} V_{HYST2} V_{HYST2}	$V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = -0.2mA$ $V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = -0.5mA$ $V^+ = 9V, V_{SET2} = 2V, I_{HYST2} = -0.5mA$		−0.25 −0.43 −0.35	−0.8 −1 −1	
V_{SET} Input Leakage Current	I_{SET}	$GND \leq V_{SET} \leq V^+$		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	$R_{OUT} = 4.7k\Omega, R_{HYST} = 20k\Omega$ $V_{OUT}LO = 1\% V^+, V_{OUT}HI = 99\% V^+$		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	$R_{OUT}, R_{HYST} = 1M\Omega$		±5	±50	
Output/Hysteresis Difference		$R_{OUT}, R_{HYST} = 1M\Omega$		±1		

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND −0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multipe supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

5

ICL7667
Dual Power MOS Driver

FEATURES

- 1.5A Peak Output Current
- Fast Rise and Fall Times
  — 40ns with 1000pF load
- Wide Supply Voltage Range
  — V_{CC} = 4.5 to 20V
- Low Power Consumption
  — 4mW with inputs low
  — 120mW with inputs high
- TTL/CMOS Input Compatible Power Driver
  — R_{OUT} = 6Ω
- Direct Interface with Common Switching Regulators
- Pin Equivalent to DS0026/DS0056

TYPICAL APPLICATIONS

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

GENERAL DESCRIPTION

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 20V. Its high speed and 1.5A peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 20V, the ICL7667 is well suited for driving power MOSFETs in high frequency switching regulators. The ICL7667's high current (1.5A peak) outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitances, while the ICL7667's inputs are TTL compatible and can be directly driven by common switching regulator IC's.

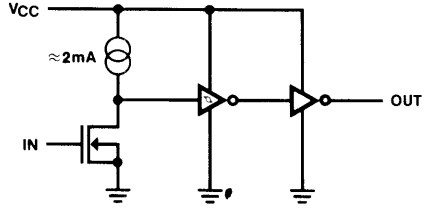
5

ORDERING INFORMATION

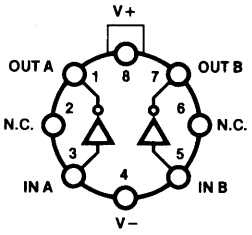
Temperature Range	Package	Order Number
−55°C to +125°C	TO-99 Can	ICL7667MTV
	8-Pin Cerdip	ICL7667MJA
0 to +70°C	8-Pin Plastic	ICL7667CPA
	8-Pin Cerdip	ICL7667CJA
	TO-99 Can	ICL7667CJA
0 to +70°C	Dice	ICL7667C/D

(pin configuration for TV and PA packages also on this page)

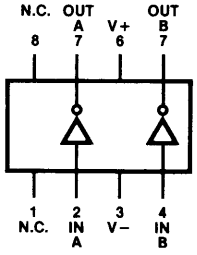
BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW
TO-99
(TV)



TOP VIEW
8-PIN DIP
(PA, JA)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Input Voltage ..... 22V to (V^- −0.3V)
Peak Output Current 1.5A
Package Dissipation, T_A = 25°C 500mW
Linear Derating Factors

TO-99	Plastic	Cerdip
6.7mW/°C	5.6mW/°C	6.7mW/°C
above 50°C	above 36°C	above 50°C

Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Operating Temperature Range
C Series ..... 0 to +70°C
M Series ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS

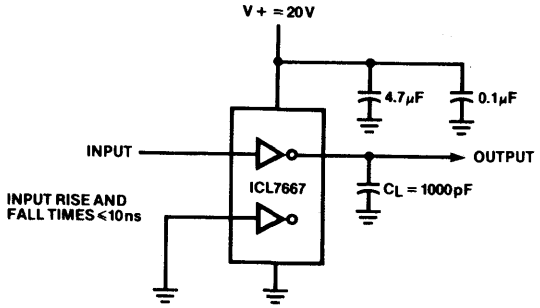
Test Conditions: V_{CC} = 4.5 to 20V, T_A = +25°C unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Logic 1 Input Voltage	V_{IH}		2.4	2.0		V
Logic 0 Input Voltage	V_{IL}			1.5	0.8	V
Input Current	I_{IL}	$0 < V_{IN} < V_{CC}$	−1	0	1	μA
Output Voltage High	V_{OH}	No Load	V_{CC} −0.05	V_{CC}		V
Output Voltage Low	V_{OL}	No Load		0	0.05	V
Output Resistance	R_{OUT}	$V_{IN} = V_{IL}$ I_{OUT} = −10mA V_{CC} = 20V		6	20	Ω
Output Resistance	R_{OUT}	$V_{IN} = V_{IH}$ I_{OUT} = 10mA V_{CC} = 20V		6	20	Ω
Power Supply Current	I_{CC}	V_{IN} = 3V (both inputs)		4	6	mA
Power Supply Current	I_{CC}	V_{IN} = 0V (both inputs)		150	400	μA

AC OPERATING CHARACTERISTICS

Test Conditions: V_{CC} = 20V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Delay Time	T_{D2}	Figure 1		50	75	ns
Delay Time	T_{D2}	Figure 2		50	75	ns
Rise Time	T_R	Figure 1		25	35	ns
Rise Time	T_R	Figure 2		35	50	ns
Fall Time	T_F	Figure 1		30	40	ns
Fall Time	T_F	Figure 2		40	55	ns
Delay Time	T_{D1}	Figure 1		20	35	ns
Delay Time	T_{D1}	Figure 2		20	35	ns



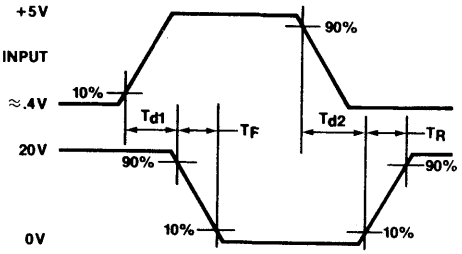
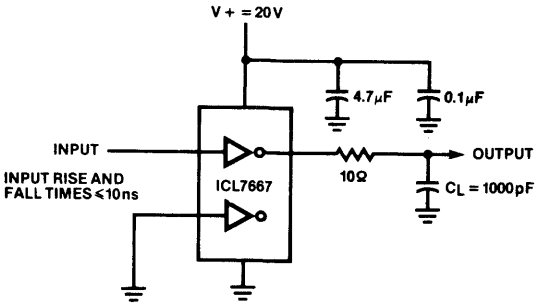


Figure 1. Test Circuit



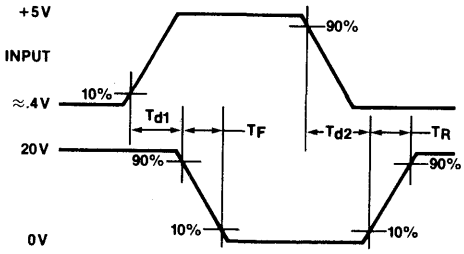
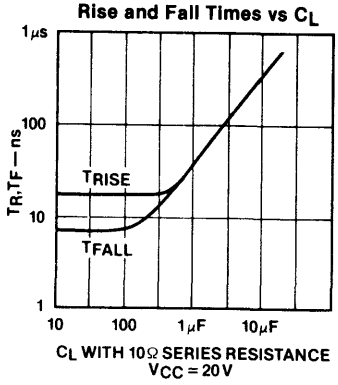
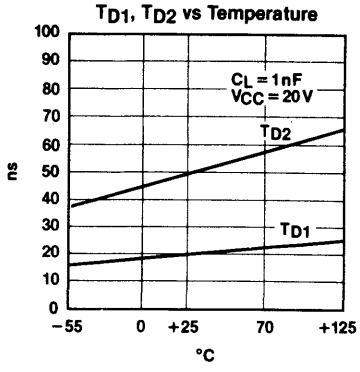


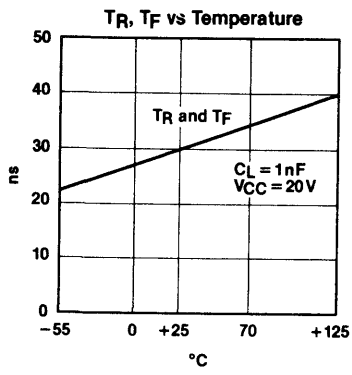
Figure 2. Test Circuit

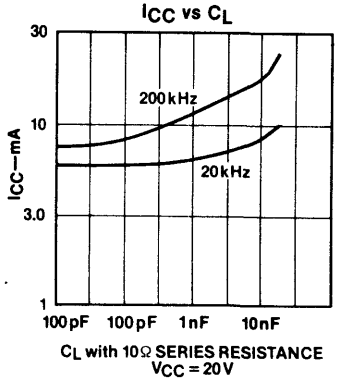
5

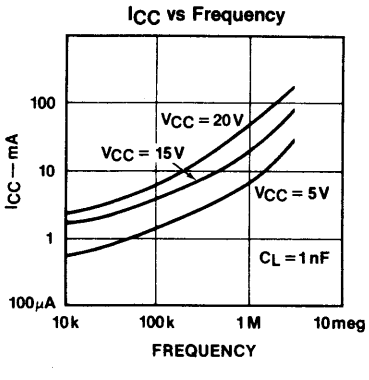
TYPICAL CHARACTERISTICS

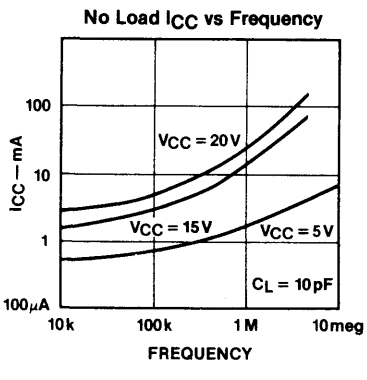




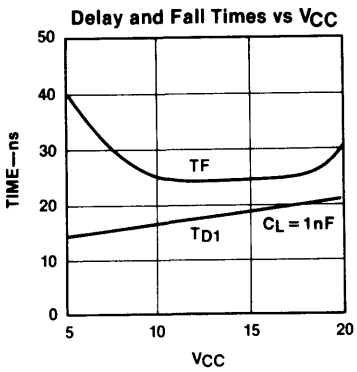


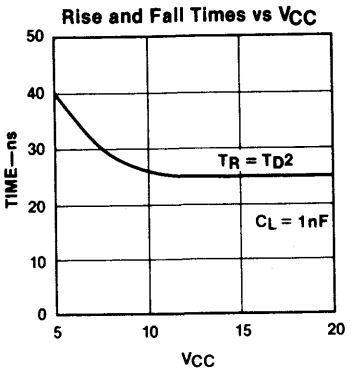






TYPICAL CHARACTERISTICS (Cont'd)





DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 20V. Its 1.5A peak output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC}, without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at $V_{CC} = 20V$, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge pump voltage inverters.

INPUT STAGE

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V_{CC} voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5-20V V_{CC} range. Being CMOS, the inputs draw less than 1μA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 6mA maximum when both inputs are the 1 logic level. A small amount of hysteresis, about 50-100mV at the input, is generated by positive feedback around the second stage.

OUTPUT STAGE

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V_{CC}. At $V_{CC} = 20V$, the output impedance of the inverter is typically 6Ω, with a peak current output of typically 1.5A. It is this high peak current capability that enables the ICL7667 to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V_{CC} to ground) during output transitions. This "crowbar" current is a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1μs.

APPLICATION NOTES

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

5

GROUNDING

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will be negative feedback, degrading the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

BYPASSING

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7μF capacitor in parallel with a low inductance 0.1μF capacitor is usually sufficient bypassing.

OUTPUT DAMPING

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1) Reduce inductance by making printed circuit board traces as short as possible.

2) Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.

3) Use a 10 to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.

4) Use good bypassing techniques to prevent ringing caused by supply voltage ringing.

POWER DISSIPATION

The power dissipation of the ICL7667 has three main components:

1) Input inverter current
2) Output stage crowbar current
3) Output stage I^2R power

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.2mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. To reduce the average power dissipation in the output stage due to transitions, the input signal rise time should be less than 1μs. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2F$$

Where C = Load Capacitance
F = Frequency

In cases where the load is a power MOSFET and the gate drive requirements are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}F$$

Where Q_G = Charge required to switch the gate, in Coulombs.
F = Frequency

POWER MOS DRIVER CIRCUITS

POWER MOS DRIVER REQUIREMENTS

Because it has very high peak current output, the ICL7667 excels at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 3 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

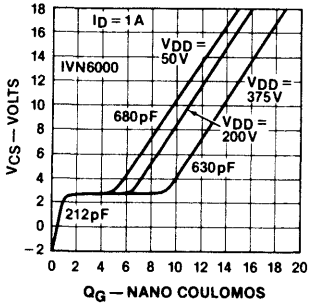


Figure 3. MOSFET Gate Dynamic Characteristics

DIRECT DRIVE OF MOSFETs

Figure 4 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speed-up capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

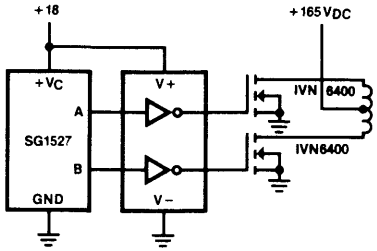


Figure 4a. Direct Drive of MOSFET Gates

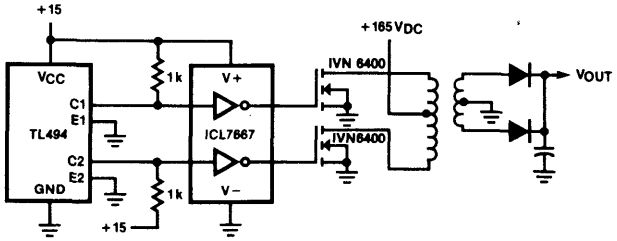


Figure 4b. Direct Drive of MOSFET Gates

TRANSFORMER COUPLED DRIVE OF MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 5 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low outputs can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

In this circuit, the transformer is driven with a symmetrical waveform, so the secondary voltage outputs are determined only by the turns ratio and the power supply voltage to the ICL7667. If the transformer drive is not symmetrical, the voltage output will be affected by the duty cycle, being highest for low duty cycles.

BUFFERED DRIVERS FOR MULTIPLE MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 6 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{gs} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

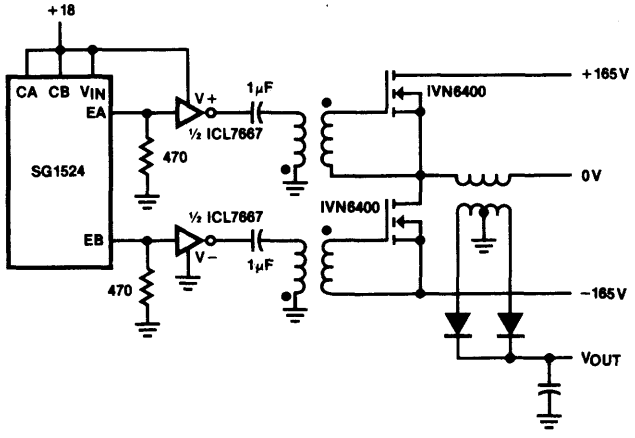
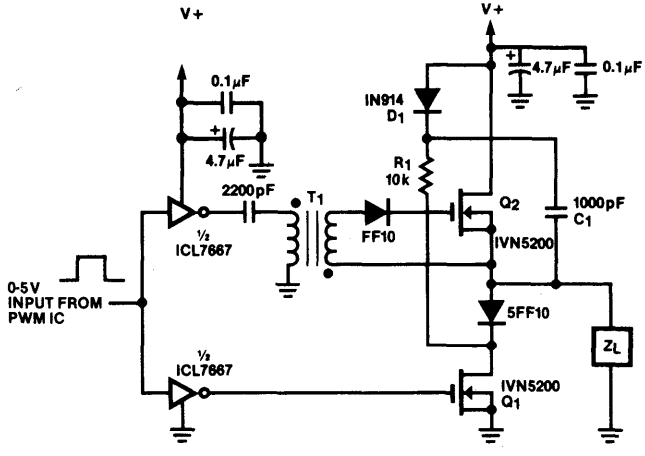


Figure 5. Transformer Coupled Drive



T1 — IS THREE TURNS 30 BIFILAR ON A FERRITE BEAD.

Figure 6. Very High-Speed Driver

OTHER APPLICATIONS

RELAY AND LAMP DRIVERS

The ICL7667 is suitable for converting low power TTL or CMOS signals to high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

CHARGE PUMP OR VOLTAGE INVERTERS AND DOUBLERS

The low output impedance and wide V_{CC} range of the ICL7667 make it well suited for charge pump circuits. Figure 7 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at −12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

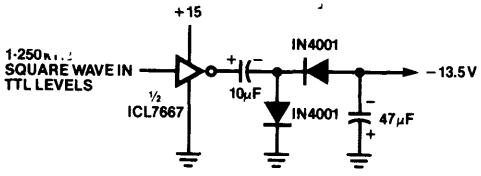


Figure 7a. Voltage Inverter

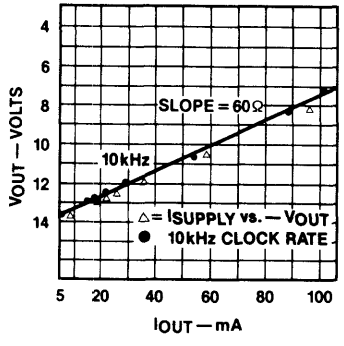


Figure 7b. Voltage Inverter

Figure 8, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

CLOCK DRIVER

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15 or 20V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

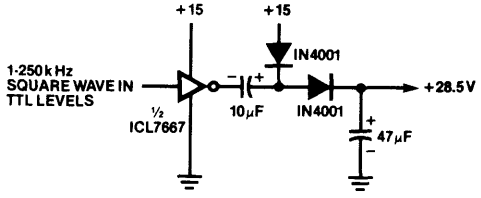
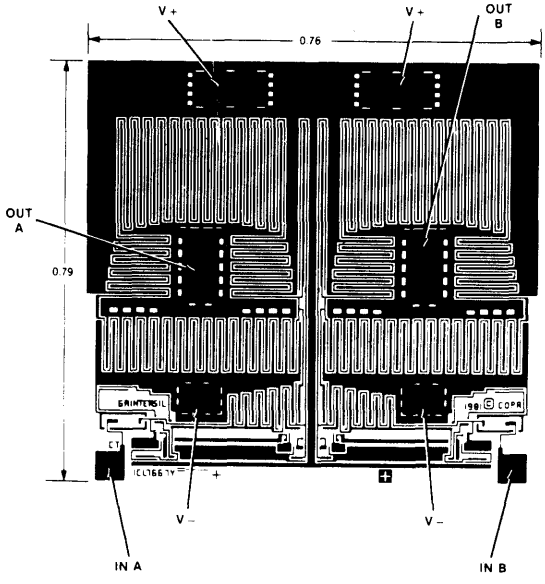


Figure 8. Voltage Doubler

CHIP TOPOGRAPHY



ICL8001
Precision Comparator

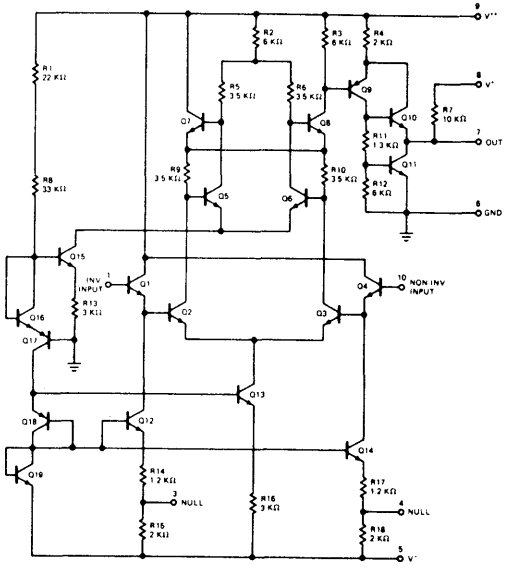
FEATURES

- Low Input Current $\leq$ 250 nA
- Low Power Consumption 30 mW
- Large Input Voltage Range $\geq \pm$10V
- Low Offset Voltage Drift 3 μV/°C
- Output Swing Compatible with Bipolar Logic

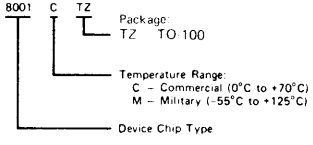
GENERAL DESCRIPTION

The Intersil 8001 integrated circuit is a monolithic voltage comparator featuring low input currents, low power consumption, and 250 ns response time. A versatile output stage enables the designer to control the output voltage swing. The use of thin film resistors ensures excellent long term stability and the device is particularly suitable for low power space and airborne applications.

SCHEMATIC DIAGRAM



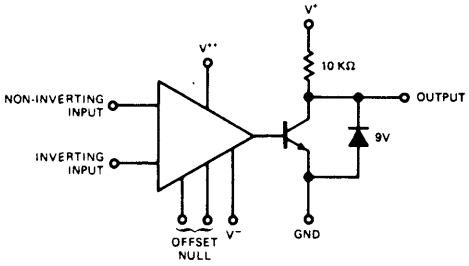
ORDERING INFORMATION



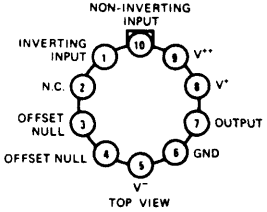
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage (Note 2)	±18V
Differential Input Voltage	±15V
Internal Power Dissipation (Note 1)	500 mW
Peak Output Current	15 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
(8001C)	0°C to +70°C
(8001M)	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

EQUIVALENT CIRCUIT



PIN CONFIGURATION



TOP VIEW

(outline dwg TO-100)

NOTE: Pin 5 connected to case.

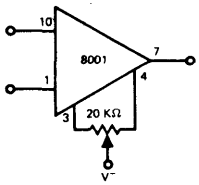
For notes and additional electrical characteristics, see next page.

ELECTRICAL CHARACTERISTICS (V^{++} = 15V, V^+ = 5V, V^- = -15V unless otherwise specified)

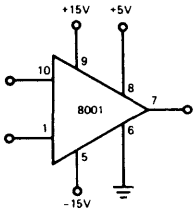
PARAMETER	CONDITIONS	8001M MIN	8001M TYP	8001M MAX	8001C MIN	8001C TYP	8001C MAX	UNITS
The following specifications apply for T_A = +25°C:								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			2	20		10	50	nA
Input Bias Current			40	100		50	250	nA
Input Resistance			10			10		MΩ
Power Consumption	V_{OUT} = 2.5V		30	60		30	60	mW
The following specifications apply for -55°C ≤ T_A ≤ +125°C (8001M) 0°C ≤ T_A ≤ +70°C (8001C)								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			4.0			6.0	mV
Average Temperature Coefficient of Input Offset Voltage			2.0	20		3.0	30	µV/°C
Input Offset Current			7	100		15	100	nA
Average Temperature Coefficient of Input Offset Current			35			35		pA/°C
Input Bias Current				250			300	nA
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio				300			300	µV/V
Differential Input Voltage Range				±15			±15	V
Voltage Gain		15,000	60,000		15,000	60,000		V/V
Positive Output Level Max (Note 3)	V^+ = +15V	7.0	9.0		7.0	9.0		V
Negative Output Level	At 2 mA Sink Current		200	500		200	400	mV
Response Time (Note 4)			250			250		ns

NOTE 1: Rating applies for ambient temperatures to +70°C.
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 3: Positive output level can be adjusted below 9V by changing V^+. See circuit.
NOTE 4: The response time specified is for a 100 mV input step with 5 mV overdrive.
NOTE 5: Input bias current is independent of V^-.

CIRCUIT NOTES:



VOLTAGE OFFSET NULL CIRCUIT

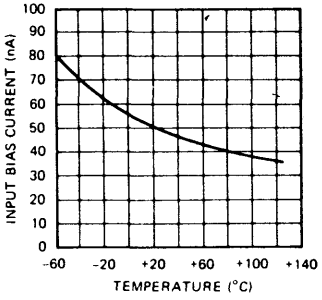


OUTPUT LEVEL COMPATIBLE WITH TTL, DTL, ETC.

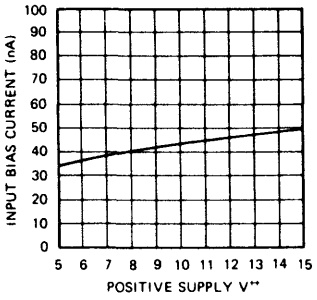
NOTE: As with all high gain comparators, care must be taken to avoid feedback between output and input. Where possible, hysteresis should be used to provide a small deadband.

TYPICAL PERFORMANCE CURVES

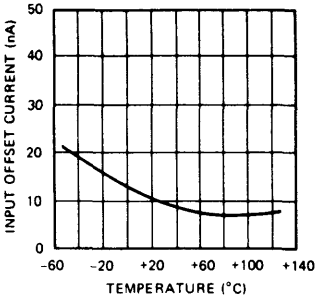
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



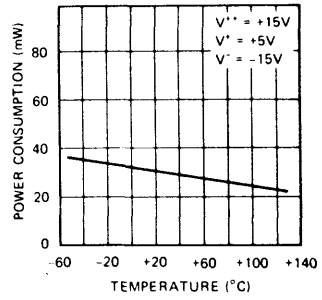
INPUT BIAS CURRENT AS A FUNCTION OF V^{++} (NOTE 5)



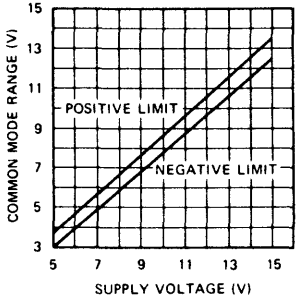
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



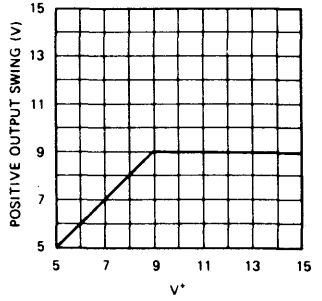
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



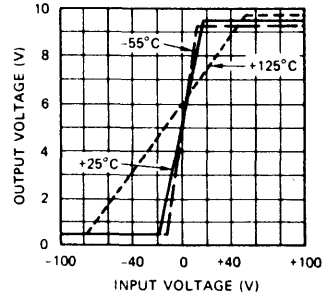
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



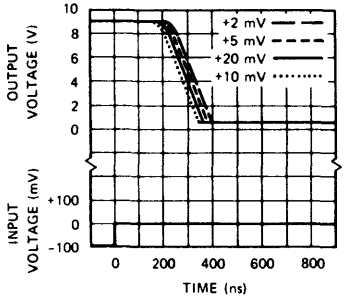
POSITIVE OUTPUT SWING AS A FUNCTION OF V^{+}



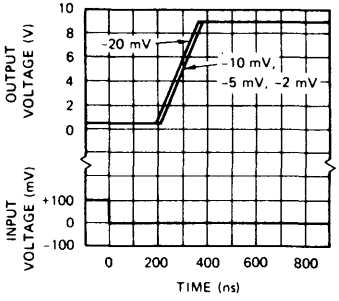
VOLTAGE TRANSFER CHARACTERISTICS



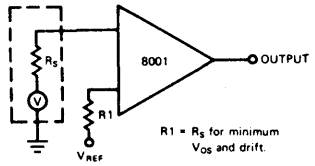
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



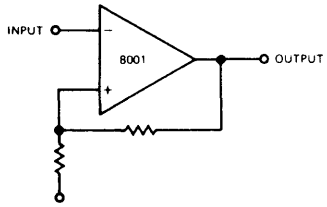
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



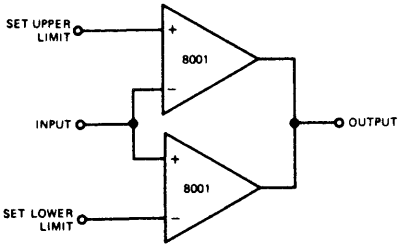
CIRCUIT AND APPLICATION NOTES



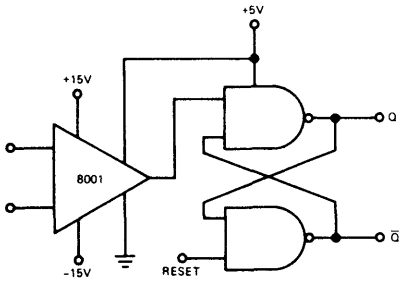
SIMPLE VOLTAGE LEVEL DETECTOR



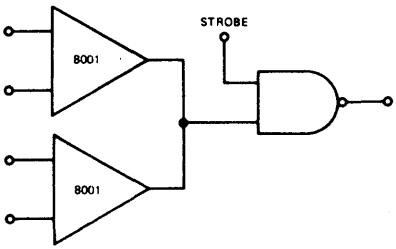
COMPARATOR WITH HYSTERESIS



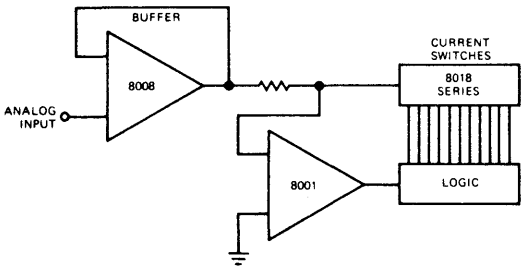
CONNECTION TO PROVIDE LOGICAL OR OF TWO COMPARATOR OUTPUTS



USE OF EXTERNAL NAND GATES TO PROVIDE OUTPUT STORAGE



WINDOW DETECTOR



A TO D CONVERTER

ICL8007
FET Input Operational Amplifier

GENERAL DESCRIPTION

The Intersil 8007 integrated circuit is a low input current FET input operational amplifier. The 8007A is selected for 4 pA max input current.

The devices are designed for use in very high input impedance applications. Because of their high slew rate, high common mode voltage range and absence of "latch-up", they are ideal for use as a voltage follower.

The Intersil 8007 and 8007A are short circuit protected. They require no external components for frequency compensation because the internal 6 dB/roll-off insures stability in closed loop applications. A unique bootstrap circuit insures unusually good commonmode rejection for an FET input amp and prevents large input currents as seen in some amplifiers at high common mode voltage.

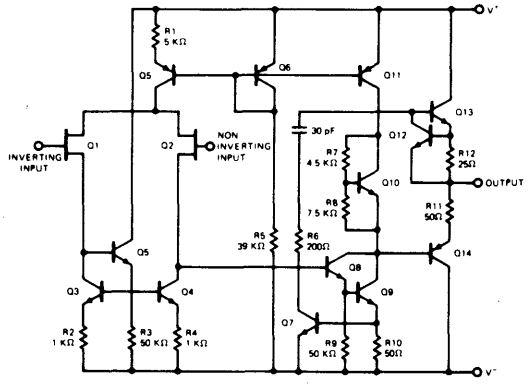
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
8007M, 8007AM	-55°C to +125°C
8007C, 8007AC	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

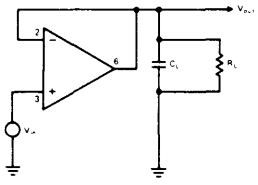
NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

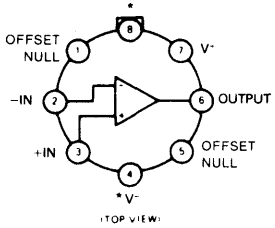
EQUIVALENT CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



PIN CONFIGURATION (outline dwg TV, TY)*



*ICL8007M/C pin 4 connected to case (TY package)
ICL8007AM/C, pin 8 connected to case (TV package)

ORDERING INFORMATION

Part Number	Temperature Range	dice	To-99 Can
ICL8007C ICL8007AC	0°C to +70°C	ICL8007C/D ICL8007AC/D	ICL8007CTY ICL8007ACTV
ICL8007M ICL8007AM	-55°C to +125°C	ICL8007M/D ICL8007AM/D	ICL8007MTY ICL8007AMTV*

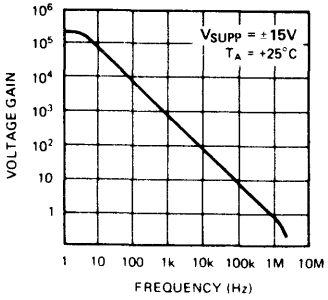
* Add /883B to order number if 883B processing is desired.

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

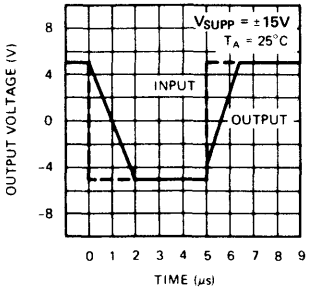
CHARACTERISTICS	CONDITIONS	8007M			8007C			8007AM & 8007AC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:											
Input Offset Voltage	$R_S \leq 100\ k\Omega$		10	20		20	50		15	30	mV
Input Offset Current			0.5			0.5			0.2		pA
Input Current (either input)			2.0	20		3.0	50		0.5	4.0	pA
Input Resistance			10^6			10^6			10^6		MΩ
Input Capacitance			2.0			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	50,000			20,000			20,000			V/V
Output Resistance			75			75			75		Ω
Output Short-Circuit Current			25			25			25		mA
Supply Current			3.4	5.2		3.4	6.0		3.4	6.0	mA
Power Consumption			102	156		102	180		102	180	mW
Slew Rate			6.0			6.0		2.5	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100\ pF$, $R_L = 2\ k\Omega$										
Risetime			300			300			300		ns
Overshoot			10			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8007C and 8007AC), −55°C ≤ T_A ≤ +125°C (8007M and 8007AM):											
Input Voltage Range		±10	±12		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		86	95		dB
Supply Voltage Rejection Ratio			70	300		70	600		70	200	μV/V
Large Signal Voltage Gain		25,000			15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		±10	±13		V
Input Current (either input)	T_A = +125°C		2.0						1.0		nA
	T_A = +70°C					50			30		pA
Average Temperature Coefficient of Input Offset Voltage				75			75			50	μV/°C

TYPICAL PERFORMANCE CURVES

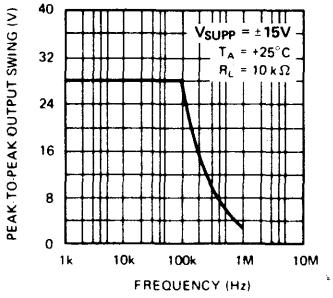
OPEN LOOP VOLTAGE GAIN



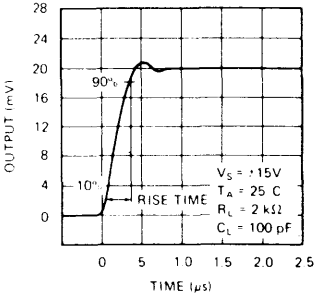
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



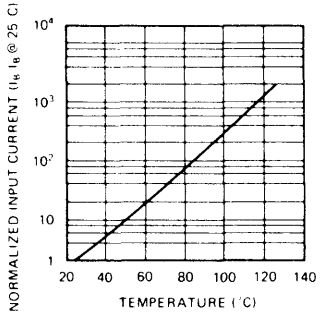
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



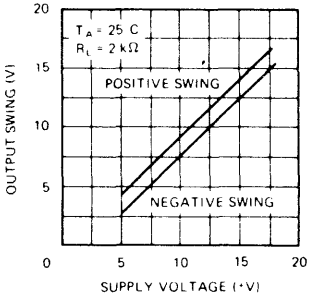
TRANSIENT RESPONSE



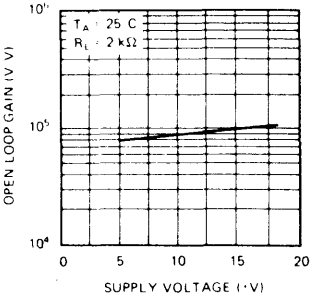
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



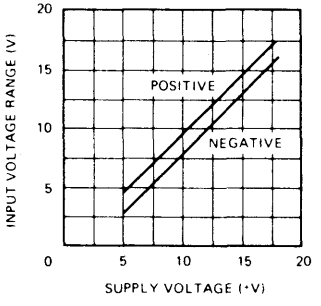
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



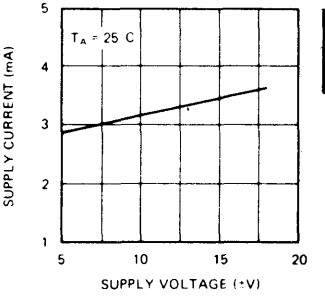
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



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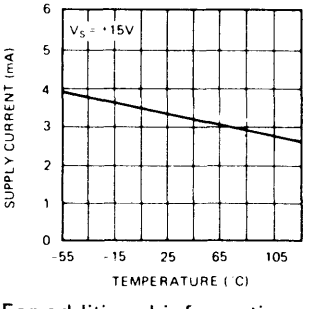
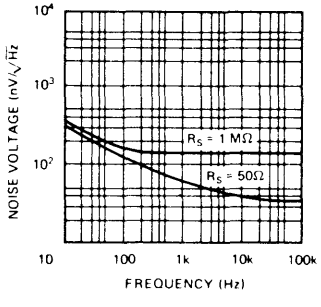
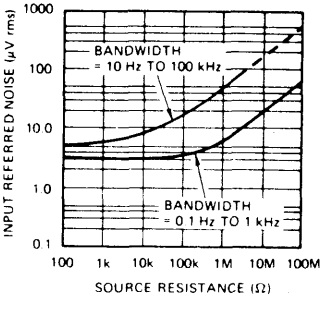
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



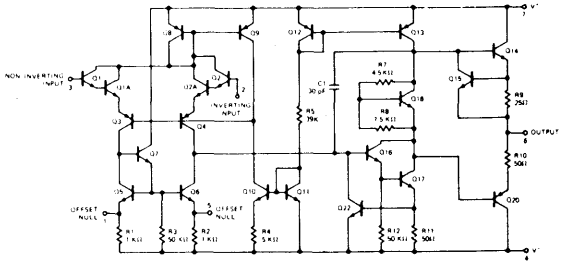
For additional information, see Application Bulletin A005.

ICL8008
Low Input Current Operational Amplifier

FEATURES

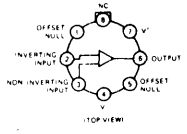
- Low Input Current
- No Frequency Compensation Required
- Offset Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch up

SCHEMATIC DIAGRAM



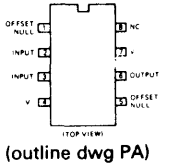
PIN CONFIGURATIONS

TO-5



(outline dwg TY)

Plastic DIP



(outline dwg PA)

NOTE: Pin 4 CONNECTED TO CASE

GENERAL DESCRIPTION

The 8008 is a high performance monolithic operational amplifier with very low input currents. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the 8008 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 8008 is short-circuit protected, has the same pin configuration as the popular 741 operational amplifier, and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V⁻	±0.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
8008M	-55°C to +125°C
8008C	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

NOTE 1: Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

ORDERING INFORMATION

ICL8008 M TY

Package:
TY—TO-99 metal can
PA—8 Pin Plastic DIP (Available only at Commercial Temperature Range) ID Dice

Temperature Range:
M—Military -55°C to +125°C
C—Commercial 0°C to +70°C

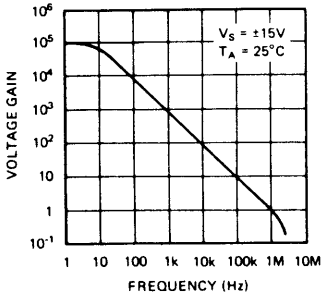
Device Type

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

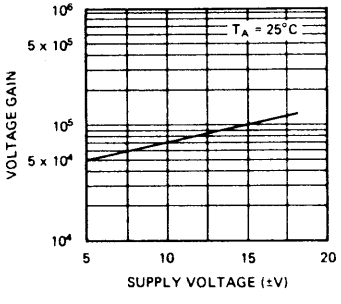
CHARACTERISTICS	CONDITIONS	8008M			8008C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5		1.0	6.0	mV
Input Offset Current			1.0	5		2.0	20	nA
Input Bias Current			2	10		5	25	nA
Input Resistance		5	25		5	25		MΩ
Input Capacitance			1.5			1.5		pF
Offset Voltage Adjustment Range			±15			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	20,000	200,000		20,000	200,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{IN} = 20 mV, R_L = 2 kΩ,							
Risetime	$C_L \leq 100$ pF		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geq 2\ k\Omega$		0.5			0.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8008C), −55°C ≤ T_A ≤ +125°C (8008M):								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.5	6		1.5	7.5	mV
Input Offset Voltage Average Temperature Coefficient	$R_S \leq 10\ k\Omega$		7			15		μV/°C
Input Offset Current				30			30	nA
Input Bias Current				50			50	nA
Input Voltage Range		±10	±12		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V

TYPICAL PERFORMANCE CURVES

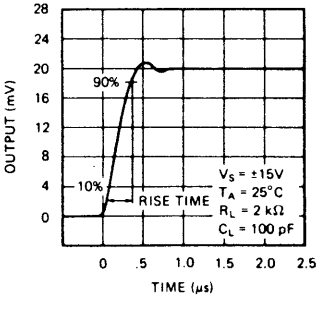
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

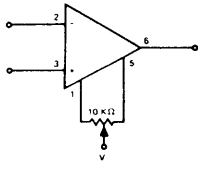


TRANSIENT RESPONSE

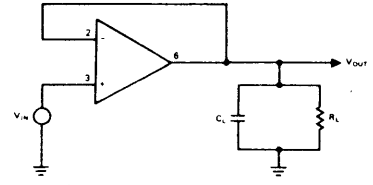


CIRCUIT NOTES:

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



ICL8013

Four Quadrant Analog Multiplier

FEATURES

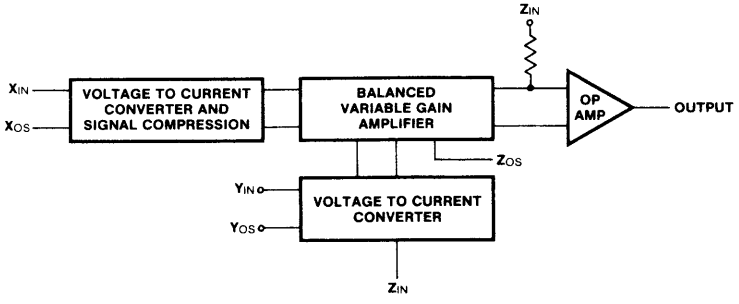
- **Accuracy of ±0.5% ("A" version)**
- **Full ±10V I/O voltage range**
- **1 MHz bandwidth**
- **Uses standard ±15V supplies**
- **Built in op amp provides level shifting, division and square root functions.**

GENERAL DESCRIPTION

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 makes it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and systems process controls.

5

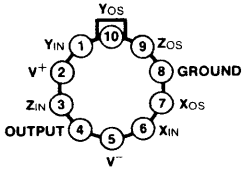
BLOCK DIAGRAM (MULTIPLIER)



ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	MULTIPLICATION ERROR		ORDER PART NUMBER
ICL8013AM	−55°C to +125°C	±.5%	MAX	ICL8013AM TZ
ICL8013BM	−55°C to +125°C	±1%		ICL8013BM TZ
ICL8013CM	−55°C to +125°C	±2%		ICL8013CM TZ
ICL8013AC	0°C to +70°C	±.5%	MAX	ICL8013AC TZ
ICL8013BC	0°C to +70°C	±1%		ICL8013BC TZ
ICL8013CC	0°C to +70°C	±2%		ICL8013CC TZ
DICE	0°C to +70°C	±2% TYP		ICL8013C/D

PIN CONFIGURATION



TOP VIEW

(outline dwg TO-100)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Note 1) ..... 500 mW
Input Voltages (X, Y, Z, X_O, Y_O, Z_O) ..... V_{SUPP}
Lead Temperature (soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C

NOTE 1: Derate at 6.8 mW/°C for operation at ambient temperature above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified T_A = 25°C, V_{SUPP} = ±15V, Gain and Offset Potentiometers Externally Trimmed)

PARAMETER	CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	−10 < X < 10 −10 < Y < 10			.5			1.0		2.0*	2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	X = −10 X = −1		0.3 1.5			0.3 1.5			0.3 1.5		% Full Scale % Full Scale
Feedthrough	X = 0 Y = $20V_{p-p}$ f = 50Hz Y = 0 X = $20V_{p-p}$ f = 50Hz			50 50			100 100		200* 150*	200 150	mV_{p-p} mV_{p-p}
Nonlinearity X Input	X = $20V_{p-p}$ Y = ±10Vdc		±0.5			±0.5			±0.8		%
Y Input	Y = $20V_{p-p}$ X = ±10Vdc		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (−3dB)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/μs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Phase Shift)			5			5			5		kHz
Settling Time (to ±2% of Final Value)	V_{IN} = ±10V		1			1			1		μs
Overload Recovery (to ±2% of Final Value)			1			1			1		μs
Output Noise	5 Hz to 10 kHz 5 Hz to 5 MHz		0.6 3			0.6 3			0.6 3		mV rms mV rms
Input Resistance X Input			10			10			10		MΩ
Y Input			6			6			6		MΩ
Z Input			36			36			36		kΩ
Input Bias Current X or Y Input			2	5			7.5			10	μA
Z Input			25			25			25		μA
Power Supply Variation Multiplication Error			0.2			0.2			0.2		%/%
Output Offset				50			75			100	mV/V
Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	−10 < X < 10, −10 < Y < 10		1.5			2			3		% Full Scale
Average Temperature Coefficient of Accuracy			0.06			0.06			0.06		%/°C
Output Offset			0.2			0.2			0.2		mV/°C
Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current X or Y Input				5			5			10	μA
Z Input				25			25			35	μA
Input Voltage (X, Y, or Z)				±10			±10			±10	V
Output Voltage Swing	$R_L \geq 2k$ C_L < 1000 pF		±10			±10			±10		V

*Dice only

CIRCUIT DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 1.

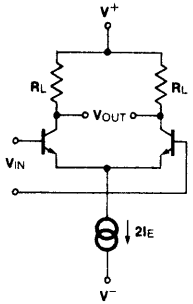


Figure 1: Differential Amplifier

The small signal differential voltage gain of this circuit is given by

$$AV = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{I}{g_m} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN}\ \frac{R_L}{r_e} = V_{IN} \bullet \frac{qI_E\ R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 2, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \simeq \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y}\ (V_X \bullet V_Y)$$

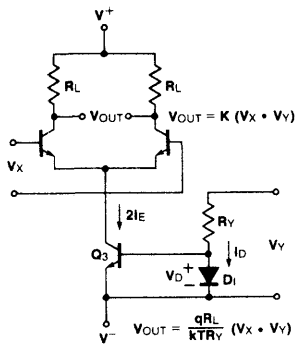


Figure 2: Transconductance Multiplier

There are several difficulties with this simple modulator:

1: V_Y must be positive and greater than V_D

2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.

3: V_X must be a small signal for the differential pair to be linear.

4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 3, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ±10 volts with excellent linearity.

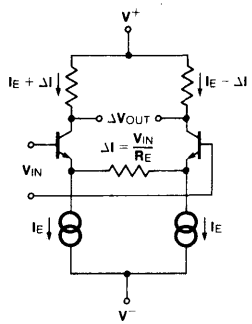


Figure 3: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 4A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 4A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

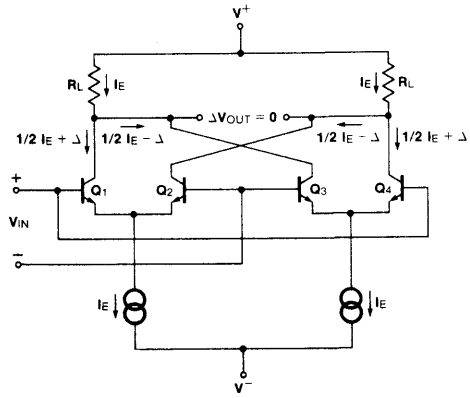


Figure 4A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

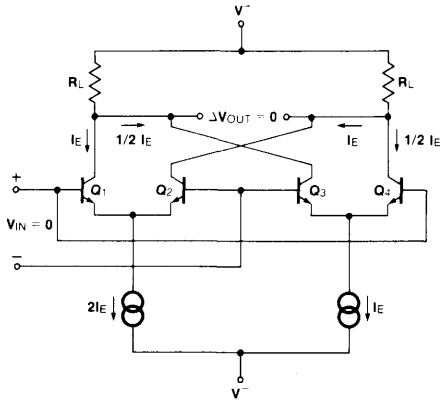


Figure 4B: No Input Signal with Unbalanced Current Sources
$\Delta V_{OUT} = 0V$

In Figure 4B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 4C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2}, the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 3 we have a balanced multiplier circuit capable of four quadrant operation (Figure 5).

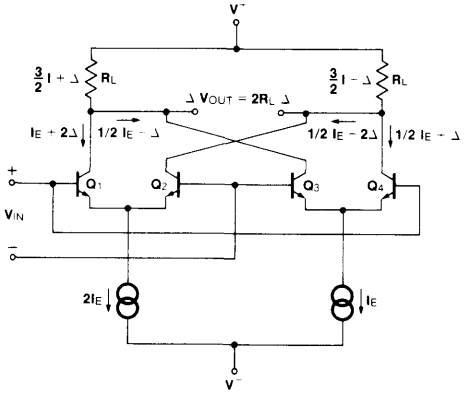


Figure 4C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

This circuit of Fig. 5 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

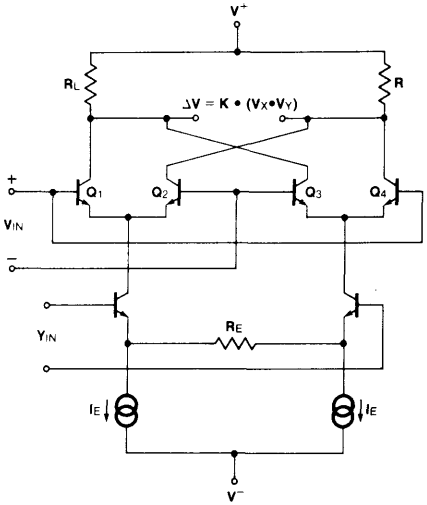


Figure 5: Typical Four Quadrant Multiplier-Modulator

Figure 3 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Fig. 6A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 6A is the

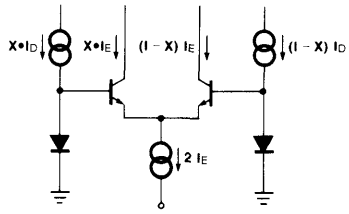


Figure 6A: Current Gain Cell

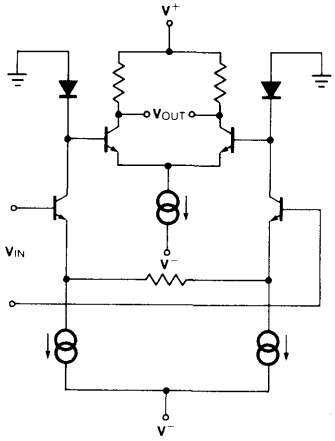


Figure 6B: Voltage Gain with Signal Compression

difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Fig. 3, we have Fig. 6B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 7. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

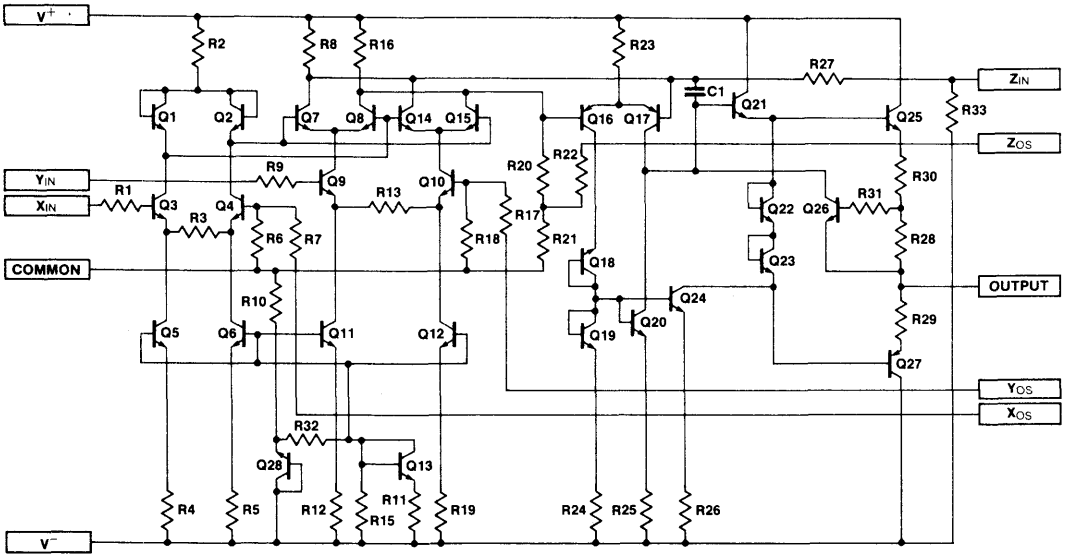


Figure 7: ICL8013 Schematic

MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

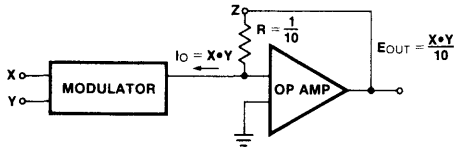


Figure 8A: Multiplier Block Diagram

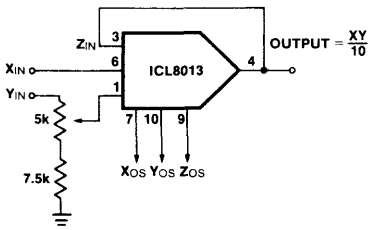


Figure 8B: Actual Circuit Connection

MULTIPLIER Trimming Procedure

1. Set X_{IN} = Y_{IN} = 0V and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤100Hz) sweep (sine or triangle) to Y_{IN} with X_{IN} = 0V, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with Y_{IN} = 0V and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With X_{IN} = 10.0V DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output − Y_{IN}) = Zero.

DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X \bullet Y = \frac{Z}{R} = 10Z$$

$$\text{Since } Y = E_{OUT},\ E_{OUT} = \frac{10Z}{X}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

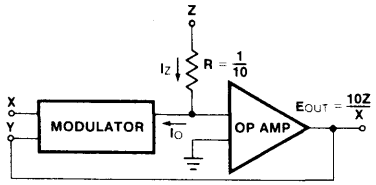


Figure 9A: Division Block Diagram

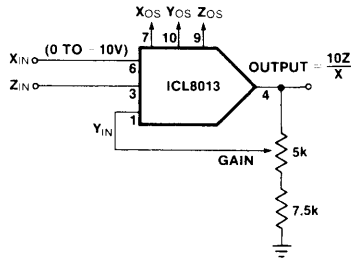


Figure 9B: Actual Circuit Connection

DIVIDER Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With Z_{IN} = 0V, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from −10V through −1V.
3. With Z_{IN} = 0V and X_{IN} = −10.0V adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from −10V to −1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (−10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from −10V to −3V.

SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2 \omega = 1/2 (\cos 2\omega + 1)$.

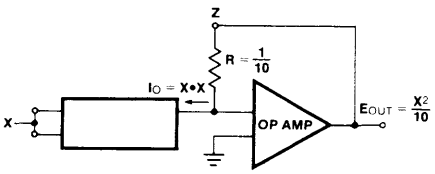


Figure 10A: Squarer Block Diagram

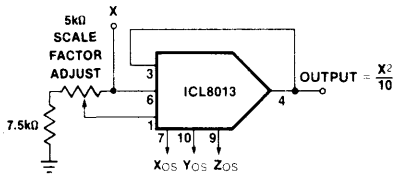


Figure 10B: Actual Circuit Connection

SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X \bullet Y = (-E_{OUT})^2 = 10Z$$

$$E_{OUT} = -\sqrt{10Z}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.

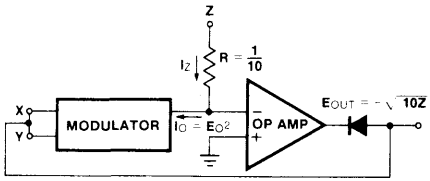


Figure 11A: Square Root Block Diagram

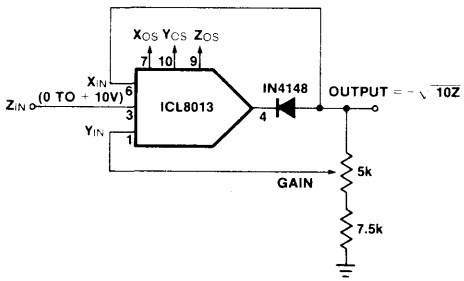


Figure 11B: Actual Circuit Connection

SQUARE ROOT Trimming Procedure

1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

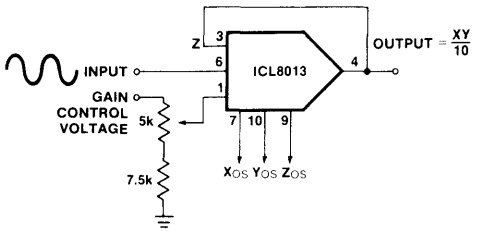
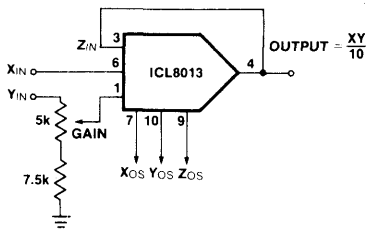


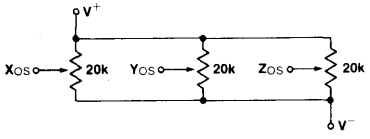
Figure 12: Variable Gain Amplifier

TYPICAL APPLICATIONS

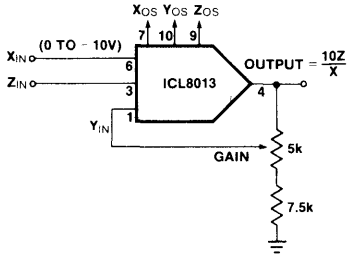
MULTIPLICATION



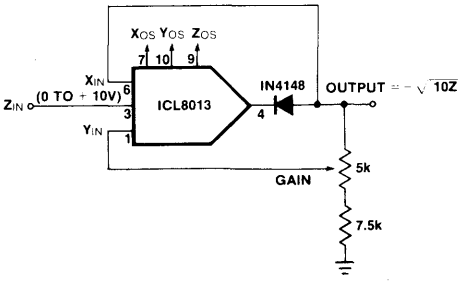
POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH



DIVISION

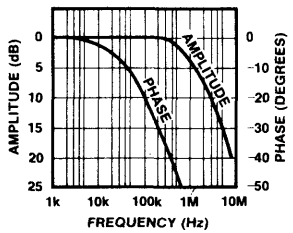


SQUARE ROOT

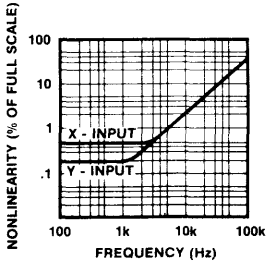


TYPICAL PERFORMANCE CURVES

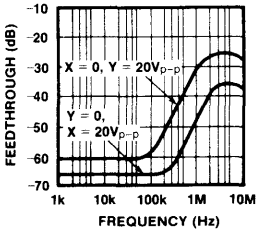
AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



NONLINEARITY AS A FUNCTION OF FREQUENCY



FEEDTHROUGH AS A FUNCTION OF FREQUENCY



DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

ICL8017
High Speed Inverting Amplifier

FEATURES

- 130 V/μs Slew Rate
- Fast Settling Time
- 50 nA Input Current
- 10 MHz Bandwidth
- Simple Frequency Compensation
- Short Circuit Protection

APPLICATIONS

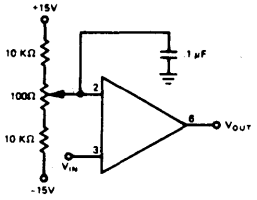
- High Speed Inverting Amplifier
- D/A Converter
- A/D Converter
- Pulse Amplifier
- Active Filter
- Sample and Hold Circuit
- Peak Detector

GENERAL DESCRIPTION

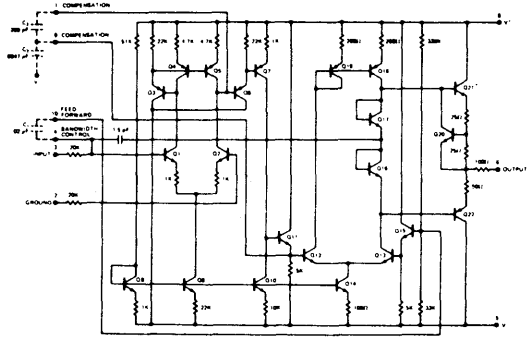
The 8017 integrated circuit is a high speed inverting amplifier combining excellent input characteristics with wide bandwidth and high slew rate. Frequency compensation is achieved with the minimum number of external components. The high slew rate and fast settling time ensure exceptional performance in high speed data acquisition circuits. Full power bandwidth of 2 MHz makes the 8017 amplifier suitable for all applications where large amplitude, high frequency signals are encountered.

The 8017 is available in the military version, 8017M, with a temperature range from −55°C to +125°C and in the commercial version, 8017C, from 0°C to +70°C.

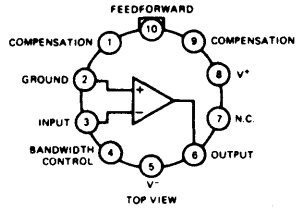
VOLTAGE OFFSET NULL CIRCUIT



SCHEMATIC DIAGRAM



PIN CONFIGURATION



TOP VIEW

(outline dwg TO-100)

ORDERING INFORMATION

ICL8017 M TW

- TW — Package: TW -- TO-100 metal can
- M — Temperature Range: M - Military (−55°C to +125°C); C - Commercial (0°C to 70°C)
- ICL8017 — Device Chip Type

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Operating Temperature Range	
ICL8017M	-55°C to +125°C
ICL8017C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (60 secs)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_S = ±15V)

PARAMETER	CONDITIONS	8017M MIN	8017M TYP	8017M MAX	8017C MIN	8017C TYP	8017C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage			2.0	5.0		2.0	7.0	mV
Input Current			50	200		50	200	nA
Input Noise Voltage (rms)	10 Hz to 1 MHz		20			20		μV
Large Signal Voltage Gain	R_L = 2 kΩ	25	1000		25	1000		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current	V_{OUT} = 0V		5.0	7.0		5.0	8.0	mA
Power Consumption	V_{OUT} = 0V		150	210		150	240	mW
Slew Rate	R_{BW} = 20 kΩ		130			130		V/μs
Unity Gain Bandwidth (Note 3)	R_{BW} = 20 kΩ		10			10		MHz
Transient Response (Note 3)	Unity Gain, R_{BW} = 20 kΩ							
Risetime			30			30		ns
Overshoot			5			5		%
Settling Time (0.1%) (Note 3)	Unity Gain, R_{BW} = 20 kΩ		1.0			1.0		μs
(.01%) (Note 3)			3.5			3.5		μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8017C), -55°C ≤ T_A ≤ +125°C (8017M):								
Input Offset Voltage				6.0			7.5	mV
Input Current				500			500	nA
Average Temperature Coefficient of Input Offset Voltage	-55°C ≤ T_A ≤ +125°C		10					μV/°C
	0°C ≤ T_A ≤ + 70°C					10		μV/°C
Large Signal Voltage Gain		15			15			V/mV
Output Voltage Swing	R_L = 2 kΩ	±10			±10			V
Supply Voltage Rejection Ratio				300			300	μV/V
Supply Current	V_{OUT} = 0V			9.0			9.0	mA

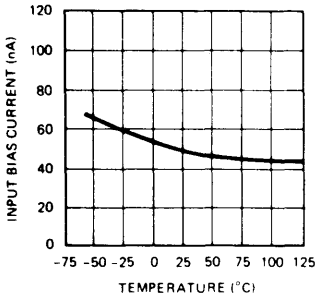
NOTE 1: The maximum junction temperature of the 8017M is 150°C, while that of the 8017C is 100°C. For operating at elevated temperatures the package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. Above 100°C it may be necessary to use a heatsink with the 8017M to avoid exceeding the maximum chip temperature.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

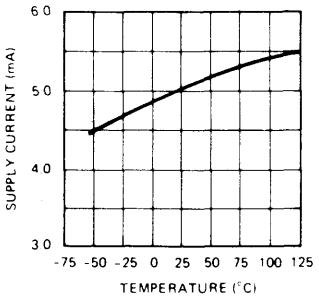
NOTE 3: Circuit and compensation as in Figure 1.

TYPICAL PERFORMANCE CURVES*

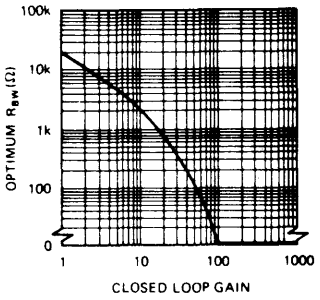
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



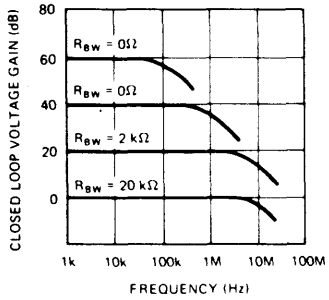
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



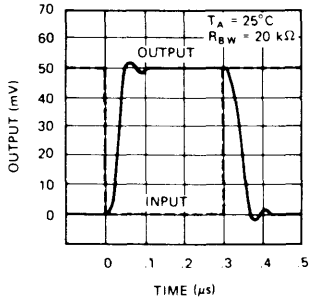
OPTIMUM VALUE OF R_{BW} AS A FUNCTION OF CLOSED LOOP GAIN (SEE FIG. 1)



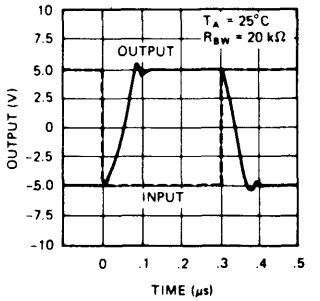
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



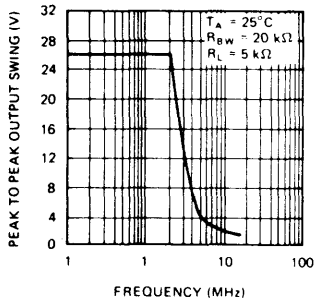
UNITY GAIN TRANSIENT RESPONSE



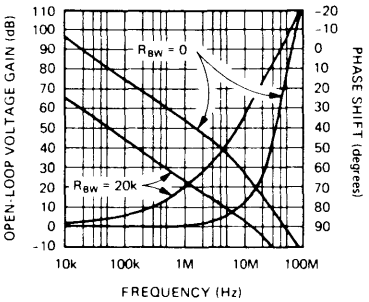
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



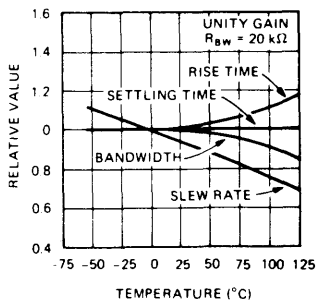
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



OPEN-LOOP FREQUENCY RESPONSE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



*8017C only guaranteed for $0°C \leq T_A \leq +70°C$

DEFINITION OF TERMS

Input Offset Voltage: Voltage which must be applied to input terminal to obtain zero output voltage.

Input Current: Current into input terminal when at ground potential.

Large Signal Voltage Gain: The ratio of maximum output swing with load to the required change in input drive voltage.

Slew Rate: The maximum rate of change of output voltage in response to a large amplitude input pulse.

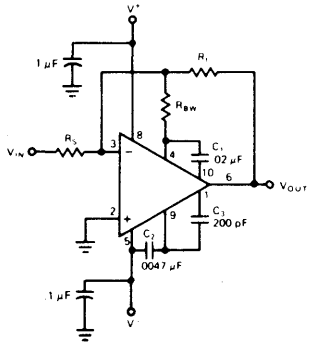
Unity Gain Bandwidth: The frequency at which the small signal gain is 3 dB below its low frequency value.

Transient Response: The 10% to 90% closed loop step-function response of the amplifier under small signal conditions.

Settling Time: The elapsed time between the application of a fast input pulse and the time at which the output has settled to its final value within a specified limit of accuracy.

APPLICATIONS INFORMATION

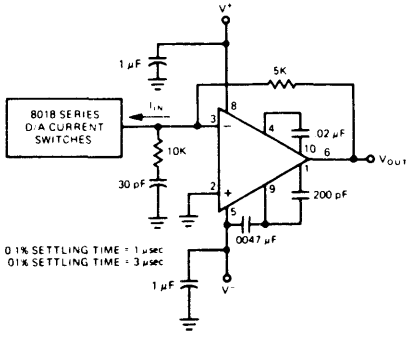
Figure 1. Inverting Voltage Amplifier



GAIN	R_S	R_f	R_{BW}	BAND-WIDTH	SLEW RATE
1X	10 kΩ	10 kΩ	20 kΩ	10 MHz	130 V/µs
10X	10 kΩ	100 kΩ	2 kΩ	6 MHz	100 V/µs
100X	1 kΩ	100 kΩ	short	800 kHz	50 V/µs

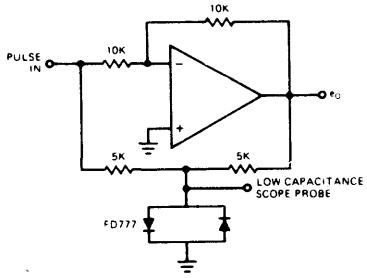
NOTE: If no bandwidth control resistor (R_{BW}) is connected between pins 3 and 4, the amplifier is unconditionally stable for normal feedback configurations. Some improvement in frequency performance can be realized by setting R_{BW} = 20 kΩ; the amplifier will still be unconditionally stable. However, for optimum frequency response, R_{BW} should be selected from the curve on page 3, based on the closed loop gain of the circuit. Additional control of the bandwidth/stability trade-off is possible by bypassing R_f with a low value capacitor. It is not necessary to alter the value of C_1, C_2 or C_3.

Figure 2. Current Summing Amplifier



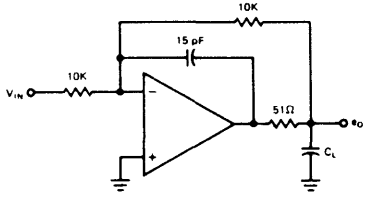
NOTE: The analog output current of the 8018 Series D/A current switches can be converted to voltage using the 8017 as shown. Input compensation of approximately 10 kΩ and 30 pF helps improve settling time.

Figure 3. Settling Time Measurement



NOTE: Settling time is measured by creating a dummy summing junction and observing the error voltage waveform on a scope. The junction is clamped with high speed diodes to avoid overdriving the scope preamp.

Figure 4. Isolation of Capacitive Loads



NOTE: Excess phase shift caused by heavy capacitive loading (above 200 to 300 pF) can cause stability problems. By providing the amplifier with a minimum real load impedance (51Ω), these difficulties can be overcome. Note that at high output currents, maximum voltage swing will be reduced.

ICL8021—ICL8023 Low Power Operational Amplifiers

FEATURES

- ΔVos = 3 mV max (adjustable to zero).
- ±1V to ±18V Power Supply Operation.
- Power Consumption – 20 μW @ ± 1V.
- Input Bias Current – 30 nA max.
- Internal Compensation.
- Pin-For-Pin Compatible With 741.
- Short Circuit Protected.

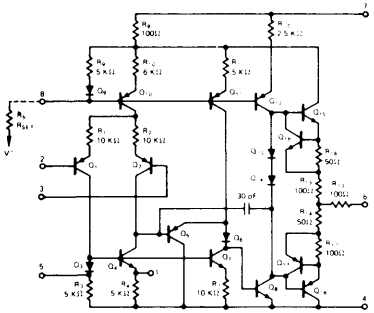
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Indefinite
Power Dissipation (Note 2)	300 mW
Operating Temperature Range	
8021M	−55°C to +125°C
8021C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

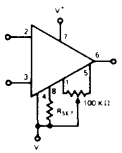
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

SCHEMATIC DIAGRAM



VOLTAGE OFFSET NULL CIRCUIT



ORDERING INFORMATION

ICL8021 C TY

- Basic Part Number: 8021—Single, 8022—Dual, 8023—Triple
- Package:
  - TY – TO-99 Metal Can — 8021 only
  - PA—8 pin Minidip — 8021 only
  - JD—14 pin CERDIP — 8022 only
  - PD—14 pin Plastic DIP — 8022 only
  - JE—16 pin CERDIP — 8023 only
  - PE—16 pin Plastic DIP — 8023 only
- Temperature:
  - C— Commercial — 0°C to 70°C
  - M— Military −55°C to +125°C

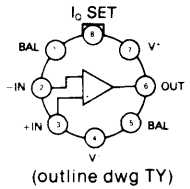
GENERAL DESCRIPTION

The Intersil 8021 integrated circuit is a low power operational amplifier specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 can be tailored to a particular application by adjusting an external resistor, R_{SET}, which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

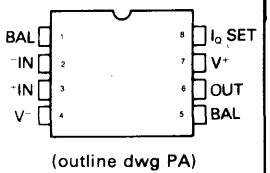
Other features of the 8021 include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

The Intersil 8022 (8023) consists of two (three) low power operational amplifiers in a single 14-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

PIN CONFIGURATIONS

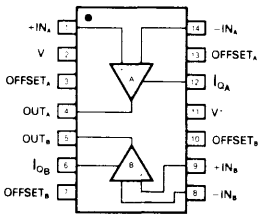


(outline dwg TY)

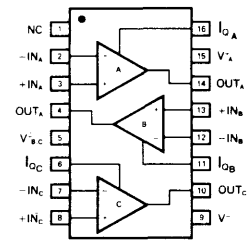


(outline dwg PA)

NOTE: Pin 4 connected to case.



(outline dwg JD, PD)



(outline dwg JE, PE)

5

ELECTRICAL CHARACTERISTICS (V_S = ±6V, I_Q = 30 μA, unless otherwise specified.)

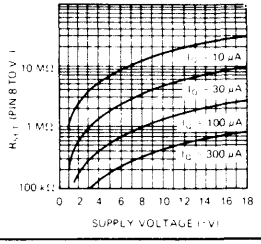
CHARACTERISTICS	CONDITIONS	8021M MIN	8021M TYP	8021M MAX	8021C MIN	8021C TYP	8021C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100\ k\Omega$		2	3		2	6	mV
Input Offset Current			.5	7.5		.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance		3	10		3	10		MΩ
Input Voltage Range	V_S = ±15V	±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20\ k\Omega$, V_S = ±15V	±12	±14		±12	±14		V
	$R_L \geq 10\ k\Omega$, V_S = ±15V	±11	±13		±11	±13		V
Output Short-Circuit Current			±13			±13		mA
Power Consumption	V_{OUT} = 0		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/μs
Unity Gain Bandwidth	R_L = 20 kΩ, V_{IN} = 20 mV		270			270		kHz
Transient Response (Unity Gain)	R_L = 20 kΩ, V_{IN} = 20 mV							
Risetime			1.3			1.3		μs
Overshoot			10			10		%
The following specifications apply for 0 C ≤ T_A ≤ +70 C (8021C) −55 C < +125 C (8021M)								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	4.0		2.0	7.5	mV
Input Offset Current			1.0	11		1.5	15	nA
Input Bias Current			10	32		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10\ k\Omega$		5			5		μV/°C
Average Temperature Coefficient of Input Offset Current			1.7			0.8		pA/°C
Large Signal Voltage Gain	R_L = 10 kΩ	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±10	±13		±10	±13		V

QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V⁻)

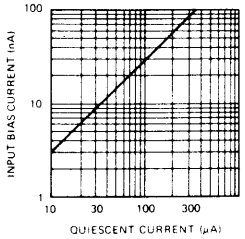
V_S \ I_Q	10 μA	30 μA	100 μA	300 μA
±1.5	1.5 MΩ	470 kΩ	150 kΩ	
± 3	3.3 MΩ	1.1 MΩ	330 kΩ	100 kΩ
± 6	7.5 MΩ	2.7 MΩ	750 kΩ	220 kΩ
± 9	13 MΩ	4 MΩ	1.3 MΩ	350 kΩ
±12	18 MΩ	5.6 MΩ	1.5 MΩ	510 kΩ
±15	22 MΩ	7.5 MΩ	2.2 MΩ	620 kΩ

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V⁻)

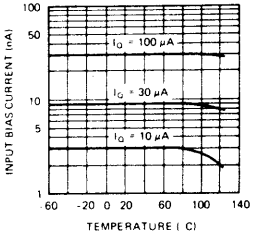


TYPICAL PERFORMANCE CURVES* (T_A = +25°C, V_S = ±6V, I_Q = 30 μA, unless otherwise specified.)

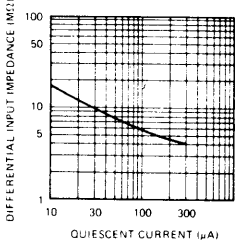
INPUT BIAS CURRENT VS QUIESCENT CURRENT



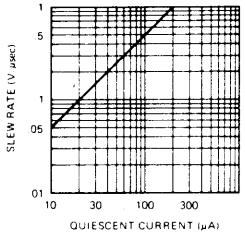
INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



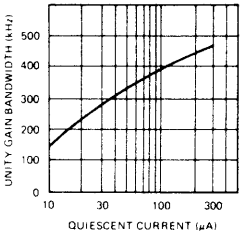
DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT



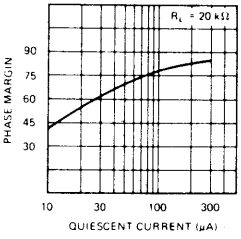
SLEW RATE VS QUIESCENT CURRENT



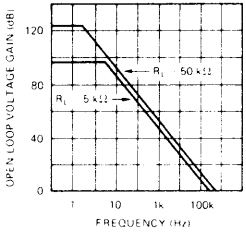
FREQUENCY RESPONSE VS QUIESCENT CURRENT



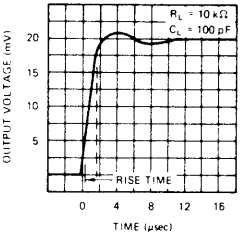
PHASE MARGIN VS QUIESCENT CURRENT



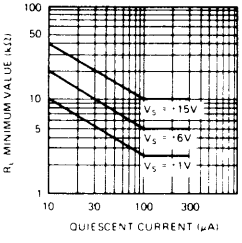
OPEN-LOOP FREQUENCY RESPONSE



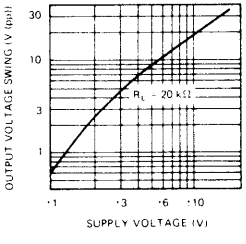
TRANSIENT RESPONSE



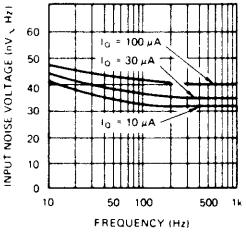
MAXIMUM LOAD VS QUIESCENT CURRENT



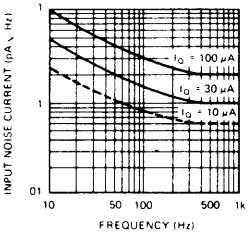
OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE



EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY



EQUIVALENT INPUT NOISE CURRENT VS FREQUENCY



*ICL8021C guaranteed only for 0°C ≤ T_A ≤ +70°C

ICL8038
Precision Waveform Generator/Voltage Controlled Oscillator

FEATURES

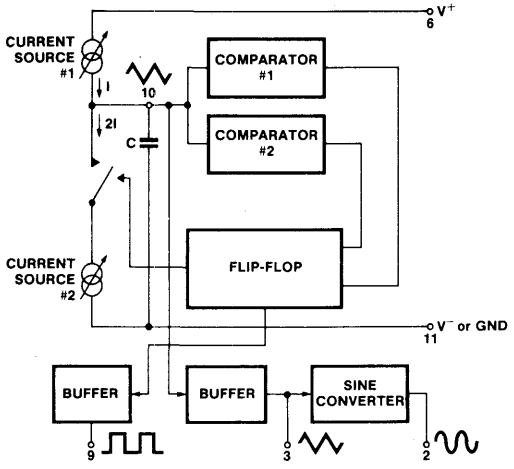
- **Low frequency drift with temperature - 50ppm/°C**
- **Simultaneous sine, square, and triangle wave outputs**
- **Low distortion - 1% (sine wave output)**
- **High linearity - 0.1% (triangle wave output)**
- **Wide operating frequency range - 0.001Hz to 0.3MHz**
- **Variable duty cycle - 2% to 98%**
- **High level outputs - TTL to 28V**
- **Easy to use - just a handful of external components required**

GENERAL DESCRIPTION

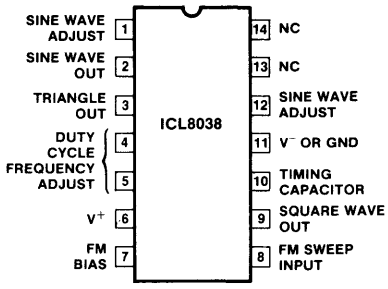
The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 50ppm/°C.

5

BLOCK DIAGRAM



PIN CONFIGURATION (outline dwg JD)



ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	STABILITY	PACKAGE	ORDER PART NUMBER
8038 CC	0°C to +70°C	250ppm/°C typ	CERDIP	ICL8038 CC JD
8038 BC	0°C to +70°C	150ppm/°C max	CERDIP	ICL8038 BC JD
8038 AC	0°C to +70°C	80ppm/°C max	CERDIP	ICL8038 AC JD
8038 BM	-55°C to +125°C	150ppm/°C max	CERDIP	ICL8038 BM JD
8038 AM	-55°C to +125°C	80ppm/°C max	CERDIP	ICL8038 AM JD

MAXIMUM RATINGS

Supply Voltage ..... ±18V or 36V Total
Power Dissipation[1] 750mW
Input Voltage (any pin) ..... Not To Exceed Supply Voltages
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Storage Temperature Range ..... −65°C to +125°C
Operating Temperature Range:
8038AM, 8038BM ..... −55°C to +125°C
8038AC, 8038BC, 8038CC ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS

(V_{SUPP} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified)

SYMBOL	GENERAL CHARACTERISTICS	8038CC			8038BC(BM)			8038AC(AM)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{SUPP}	Supply Voltage Operating Range										
V^+	Single Supply	+10		+30	+10		30	+10		30	V
V^+, V^-	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I_{SUPP}	Supply Current (V_{SUPP} = ±10V)[2]										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)											
f_{max}	Maximum Frequency of Oscillation	100,000			100,000			100,000			Hz
f_{sweep}	Sweep Frequency of FM		10			10			10		kHz
	Sweep FM Range[3]		35:1			35:1			35:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
$\Delta f/\Delta T$	Frequency Drift With Temperature[5] +25°C to +70°C (+125°C)		250				150			80	ppm/°C
	0°C (−40°C) to +25°C		250				200			120	ppm/°C
$\Delta f/\Delta V$	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V_{SUPP}
	Recommended Programming Resistors (R_A and R_B)	1000		1M	1000		1M	1000		1M	Ω
OUTPUT CHARACTERISTICS											
I_{OLK}	**Square-Wave** Leakage Current (V_9 = 30V)			1			1			1	μA
V_{SAT}	Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
t_r	Rise Time (R_L = 4.7kΩ)		180			180			180		ns
t_f	Fall Time (R_L = 4.7kΩ)		40			40			40		ns
	Duty Cycle Adjust	2		98	2		98	2		98	%
	Triangle/Sawtooth/Ramp Amplitude (R_{TRI} = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPP}
	Linearity		0.1			0.05			0.05		%
Z_{OUT}	Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
	Sine-Wave Amplitude (R_{SINE} = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPP}
	THD (R_S = 1MΩ)[4]		2.0	5		1.5	3		1.0	1.5	%
	THD Adjusted (Use Fig. 8b)		1.5			1.0			0.8		%

NOTE 2: R_A and R_B currents not included.
NOTE 3: V_{SUPP} = 20V; R_A and R_B = 10kΩ, f ≅ 9kHz; Can be extended to 1000.1. See Figures 13 and 14.
NOTE 4: 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
NOTE 5: Fig. 2, pins 7 and 8 connected, V_{SUPP} = ±10V. See Fig. 6c for T.C. vs V_{SUPP}.

TEST CONDITIONS

PARAMETER	R_A	R_B	R_L	C_1	SW_1	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Maximum Frequency of Oscillation	1kΩ	1kΩ	4.7kΩ	100pf	Closed	Frequency at Pin 9
Sweep FM Range[1]	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Frequency Drift with Supply Voltage[2]	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude: Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off)[3]	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on)[3]	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust: MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTE 1: The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 ($2/3\ V_{SUPP} + 2V) \leq V_{SWEEP} \leq V_{SUPP}$ where V_{SUPP} is the total supply voltage. In Fig. 2, pin 8 should vary between 5.3V and 10V with respect to ground.

NOTE 2: $10V \leq V^+ \leq 30V$, or $\pm 5V \leq V_{SUPP} \leq \pm 15V$.

NOTE 3: Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.

DEFINITION OF TERMS:

Supply Voltage (V_{SUPP}). The total supply voltage from V^+ to V^-

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$(2/3\ V_{SUPP} + 2V) < V_{SWEEP} < V_{SUPP}$$

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

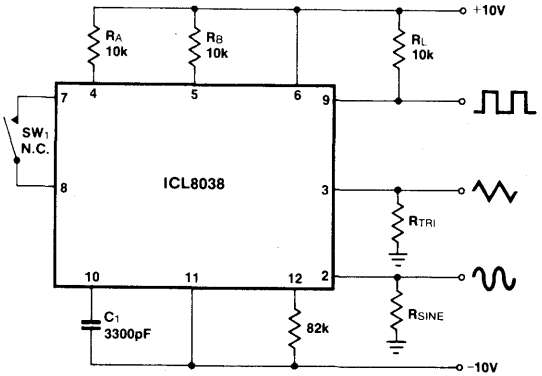
Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

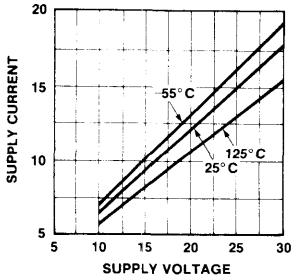
Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

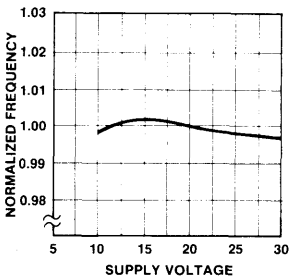
Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

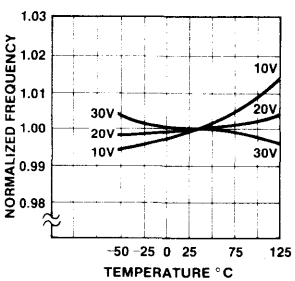
TEST CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS







THEORY OF OPERATION (see block diagram, first page)

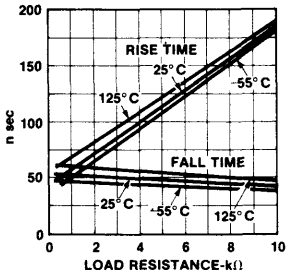
An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearily with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

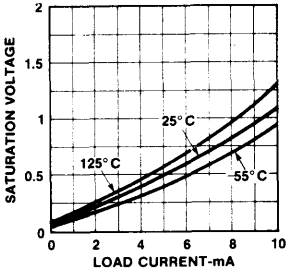
Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

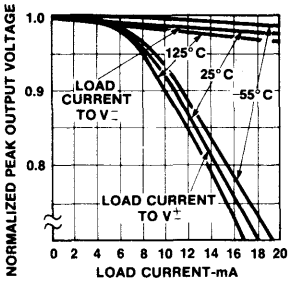
The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

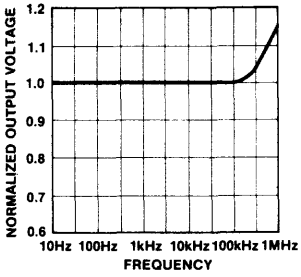
Performance of the Square-Wave Output

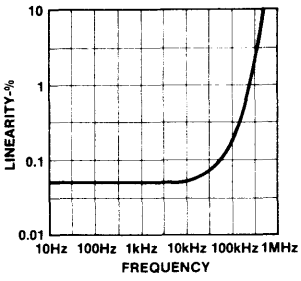




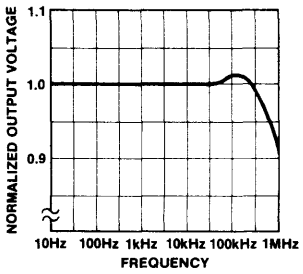
Performance of Triangle-Wave Output

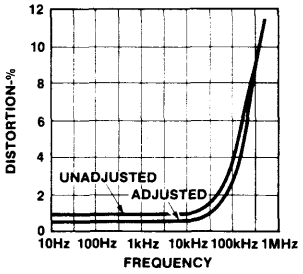


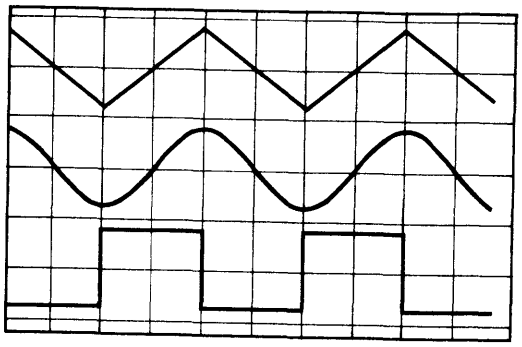




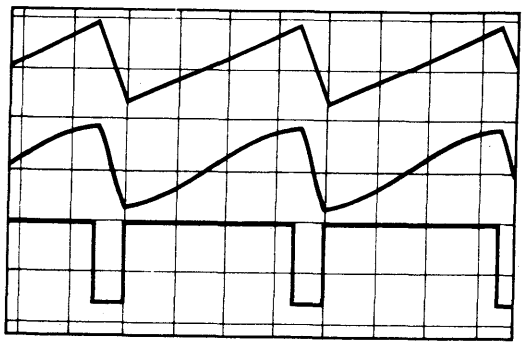
Performance of Sine-Wave Output







Square-Wave Duty Cycle — 50%



Square-Wave Duty Cycle — 80%

Phase Relationship of Waveforms

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 1. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{SUPP}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V^+ \times R_A}{1/5 \times V^+} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V^+}{\frac{2}{5} \times \frac{V_{SUPP}}{R_B} - \frac{1}{5} \times \frac{V_{SUPP}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 1b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 1c. This connection, however, causes an inherently larger variation of the duty-cycle, frequency, etc.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{RC} \text{ (for Figure 1a)}$$

If a single timing resistor is used (Figure 1c only), the frequency is

$$f = \frac{0.15}{RC}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 2; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.

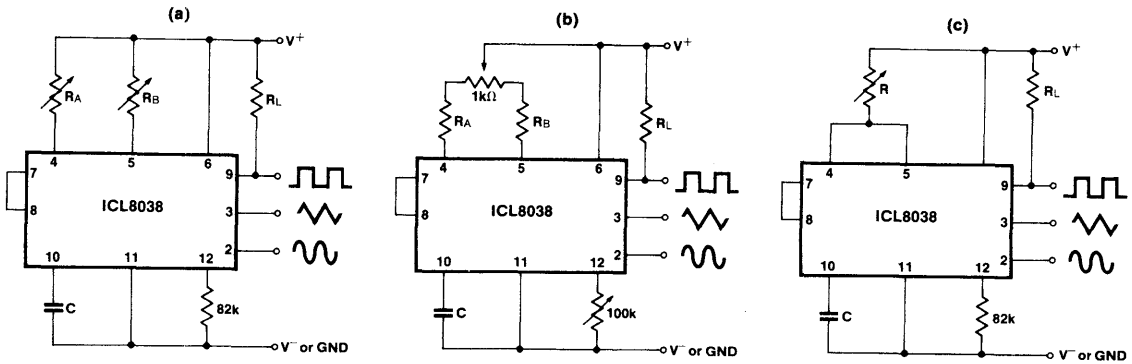


Figure 1: Possible Connections for the External Timing Resistors.

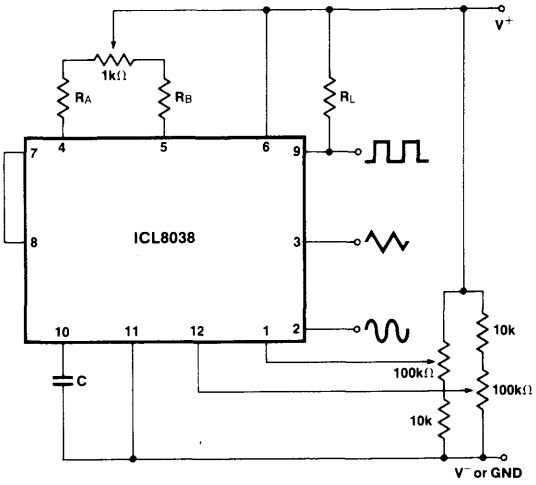


Figure 2: Connection to Achieve Minimum Sine-Wave Distortion.

SELECTING R_A, R_B AND C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times V_{SUPP}}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{V_{SUPP}}{5R_A}$$

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V^+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V^+). By altering this voltage, frequency modulation is performed.

For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 3a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 3b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at V_{sweep} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V^+ by (1/3 V_{SUPP} − 2V).

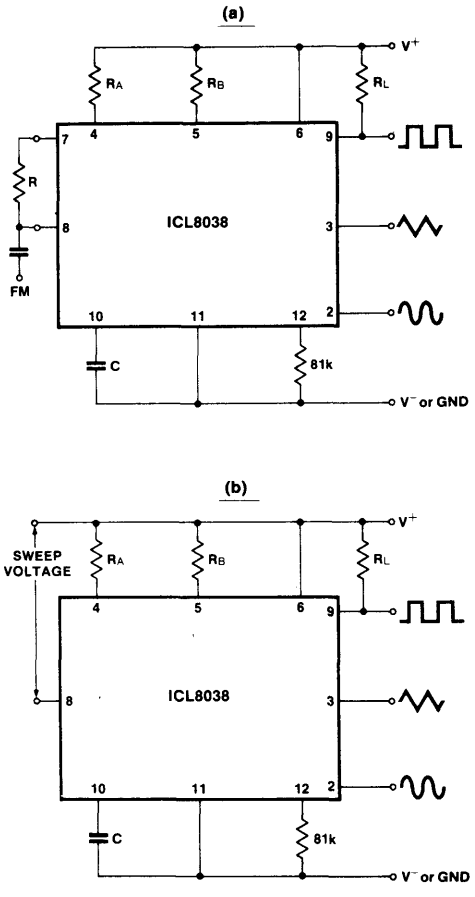


Figure 3: Connections for Frequency Modulation (a) and Sweep (b)

APPLICATIONS

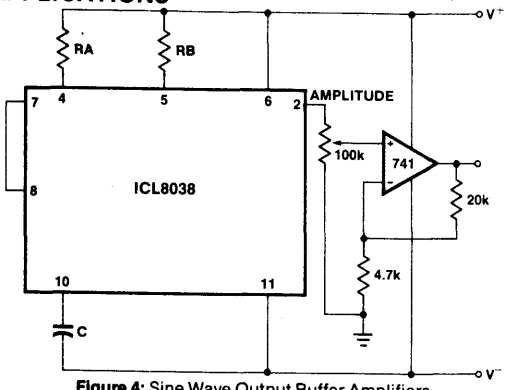


Figure 4: Sine Wave Output Buffer Amplifiers.
The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 4 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

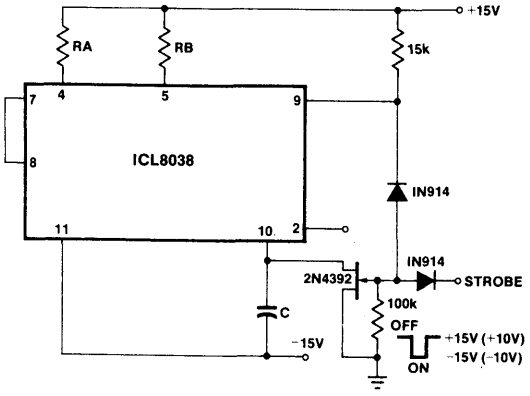


Figure 5: Strobe-Tone Burst Generator.
With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the 8038 oscillation. Figure 5 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

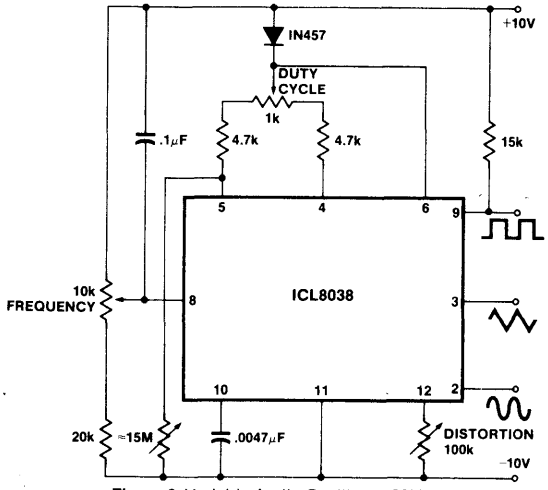


Figure 6: Variable Audio Oscillator, 20Hz to 20kHz.
To obtain a 1000:1 Sweep Range on the 8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred millivolts.
The Circuit of Figure 6 achieves this by using a diode to lower the effective supply voltage on the 8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

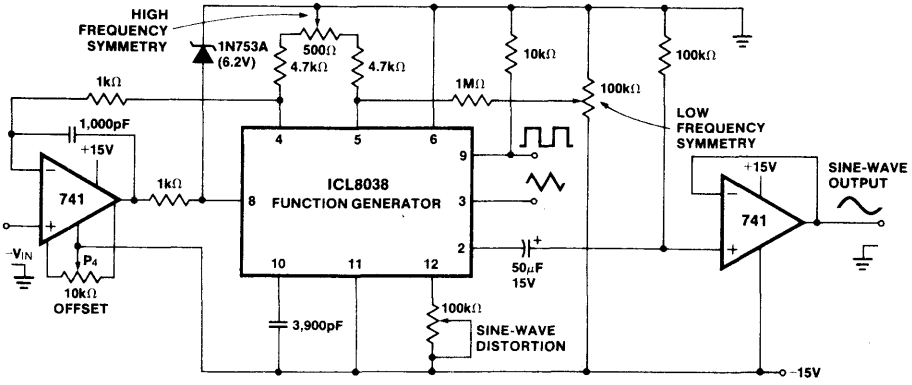


Figure 7: Linear Voltage Controlled Oscillator
The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 7.

USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop. In this application the remaining functional blocks, the phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC 4344, NE 562, HA 2800, HA 2820).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, $0.8 \times V^+$). The simplest solution here is to provide a voltage divider to V^+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Bulletin A013, "Everything You Always Wanted to Know About The 8038."

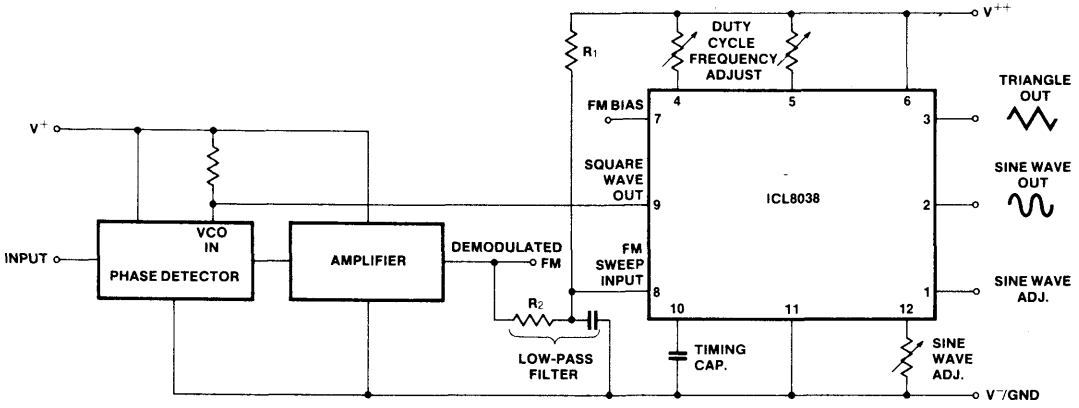
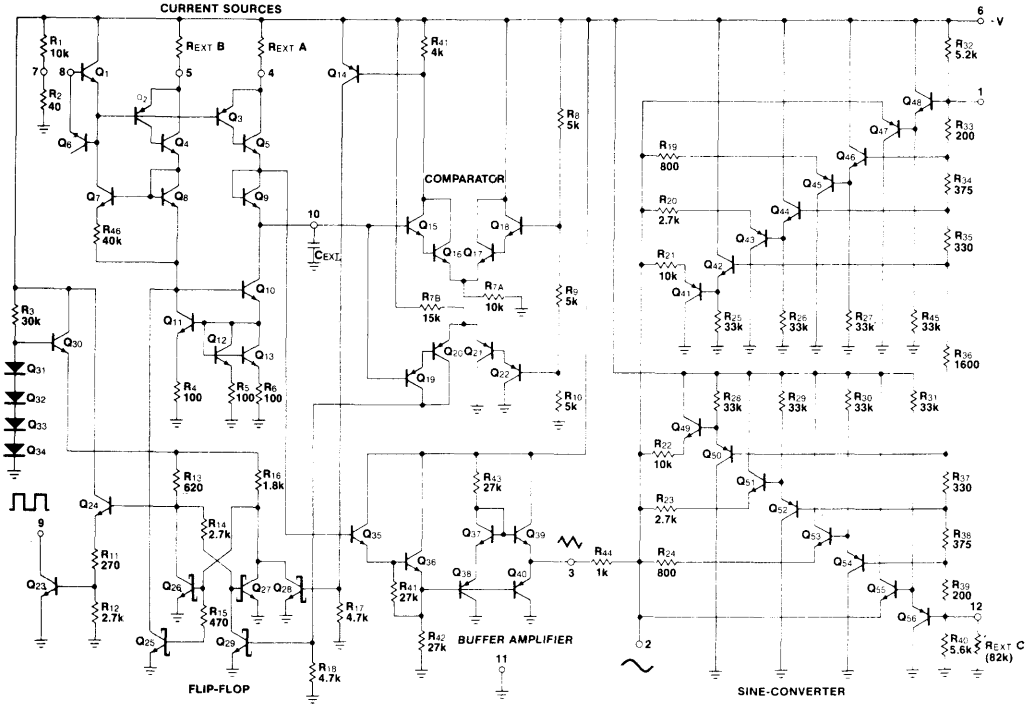


Figure 8: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

DETAILED SCHEMATIC



ICL8043

Dual Fet Input OpAmp

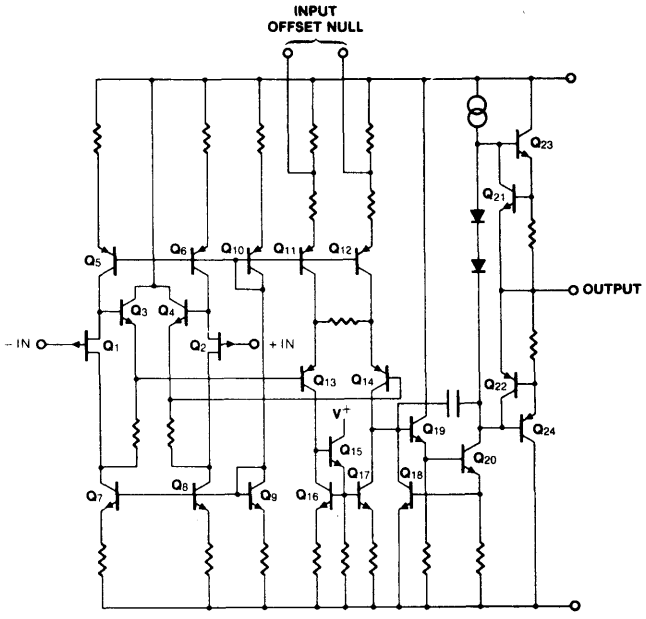
FEATURES

- **Very low input current — 2pA typ**
- **High slew rate — 6V/μs**
- **Internal frequency compensation**
- **Low power dissipation — 135mW typ**
- **Monolithic construction**

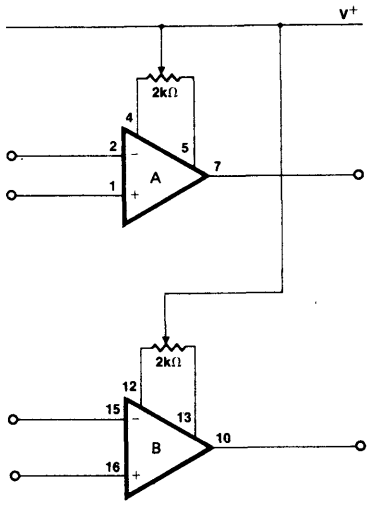
GENERAL DESCRIPTION

The ICL8043 contains two FET input op amps, each similar in performance to the ICL8007. The inputs and outputs are fully short circuit protected, and no latch-up problems exist. Offset nulling is accomplished by using a single pot (for each amplifier) connected to the positive supply voltage. The devices have excellent common mode rejection.

EQUIVALENT CIRCUIT (One Side)



OFFSET VOLTAGE NULL CIRCUIT

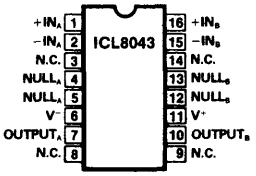


ORDERING INFORMATION

TYPE	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
8043M	ICL8043MJE	Ceramic 16 Pin DIP	-55°C to 125°C
8043C	ICL8043CPE	Plastic 16 Pin DIP	0°C to 70°C
8043C	ICL8043CJE	Ceramic 16 Pin DIP	0°C to 70°C

PIN CONFIGURATION

16 PIN DIP (TOP VIEW)



(outline dwgs JE, PE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V^+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
8043M	−55°C to +125°C
8043C	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. Rating applies for case temperatures to 125°C; derate linearly at 9mW/°C for ambient temperatures above +95°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

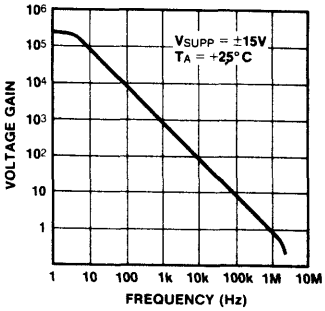
5

ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

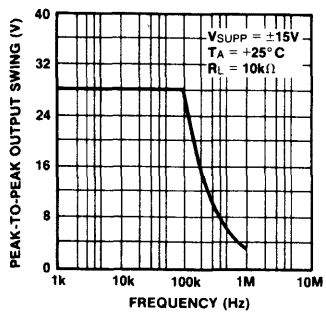
SYMBOL	CHARACTERISTICS	CONDITIONS	8043M			8043C			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
The following specifications apply for T_A = 25°C:									
V_{OS}	Input Offset Voltage	R_S < 100kΩ		10	20		20	50	mV
I_{OS}	Input Offset Current			0.5			0.5		pA
I_{IN}	Input Current (either input)			2.0	20		3.0	50	pA
R_{IN}	Input Resistance			10^6			10^6		MΩ
C_{IN}	Input Capacitance			2.0			2.0		pF
A_V	Large Signal Voltage Gain	R_L > 2kΩ, V_{out} = ±10V	50,000			20,000			V/V
R_O	Output Resistance			75			75		Ω
I_{SC}	Output Short-Circuit Current			25			25		mA
I_{SUPP}	Supply Current (Total)			4.5	6		4.5	6.8	mA
Pd	Power Consumption			135	180		135	204	mW
SR	Slew Rate			6.0			6.0		V/μs
GBW	Unity Gain Bandwidth			1.0			1.0		MHz
t_r	Transient Response (Unity Gain)	C_L < 100pF, R_L = 2kΩ							
	Risetime			300			300		ns
	Overshoot			10			10		%
The following specifications apply for 0°C < T_A < +70°C (8043C), −55°C < T_A < +125°C (8043M):									
ΔV_{IN}	Input Voltage Range		±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio		70	90		70	90		dB
PSRR	Supply Voltage Rejection Ratio			70	300		70	600	μV/V
A_V	Large Signal Voltage Gain		25,000			15,000			V/V
±V_O	Output Voltage Swing	R_L > 10kΩ	±12	±14		±12	±14		V
		R_L > 2kΩ	±10	±13		±10	±13		V
V_{OS}	Input Offset Voltage			15	30		30	60	mV
I_{IN}	Input Current (either input)	T_A = +125°C		2.0	15				nA
		T_A = +70°C					50	175	pA
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage				75			75	μV/°C

TYPICAL PERFORMANCE CURVES

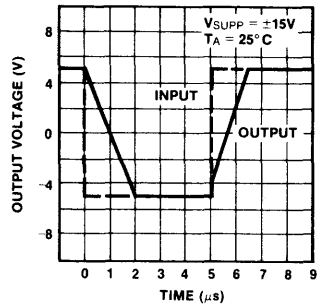
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



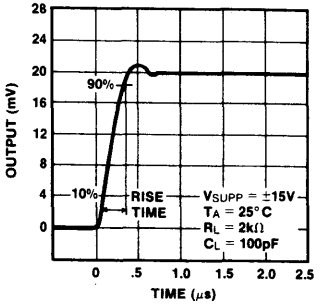
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



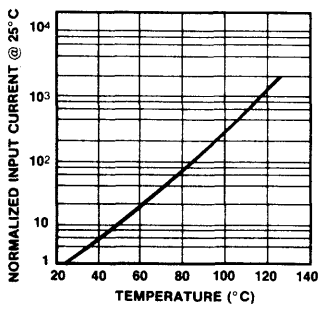
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



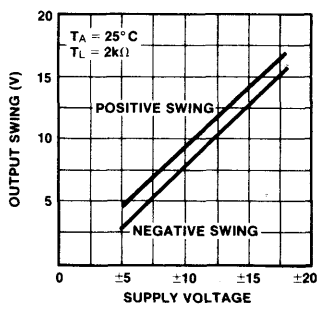
TRANSIENT RESPONSE



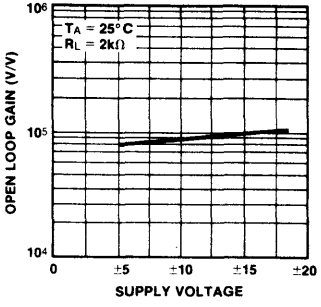
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



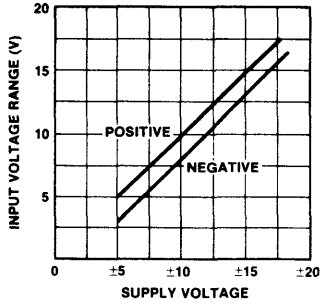
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



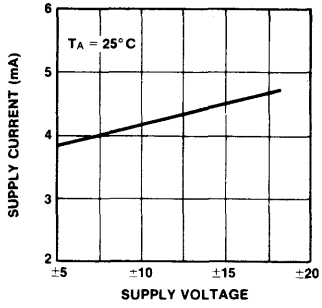
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



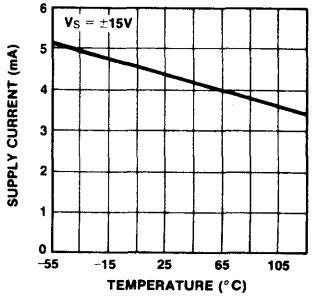
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



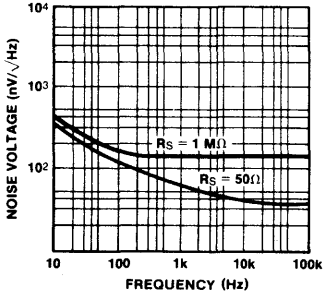
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



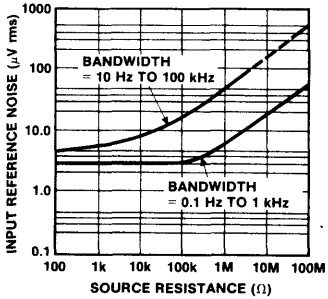
TOTAL QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



5

CHANNEL SEPARATION

Channel separation or crosstalk is measured using the circuit of Figure 1. One amplifier is driven so that its output swings ±10V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Figure 2.

$$\text{Channel Separation} = 20 \log \left(\frac{V_{OUT(A)}}{V_{IN(B)}} \right)$$

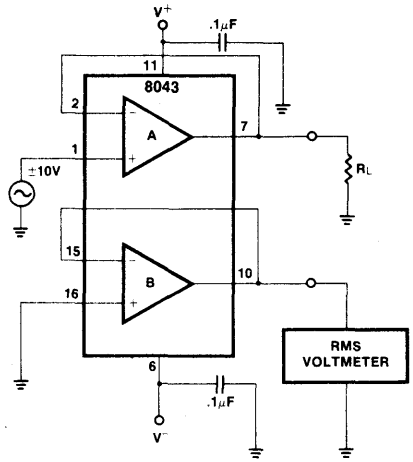


Figure 1

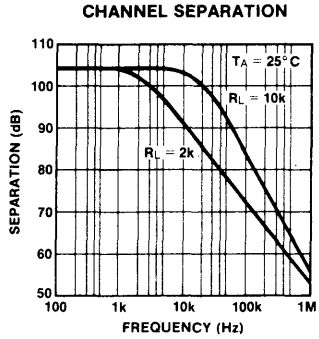


Figure 2

5

APPLICATIONS

Applications for any dual amplifier fall into two categories. There are those which use the two-in-one package concept simply to save circuit-board space and cost, but more interesting are those circuits where the two sides of the dual are used to complement one another in a subsystem application. The circuits which follow have been selected on this basis.

AUTOMATIC OFFSET SUPPRESSION CIRCUIT

The circuit shown in Figure 3 uses one amplifier (A_1) as a normal gain stage, while the other (A_2) forms part of an offset voltage zeroing loop. There are two modes of operation which occur sequentially; first, an offset null correction mode during which the offset voltage of A_1 is nulled out. Following this nulling operation, A_1 is used as a normal amplifier while the voltage necessary to zero its offset voltage is stored on the integrator comprised of A_2 and C_1.

The advantage of this circuit is that it allows chopper amplifier performance to be achieved at one-tenth the cost. The only limitation is that during the offset nulling mode, A_1 is disconnected from the input. However, in most data acquisition systems, many inputs are scanned sequentially. It is fairly simple to synchronize the offset nulling operation so that it does not occur when that particular amplifier is being "looked at". For the component values shown in Figure 3, and assuming a total leakage of 50pA at the inverting input of A_2, the offset voltage referred to the input of A_1 will drift away from zero at only 40μV/sec. Thus, the offset nulling information stored on C_1 can be "refreshed" relatively infrequently. The measured offset voltage of A_1 during the amplification mode was 11μV; offset voltage drift with temperature was less than 0.1μV/°C.

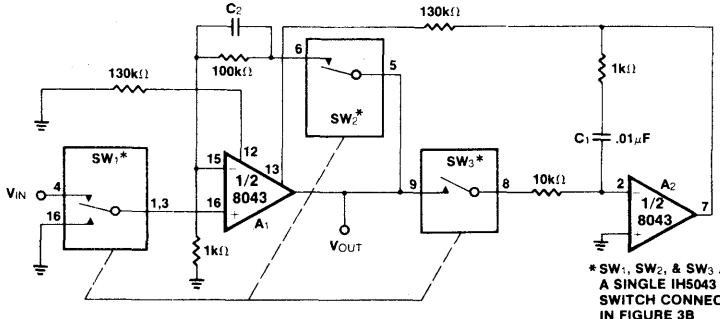
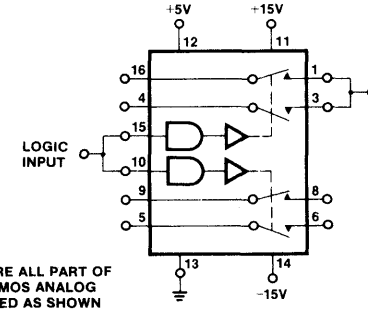


Figure 3A.



*SW1, SW2, & SW3 ARE ALL PART OF A SINGLE IH5043 CMOS ANALOG SWITCH CONNECTED AS SHOWN IN FIGURE 3B

Figure 3B.

STAIRCASE GENERATOR

The circuit shown in Figure 4 is a high input impedance version of the so-called "diode pump" or staircase generator. Note that charge transfer takes place at the negative-going edge of the input-signal.

The most common application for staircase generators is in low cost counters. By resetting the capacitor when the output reaches a predetermined level, the circuit may be made to count reliably up to a maximum of about 10. A straightforward circuit using a LM311 for the level detector, and a CMOS analog gate to discharge the capacitor, is shown in Figure 5. An important property of this type of counter is the ease with which the count can be changed; it is only necessary to change the voltage at which the comparator trips. A low cost A-D converter can also be designed using the same principle since the digital count between reset periods is directly proportional to the analog voltage used as a reference for the comparator.

A considerable amount of hysteresis is used in the comparator shown in Figure 5. This ensures that the capacitor is completely discharged during the reset period. In a more sophisticated circuit, a dual comparator "window detector" could be used, the lower trip point set close to ground to assure complete discharge. The upper trip point could then be adjusted independently to determine the pulse count.

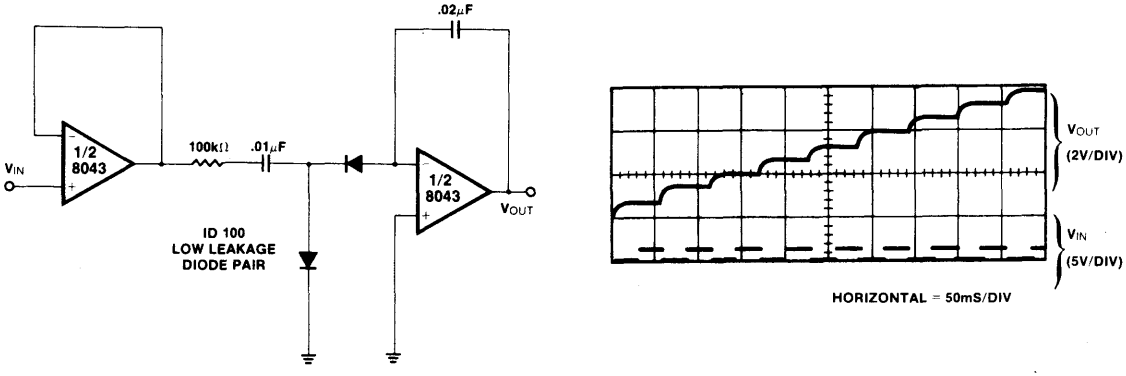


Figure 4

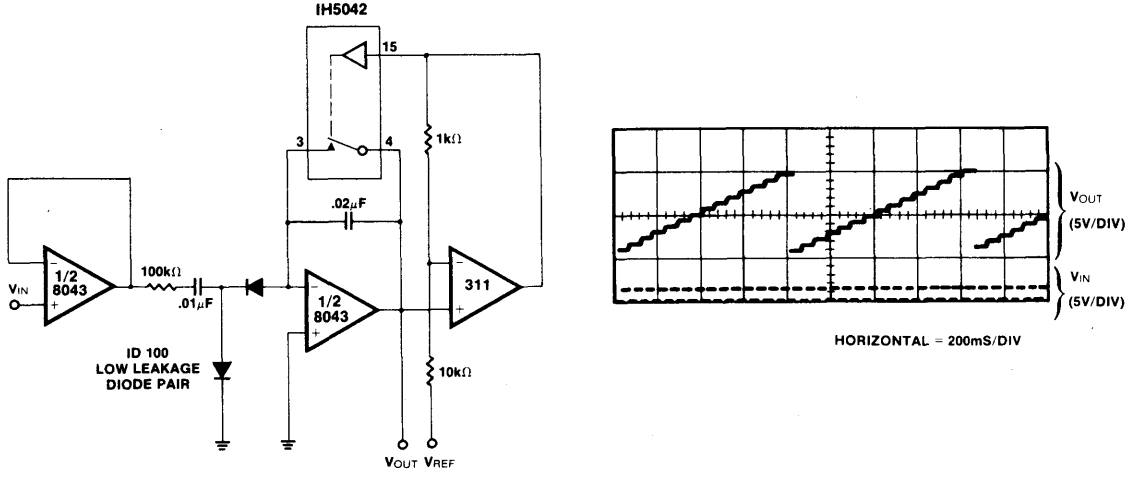


Figure 5

SAMPLE & HOLD CIRCUIT

Two important properties of the 8043 are used to advantage in this circuit. The low input bias currents give rise to slow output decay rates ("droop") in the hold mode, while the high slew rate (6V/μS) improves the tracking speed and the response time of the circuit. See Figure 6.

The ability of the circuit to track fast moving inputs is shown in Figure 7A. The upper waveform is the input (10V/div), the lower waveform the output (5V/div). The logic input is high.

Actual sample and hold waveforms are shown in Figure 7B. The center waveform is the analog input, a ramp moving at about 67V/ms, the lower waveform is the logic input to the sample & hold; a logic "1" initiates the sample mode. The upper waveform is the output, displaced by about 1 scope division (2V) from the input to avoid superimposing traces. The hold mode, during which the output remains constant, is clearly visible. At the beginning of a sample period, the output takes about 8μsec to catch up with the input, after which it tracks until the next hold period.

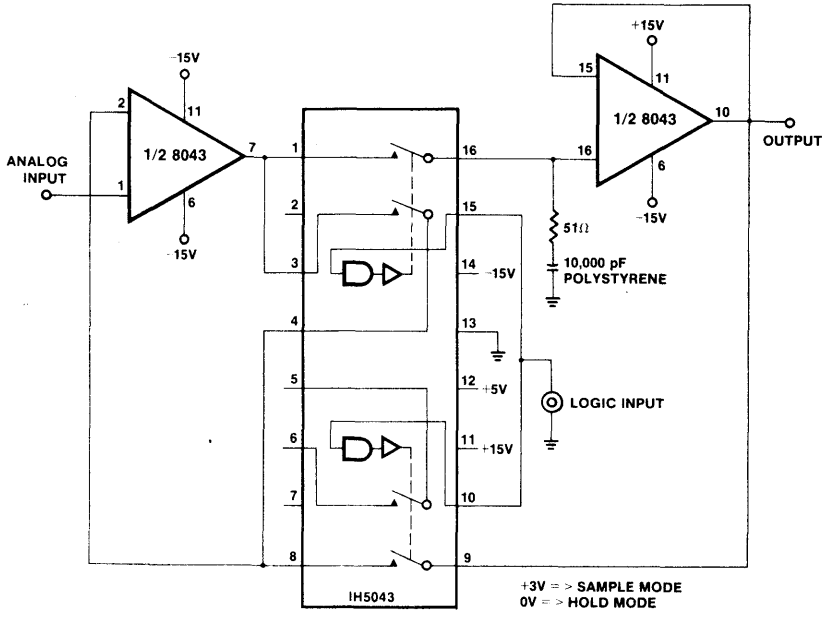
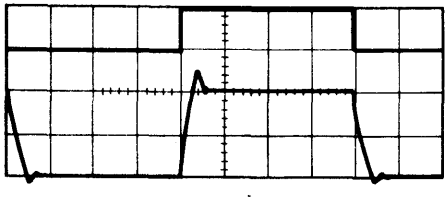
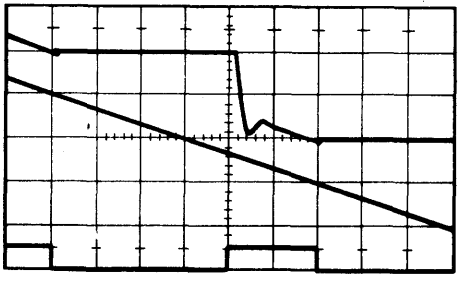


Figure 6



TOP: INPUT (10V/DIV)
BOTTOM: OUTPUT (5V/DIV)
HORIZONTAL: 10μs/DIV

Figure 7A



TOP: 2V/DIV
CENTER: 2V/DIV
BOTTOM: 10V/DIV
HORIZONTAL: 10μs/DIV

Figure 7B

INSTRUMENTATION AMPLIFIER

A dual FET input operational amplifier is an attractive component around which to build an instrumentation amplifier because of the high input resistance. The circuit shown in Figure 8 uses the popular triple op-amp approach. The output amplifier is a High Speed 741 (741 HS, slew rate guaranteed $\geq 0.7V/\mu s$) so as to utilize the high slew rate of the 8043 to the maximum extent. Input resistance of the circuit (either input, regardless of gain configuration) is in excess of 10^{12} ohms.

For the component values shown, the overall amplifier gain is 200 (front end gain = $\frac{2R_1 + R_2}{R_2}$, back end gain, = R_6/R_4).

Common mode rejection is largely determined by the matching between R_4 and R_5, and R_6 and R_7. In applications where offset nulling is required, a single potentiometer can be connected as shown in Figure 9.

Another popular circuit is given in Figure 10. In this case the gain is $1 + R_1/R_2$, and the CMRR determined by the match between R_1 and R_4, R_2 and R_3.

For more information on FET input operational amplifiers, see Intersil Application Bulletin A005 "The 8007: A High Performance FET-input Operational Amplifier."

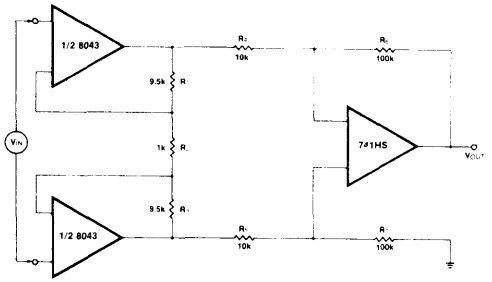


Figure 8

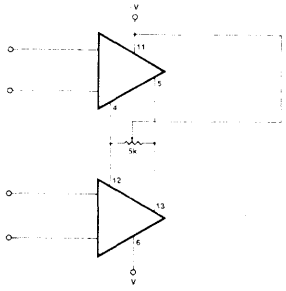


Figure 9

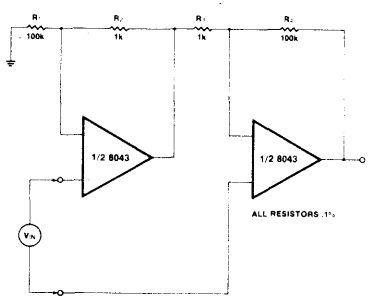
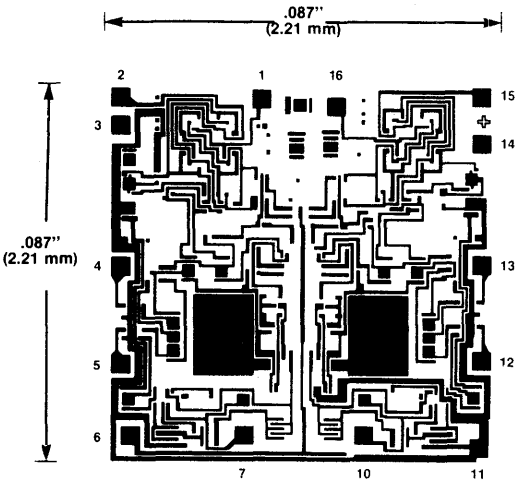


Figure 10

CHIP TOPOGRAPHY



ICL8048/8049
Monolithic Log Amplifier/ Monolithic Antilog Amplifier

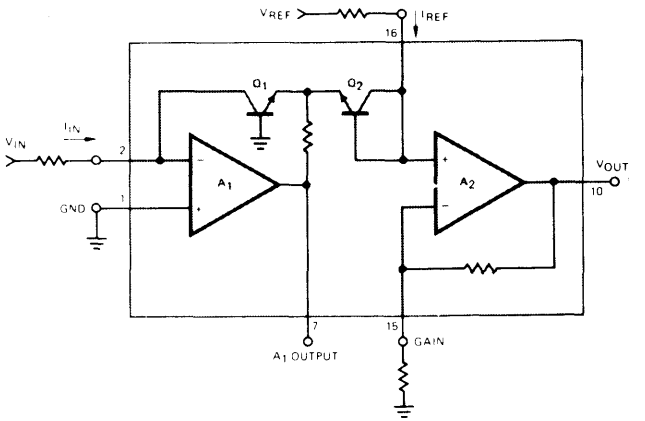
FEATURES
- 1/2% Full Scale Accuracy
- Temperature Compensated 0°C to +70°C
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual FET-Input Op-Amps

GENERAL DESCRIPTION
The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

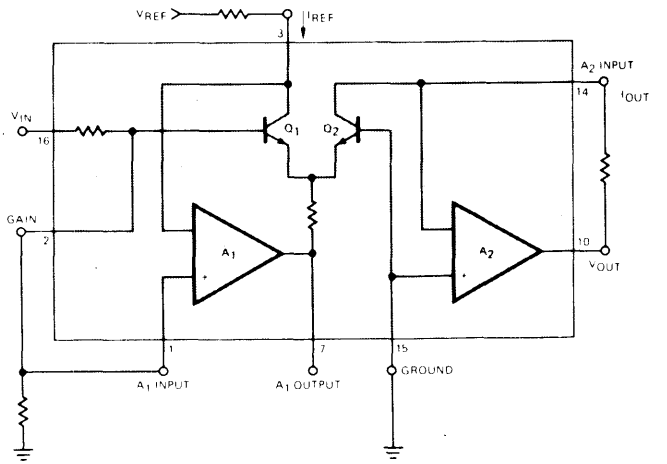
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

5

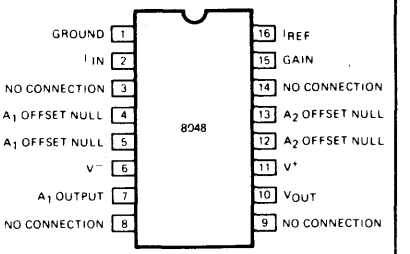
SCHEMATIC DIAGRAM (8048)

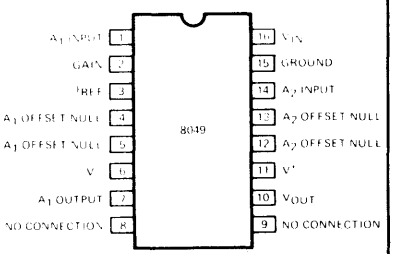


SCHEMATIC DIAGRAM (8049)



PIN CONFIGURATION
(outline dwgs JE, PE)





ABSOLUTE MAXIMUM RATINGS (8048)

See note under 8049 Absolute Maximum Ratings.

Supply Voltage . . . . . ±18V
I_{IN} (Input Current) 2mA
I_{REF} (Reference Current) 2mA
Voltage between Offset Null and V^+ . . . . . ±0.5V
Power Dissipation 750mW

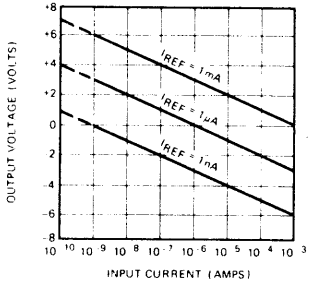
Operating Temperature Range . . . . . .0°C to +70°C
Output Short Circuit Duration . . . . . .Indefinite
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature (Soldering, 60 sec.) . . . . . .300°C

OPERATING CHARACTERISTICS (8048)

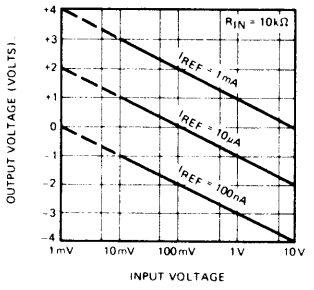
V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1V/decade unless otherwise specified.

PARAMETER	CONDITION	8048BC MIN.	8048BC TYP.	8048BC MAX.	8048CC MIN.	8048CC TYP.	8048CC MAX.	UNITS
Dynamic Range								
I_{IN} (1nA–1mA)		120			120			dB
V_{IN} (10mV–10V)	R_{IN} = 10kΩ	60			60			dB
Error, % of Full Scale	T_A = 25°C, I_{IN} = 1nA to 1mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	T_A = 0°C to +70°C, I_{IN} = 1nA to 1mA		.60	1.25		.80	2.5	%
Error, Absolute Value	T_A = 25°C, I_{IN} = 1nA to 1mA		12	30		14	60	mV
Error, Absolute Value	T_A = 0°C to +70°C, I_{IN} = 1nA to 1mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1nA to 1mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for I_{IN} = 100μA		250			250		μV(RMS)
Output Voltage Swing	R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

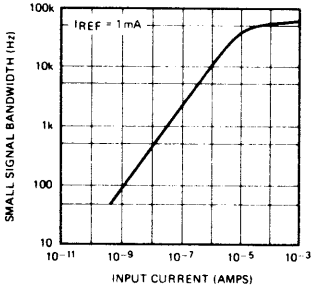
TRANSFER FUNCTION FOR CURRENT INPUTS



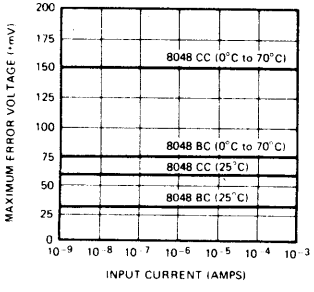
TRANSFER FUNCTION FOR VOLTAGE INPUTS



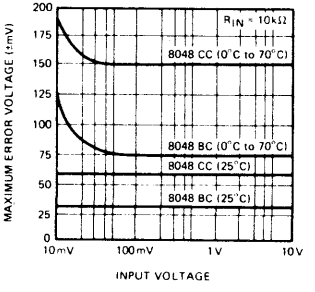
SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT



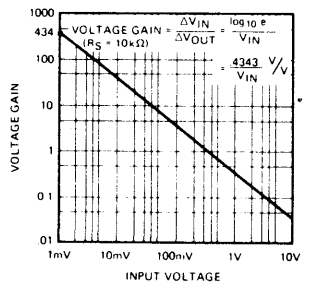
MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT



MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR R_S = 10 kΩ



ABSOLUTE MAXIMUM RATINGS (8049)

Supply Voltage . . . . . ±18V
V_{IN} (Input Voltage) . . . . . ±15V
I_{REF} (Reference Current) 2mA
Voltage between Offset Null and V^+ . . . . . ±0.5V
Power Dissipation 750mW

Operating Temperature Range . . . . . 0°C to +70°C
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec.) . . . . . 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

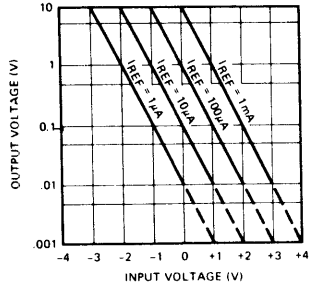
OPERATING CHARACTERISTICS (8049)

V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1 decade (out) per volt (in), unless otherwise specified.

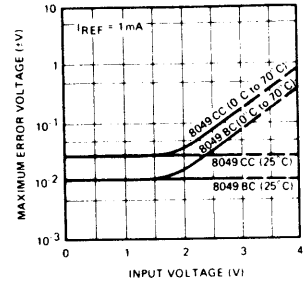
PARAMETER	CONDITION	8049BC MIN.	8049BC TYP.	8049BC MAX.	8049CC MIN.	8049CC TYP.	8049CC MAX.	UNITS
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60			60			dB
Error, Absolute Value	T_A = 25°C, 0V≤V_{IN}≤3V		3	10		5	25	mV
Error, Absolute Value	T_A = 0°C to +70°C, 0V≤V_{IN}≤3V		20	75		30	150	mV
Temperature Coefficient, Referred to V_{IN}	V_{IN} = 3V		0.38			0.55		mV/°C
Power Supply Rejection Ratio	Referred to Input, for V_{IN} = 0V		2.0			2.0		µV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	Referred to Input, for V_{IN} = 0V		26			26		µV(RMS)
Output Voltage Swing	R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

5

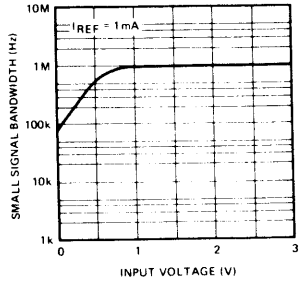
TRANSFER FUNCTION
(V_{OUT} AS A FUNCTION OF V_{IN})



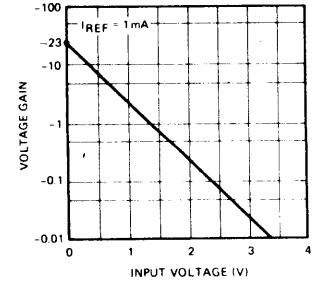
MAXIMUM ERROR VOLTAGE
REFERRED TO THE INPUT AS A
FUNCTION OF V_{IN}



SMALL SIGNAL BANDWIDTH
AS A FUNCTION OF
INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN
AS A FUNCTION OF
INPUT VOLTAGE



THEORY OF OPERATION

The 8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S\left[e^{q V_{BE}/kT} - 1\right] \quad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S\, e^{q V_{BE}/kT} \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log 10 \left[I_{C1}/I_{C2}\right] \quad (3)$$

Referring to Fig. 1, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{kT}{q}\right) \log 10 \left[I_{IN}/I_{REF}\right] \quad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the 8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

OFFSET AND SCALE FACTOR ADJUSTMENT*

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and open the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Fig. 1, this is done as follows:

1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.

2) Set $I_{IN} = I_{REF} = 1mA$. Adjust R_5 such that the output of A_2 (pin 10) is zero.

3) Set $I_{IN} = 1\mu A$, $I_{REF} = 1mA$. Adjust R_2 for $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu A$ in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

*See A053 for an automatic offset nulling circuit.

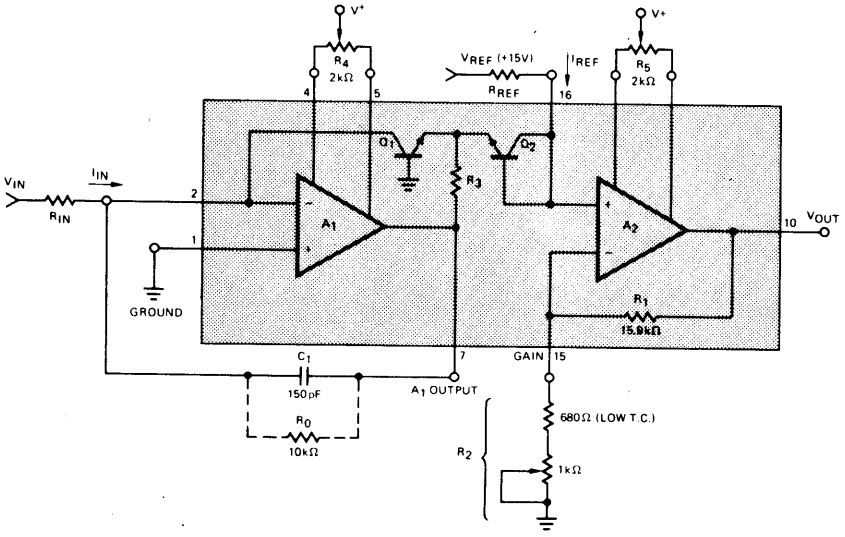


FIGURE 1. ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT

THEORY OF OPERATION

The 8049 relies on the same logarithmic properties of the transistor as the 8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Fig. 2). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on Page 3 and is as follows:

$$I_{C_1}/I_{C_2} = \exp\left[q\Delta V_{BE}/kT\right] \quad (5)$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on Page 3.

The overall transfer function is as follows:

$$I_{OUT}/I_{REF} = \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q\,V_{IN}}{kT}\right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q\,V_{IN}}{kT}\right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1+R_2} \times \frac{q\,V_{IN}}{kT}\right] \quad (8)$$

OFFSET AND SCALE FACTOR ADJUSTMENT*

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Fig. 2, the exact procedure for 1 decade/volt is as follows:

1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i. e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.

*See A053 for an automatic offset nulling circuit.

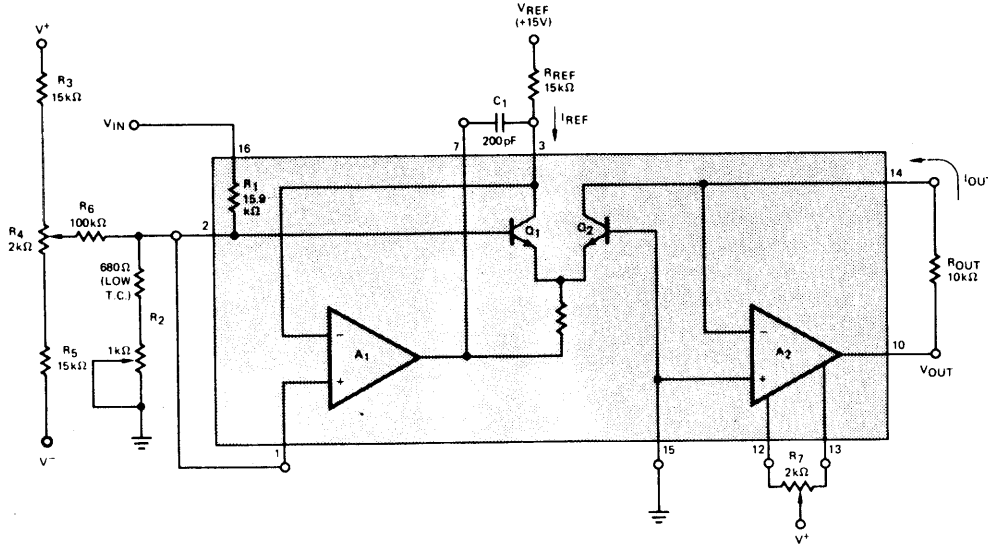


FIGURE 2. ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT

APPLICATIONS INFORMATION

Scale Factor Adjustment

The scale factor adjustment procedures outlined on Page 3 (8048) and Page 5 (8049) are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10}\left[I_{IN}/I_{REF}\right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT}\, I_{REF}\, 10^{-V_{IN}/K} \quad (10)$$

By adjusting R_2 (Fig. 1 and Fig. 2) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Fig. 3 for the log amp, and Fig. 4 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - .059)}\ \Omega \quad (11)$$

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

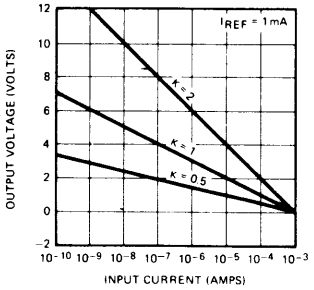


FIGURE 3

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

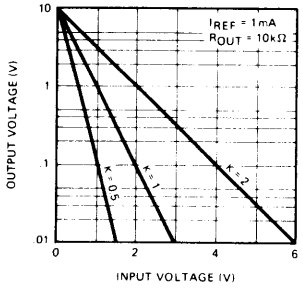


FIGURE 4

Frequency Compensation

Although the op-amps in both the 8048 and the 8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150 pF should be connected between Pins 2 and 7 (Fig. 1). In the 8049, 200 pF between Pins 3 and 7 is recommended (Fig. 2).

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given on Pages 2 and 4.

The various error terms in the log amplifier, the 8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the 8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Fig. 5.

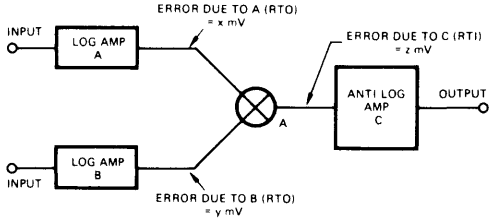


FIGURE 5

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2} \quad \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain plot on Page 4.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots given on Pages 2 and 4. For example, with the 8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures on Page 3. Fig. 6 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i. e., the horizontal axis. It will be noticed that the maximum error voltage of the 8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At V_{IN} = 3V, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

5

It is important to note that both the 8048 and the 8049 require positive values of I_{REF}, and the input (8048) or output (8049) currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the 8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the 8048 and the 8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the 8048, a fraction of the output voltage is seen on Pin 16 (Fig. 1). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the 8049, a fraction of the input voltage appears on Pin 3 (Fig. 2), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Fig. 7.

LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (9)$$

Clearly it is possible to perform division using just one 8048, followed by an 8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Fig. 7 is again recommended if the I_{REF} input is to be modulated.

APPLICATION NOTES

For further applications assistance, see

A007 "The ICL8048/8049 Monolithic Log-Antilog Amplifiers", by Ray Hendry

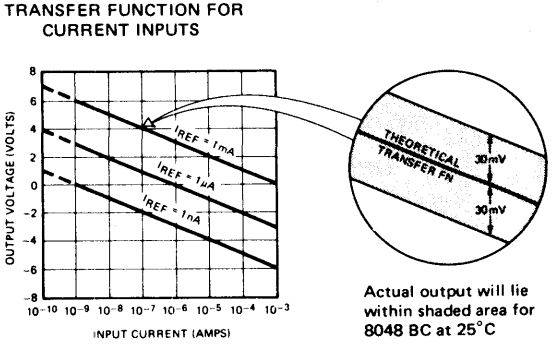


FIGURE 6

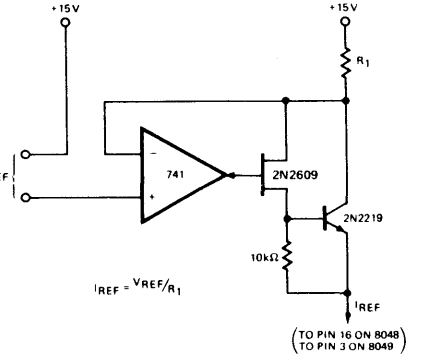


FIGURE 7

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on Page 6.

DYNAMIC RANGE The dynamic range of the 8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the 8049 the dynamic range refers to the range of output voltages over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined on Pages 3 (8048) or 5 (8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the 8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the 8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the 8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the 8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the 8048, V_{IN} for the 8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the 8048, this is the noise occurring at the output under the specified conditions. In the case of the 8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

5

ORDERING INFORMATION

TYPE	PACKAGE	MAX. ABSOLUTE ERROR (25°C)	TEMPERATURE RANGE	ORDER PART NUMBER
8048 BC	16 Pin CERDIP	30mV	0°C to +70°C	ICL 8048 BC JE
8048 BC	16 Pin Plastic DIP	30mV	0°C to +70°C	ICL 8048 BC PE
8048 CC	16 Pin CERDIP	60mV	0°C to +70°C	ICL 8048 CC JE
8048 CC	16 Pin Plastic DIP	60mV	0°C to +70°C	ICL 8048 CC PE
8049 BC	16 Pin CERDIP	10mV	0°C to +70°C	ICL 8049 BC JE
8049 BC	16 Pin Plastic DIP	10mV	0°C to +70°C	ICL 8049 BC PE
8049 CC	16 Pin CERDIP	25mV	0°C to +70°C	ICL 8049 CC JE
8049 CC	16 Pin Plastic DIP	25mV	0°C to +70°C	ICL 8049 CC PE

ICL8063
Power Transistor Driver-Amplifier

FEATURES:

- **Converts ±12V Outputs from Op Amps and other linear functions to ±30V levels**
- **When used in conjunction with general-purpose op amps and external complementary power transistors, system can deliver > 50 Watts to external loads**
- **Has built-in Safe Area Protection and short-circuit protection**
- **Produces 25mA quiescent current in power amp configuration while delivering ±2 Amps output current**
- **Has built in ±13V Regulators to power op amps or other external functions**
- **500kΩ input impedance with R_{BIAS} = 1MΩ**

GENERAL DESCRIPTION

The ICL8063 is a unique monolithic power transistor driver and amplifier that allows construction of minimum chip power amplifier systems, complete with built in safe operating area circuitry, short circuit protection and voltage regulators. It is primarily intended for complementary symmetrical outputs.

Designed to operate with all varieties of operational amplifiers and other functions, two external power transistors of any construction technique, and 8 to 10 passive components, the ICL8063 is ideal for use in such applications as linear and rotary actuator drivers, stepper motor drivers, servo motor drivers, power supplies, power DACs and electronically controlled orifices.

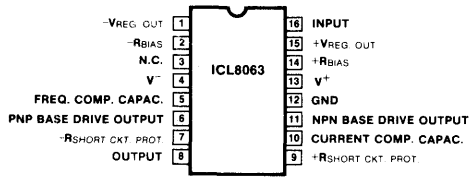
The ICL8063 takes the output levels (typically ±11V) from an op amp and boosts them to ±30V to drive power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 supply up to 100mA to the base leads of the external power transistors.

This amplifier-driver contains internal positive and negative regulators, to drive an op amp or numerous other functions; thus, only ±30V supplies are needed for a complete power amp.

The ICL8063 provides built-in power supplies and will operate from inputs generated by most of the op amps in use today—regardless of technology—as well as many other linear functions, such as timers, comparators and waveform generators. And it will drive almost all power transistors with breakdown voltages up to 70 volts.

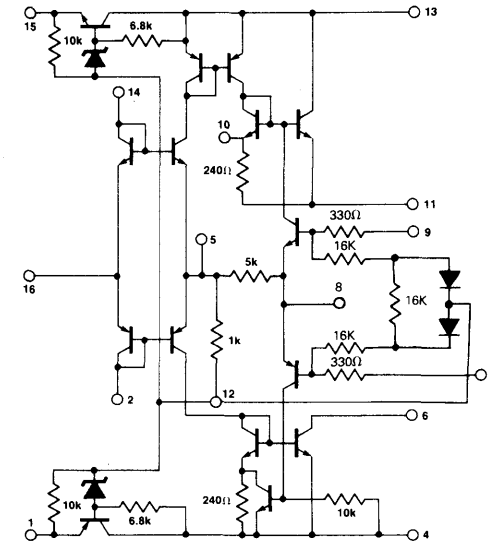
5

PIN CONFIGURATION



(outline dwg JE, PE)

SCHEMATIC DIAGRAM



ORDERING INFORMATION

ICL8063MJE	- CERDIP, −55°C TO 125°C
ICL8063CJE	- CERDIP, 0°C TO +70°C
ICL8063CPE	- PLASTIC DIP, 0°C TO 70°C

ABSOLUTE MAXIMUM RATINGS @ $T_A = 25°C$

Supply Voltage ..... ±35V
Power Dissipation 500mW
Input Voltage (Note 1) ..... ±30V
Operating Temperature Range ..... ICL8063MJE −55°C to +125°C
ICL8063CPE 0°C to 70°C
ICL8063CJE 0°C to 70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Regulator Output Currents ..... 10 mA

Note 1: For supply voltages less than ±30V the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C; $V_{SUPP} = \pm 30V$)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS						UNITS
			ICL8063M			ICL8063C			
			−55°C	+25°C	+125°C	0°C	+25°C	+70°C	
V_{OS}	Max. Offset Voltage	See Figure 1	150	50	50	150	75	75	mV
I_{OH}	Min. Positive Drive Current	See Figure 2	50	50	50	40	40	40	mA
I_{OQ}	Max. Positive Output Quiescent Current	See Figure 3	500	250	250	600	300	300	µA
I_{OL}	Min. Negative Drive Current	See Figure 2	25	25	25	20	20	20	mA
I_{QL}	Max. Negative Output Quiescent Current	See Figure 4	500	250	250	600	300	300	µA
$V_{\pm REG}$	Regulator Output Voltages Range	See Figure 5	±13.7 ±1.2V	±13.7 ±1.0V	±13.7 ±1.5V	±13.7 ±1.0V	±13.7 ±1.0V	±13.7 ±1.0V	V
Z_{IN}	A.C. Input Impedance	See Figure 6	400	400	400	400	400	400	kΩ
V_{SUPP}	Power Supply Range				±5 to ±35V				V
I_Q	Power Supply Quiescent Currents		10	6	6	12	7	7	mA
A_V	Range of Voltage Gain	See Figure 7 V_{IN} = 8Vp-p	6±2	6±2	6±2	6±2	6±2	6±2	V/V
$V_{OUT(MIN)}$	Minimum Output Swing	See Figure 7; Increase V_{IN} until V_{OUT} flattens	±27	±27	±27	±27	±27	±27	V
I_{IN}	Input Bias Current	See Figure 8	100	100	100	100	100	100	µA
I_{REG}	Regulator Output Current	(See Note 2)	10	10	7	10	10	7	mA

Note 2: Care should be taken to ensure that maximum power dissipation is not exceeded.

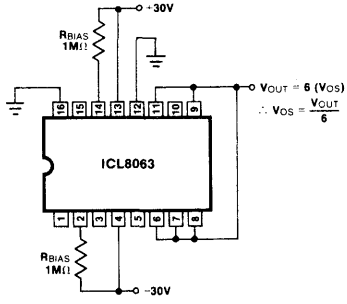
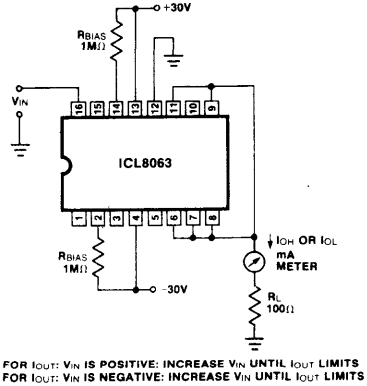


Figure 1: Offset Voltage Measurement



FOR I_{OUT}: V_{IN} IS POSITIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS
FOR I_{OUT}: V_{IN} IS NEGATIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS

Figure 2: Output Current Measurement

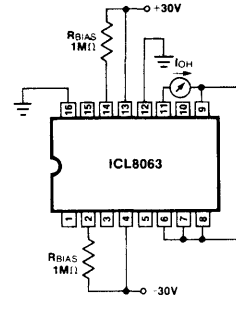


Figure 3: Positive Output Quiescent Current

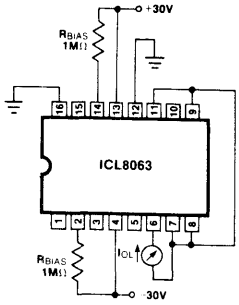


Figure 4: Negative Output Quiescent Current

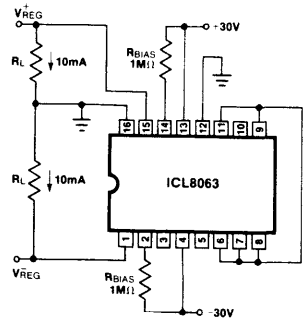


Figure 5: On Chip Regulator Measurement

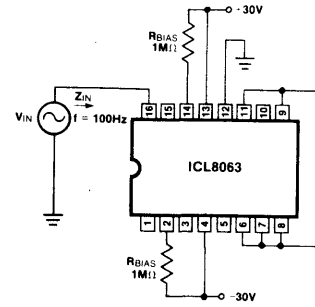


Figure 6: A.C. Input Impedance Measurement

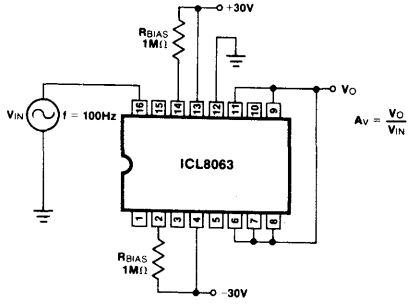


Figure 7: Gain and Output Voltage Swing Measurement

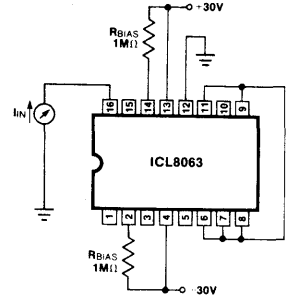


Figure 8: Input Bias Current Measurement

APPLICATION

One problem faced almost every day by circuit designers is how to interface low voltage, low current output world of standard linear and digital devices to that of power transistors and darlingtons—higher by several orders of magnitude.

For example, a low level op amp has a typical voltage range of ±6 to ±12V, and output current usually on the order of about 5 milliamperes. A power transistor with a ±35 volt supply, a collector current of 5 amperes, and a beta, or gain of 100 needs at least 50 milliamperes of drive.

In the past, connecting two transistors with widely dissimilar requirements meant that a rather ornate discrete circuit had to be built to convert the weak output signals from the first into levels large enough to drive the second. However, in addition to converting voltage and current, it was also necessary to include a number of protection circuits to guard against damage from shorts, for example, and all this design work was both tedious and expensive.

The ICL8063 provides a solution to these problems. It's a monolithic power transistor driver and power transistor amplifier circuit on the same chip, has all the necessary safe operating area circuitry and short circuit protection, and has on-chip ±13V voltage regulators to eliminate the need for extra external power supplies.

1. Using the ICL8063 to make a complete Power Amplifier

As Figure 9 shows, using the ICL8063 allows the circuit designer to build a power amplifier block capable of delivering ±2 amperes at ±25 volts (50 watts) to any load, with only three additional discrete devices and 8 passive components. Moreover, the circuit draws only about ±30 milliamperes of quiescent current from either of the ±30V power supplies. A similar design using discrete components would require anywhere from 50 to 100 components.

Slew rate is about the same as that of a 741 op amp, except that the output current can slew up to 2 amps at roughly 1V/μs (that's a 10 ohm load to ground and ±20V output across this resistance). Input current, voltage offset, CMRR and PSRR are also the same. Use of 1,000 picofarad

compensation capacitors (three in this configuration) allows good stability down to unity gain non-inverting (the worst case). This circuit will drive a 1000pF C_L to Gnd, or in other words, the circuit can drive 30 feet of RG-58 coaxial cable for line driver applications with no problems.

As Figure 10 indicates, setting up a current limiting (safe area) protection circuit is straightforward. The 0.4 ohm, 5 watt resistors set the maximum current one can get out of the output. The equation this SOA circuit follows is:

for V_{OUT} positive,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2}(V_{OUT} + I_L R_3 - 0.7V)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2}(V_{OUT})$$

for V_{OUT} negative,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4}(V_{OUT} + I_2 R_3 + 0.7)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4}(V_{OUT})$$

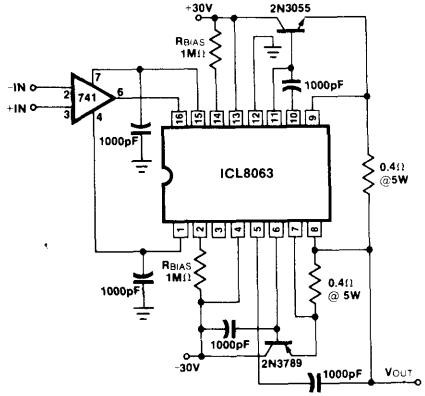


Figure 9: Standard Circuit Diagram

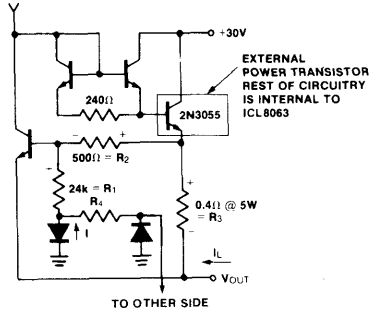
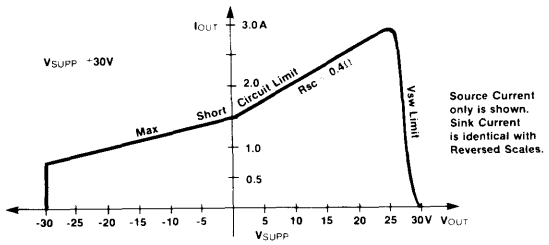


Figure 10: Current Limiting (Safe Area) Protection Circuit (one side shown)



Solving these equations we get the following:

V_{OUT}	I	I_L @ 25°C	I_L @ 125°C
24V	1mA	3 amps	2.4 amps
20V	830μA	2.8 amps	
16V	670μA	2.6 amps	
12V	500μA	2.4 amps	1.8 amps
8V	333μA	2.1 amps	
4V	167μA	1.9 amps	
0V	0μA	1.7 amps	1.1 amps

As these equations indicate, maximum power delivered to a load is obtained when $V_{OUT} \geq 24V$.

Often design requirements necessitate an unsymmetrical output current capability. In that case, instead of the 0.4 ohm resistors protecting the npn and pnp output stages, as shown in Figure 9, simply substitute any other value. For example, if up to 3 amps are required when $V_{OUT} \geq +24V$ and only 1 amp out when $V_{OUT} \geq -24V$, use a 0.4 ohm resistor between pin 8 and pin 9 on the ICL8063 and a 1 ohm, 2 watt resistor between pin 7 and pin 8. Maximum output current versus V_{OUT} for varying values of protection resistors are as follows:

V_{OUT}	0.4Ω @ 25°C	0.68Ω @ 25°C	1Ω @ 25°C
24V	3 amps	1.7 amps	1.2 amps
12V	2.4 amps	1.4 amps	0.9 amps
0V	1.7 amps	1.0 amps	0.7 amps

The biasing resistors located between pin 13 and pin 14 and between pin 2 and pin 4 are typically 1M-ohm for $V_{SUPP} = \pm 30V$, which guarantees adequate performance in such applications as DC motor drivers, power DACs, programmable power supplies and line drivers (with ±30 volt supplies). The table that follows shows the proper value for R_{BIAS} for optimum output current capability with supply voltages between ±5V and ±30V.

$\pm V_{CC}$	R_{BIAS}
30V	1 MΩ
25V	680kΩ
20V	500kΩ
15V	300kΩ
10V	150kΩ
5V	62kΩ

If 30V and 1 meg ohms are used, performance curves appear as shown in Figure 11.

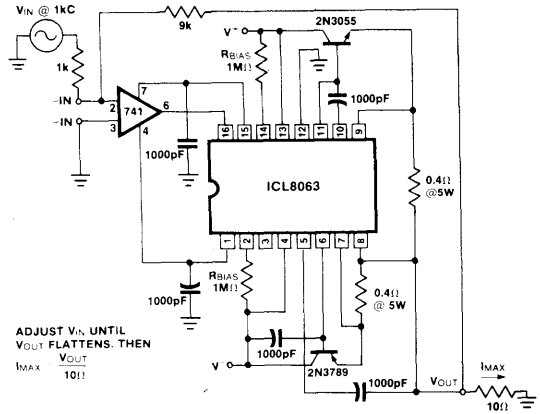
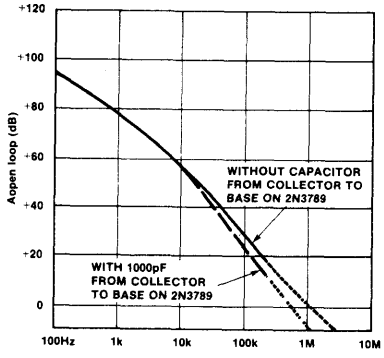


Figure 11: Typical Performance Curve of Max. Output Current Vs. V_{SUPP} For Fixed $R_{BIAS} = 1M\Omega$

When buying external power transistors, careful attention should be paid to beta values. For 2N3055 and 2N3789 transistors used in this circuit, beta should be no more than 150 max at I_C = 20mA and V_{CE} = 30V. This beta value sets the quiescent current at less than 30mA when not delivering power to a load.

The design in Figure 9 will tolerate a short to ground indefinitely, provided adequate heat sinking is used. However if V_{OUT} is shunted to ±30V the output transistors (2N3055 and 2N3789) will be destroyed, but since the safe operating area for these devices is 4 amps at 30 volts, the problem does not occur for V_{SUPP} = ±15V.

A typical bode plot of the power amplifier system is shown in Figure 12. Referring to Figure 6, the schematic for this bode plot is shown below:



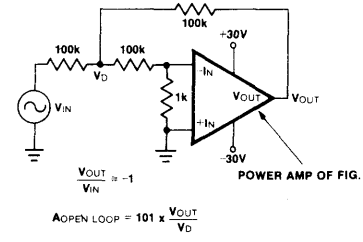
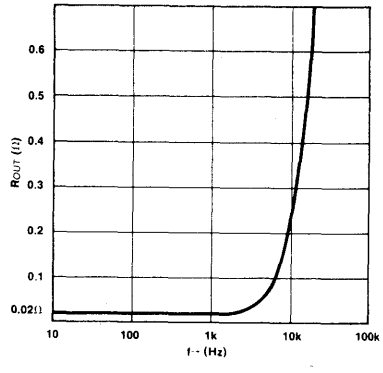


Figure 12: Bode Plot of Open Loop Gain of Above Schematic



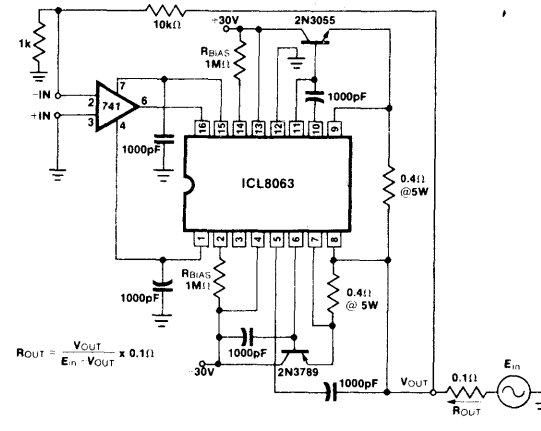


Figure 13: Typical Performance of R_{OUT} vs. Frequency of Power Amplifier System

2. Designing A Simple Functi n Generator

Using a variation of the fundamental power amplifier building block described in the previous section, the ICL8063 can be implemented in the design of a simple, low cost function generator (Figure 14). It will supply sine waves, triangular waves and square waves from 2 hertz to 20 kilohertz. This complete test instrument can be plugged into a standard 110VAC line for power. V_{OUT} will be up to ±25V (50V p-p) across loads as small as 10 ohms (about 2.5 amps maximum output current).

Capacitor working voltages should be greater than 50V DC and all resistors should be 1/2W, unless otherwise indicated. The interconnecting leads from the 741 pins 2 and 3 to their respective resistors should be kept short, less than 2 inches if possible; longer leads may result in oscillation.

Full output swing is possible to about 5KHz; after that the output begins to taper off due to the slew rate of the 741, until at 20KHz the output swing will be about $20V_{pp}$ (±10V). This problem can be remedied by simply using an op amp with a higher slew rate, such as the LF156.

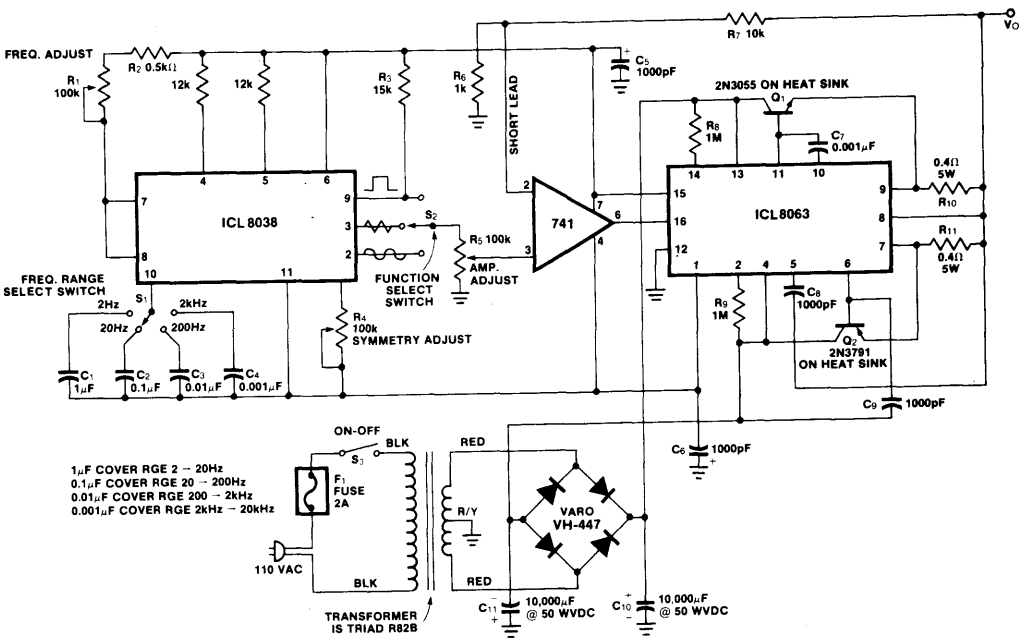


Figure 14: Power Function Generator

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3. Building a Constant Current Motor Drive Circuit

The constant current motor drive configuration shown in Figure 15 is an extremely simple circuit to construct using the ICL8063. This minimum device circuit can be used to drive DC motors where there is some likelihood of stalling or lock up; if the motor locks, the current drive remains constant and the system does not destroy itself. Using this approach two 6V batteries are sufficient for decent performance. A 10 volt input will produce one amp of output current to drive the motor, and if the motor is stalled, I_{OUT} remains at 1 amp.

For example, suppose it's necessary to drive a 24V DC motor with 1 amp of drive current. First make V_{SUPP} at least 6 volts more than the motor being driven (in this case 30 volts). Next select R_{BIAS} according to V_{SUPP} from the data sheet, which indicates $R_{BIAS} = 1M\Omega$. Then choose R_1, R_2, and R_a for optimum sensitivity. That means making $R_a = 1\Omega$ to minimize the voltage drop across R_a (the drop will be 1 amp x 1 ohm or 1 volt). If 1 amp/volt sensitivity is desirable let $R_2 = R_1 = 10k\Omega$ to minimize feedback current error. Then a ±1V input voltage will produce a ±1 amp current through the motor.

Capacitors should be at least 50 volts working voltage and all resistors 1/2W, except for those valued at 0.4 ohms, and R_a. Power across $R_a = I \times V = 1$ amp x 1 volt = 1 watt, so at least a 2 watt value should be used. Use large heat sinks for the 2N3055 and 2N3791 power transistors. A Delta NC-641 or the equivalent is appropriate. Use a thermal compound when mounting the transistor to the heat sink. (See Intersil ICH8510 data sheet).

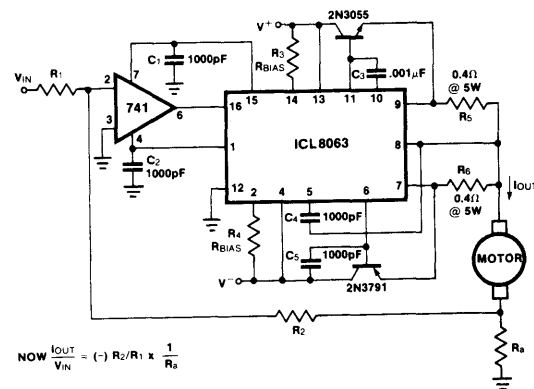


Figure 15: Constant Current Motor Drive

4. Building A Low Cost 8 ohm per channel Hi-fi Amplifier.

For about $20 per channel, it's possible to build a high fidelity amplifier using the ICL8063 to drive 8 ohm speakers. A channel is defined here as all amplification between turntable or tape output and power out. (Figure 16)

The input 741 stage is a preamplifier with R.I.A.A. equalization for records. Following the first 741 stage is a 10kΩ control pot, whose wiper arm feeds into the power amplifier stage consisting of a second 741, the ICL8063 and

the power transistors. To achieve good listening results, selection of proper resistance values in the power amplifier stage is important. Best listening is to be found at a gain value of 6 [(5kΩ + 1kΩ/1kΩ = 6)]. 3 is a practical minimum, since the first stage 741 preamp puts out only ±10 volt maximum signals, and if maximum power is necessary this value must be multiplied by 3 to get ±30 volt levels at the output of the power amp stage.

Each channel delivers about 56 volts p-p across an 8 ohm speaker and this converts to 50 watts RMS power. This is derived as follows:

$$\text{Power} = \frac{V_{rms}^2}{8\ \text{ohms}},\quad V_{rms} = \frac{56V\ p\text{-}p}{2.82} = 20V,\ 20V^2 = 400V^2$$

$$\therefore \text{Power} = \frac{400^2}{8\ \text{ohms}} = 50\ \text{watts RMS Power.}$$

Distortion will be < 0.1% up to about 100Hz, and then it increases as the frequency increases, reaching about 1% at 20kHz.

The ganged switch at the input is for either disc playing or FM, either from an FM tuner or a tape amplifier. Assuming DC coupling on the outputs, there is no need for a DC reference to ground (resistor) for FM position. To clear the signal in the FM position, place a 51kΩ resistor to ground as shown in Figure 16 (from FM input position to ground).

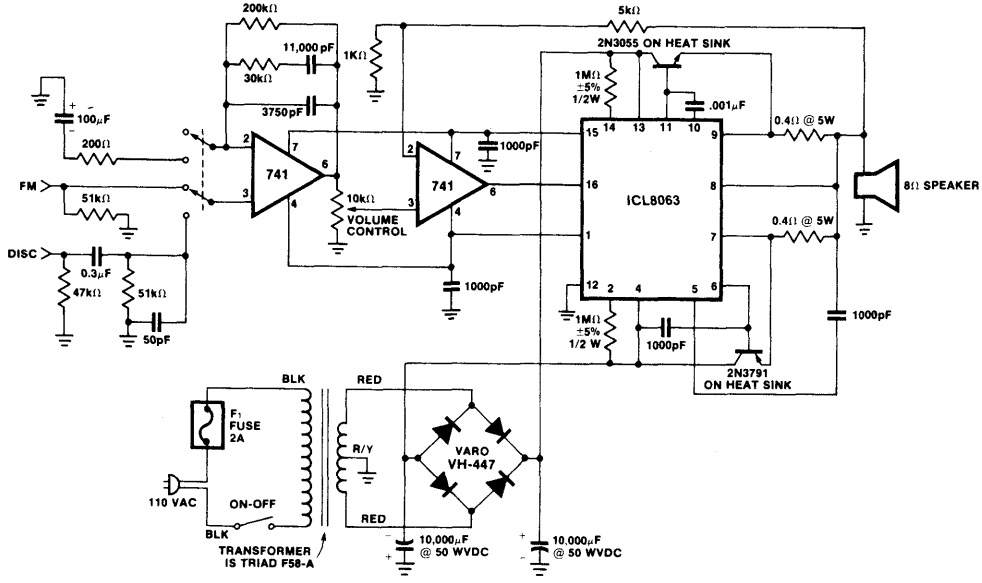
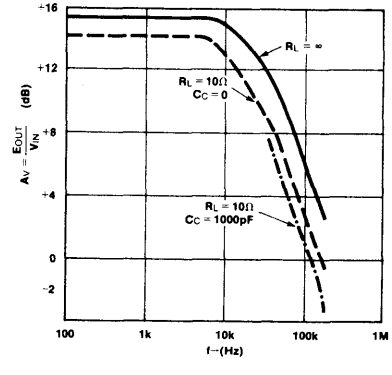


Figure 16: Hi Fi Amplifier



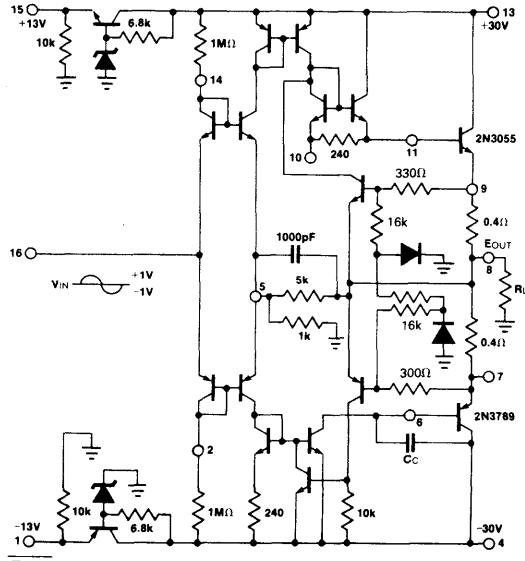
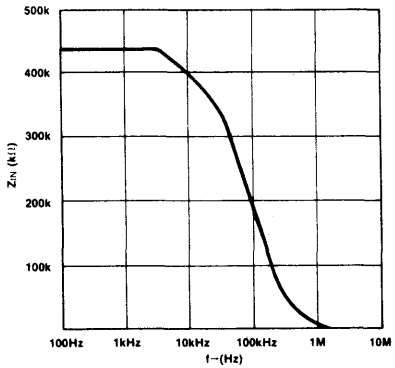


Figure 17: Typical Performance Curve of $\frac{E_{OUT}}{V_{IN}}$ vs. Frequency For Typical Circuit Shown



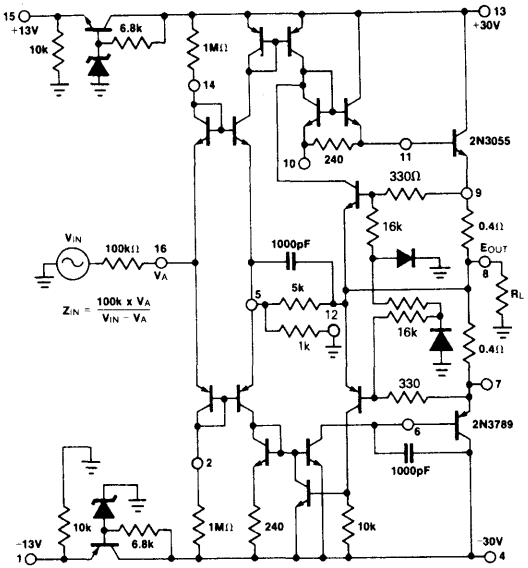
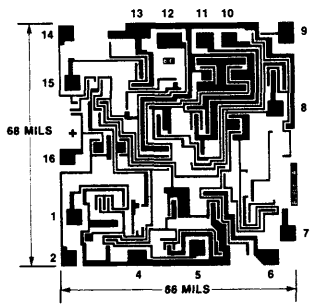


Figure 18: Typical Performance Curve of Input Impedance Versus Frequency for Typical Circuit Shown

5

CHIP TOPOGRAPHY



Note: Intersil offers a hybrid power amplifier similar to that shown in fig. 9. See ICH8510/8520/8530 data sheet for details.

ICL8069 Series
Low Voltage Reference

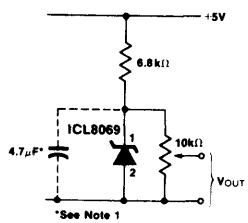
FEATURES

- **Temperature Coefficient guaranteed to 10 ppm/°C max.**
- **Low Bias Current . . . 50μA min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

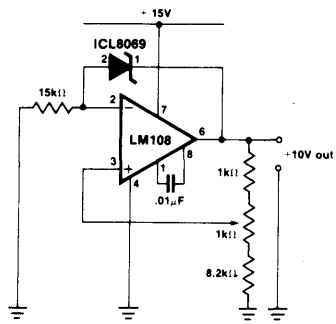
GENERAL DESCRIPTION

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

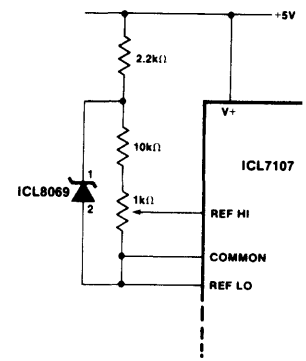
TYPICAL CONNECTION DIAGRAMS



(a) Simple Reference (1.2 volts or less)



(b) Buffered 10V Reference using a single supply.



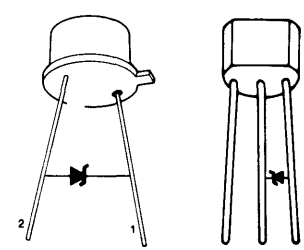
(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

ORDERING INFORMATION

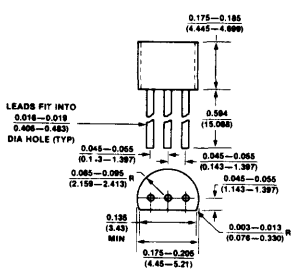
Max. Temp. Coeff. of V_{REF}	Temp. Range	Order P/N TO-92	Order P/N TO-52
0.001%/°C	0°C to +70°C		ICL8069ACSQ
0.0025%/°C	0°C to +70°C		ICL8069BCSQ
0.005%/°C	0°C to +70°C	ICL8069CCZR	ICL8069CCSQ
0.005%/°C	-55°C to +125°C	—	ICL8069CMSQ
0.01%/°C	0°C to +70°C	ICL8069DCZR	ICL8069DCSQ
0.01%/°C	-55°C to +125°C	—	ICL8069DMSQ

PIN CONFIGURATION

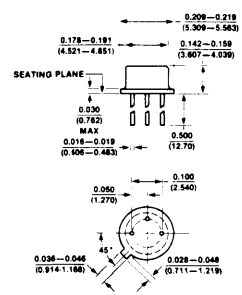
TO-52 TO-92



PACKAGE DIMENSIONS

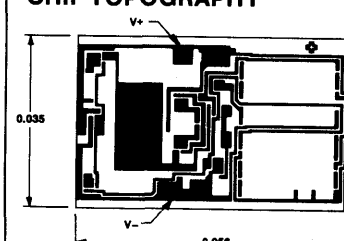


TO-92



TO-52

CHIP TOPOGRAPHY



ABSOLUTE MAXIMUM RATINGS

Reverse Voltage ..... See Note 2
Forward Current 10mA
Reverse Current 10mA
Power Dissipation . Limited by max forward/reverse current
Storage Temperature ..... −65°C to +150°C
Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... −55°C to +125°C
Lead Temperature (Soldering, 10 Sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

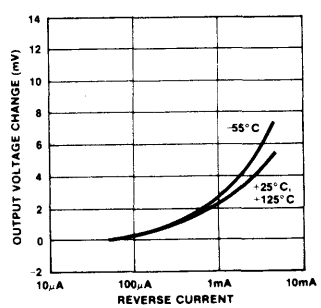
ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse breakdown Voltage	I_R = 500μA	1.20	1.23	1.25	V
Reverse breakdown Voltage change	50μA ≤ I_R ≤ 5mA		15	20	mV
Reverse dynamic Impedance	I_R = 50μA I_R = 500μA		1 1	2 2	Ω
Forward Voltage Drop	I_F = 500μA		.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500μA		5		μV
Breakdown voltage Temperature coefficient: ICL8069A ICL8069B ICL8069C ICL8069D	I_R = 500μA T_A = operating temperature range (Note 3)			.001 .0025 .005 .01	%/°C
Reverse Current Range		.050		5	mA

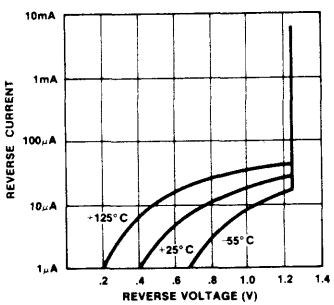
5

TYPICAL PERFORMANCE CHARACTERISTICS

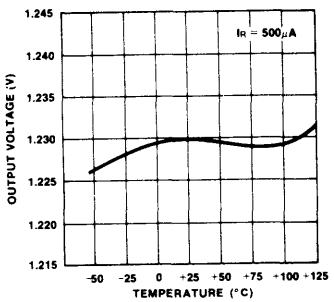
VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



REVERSE VOLTAGE AS A FUNCTION OF CURRENT



REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



Notes:

1) If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.
2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
3) For the military part, measurements are made at 25°C, −55°C, and +125°C. The unit is then classified as a function of the worst case T.C. from 25°C to −55°C, or 25°C to +125°C.

ICL8075–9

Ultra Precision Temperature Stabilized Voltage References

FEATURES

- **Laser-trimmed to precise voltage**
- **Extremely low temperature coefficient (typ < 1ppm/°C)**
- **Short-circuit protected**
- **Thermally isolated die for minimum power consumption**
- **Separate heater supply for good noise rejection, application flexibility**
- **Wide range of end-use oriented output voltages**
- **Wide operating voltage range on both reference and heater**
- **Heater control system operates correctly at low voltage, avoiding thermal latchup problems**

GENERAL DESCRIPTION

5

The ICL8075-9 are a family of precision laser-trimmed voltage references that incorporate a substrate heater to produce extremely low overall voltage temperature coefficients.

The series of devices is produced by adjusting basic parts with various metal masks so that exact voltages are available for the most popular A/D and D/A converters. This avoids the necessity to perform adjustments in most cases, and reduces the problems with trim range and temperature coefficient loss in all others.

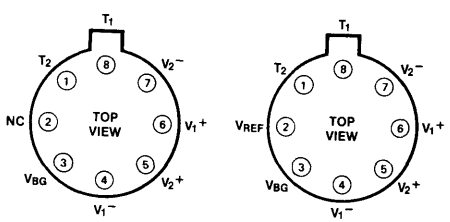
This series is divided into two basic groups, those with outputs less than the band-gap voltage (ICL8075/6), and those with higher outputs (ICL8077/8/9). The nominal reference voltage (cardinal value) is coded in the second part of the number, with two digits and a "D" for a decimal value or a "B" for a binary value, at the decimal point location.

Each device is packaged in a standard 8-pin TO-99 package, but the die is mounted on an insulating ceramic substrate to ensure a high thermal resistance from the die to the case. This usually undesirable condition is beneficial in this case, since it reduces the power consumption of the heater as far as possible, and facilitates maintaining the die temperature at about 85°C, even in cold ambient conditions.

ORDERING INFORMATION

PART NUMBER	VOLTAGE	0.4% (8-BIT)	0.03% (12-BIT)
ICL8075-0D1	0.10	ICL8075-0D1JCTV	ICL8075-0D1LCTV
ICL8076-1D0	1.00	ICL8076-1D0JCTV	ICL8076-1D0LCTV
ICL8077-2D5	2.50	ICL8077-2D5JCTV	ICL8077-2D5LCTV
ICL8077-2B5	2.56	ICL8077-2B5JCTV	ICL8077-2B5LCTV
ICL8078-5D0	5.00	ICL8078-5D0JCTV	ICL8078-5D0LCTV
ICL8078-5B1	5.12	ICL8078-5B1JCTV	ICL8078-5B1LCTV
ICL8079-10D	10.00	ICL8079-10DJCTV	ICL8079-10DLCTV
ICL8079-10B	10.24	ICL8079-10BJCTV	ICL8079-10BLCTV

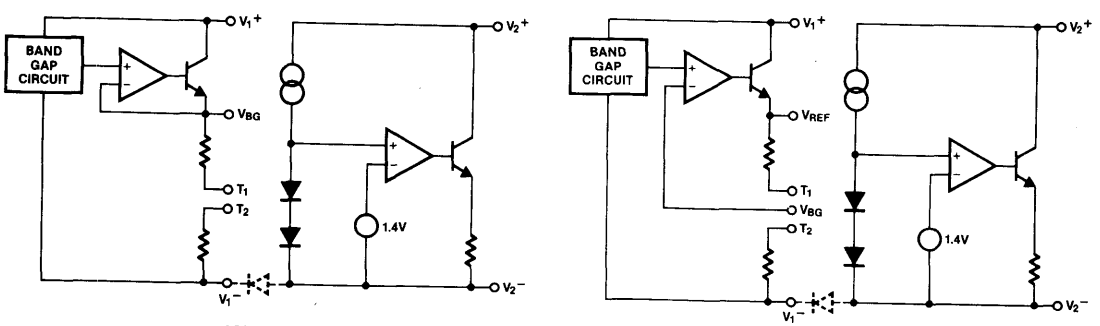
PIN CONFIGURATION (outline dwg TV)



ICL8075/6 ICL8077/8/9

TO-99

BLOCK DIAGRAMS



ICL8075/6 ICL8077/8/9

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_1^+ to V_1^- 36V
Heater Supply V_2^+ to V_2^- 36V
Supply Differential V_1^- to V_2^- 0V-36V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −65°C to +160°C
Power Dissipation (@ 25°C) 450mW
derate @ other temperatures @ 4mW/°C
Heater Current 150mA
Output Current 35mA
Lead Temperature (Soldering, 10 sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V_1^+ = 15V$, $V_2^+ = 15V$, $V_1^- = V_2^- = 0V$, $T_A = 25°C$ unless otherwise specified.

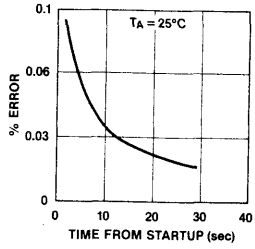
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Ranges Reference Supply Heater Supply	 V_1^+ V_2^+	 ($V_{REF} > 1.2$)	 3.2 $V_{OUT} + 2$ 8		 30 30 30	 V
Absolute Accuracy of V_{OUT}		Heater Settled J Grade L Grade		0.1 0.02	0.4 0.03	%
Line Regulation		V_1^+ to V_1^- = 15V to 30V		0.002	0.005	%/V
Load Regulation of V_{OUT} (ICL8077/8/9 Only)		I_{OUT} = 0mA to 5mA		0.03	0.05	%/mA
Short-Circuit Limits V_{OUT} (ICL8075/6) (ICL8077/8/9) V_{BG} (ICL8075/6) (ICL8077/8/9)	I_{SC}	 (Note 1)		 1 20 20 1	 40 40	mA
Output Drive Capability V_{OUT} V_{BG}		 ICL8077/8/9 Only (Note 2) ICL8075/6 Only	 5 0	 7		mA
Maximum Heater Current	I_{HTR}			90	130	mA
Supply Current Reference Section Heater Section	 I_1^+ I_2^+	 Device Warmed Up (Still Air)	 10	 250 15	 450 20	 μA mA
Temperature Coefficient of V_{OUT}		$V_2^+ > 8V$, $-55°C < T_A < +85°C$ $+85°C < T_A < +125°C$ (or $V_2^+ = 0$)		1 20		ppm/°C
Settling Time, Heater Power-Up		To 0.03% of Final Value		10	30	sec

Note 1. This will cause the output voltage to rise to approximately V_1^+, potentially hazardous to the load.
Note 2. The output impedance of V_{OUT} on the ICL8075/6 and of V_{BG} on the ICL8077/8/9 is about 5kΩ. Loading either of these points can lead to serious errors.

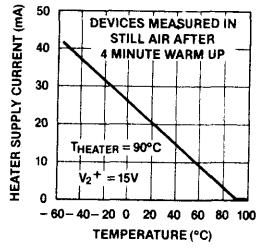
5

TYPICAL CHARACTERISTICS

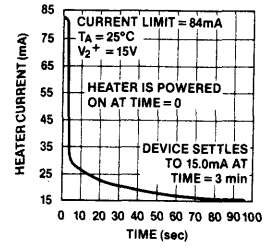
Output Voltage vs Warm-Up Time



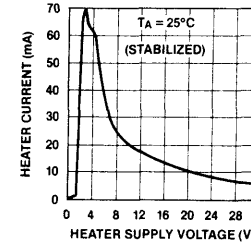
Heater Current vs Ambient Temperature



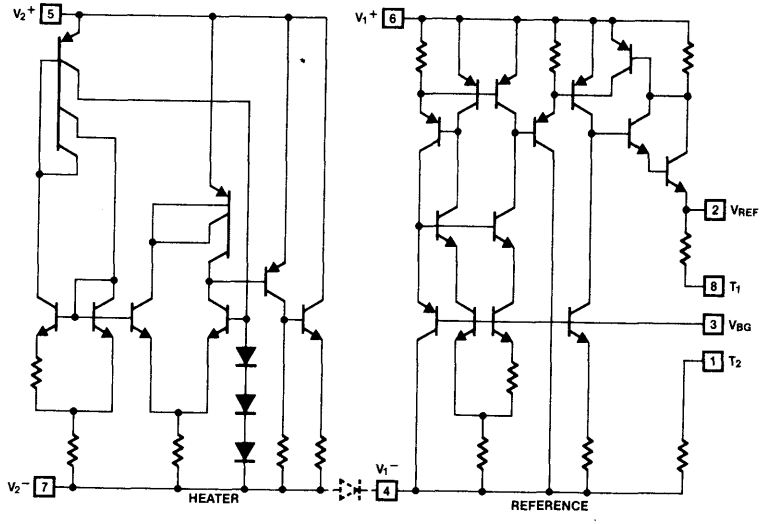
Heater Current vs Warm-Up Time



Heater Current vs Heater Voltage



EQUIVALENT SCHEMATIC DIAGRAM (ICL8077/8/9 Shown)



DETAILED DESCRIPTION

The ICL8075-9 family consists of two semi-independent circuits within one die. One of these is a band-gap reference circuit with several possible mask options, each of which can be laser-trimmed to a specific value of output voltage. The circuit configuration depends on whether this voltage is less than or greater than the actual band-gap voltage (1.25V) itself. The laser-trimming is also used to reduce as far as possible the intrinsic temperature coefficient of the basic band-gap circuit. For devices whose output is lower than 1.2V, the band-gap voltage is divided by a pair of resistors to provide the required output, with the ratio of these resistors being adjusted to achieve the desired result. The higher output devices divide down the output of the internal amplifier to the band-gap value, again adjusting the resistor ratio to the requisite value.

The other section of the circuit is a constant temperature heater system, which takes another band-gap type voltage and compares it to the voltage drop across a string of diodes. The result of the comparison is used to drive a pair of large heater transistor/resistor elements. The inherent feedback of this combination causes the die to be heated until the diode drop matches the band-gap-derived reference level, thus ensuring an almost constant temperature on the die. Care has been taken in the die layout to ensure that the large currents and temperature gradients associated with the heater do not degrade the accuracy and consistency of the band-gap reference output of the other section. Also, the die has been mounted on a thermally isolating substrate to reduce the required heater power and the temperature gradients across the die. The result is that the reference circuit sees only about 1/100 of the ambient temperature change, allowing a 1ppm/°C temperature coefficient to be achieved in monolithic form.

The coexistence of two circuits on one die has some implications, however. The high currents that flow in the heater section need to be isolated from the reference section, so separate supply pins are provided for the two sections. Although these are fairly independent, there is only one substrate for the die, which must be attached to one of the supplies, and therefore restrict the "freedom" of the other. In the ICL8075 family, the substrate is tied to the negative terminal of the heater supply (V_2^-), and the negative supply of the reference section (the V_1^- pin) must not be allowed to be negative with respect to this point.

The heater will take some time to heat the die up to its operating temperature. During this time, the output voltage will change at a rate determined by the intrinsic temperature coefficient of the reference, leading to some appreciable "warm-up" drift. The time required for this drift is given as the settling time for the heater, although the heater dissipation settling time is substantially longer, owing to the longer thermal time constants of the package. Further, the choice of the die operating temperature leads to some compromises also. Clearly, the higher the operating temperature, the more power needed to sustain it at any given ambient temperature, and also the poorer the reliability of the device. On the other hand, if too low a temperature is chosen, the point at which temperature stabilization breaks down will be within the desirable operating range, leading to a degraded temperature coefficient. The ICL8075 family is laser-trimmed to stabilize at about + 85°C, so that the temperature coefficient break point is outside the commercial and industrial temperature ranges.

The trim pads on the ICL8075/6 and ICL8077/8/9 can be used to adjust the output voltage, in either direction, to finer precision than is available in the part itself. Figures 1 and 2 show two methods of adjustment, suitable for either type of device.

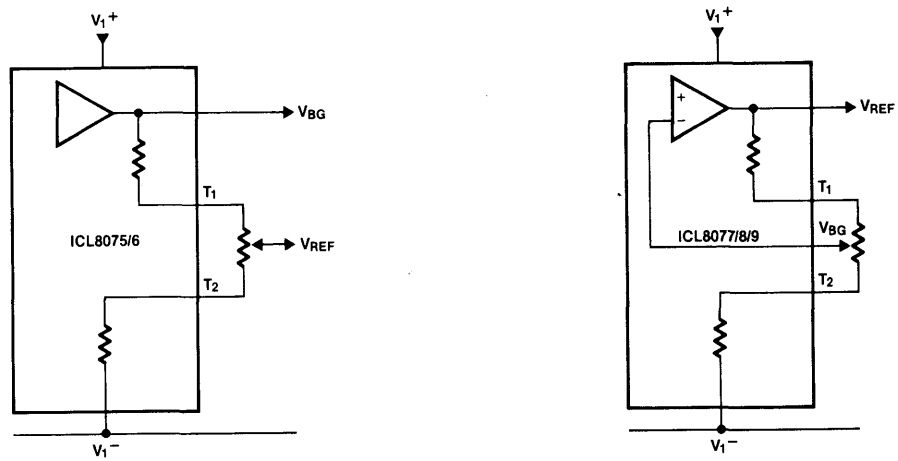


Figure 1. Fine Trim Circuit

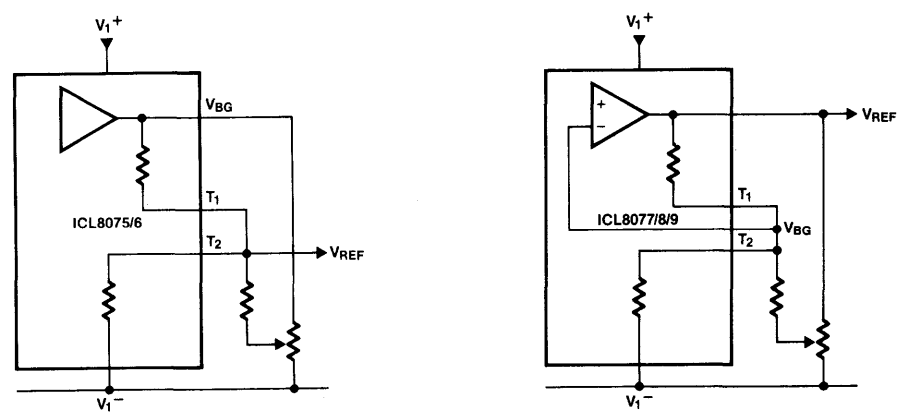


Figure 2. Alternative Trim Circuit

APPLICATIONS

There are many possible applications of reference circuits, of course. One typical use is in A/D converters, such as the 4½-digit integrating converter shown in Figure 3. This schematic is roughly that of the ICL7135EV/Kit evaluation kit, on which provision has been made to accept an ICL8076-1D0 as a 1.000V reference. The PC board includes space for a potentiometer for fine adjustment of the voltage, since the accuracy of the ICL7135 is higher than that of the best grade of ICL8076.

Another common requirement is for references for D/A converters, such as the ICL7134 shown in Figure 4. This device offers 14-bit accuracy, without laser-trimming, by the expedient of using a CMOS PROM on the die to correct for the errors of the analog section. The circuit shown is that with a bipolar output, using a chopper-stabilized op amp, the ICL7650, to achieve high accuracy without adjustments and at low cost. A "binary" type of reference here will lead to a decimal value for the LSB; thus a 10.24V reference gives an LSB of 1/16mV.

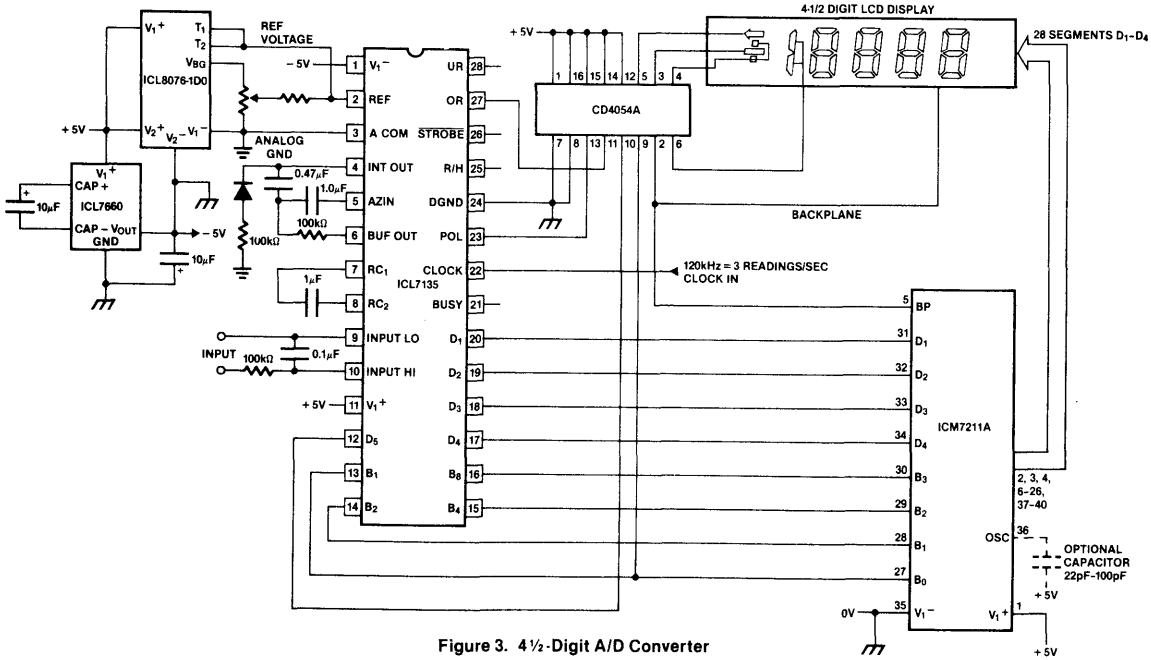


Figure 3. 4½-Digit A/D Converter

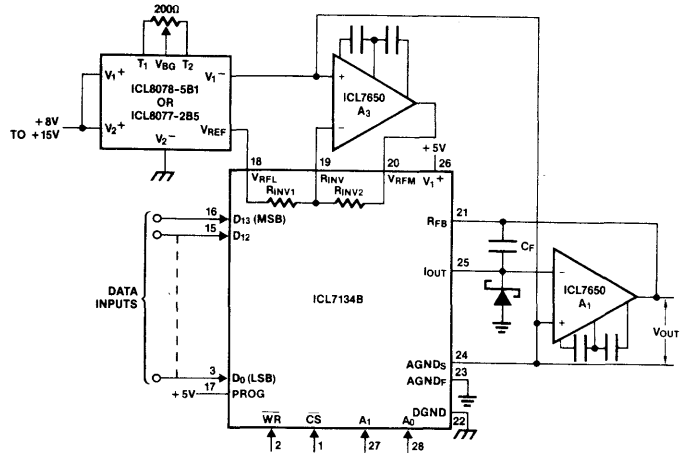


Figure 4. 14-Bit D/A Converter Without Adjustments

APPLICATIONS (Continued)

Other applications are in accurate power supply circuits, such as that shown in Figure 5, which uses an ICH8530 power amplifier and a standard AD7541 DAC to set the output value.

Up to 3A at up to ± 30V can be controlled by this circuit, with errors well under 0.1%. The circuit is based on the same principle as Figure 4, but with a power output buffer.

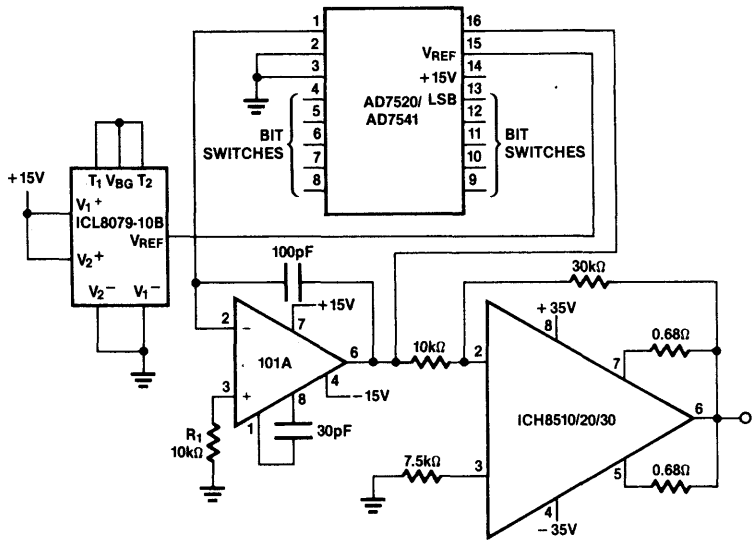


Figure 5. Accurate Power Supply Circuit

ICL8211, ICL8212

Programmable Voltage Reference

FEATURES

- **High accuracy voltage sensing and generation: internal reference 1.15 volts typical**
- **Low sensitivity to supply voltage and temperature variations**
- **Wide supply voltage range: Typ. 1.8 to 30 volts**
- **Essentially constant supply current over full supply voltage range**
- **Easy to set hysteresis voltage range**
- **Defined output current limit - ICL8211**
  High output current capability - ICL8212

GENERAL DESCRIPTION

The Intersil ICL8211/12 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

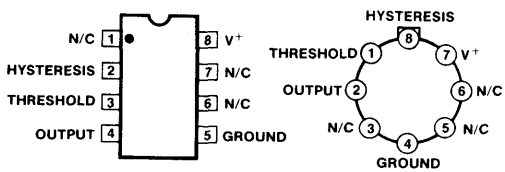
Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Applications include:

1. Low voltage sensor/indicator
2. High voltage sensor/indicator
3. Non volatile out-of-voltage range sensor/indicator
4. Programmable voltage reference or zener diode
5. Series or shunt power supply regulator
6. Fixed value constant current source

5

PIN CONFIGURATION

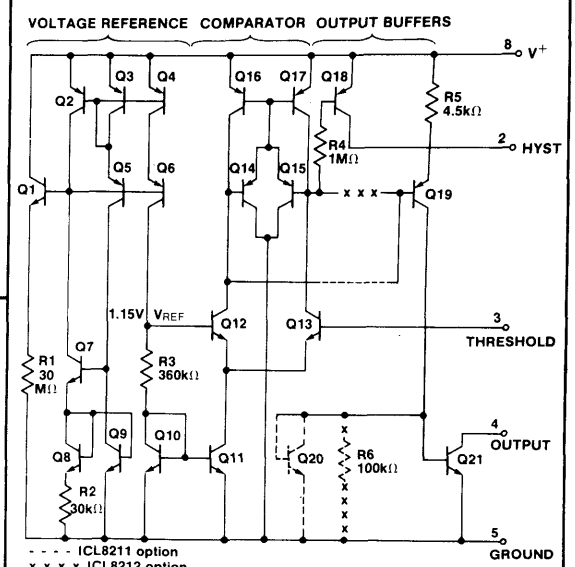


(outline dwg PA) (outline dwg TY)

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0 to +70°C	8 lead Mini DIP
ICL8211CTY	0 to +70°C	TO-99 Can
ICL8211MTY	−55° to +125°C	TO-99 Can
ICL8212CPA	0 to 70°C	8 lead Mini DIP
ICL8212CTY	0 to 70°C	TO-99 Can
ICL8212MTY	−55 to +125°C	TO-99 Can
ICL8211D	Dice only	
ICL8212D	Dice only	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... −0.5 to +30 volts
Output Voltage ..... −0.5 to +30 volts
Hysteresis Voltage ..... +0.5 to −10 volts
Threshold Input Voltage ..... +30 to −5 volts with respect to GROUND and +0 to −30 volts with respect to V^+
Current into Any Terminal ..... ±30mA
Power Dissipation (Note 1 & 2) 300mW
Operating Temperature Range ICL8211M/12M ..... −55°C to +125°C
Operating Temperature Range ICL8211C/12C ..... 0 to +70°C
Storage Temperature Range ..... −65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/12MTY products. Derate linearly at −10mW/°C for ambient temperatures above 100°C.

NOTE 2: Derate linearly above 50°C by −10mW/°C for ICL8211C/12C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

TYPICAL OPERATING CHARACTERISTICS (V^+ = 5V, T_A = 25°C unless otherwise specified)

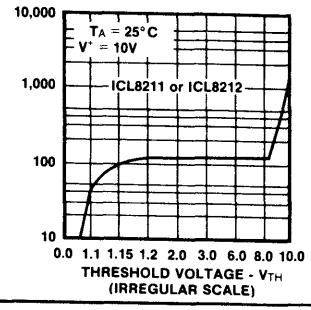
PARAMETER	SYMBOL	CONDITIONS	ICL8211			ICL8212			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I^+	2.0 < V^+ < 30							
		V_T = 1.3V	10	22	40	50	110	250	μA
		V_T = 0.9V	50	140	250	10	20	40	μA
Threshold Trip Voltage	V_{TH}	I_{OUT} = 4mA V^+ = 5V	0.98	1.15	1.19	1.00	1.15	1.19	V
		V_{OUT} = 2V V^+ = 2V	0.98	1.145	1.19	1.00	1.145	1.19	V
		V^+ = 30V	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	I_{OUT} = 4 mA V_{OUT} = 2V I_{HYST} = 7μA V_{HYST} = 3V		−8.0			−0.5		mV
Guaranteed Operating Supply Voltage Range	V_{SUPP}	+25°C	2.0		30	2.0		30	V
		0 to +70°C	2.2		30	2.2		30	V
		−55°C to +125°C	2.8		30	2.8		30	V
Typical Operating Supply Voltage Range	V_{SUPP}	+25°C	1.8		30	1.8		30	V
		+125°C	1.4		30	1.4		30	V
		−55°C	2.5		30	2.5		30	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	I_{OUT} = 4mA V_{OUT} = 2V		+200			+200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	$\Delta V_{TH}/\Delta V^+$	Δ V^+ = 10% at V^+ = 5V		1.0			1.0		mV
Threshold Input Current	I_{TH}	V_{TH} = 1.15V		100	250		100	250	nA
		V_{TH} = 1.00V		5			5		nA
Output Leakage Current	I_{OLK}	V_{OUT} = 30V V_{TH} = 1.0V						10	μA
		V_{OUT} = 30V V_{TH} = 1.3V			10				μA
		V_{OUT} = 5V V_{TH} = 1.0V						1	μA
		V_{OUT} = 5V V_{TH} = 1.3V			1				μA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 4mA V_{TH} = 1.0V		0.17	0.4				V
		V_{TH} = 1.3V					0.17	0.4	V
Max Available Output Current	I_{OH}	(Note 3 & 4) V_{TH} = 1.0V	4	7.0	12				mA
		V_{OUT} = 5V V_{TH} = 1.3V				15	35		mA
		−55°C ≤ T_A ≤ 125°C V_{TH} = 1.0V			15	12			mA
Hysteresis Leakage Current	I_{LHYS}	V^+ = 10V V_{TH} = 1.0V V_{HYST} = V^-			0.1			0.1	μA
Hysteresis Sat Voltage	$V_{HYS\ (max)}$	I_{HYST} = −7μA V_{TH} = 1.3V measured with respect to V^+		−0.1	−0.2		−0.1	−0.2	V
Max Available Hysteresis Current	$I_{HYS\ (max)}$	V_{TH} = 1.3V	−15	−21		−15	−21		μA

NOTE 3: The maximum output current of the ICL8211 is limited by design to 15ma under any operating conditions. The output voltage may be sustained at any voltage up to +30 as long as the maximum power dissipation of the device is not exceeded.

NOTE 4: The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30ma and that the maximum power dissipation of the device is not exceeded.

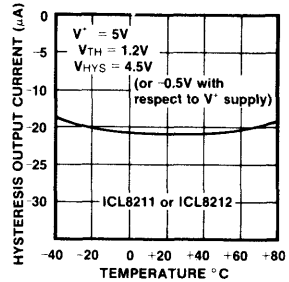
TYPICAL OPERATING CHARACTERISTICS

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



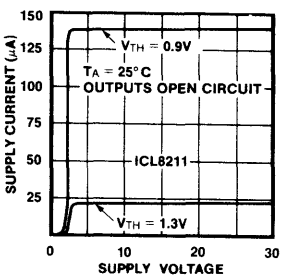
Characteristics common to both the ICL8211 and the ICL8212

HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

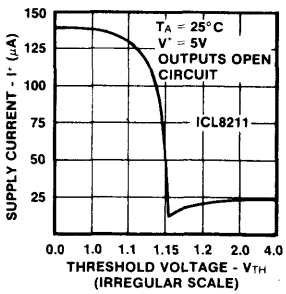


Characteristics ICL8211

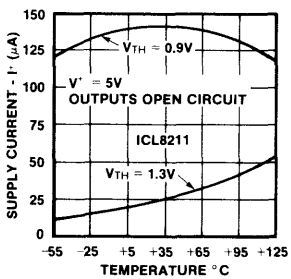
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



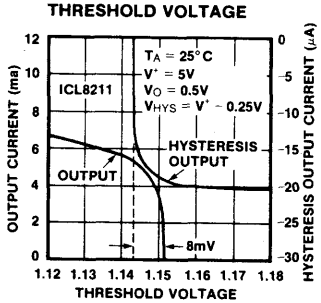
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



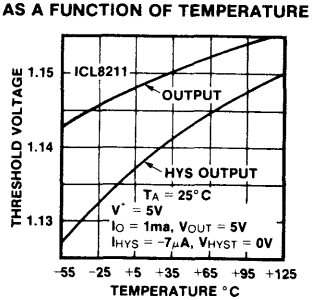
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



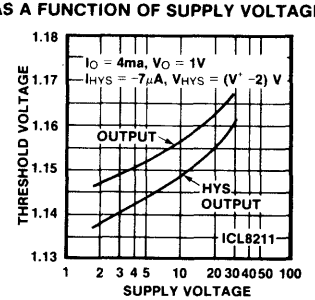
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



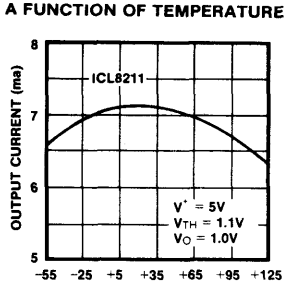
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



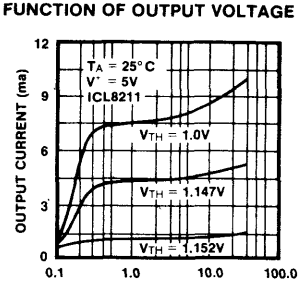
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



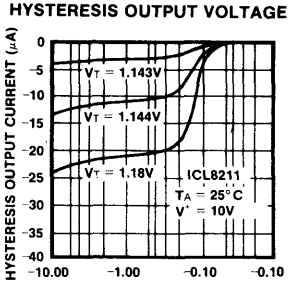
OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



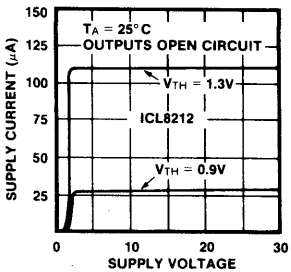
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



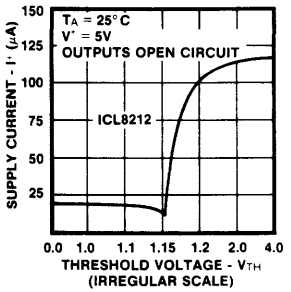
TYPICAL OPERATING CHARACTERISTICS

Characteristics ICL8212

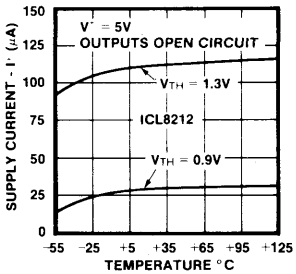
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



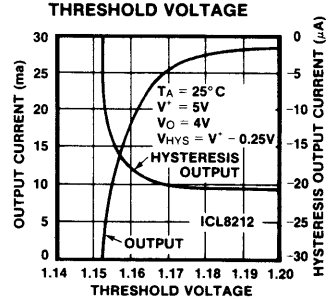
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



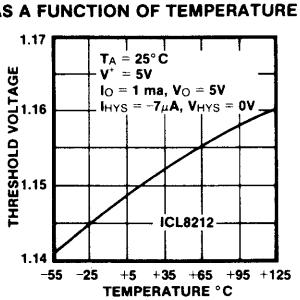
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



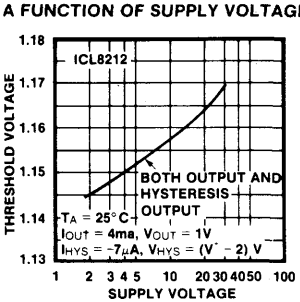
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



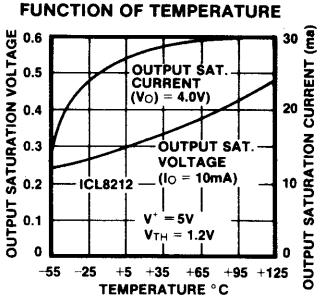
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



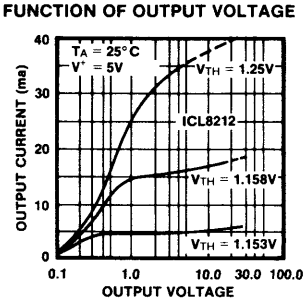
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



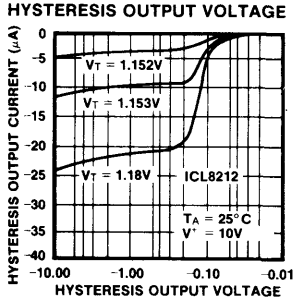
OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



CIRCUIT DESCRIPTION

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 thru Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per °C).

Components Q_2 thru Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9, and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and

Q_9 is

$$I_C\ (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ell n\ 7$$

or approximately 1μA at 25°C

Where k = Boltzman's constant
q = charge on an electron
and T = absolute temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the V_{CE} of Q_3, Q_4, and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant current source; there being two stable states for this type of circuit - either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; Q_{10} is matched to Q_9. Thus the I_C and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

5

$$\text{Thus } 1.15 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ell n\ 7$$

$$\text{which provides } \frac{R_3}{R_2} = 12 \text{ (approx.)}$$

The total supply current consumed by the voltage reference section is approximately 6μA at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17}. The outputs from the comparator are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100μA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximaely 7mA, whereas for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21}, resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

1. GENERAL INFORMATION

THRESHOLD INPUT CONSIDERATIONS

Although any voltage between -5V and V^+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6 volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

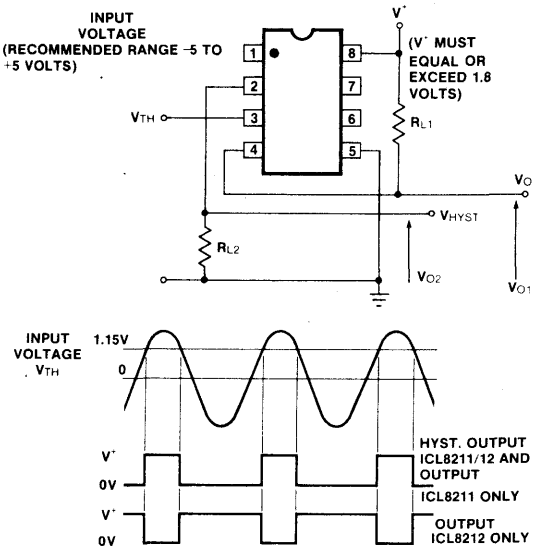


Figure 1: Voltage Level Detection

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 1 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

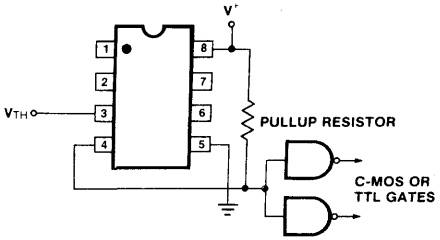


Figure 2: Output Logic Interface

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V_{TH}. For high accuracy, currents as large as 50μA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6μA may be considered without a great loss of accuracy. 6μA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

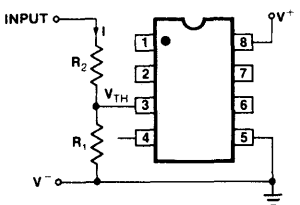


Figure 3: Input Resistor Network Considerations

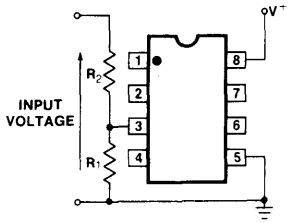
Case 1. High accuracy required, current in resistor network unimportant Set I = 50μA for V_{TH} = 1.15 volts $\therefore$ $R_1 \rightarrow$ 20k ohms.

Case 2. Good accuracy required, current in resistor network important Set I = 7.5μA for V_{TH} = 1.15 volts $\therefore$ $R_1 \rightarrow$ 150k ohms.

SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection - no hysteresis

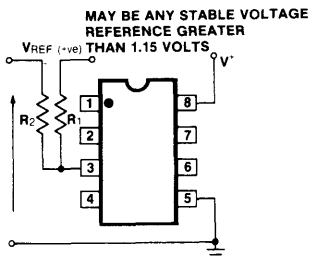
Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 4 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.



a) Range of input voltage greater than +1.15 volts.

Input voltage to change the output states

$$= \frac{(R_1 + R_2)}{R_1} \quad X\ 1.15 \text{ volts}$$



b) Range of input voltage less than +1.15 volts.

Input voltage to change the output states

$$= \frac{(R_1 + R_2)\ X\ 1.15}{R_1} - \frac{R_2\ V_{REF}}{R_1}$$

Figure 4: Input Resistor Network Setup Procedures

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 5.

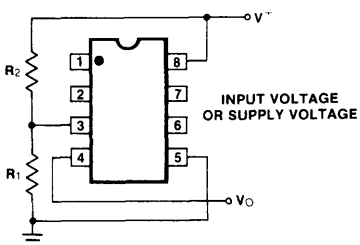


Figure 5: Combined Input and Supply Voltages

Conditions for correct operation of OUTPUT (terminal #4).

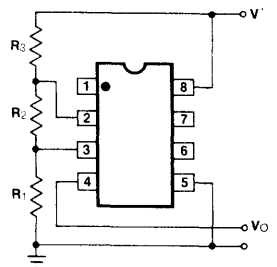
1. ICL8211
   $1.8V \leq V^+ \leq 30V$
2. ICL8212
   $0 \leq V^+ \leq 30V$

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications - refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 6.

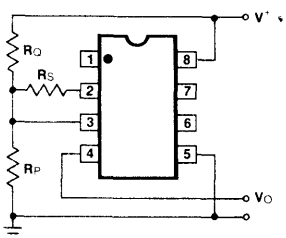


a) Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2) \times 1.15}{R_1} + 0.1\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



b) Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + R_P\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$

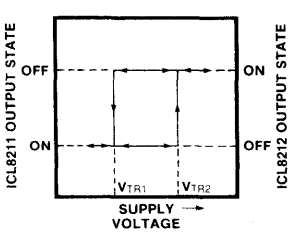


Figure 6: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

Circuit (a) requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

3. PRACTICAL APPLICATIONS

a) Low Voltage Battery Indicator

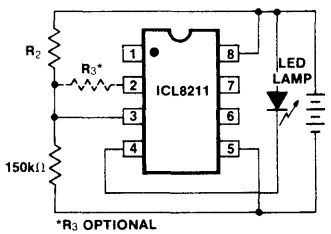


Figure 7: Low Voltage Battery Indicator

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7mA when the lamp is turned on. R_3 will provide hysteresis if required.

b) |Non-Volatile| Low Voltage Detector

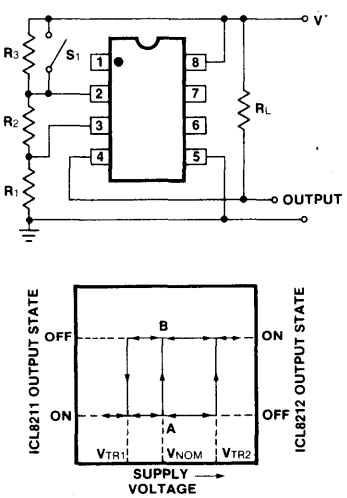


Figure 8: Low Voltage Detector and Memory

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the

supply voltage drops below V_{TR1}, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

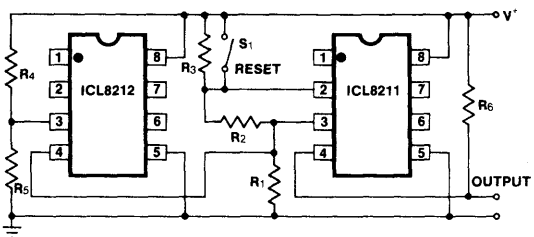


Figure 9: Schematic of Recorder

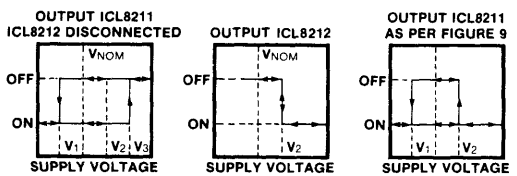


Figure 10: Output States of the ICL8211 and ICL8212 as a Function of the Supply Voltage

Referring to Figure 9, the ICL8212 is used to detect a voltage, V_2, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 - the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the CL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

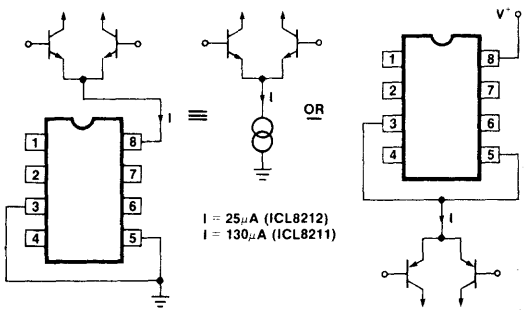


Figure 11: Constant Current Source Applications

e) Zener or Precision Voltage Reference

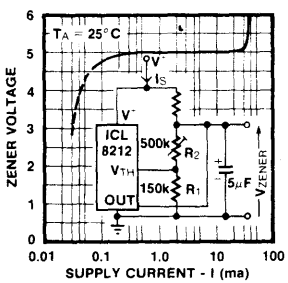


Figure 12: Programmable Zener or Voltage Reference

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

$$(V_{zener} = \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}).$$

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300μA and 25mA will range from 4 to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.

f) Precision Voltage Regulators

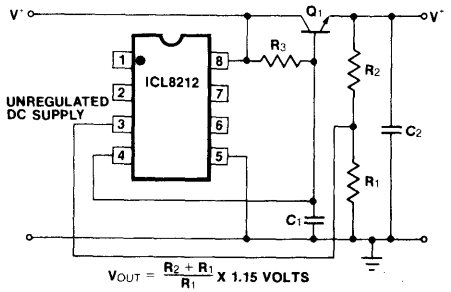


Figure 13: Simple Voltage Regulator

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

f) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

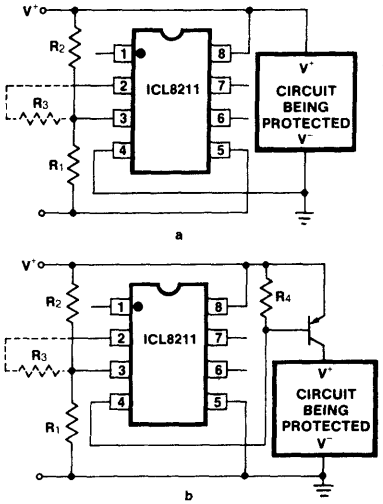


Figure 14: High Voltage Dump Circuits

g) Frequency limit detectors

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/12. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

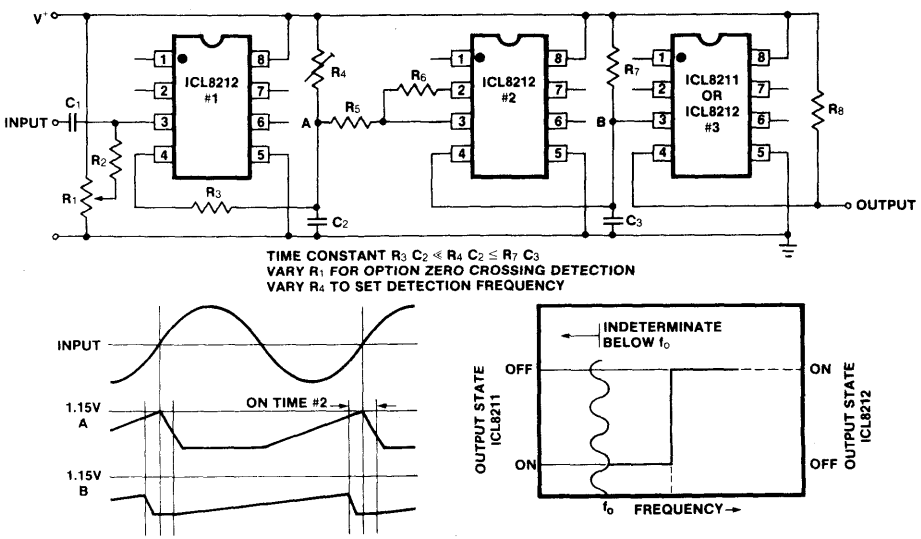


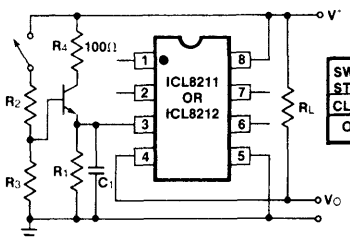
Figure 15: Frequency Limit Detector

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

h) Switch bounce filter

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the elctrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times.

The circuit shown in Figure 16 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of R_1 C_1 to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/12 will be a single transition of state per desired switch closure.



SWITCH STATUS	OUTPUT ICL8211	OUTPUT ICL8212
CLOSED	HI	LO
OPEN	LO	HI

Figure 16: Switch Bounce Filter

j) Low voltage power disconnector

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

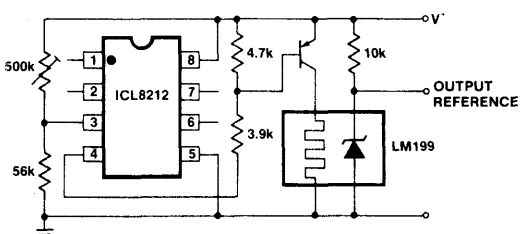


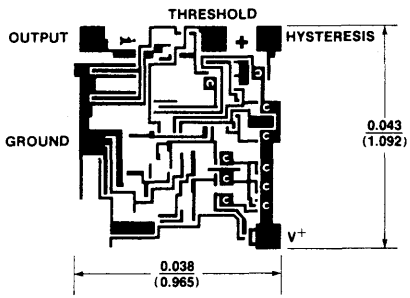
Figure 17: Low Voltage Power Supply Disconnect

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212" by D. Watson.

CUSTOM OPTIONS

The ICL8211/12 have been designed with more on chip components than are used, in anticipation of more dedicated high volume system usage. The trigger voltage and hysteresis resistor network is integrated on chip but not connected. Consult the factory for more information on custom options.

CHIP TOPOGRAPHY



DIE IS PASSIVATED WITH A DEPOSITED OXIDE. BONDING PAD OXIDE WINDOWS ARE 3.6 x 3.6 MILS SQUARE.

5

ICH8500/A
Ultra Low Bias Current Operational Amplifier

FEATURES

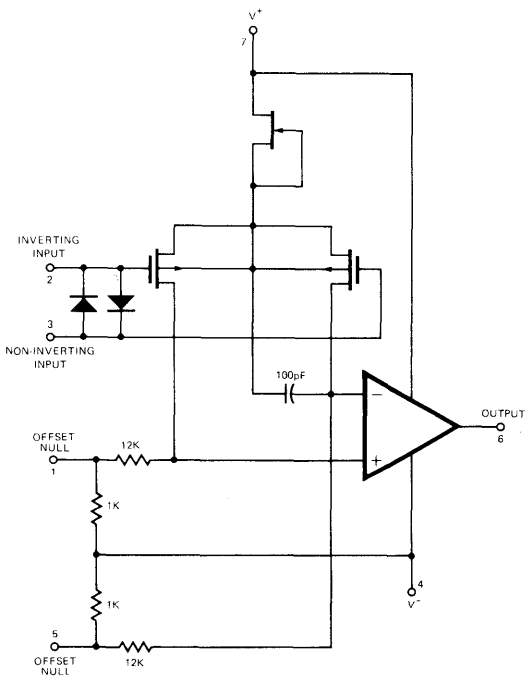
- **Input diode protection**
- **Input bias current less than 0.01 pA at all operating temperatures**
- **No frequency compensation required**
- **Offset voltage null capability**
- **Short circuit protection**
- **Low power consumption**

APPLICATIONS

- **Femto Ammeter**
- **Electrometers**
- **Long time integrators**
- **Flame detectors**
- **pH meter**
- **Proximity detector**
- **Sample and Hold Circuits**

5

SCHEMATIC DIAGRAM



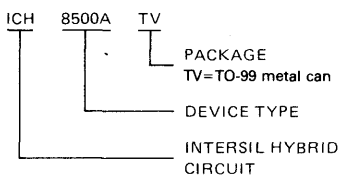
GENERAL DESCRIPTION

The ICM8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

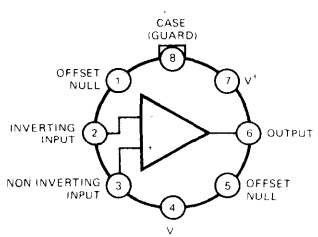
Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20k potentiometer. The input bias current for the inverting and non-inverting inputs is 0.1 pA maximum for the ICH8500, and 0.01 pA maximum for the ICH8500A and are constant over the operating temperature range of -25° C to +85° C.

Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential, the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.

ORDERING INFORMATION



PIN CONFIGURATION (outline dwg TV)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation[1] ..... 500 mW
Differential Voltage ..... ±0.5V
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -25°C to +85°C
Lead Temperature (Soldering 10 sec) ..... 300°C
Output Short Circuit Duration ..... Indefinite

Note: 1. Rating applies for ambient temperature to +70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

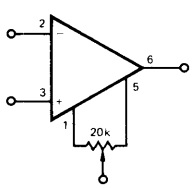
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_{SUPP} = ±15V)

CHARACTERISTICS	SYMBOL	ICH8500			ICH8500A			UNITS	TEST CONDITIONS
		MIN	TYP.	MAX	MIN	TYP	MAX		
Input Leakage Current (Inverting and Non-Inverting)	I_{ILK}			0.1			0.01	pA	Case at same potential as inputs
Input Offset Voltage	V_{OS}			50			50	mV	
Offset Voltage Adjustment Range	$\pm V_{OS}$			±50			±50	mV	20kΩ Potentiometer
Change in Input Offset Voltage Over Temperature	$\Delta V_{OS}/\Delta T$						±5.0 ±5.0	mV mV	+25 to +85°C -25 to +25°C
Common Mode Rejection Ratio	CMRR	60	75		60	75		dB	±5 volts common mode voltage
Output Voltage Swing	$\pm V_O$	±11			±11			V	$R_L \geq 10k\Omega$
Common Mode Voltage Range	CMVR	±10			±10			V	
Large Signal Voltage Gain	A_{VOL}	20,000	10^5		20,000	10^5		—	
Feedback Capacitance	C_{fb}			0.1			0.1	pF	Case guarded
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$			±3.0			±3.0	mV	At 25°C
Slew Rate	SR		0.5			0.5		V/μs	$R_L \geq 2k\Omega$
Input Capacitance	C_{IN}		0.7			0.7		pF	Case guarded
Input Capacitance	C_{IN}		1.5			1.5		pF	Case grounded

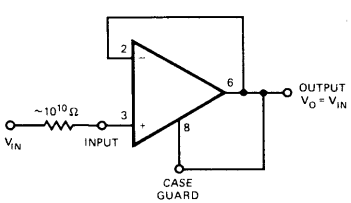
5

CIRCUIT NOTES

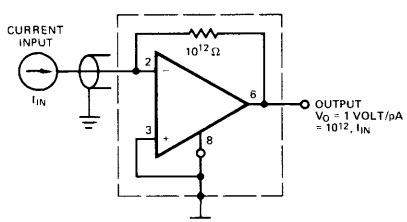
VOLTAGE OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER



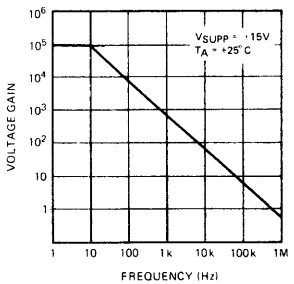
LOW LEVEL CURRENT MEASURING CIRCUIT



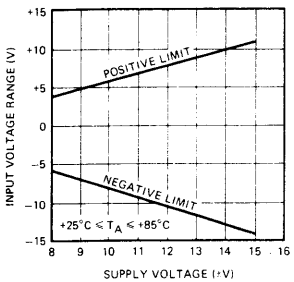
NOTE: Adjust input offset voltage to 0V ± 10μV before measuring leakage.

TYPICAL PERFORMANCE CURVES

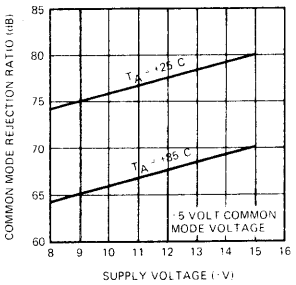
OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



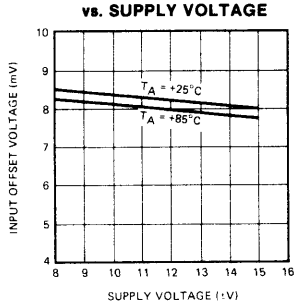
INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



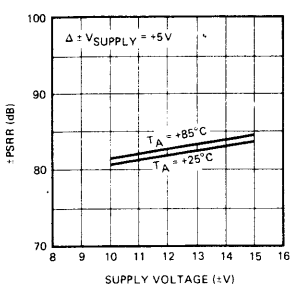
COMMON MODE REJECTION RATIO vs. SUPPLY VOLTAGE



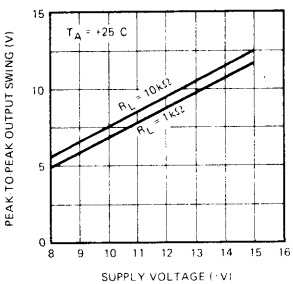
INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



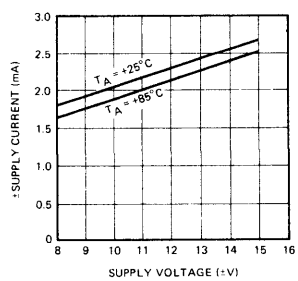
±POWER SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



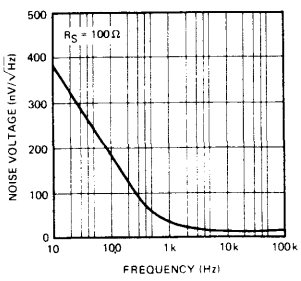
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



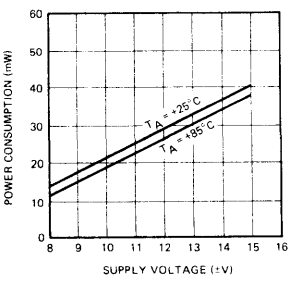
±QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



INPUT REFERRED NOISE VOLTAGE



POWER CONSUMPTION vs. SUPPLY VOLTAGE



APPLICATIONS

The Pico Ammeter

A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 1) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case the potential of the input is at virtual ground, or 0V, therefore, the case of the device is grounded to intercept any stray leakage currents that may otherwise exist between the ±15V input terminals and the inverting input summing junctions. Feedback capacitance* should be kept to a minimum in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance C_{fb} times the feedback resistor R_{fb}. For instance, the time constant of the circuit in Figure 1 is 1 sec if C_{fb} = 1 pF. Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied. C_{fb} of less than 0.2 to 0.3 pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 2.

The internal diodes CR1 and CR2 together with external resistor R1 protect the input stage of the amplifier from voltage transients. The two diodes contribute no error currents, since under normal operating conditions there is no voltage across them.

*Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.

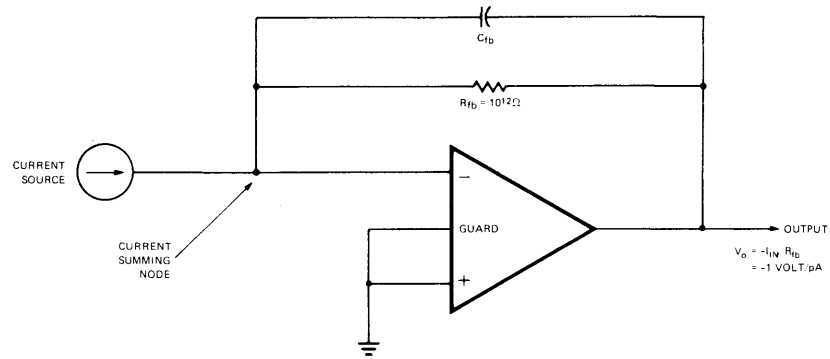


Figure 1. Basic Pico Ammeter Circuit

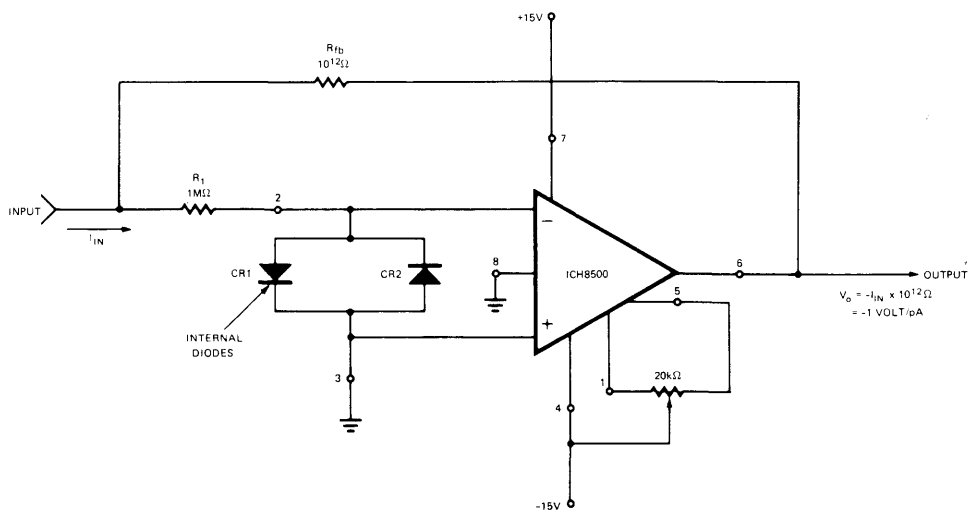


Figure 2. Pico Ammeter Circuit

Sample and Hold Circuit (Figure 3)

The basic principle of this circuit is to rapidly charge a capacitor C_{STO} to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on C_{STO}. Since C_{STO} is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across C_{STO} will remain constant, thus the output of the amplifier will also be constant, however, the voltage across C_{STO} will decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of C_{STO}, leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existant (<0.01 pA). Note that the voltages on the source, drain and gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a quality sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA. The rate of change of the voltage across the 0.01 μF storage capacitor is then 10mV/sec. In contrast, if an operational amplifier which exhibited an input bias current of 1 nA were employed, the rate of change of the voltage across C_{STO} would be 0.1V/sec. An error build up such as this could not be tolerated in most applications.

Wave forms illustrating the operation of the sample and hold circuit are shown in Figure 4.

The Gated Integrator

The circuit in Figure 3 can double as an integrator. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of R1 and C_{STO}. Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of R1 (Up to 10^{12} ohms) can be employed; this permits the use of small values of integrating capacitor (C_{STO}) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 5.

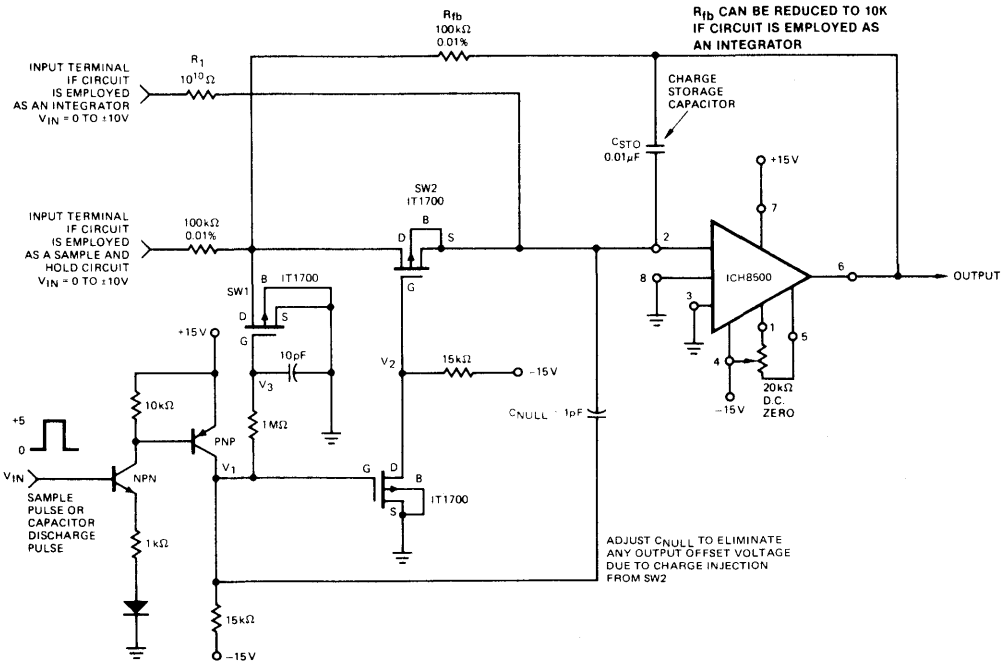


Figure 3. Sample and Hold Circuit or Integrator Circuit

WAVEFORMS

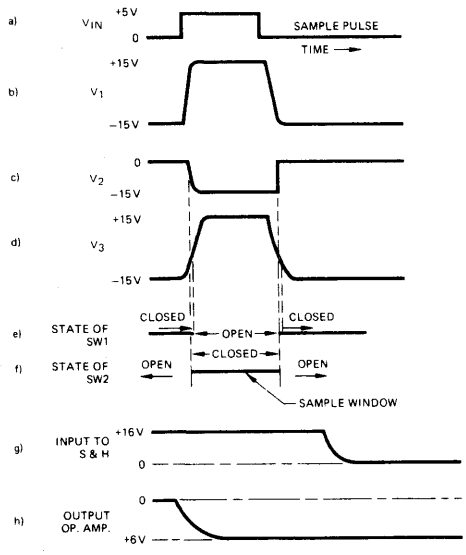


Figure 4. Sample and Hold Circuit Waveforms

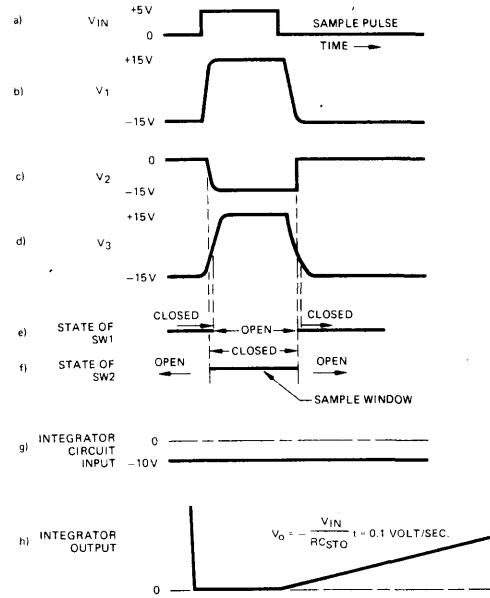


Figure 5. Gated Integrator Waveforms

ICH8510/8520/8530 Power Amplifier/ Motor & Actuator Driver

KEY FEATURES:

- **Delivers up to 2.7 amps @ 24-28V DC (30V supplies)**
- **Protected against inductive kick back with internal power limiting**
- **Programmable current limiting (short circuit protection)**
- **Package is electrically isolated (allowing easy heat sinking)**
- **DC gain > 100dB**
- **20mA typical standy quiescent current**
- **Popular 8 pin TO-3 package**
- **Internal frequency compensation**
- **Can drive up to 0.1 horsepower motors.**

DESCRIPTION:

The ICH8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

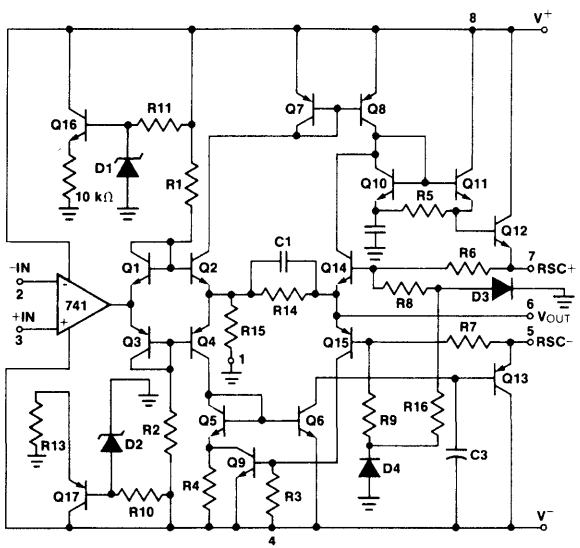
There are three models available for up to +30V power supply operation: 2.7 amps @ 24 volt output levels, 2 amps @ 24V and 1 amp @ 24V. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors. For a device operating at lower voltages, see the ICH8515.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate for optimum heat transfer to the metal package; this substrate provides electrical isolation between amplifiers and metal package.

The I.C. power driver chip has built-in regulators to drive the 741 @ typically ±13V supply voltages.

5

SCHEMATIC DIAGRAM



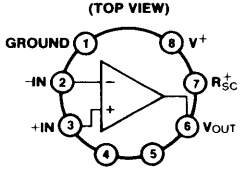
ORDERING INFORMATION

ICH8510 M KA

- Package
  - KA = 8 lead TO-3 can
- Temperature Range
  - M = Military −55°C to +125°C
  - I = Industrial −20°C to +85°C
- Basic Part Number
  - 8510 = 1A output
  - 8520 = 2A output
  - 8530 = 2.7A output

PIN CONFIGURATION (outline dwg KA)

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage ..... ±32V
Power Dissipation, Safe Operating Area ..... See Curves
Differential Input Voltage ..... ±30V
Input Voltage ..... ±15V (Note 1)
Peak Output Current ..... See Curves (Note 2)
Output Short Circuit Duration (to ground) ..... Continuous (Note 2)
Operating Temperature Range M ..... −55°C → +125°C
I ..... −20°C → +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Max Case Temperature ..... 150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPP}$.
Note 2: Ratings apply as long as package dissipation is not exceeded. Device must be mounted on heat sink, see Figures 8 and 12.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS T_A = +25°C. V_{SUPP} = ±30V (unless otherwise stated)

DESCRIPTION	SYMBOL	CONDITIONS	ICH8510I		ICH8510M		ICH8520I		ICH8520M		ICH8530I		ICH8530M		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX	MIN.	MAX.	
Input Offset Voltage Change with Power Dissipation	$\Delta V_{OS}/\Delta Pd$	Mtd. on Wakefield 403 Heat Sink		4		2		4		2		4		2	mV/W
Input Offset Voltage	V_{OS}	$R_S \leq 10\ k\Omega$ $Pd \leq 1W$	−6	+6	−3	+3	−6	+6	−3	+3	−6	+6	−3	+3	mV
Input Bias Current	I_{BIAS}	$R_S \leq 10\ k\Omega$ $Pd \leq 1W$		500		250		500		250		500		250	nA
Input Offset Current	I_{OS}	$R_S \leq 10\ k\Omega$ $Pd \leq 1W$		200		100		200		100		200		100	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 20\Omega$ $V_O = 2/3\ V_{SUPP}$	100		100		100		100		100		100		dB
Input Voltage Range	V_{CMR}		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	V
Common Mode Rejection Ratio	CMRR	$R_S = 10\ k\Omega$	70		70		70		70		70		70		dB
Power Supply Rejection Ratio	PSRR	$R_S = 10\ k\Omega$	77		77		77		77		77		77		dB
Slew Rate	SR	$C_L = 3\ pF$, $A_V = 1$ $R_L = 10\Omega$ $V_O = 2/3\ V_{SUPP}$	0.5		0.5		0.5		0.5		0.5		0.5		V/μs
Output Voltage Swing	V_{OMAX}	$R_L = 20\Omega$ $A_V = 10$	(R_L=30Ω) ±26V		(R_L=30Ω) ±26V		±26V		±26V		±25V		±25V		V
Output Current (3)	I_{MAX}	$R_L = 8\Omega$ $A_V = 10$	1.0		1.0		2.0		2.0		2.7		2.7		A
Power Supply Quiescent Current	I_Q	$R_L = \infty$ $V_{IN} = 0V$		125		100		125		100		125		100	mA

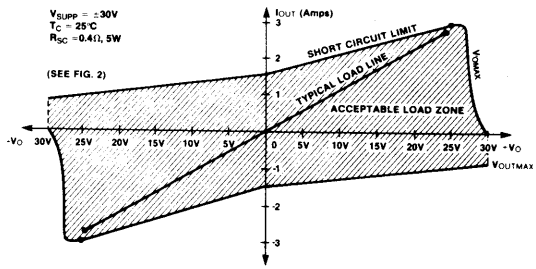
Note 3: See Figure #9 if Power Supplies are less than ±30V.

ELECTRICAL SPECIFICATIONS (continued) T_A = −55°C. to +125°C.(M) or T_A = −20°C. to +85°C.(I)

Input Offset Voltage	V_{OS}	$Pd \leq 1W$	−10	+10	−9	+9	−10	+10	−9	+9	−10	+10	−9	+9	MV
Input Bias Current	I_{BIAS}	$Pd \leq 1W$		1500		750		1500		750		1500		750	nA
Input Offset Current	I_{OS}			500		200		500		200		500		200	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 20\Omega$ $\Delta V_O = 2/3\ V_{SUPP}$	90		90		90		90		90		90		dB
Output Voltage Swing	V_{OMAX}	$R_L = 20\Omega$, $A_V = 10$	±24		±24		±24		±24		±24		±24		V
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Without Heat Sink		40		40		40		40		40		40	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$			2.5		2.5		2.5		2.5		2.5		2.5	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Mtd. on Wakefield 403 Heat Sink		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0	°C/W
Supply Voltage Range	V_{SUPP}		±18	±30	±18	±30	±18	±30	±18	±30	±18	±30	±18	±30	V

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors, R_{SC}^{+} and R_{SC}^{-}. Because of the current power limiting circuitry, the maximum output current is available only when V_O is close to either power supply. As V_O moves away from V_{SUPP}, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.



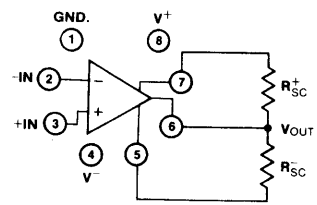


Figure 1: Maximum Output Current for Given R_{SC}

In general, for a given V_O, I_{SC} limit, and case temperature T_C, R_{SC} can be calculated from the equation below for V_O positive, I_{OUT} positive.

$$R_{SC} = \frac{(20.6V_O)^* + 680 - 2.2\,(T_C - 25°C)}{I_{SC(LIMIT)}}$$

*For V_O negative, replace this term with $10.3\,(V_O - 1.2)$

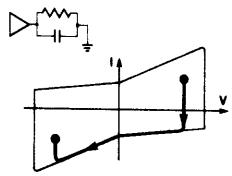
For example, for I_O = 1.5A @ V_O = 25V and T_C = 25°C,

$$R_{SC} = \frac{1195}{1500} = 0.797$$

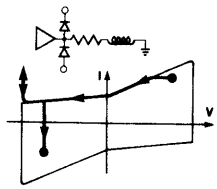
Therefore for this application, R_{SC} = .82Ω (closest standard value)

When 0.82Ω is used, I_{SC} @ V_O = 0V will be reduced to about 1A. Except for small changes in the "$\pm V_{O(max)}$ Limit" area, the effects of changing R_{SC} on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Fig. 1 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This internal power limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 1. Clearly, as V_O decreases, the I_O requirement falls also, more steeply than the I_O available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:



Capacitive Load



Inductive Load
(Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 24-28VDC motor/actuator, the R_{SC} resistors must be calculated to get proper power delivered to the motor (up to a maximum of 2.7A) and V_{SUPP} set at ±30V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 1 and 5.

NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where

T_J = Maximum junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from transistor junction to case of package

$R_{\theta CH}$ = Thermal resistance from case to heat sink

$R_{\theta HA}$ = Thermal resistance from heat sink to ambient air

And since

T_J = 200°C for silicon transistors

$R_{\theta JC} \cong$ 2.0C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate to header

$R_{\theta CH}$ = .045°C/W for 1 mil thickness of Wakefield type 120 thermal joint compound
.09°C/W for 2 mil thickness of type 120
.13°C/W for 3 mil thickness of type 120
.17°C/W for 4 mil thickness for type 120
.21°C/W for 5 mil thickness of type 120
.24°C/W for 6 mil thickness of type 120

$R_{\theta HA}$ = The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $R_{\theta HA} \cong$ 2.0°C/W. Using 4 mil joint compound,

$$P_D = \frac{200°C - T_A}{2.0° + 0.17° + 2.0} = \frac{200°C - T_A}{4.17°C/W}$$

or @ T_A = 25°C,

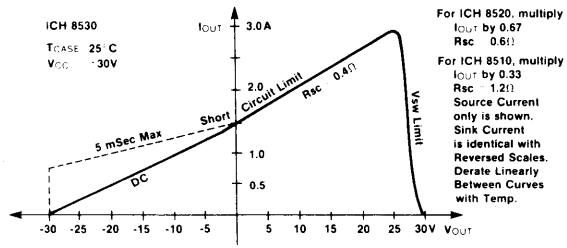
$$\frac{200°C - 25°C}{4.17°C/W} = 42W$$

and @ T_A = 125°C,

$$\frac{200°C - 125°C}{4.17°C/W} = 18W$$

From Fig. 2 the worst case steady state power dissipation for an IH8520 (R_{SC} = 0.62Ω) is about 30W and 18W respectively. Thus this heat sink is adequate.

TYPICAL PERFORMANCE CURVES



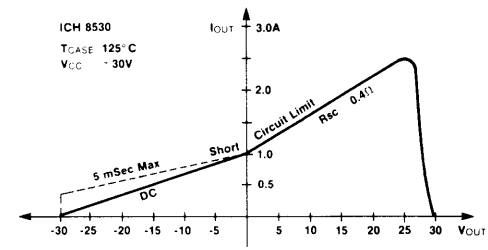
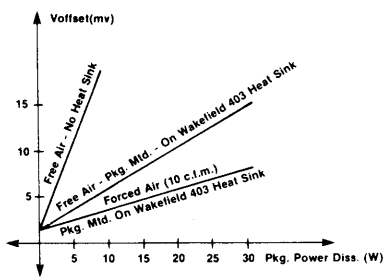


Figure 2: Safe Operating Area; I_{OUT} vs V_{OUT} vs T_C



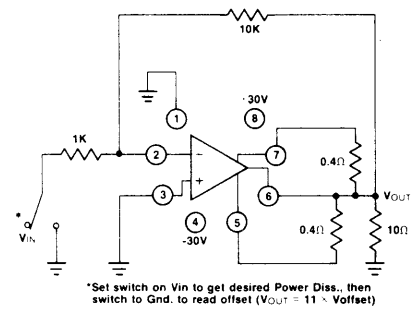
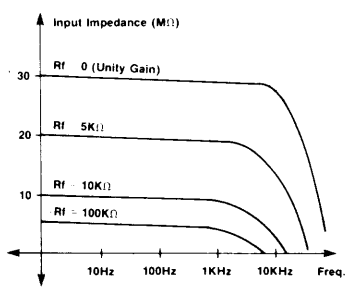


Figure 3: Input Offset Voltage vs Power Dissipation



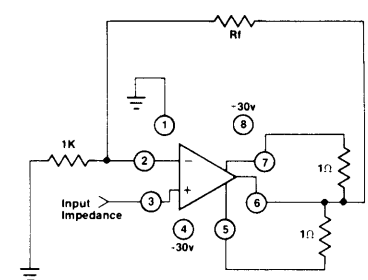
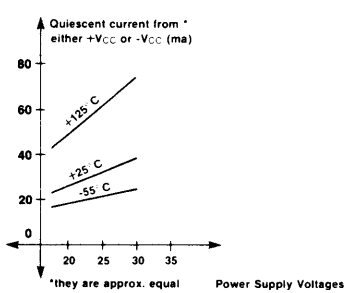


Figure 4: Input Impedance vs Gain vs Frequency



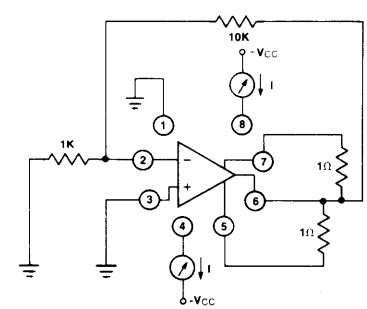


Figure 5: Quiescent Current vs Power Supply Voltage

TYPICAL PERFORMANCE CURVES, CONTINUED.

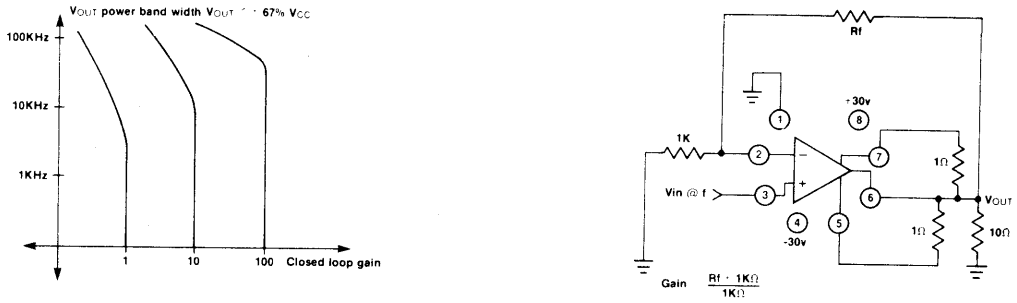


Figure 6: Large Signal Power Band Width

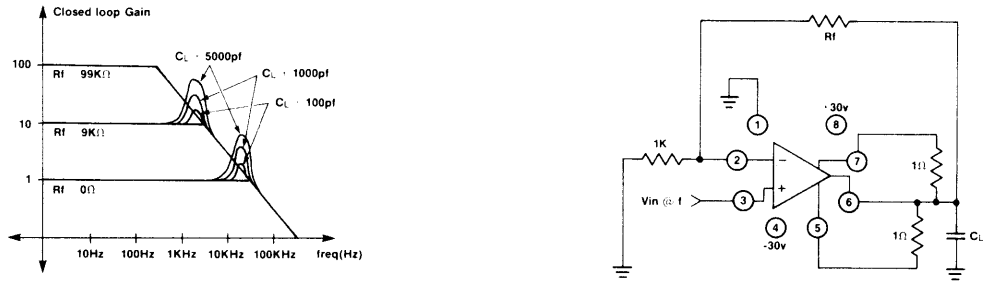


Figure 7: Small Signal Frequency Response

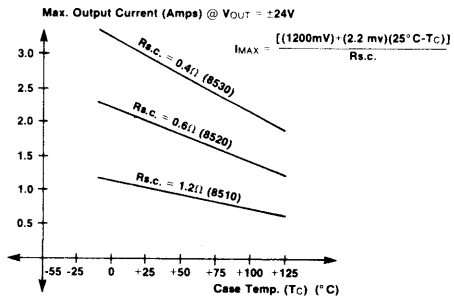


Figure 8: Maximum Output Current vs. Case Temperature

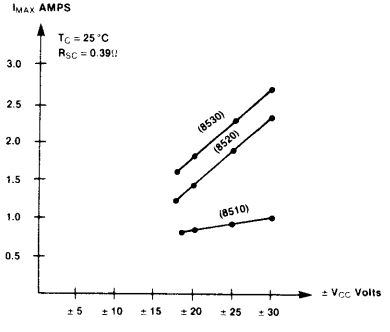


Figure 9: Maximum Output Current vs. V_{SUPP}

BRIEF APPLICATION NOTES

The maximum input voltage range, for $V_{SUPP} < \pm 15V$, is substantially less than the available output voltage swing. Thus non-inverting amplifiers, as in Figure 10, should always be set up with a gain greater than about 2.5, (with ±30V supplies), so that the full output swing is available without hazard to the input. At first sight, it would seem that no restrictions would apply to inverting amplifiers, since the inputs are virtual ground and ground. However, under fault (output short-circuited) or high slew conditions, the input can be substantially removed from ground. Thus for inverting amplifiers with gains less than about 5, some protection should be provided at this input. A suitable resistor from the input to ground will provide protection, but also increases the effect of input offset voltage at the output. A pair of diodes, as shown in Figure 12, has no effect on normal operation, but gives excellent protection.

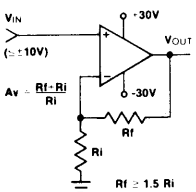


Figure 10: Non-Inverting Amplifier

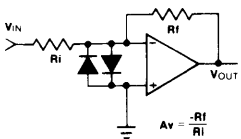


Figure 11: Inverting Amplifier

Power dissipation is another important parameter to consider. The current protection circuit protects the device against short circuits to ground, (but only for transients to the opposite supply) provided the device has adequate heat sink. A curve of power dissipation vs V_O under short circuit conditions is given in Figure 12. The limiting circuit is more closely dependent on case temperature than (output transistor) junction temperatures. Although these operating conditions are unlikely to be attained in actual use, they do represent the limiting case a heat sink must cope with. For fully safe design, the anticipated range of V_O values that could occur, (steady state, including faults) should be examined for the highest power dissipation, and the device provided with a heat sink that will keep the junction temperature below 200° C and the case temperature below 150° C with the worst case ambient temperature expected.

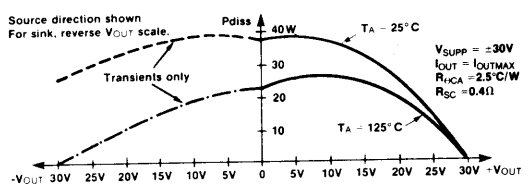


Figure 12: Power Dissipation under Short Circuit Conditions

5

TYPICAL APPLICATIONS

I. Actuator Driving Circuit (24→28 VDC rated)

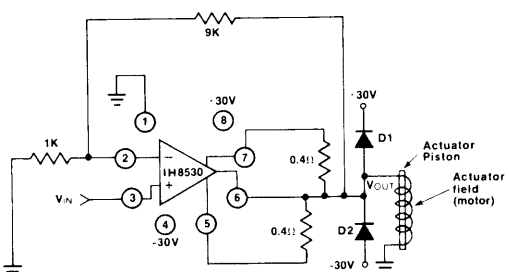


Figure 13: Power Amp Driving Actuator

The gain of the circuit is set to +10, so a V_{IN} = +2.4V will produce a +24V output (and deliver up to 2.7 amps output current). To reverse the piston travel, invert V_{IN} to −2.4V and V_{OUT} will go to −24V. Diodes D1 and D2 absorb the inductive kick of the motor during transients (turn-on or turn-off); their breakdown should exceed 60V.

II. Obtaining Up To 5 Amps Output Current Capability By Paralleling Amplifiers

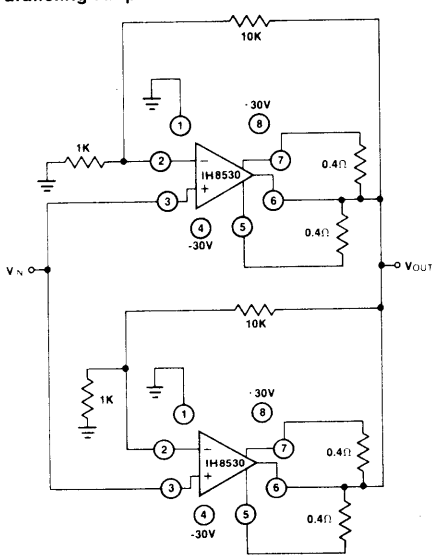


Figure 14: Paralleling Power Amps for Increased Current Capability

This paralleling procedure can be repeated to get any desired output current. However, care must be taken to provide sufficient load to avoid the amplifiers pulling against each other.

III. Driving A 48VDC Motor

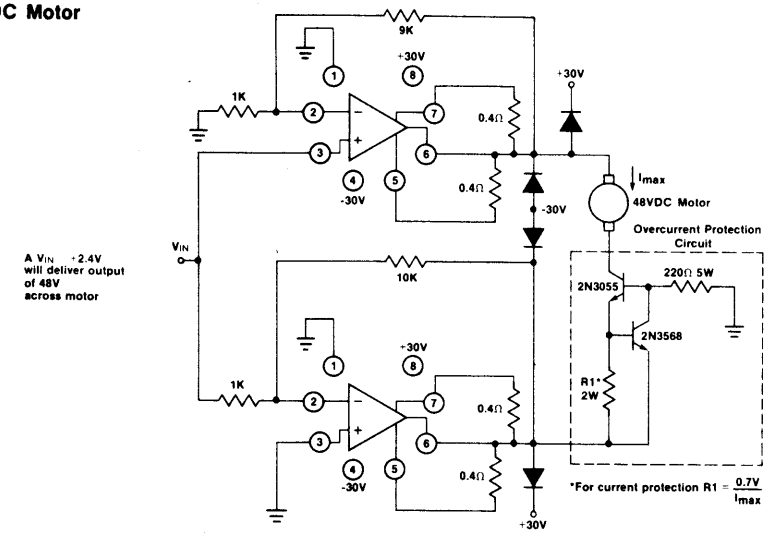


Figure 15: Power Amp Driving 48 VDC Motor

IV. Precise Rate Control of an Electronic Valve

There are two methods to get very fine control of the opening of an orifice driven by an electronic valve.

1. Keep the voltage constant, i.e., 24VDC or 12VDC, and vary the time the voltage is applied, i.e., if it takes five seconds to completely open an orifice at 24VDC, then applying 24V for only 2½ seconds opens it only 50%.
2. Simply vary the DC driving voltage to valve. Most valves obtain full opening as an inverse of applied voltage, i.e., valves open 100% in five seconds at 24VDC and in 10 seconds at 12VDC.

A circuit to perform the second method is shown below; the advantage of this is that digit switches can precisely set driving voltage to 0.2% accuracy (8-bit DAC), thereby controlling the rate at which the valve opens.

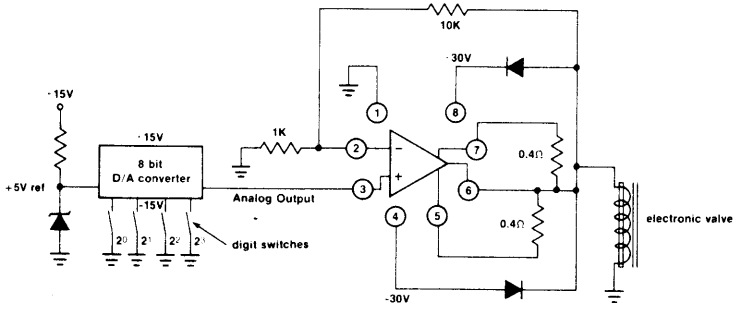
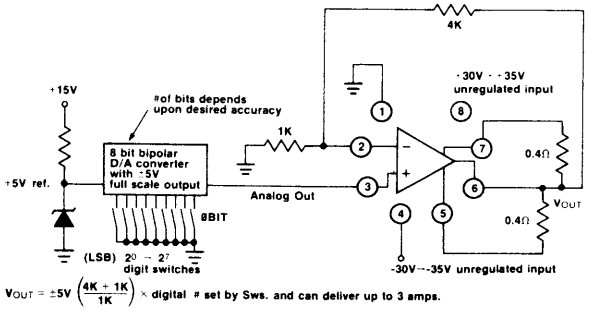


Figure 16: Digitally Controlled Electronic Value

V. The circuit presented in Fig. 16 is also an excellent way to get a precise power supply voltage; in fact, it is possible to build a precision variable power supply using a BCD coded DAC with BCD Thumbwheel switches.



2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	Ø BIT	Vout
1	1	1	1	1	1	1	1	1	+25VDC
1	1	1	1	1	1	1	1	0	−25VDC
0	1	0	1	1	0	0	1	1	+15VDC
0	1	0	1	1	0	0	1	0	−15VDC
1	0	0	0	0	0	0	0	1	+0.098VDC
1	0	0	0	0	0	0	0	0	-0.098VDC

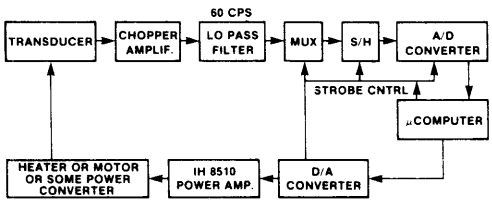
Etc.

Figure 17: Digitally Programmable Power Supply

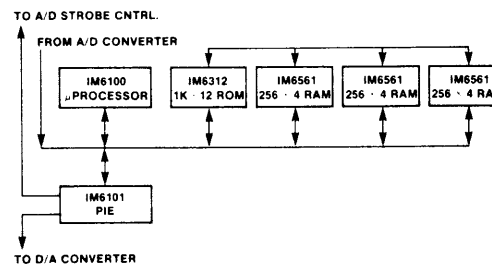
The power supply can be set to ±0.1VDC.

VI. There is great power available in the sub-systems shown in IV and V; there the D/A converter is shown being set manually (via digit switches) to get a precise analog output (binary # × full scale voltage), then the driver amplifier multiplies this voltage to produce the final output voltage. It seems obvious that the next logical step is to let a micro-processor (local) or C.P.U. program the D/A converter. Then total, pre-programmable, electronic control of an actuator, electronic valve, motor, etc., is obtained. This would be used in conjunction with a transducer/multiplex system for electronic monitoring and control of any electro-mechanical function.

ELECTRONIC CONTROL SYSTEM:



MUX = INTERSIL IH5060 (1/16) or IH5070 (2/16)
S/H (SAMPLE & HOLD) = INTERSIL IH5111
D/A CONVERTER = INTERSIL 7520 or INTERSIL 7105
POWER AMP = IH8510 (1 AMP) or IH8520 (2 AMP) or IH8530 (2.7 AMP)
A/D CONVERTER = ICL8052/7103 or ICL8052/7104
μ COMPUTER = IM6100 family:



HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a $R_{\theta HA}$ = 1.3°C/watt. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

NOTE: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

APPLICATION NOTES

For Futher Applications Assistance, See:

A021 "Power D/A Converters Using The ICH8510/20/30," by Dick Wilenken
A026 "DC Servo Motor Systems Using The ICH8510/20/30," by Ken McAllister
A029 "Power Op Amp Heat Sink Kit," by Skip Osgood

ICH8515
Power Amplifier
Motor & Actuator Driver

KEY FEATURES:

- **Delivers up to 1.5 amps @ +12VDC (±15VDC supplies)**
- **Protected against inductive kick back by internal power limiting**
- **Programmable current limiting (short circuit protection)**
- **Package is electrically isolated (allowing easy heat sinking)**
- **DC gain > 100dB**
- **Popular 8 pin TO-3 package**
- **Internal frequency compensation**
- **Can drive up to 0.033 horsepower motors**
- **Pin equivalent to ICH8510/20/30 family**

DESCRIPTION:

The ICH8515 is a hybrid power amplifier specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

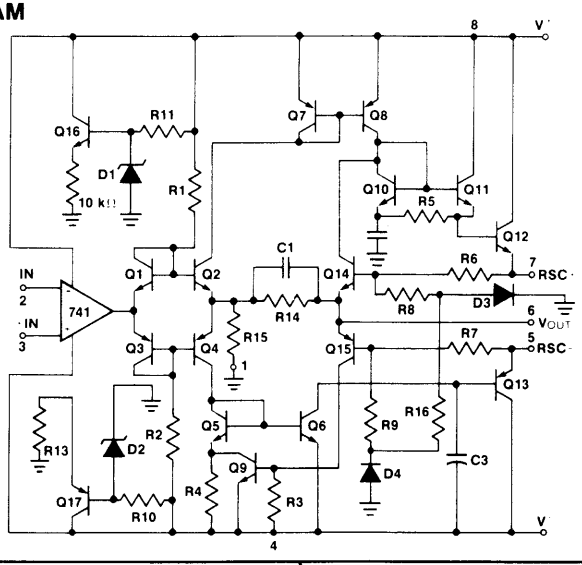
The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and an internal frequency compensating capacitor. The chips are mounted on a beryllium oxide substrate, for optimum heat transfer to the metal package; this substrate provides electrical isolation between the amplifier and the metal package.

The 8515 has special SOA (safe operating area) circuitry which allows it to withstand a direct short to ground or to either supply indefinitely. It has been designed to operate with ±12 or ±15VDC supplies and will deliver typically 1.5 to 1.8A @ 13V out using +15V supplies.

Internal frequency compensation provides stability down to unity gain (either inverting or noninverting) even when using inductive loads.

5

SCHEMATIC DIAGRAM

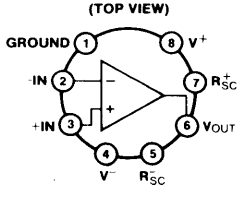


ORDERING INFORMATION

DEVICE	TEMPERATURE	OUTPUT
ICH8515MKA	−55°C to +125°C	1.5A
ICH8515IKA	−20°C to +85°C	1.25A

PIN CONFIGURATION (OUTLINE DWG. KA)

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage ..... ±18V
Power Dissipation, Safe Operating Area ..... See Curves
Differential Input Voltage ..... ±30V
Input Voltage ..... ±15V (Note 1)
Peak Output Current ..... See Curves (Note 2)
Output Short Circuit Duration (to ground) ..... Continuous (Note 2)
Operating Temperature Range M ..... −55°C → +125°C
I ..... −20°C → +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Max Case Temperature ..... 150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPP}$.
Note 2: Rating applies as long as package dissipation is not exceeded for heat sink attached.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS T_A = +25°C, V_{SUPP} = ±15V (unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	ICH8515I			ICH8515M			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage Change with Power Dissipation	$\Delta V_{OS}/\Delta Pd$	Mtd. on Wakefield 403 Heat Sink			4			2	mV/W
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$, Pd < 1W	−6	1	6	−3	0.7	3	mV
Input Bias Current	I_{BIAS}	$R_S \leq 10k\Omega$, Pd < 1W			500			250	nA
Input Offset Current	I_{OS}	$R_S \leq 10k\Omega$, Pd < 1W			200			100	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 10\Omega$, $V_O > 2/3\ V_{SUPP}$	100			100			dB
Input Voltage Range	V_{CMR}		−10		+10	−10		+10	V
Common Mode Rejection Ratio	CMRR	$R_S = 10k\Omega$	70			70			dB
Power Supply Rejection Ratio	PSRR	$R_S = 10k\Omega$	77			77			dB
Slew Rate	SR	C_L = 30pF, A_V = 1, $R_L = 10\Omega$ $V_O \geq 2/3\ V_{SUPP}$	0.5			0.5			V/μs
Output Voltage Swing	V_{OMAX}	$R_L = 10\Omega$, A_V = 10	±12			±12			V
Output Current	I_{MAX}	$R_L = 5\Omega$, A_V = 10	±1.25	1.4		±1.5	1.8		A
Power Supply Quiescent Current	I_Q	$R_L = \infty$, V_{IN} = 0V		80	125		70	100	mA

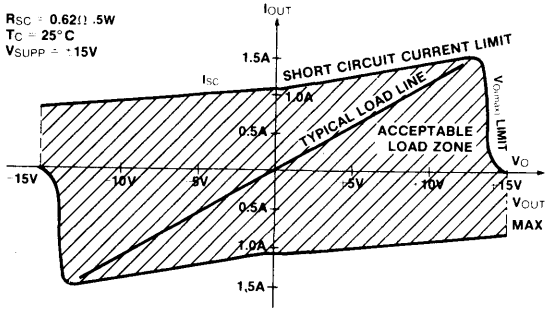
OPERATING CHARACTERISTICS (continued) T_A = −55°C. to +125°C (M) or T_A = −20°C. to +85°C. (I)

Input Offset Voltage	V_{OS}	Pd<1W	−10		+10	−9		+9	mV
Input Bias Current	I_{BIAS}	Pd<1W			1500			750	nA
Input Offset Current	I_{OS}				500			200	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 10\Omega$, $\Delta V_O = 2/3\ V_{SUPP}$	90			90			dB
Output Voltage Swing	V_{OMAX}	$R_L = 10\Omega$, A_V = 10	±10			±10			V
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Without Heat Sink			40			40	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$				3.0			3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Mtd. on Wakefield 403 Heat Sink		4.5			4.5		°C/W
Supply Voltage Range	V_{SUPP}		±11		±17	±11		±17	V

5

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors. R_{SC}^{+} and R_{SC}^{-}. Because of the internal power limiting circuitry, the maximum output current is available only when V_O is close to either power supply. As V_O moves away from V_{SUPP}, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.



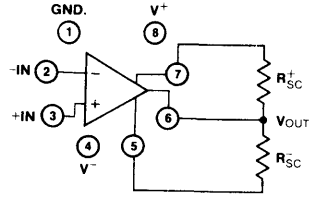


Figure 1: Maximum Output Current for Given R_{SC}

In general, for a given V_O, I_{SC} limit, and case temperature T_C, R_{SC} can be calculated from the equation below for V_O positive, I_{OUT} positive.

$$R_{SC} = \frac{(20.6V_O)^* + 680 - 2.2(T_C - 25°C)}{I_{SC\ (limit)}\ \text{in mA}}$$

*For V_O negative, replace this term with 10.3 (V_O−1.2)

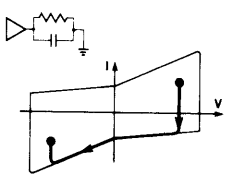
For example, for I_O = 1.5A @ V_O = 12V and T_C = 25°C,

$$R_{SC} = \frac{(20.6)(12) + 680}{1500} = \frac{927.2}{1500} = .618$$

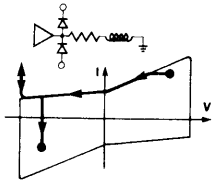
Therefore for this application, R_{SC} = .62Ω (closest standard value)

When 0.62Ω is used, I_{SC} @ V_O = 0V will be reduced to about 1A. Except for small changes in the "$\pm V_{O(max)}$ Limit" area, the effects of changing R_{SC} on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Fig. 1 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This internal power limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 1. Clearly, as V_O decreases, the I_O requirement falls also, more steeply than the I_O available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:



Capacitive Load



Inductive Load
(Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 12VDC motor/actuator, the R_{SC} resistors must be calculated to get proper power delivered to the motor (up to a maximum of 1.5 amps) and V_{SUPP} set at ±15V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 1 and 9.

NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where

T_J = Maximum junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from transistor junction to case of package

$R_{\theta CH}$ = Thermal resistance from case to heat sink

$R_{\theta HA}$ = Thermal resistance from heat sink to ambient air

And since

T_J = 150°C for silicon transistors

$R_{\theta JC} \cong$ 2.0C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate to header

$R_{\theta CH}$ = .045° C/W for 1 mil thickness of Wakefield type 120 thermal joint compound
.09° C/W for 2 mil thickness of type 120
.13° C/W for 3 mil thickness of type 120
.17° C/W for 4 mil thickness for type 120
.21° C/W for 5 mil thickness of type 120
.24° C/W for 6 mil thickness of type 120

$R_{\theta HA}$ = The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $R_{\theta HA} \cong$ 2.0°C/W. Using 4 mil joint compound,

$$P_D = \frac{150°C - T_A}{2.0° + 0.17° + 2.0} = \frac{150°C - T_A}{4.17°C/W}$$

or @ T_A = 25°C,

$$\frac{150°C - 25°C}{4.17°C/W} = 30W$$

and @ T_A = 125°C,

$$\frac{150°C - 125°C}{4.17°C/W} = 6W$$

From Fig. 2 the worst case steady state power dissipation for the IH8515 (R_{SC} = 0.62Ω) is about 15W and 11W respectively. Thus this heat sink is adequate.

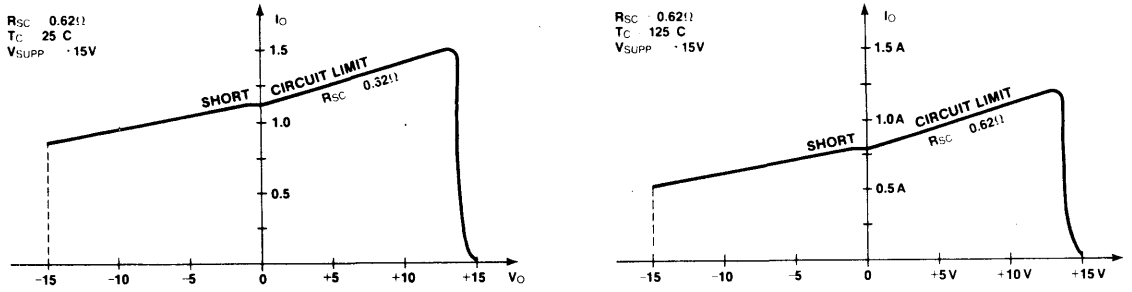
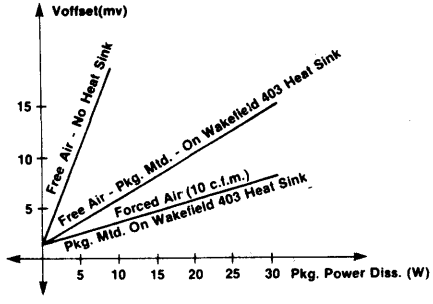


Figure 2: I_{OUT} vs. V_{OUT}

TYPICAL PERFORMANCE CURVES



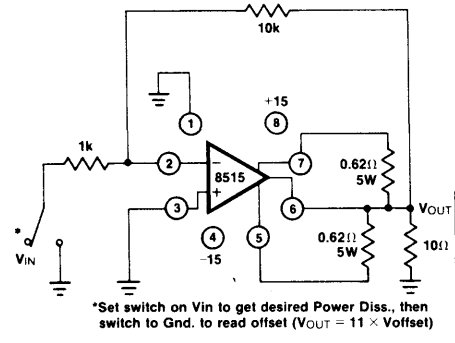
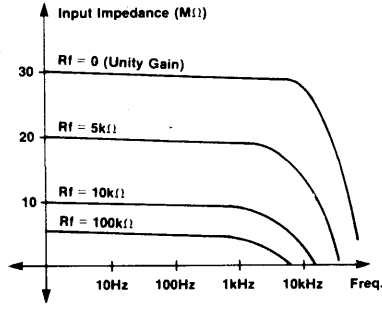


Figure 3: Input Offset Voltage vs Power Dissipation



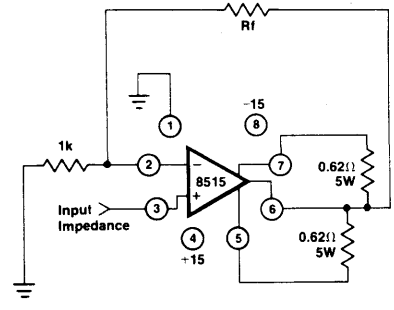
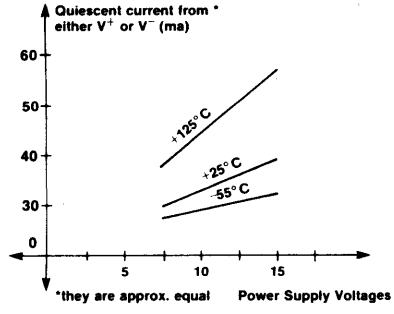


Figure 4: Input Impedance vs Gain vs Frequency



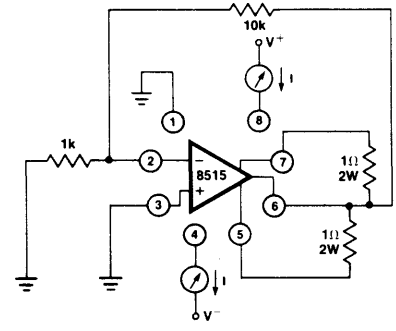
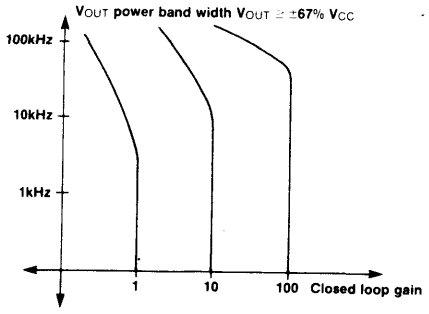


Figure 5: Quiescent Current vs Power Supply Voltage



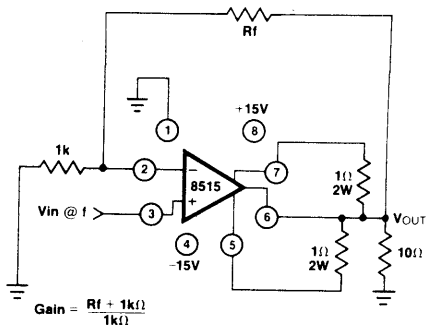
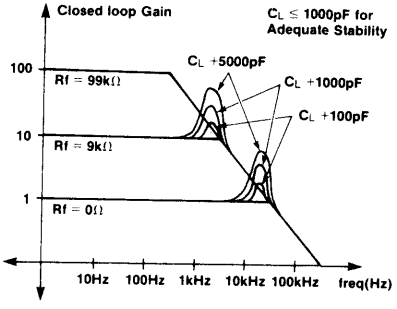


Figure 6: Large Signal Power Band Width



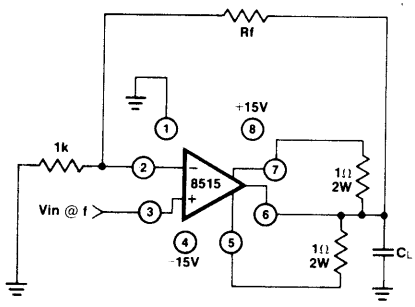


Figure 7: Small Signal Frequency Response

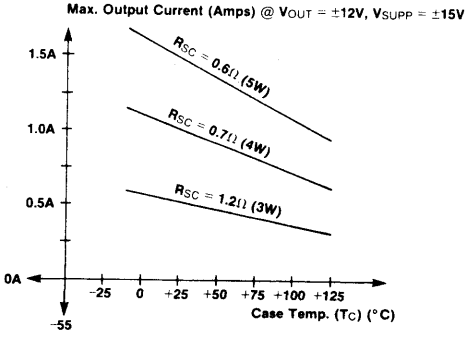


Figure 8: Maximum Output Current vs. Case Temperature

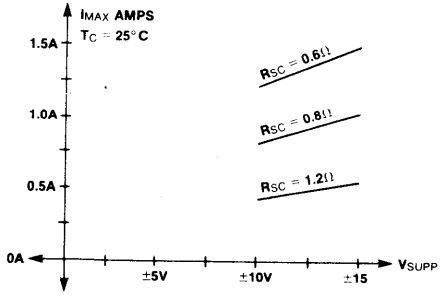
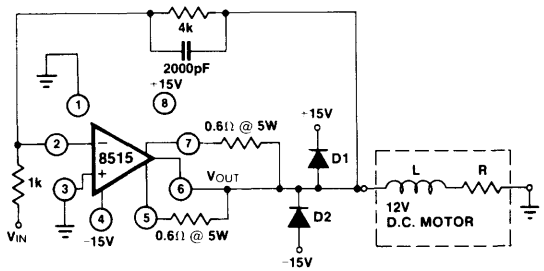


Figure 9: Maximum Output Current vs. V_{SUPP}

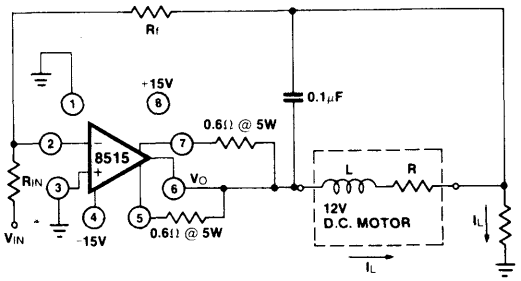
TYPICAL APPLICATIONS

I. CONSTANT VOLTAGE DRIVE FOR D.C. MOTORS

Here $V_{OUT}/V_{IN} = 4$, and if $V_{IN} = -3V$, $V_{OUT} = +12V$, and vice versa for $V_{IN} = +3V$. Diodes D1, D2 should be 1N4001 types; these absorb the inductive kickbacks of the motor. The 2000pF Miller capacitor is used to prevent system oscillation, by providing gain rolloff @ approx. 20kHz (−3dB).



II. CONSTANT CURRENT DRIVE FOR D.C. MOTORS



$$\frac{I_L}{V_{IN}} = -\frac{R_f}{R_{IN}} \bullet \frac{1}{R_L}$$, assuming $R_f >> R_L$.

This circuit allows precisely set motor drive current with op. amp. feedback accuracy. If $R_{IN} = R_F = 1k\Omega$, and $R_L = 10\Omega$, then $\frac{I_L}{V_{IN}} = -0.1$ Amps/Volt, and if $R_L = 1\Omega$ (use 4W or more) and $R_F = R_{IN} = 1k\Omega$, $\frac{I_L}{V_{IN}} = -1 \times 1 = \frac{1\ Amp}{Volt}$. Thus if $V_{IN} = 1.5V$, 1.5 amps will flow thru the motor. Since one side of the motor will have a 1.5V drop (with respect to GND), the V_O point will go to 13.5V and develop 12V across motor.

HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a $R_{\theta HA} = 1.3°C/watt$. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

NOTE: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

Timers, Counters, and Display Drivers

Timers

	Page
ICM7240/50/60	6-116
ICM7242	6-127
ICM7555	6-155
ICM7556	6-155

Counters

ICM7208	6-7
ICM7216	6-24
ICM7217/27	6-39
ICM7224/25	6-64
ICM7226	6-72
ICM7236	6-110

Counter Timebase

ICM7207/A	6-3

Display Drivers

ICM7211/12	6-14
ICM7218	6-55
ICM7231-34	6-84
ICM7235	6-104
ICM7243	6-133
ICM7281	6-143

Counters, Timers and Display Drivers

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7207 ICM7207A	Frequency counter timebase.	14-Pin DIP 14-Pin DIP	6.5536 MHz 5.2488 MHz	0.01, 0.1, or 1-second count window plus store, reset and MUX.
ICM7208	7-digit unit counter. With addition of 7207 the circuit becomes a complete timer-frequency counter.	28-Pin DIP	—	LED display drive
ICM7211 ICM7212	Four-digit display decoder drivers; ICM7211 is LCD; ICM7212 is LED; Non-multiplexed for low noise. BCD input, decoded display drive output.	40-Pin DIP (plastic)	—	Four-digit, seven-segment direct display drive; LED or LCD
ICM7216 ICM7226	Eight-digit universal counter measures frequency, period, frequency ratio, time interval, units; on-board time base.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	1 or 10 MHz	Eight-digit-common anode or common cathode direct LED drive; BCD output
ICM7217 ICM7227	Four-digit CMOS up/down counter; presettable start/count and compare register; for hard-wired or microprocessor control applications; cascadable.	28-Pin Cerdip or plastic	—	Four-digit, seven-segment common anode or common cathode direct LED display drive; equal, zero, carry/borrow
ICM7218A/D ICM7218E	LED display driver system with 8x8 memory; numeric or dot (1 of 64) decoding; microprocessor compatible.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	—	Eight-digit, seven-segment plus decimal point, common cathode or common anode
ICM7224 ICM7225	4½-digit high speed counter/decoder/driver; 25 MHz typ; ICM7224 is LCD; ICM7225 is LED; direct display drive; cascadable.	40-Pin DIP (plastic)	—	4½-digit seven-segment direct display driver; LED or LCD
ICM7231	8-digit CMOS multiplexed LCD driver. Parallel input.	40-Pin DIP (plastic)	—	Eight-digit, seven-segment plus two flags per digit
ICM7232	10½-digit CMOS multiplexed LCD driver. Serial input.	40-Pin DIP (plastic)	—	10½-digit, seven-segment plus two flags per digit
ICM7233	4-character CMOS multiplexed LCD driver. Parallel alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Four-character, 16-segment plus colon
ICM7234	5-character CMOS multiplexed LCD driver. Serial alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Five-character, 16-segment plus colon
ICM7235/A	4-digit CMOS decoder/driver for direct drive vacuum fluorescent displays. BCD input.	40-Pin DIP (plastic)	—	Four-digit, seven-segment, vacuum fluorescent display drive, either HEX or CODE B
ICM7235M/AM	Same as above but microprocessor compatible.			
ICM7236	4½-digit high speed CMOS counter/decoder/driver for vacuum fluorescent displays; 25 MHz typ counting speed.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7236A	Same as above but counting to 15959.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7240 ICM7250 ICM7260	Programmable CMOS counter/timers using external RC time base. Programmable from μs to years.	16-Pin DIP	External	Timed output
ICM7242	Fixed CMOS counter/timer. Uses external RC time base; sequence timing from μs to minutes.	8-Pin DIP	External	Timed output
ICM7243	8-character multiplexed LED display driver with alphanumeric (6-bit ASCII) input.	40-Pin Cerdip	—	Eight-character, 14/16-segment common cathode alphanumeric LED display drive
ICM7281	LCD Dot Matrix Column Driver	40-Pin DIP	—	Up to 256 x 256 dots
ICM7555 ICM7556	Single or dual CMOS version of industry-standard 555 timer; 80 μA typ. supply current; 500 kHz guaranteed; 2-18V power supply.	8-Pin DIP 14-Pin DIP	—	

ICM7207/A CMOS Oscillator Controller

FEATURES

- **Stable HF oscillator**
- **Low power dissipation ≤ 5mW with 5 volt supply**
- **Counter chain has outputs at ÷ 2^{12} and ÷ 2^n or ÷ (2^n x 10); n = 17 for 7207, and 20 for 7207A**
- **Low impedance output drivers ≤100 ohms**
- **Count windows of 10/100ms (7207 with 6.5536MHz crystal) or 0.1/1 sec. (7207A with 5.24288MHz crystal)**

APPLICATIONS

- **System timebases**
- **Oscilloscope calibration generators**
- **Marker generator strobes**
- **Frequency counter controllers**

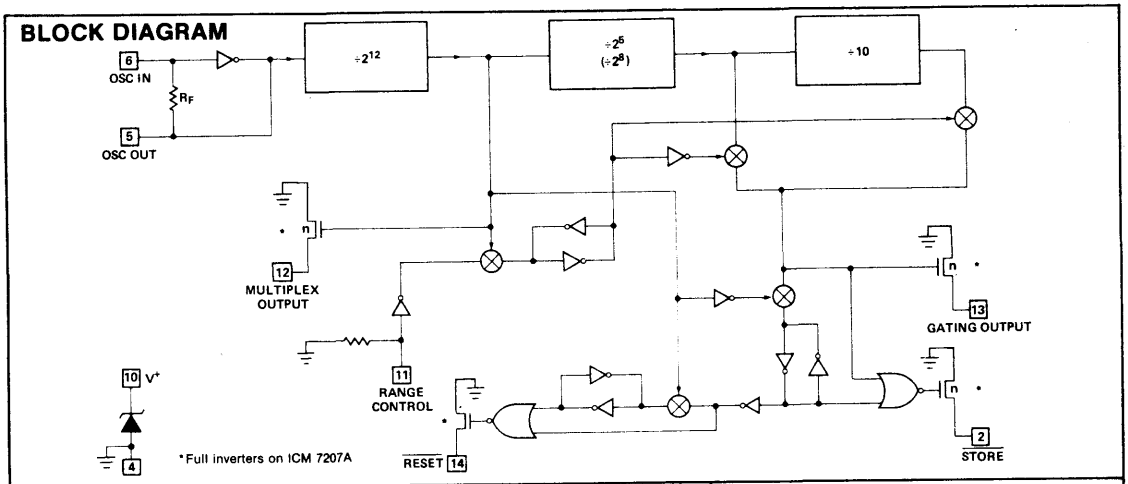
DESCRIPTION

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts at which the typical dissipation is less than 2mW using an oscillator frequency of 6.5536MHz (5.24288MHz).

In the 7207/A the GATING output, $\overline{\text{RESET}}$, and the MULTIPLEX output provide both pull up and pull down, eliminating the need for 3 external resistors; although, buffering must be provided if interfacing with T^2L is required.

BLOCK DIAGRAM



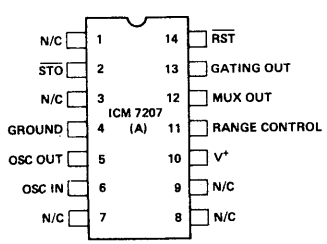
ORDERING INFORMATION

PART	PACKAGE	ORDER NUMBER
ICM7207	14-Pin DIP	ICM7207IPD
	DICE	ICM7207/D
	EV/Kit*	ICM7207EV/Kit
ICM7207A	14-Pin DIP	ICM7207AIPD
	DICE	ICM7207A/D
	EV/Kit*	ICM7207AEV/Kit

Temperature Range on packaged parts is −20°C to +85°C

*These EV/Kits contain just the IC and the corresponding crystal. The ICM7207A is also used in the 4½-Digit Counter/Driver kits, the ICM7224 EV/Kit, ICM7225 EV/Kit, and ICM7236 EV/Kit, which include several ICs, a crystal, PC board, and some passive components.

PIN CONFIGURATION



(outline dwg PD)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.0V
Input Voltages ..... Equal to or less than supply voltage
Output Voltages (7207) .... Not more positive than +6V with respect to GROUND
(7207A) ..... V^+ to V^-
Output Currents 25mA
Power Dissipation @ 25°C Note 1 ..... 200mW
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

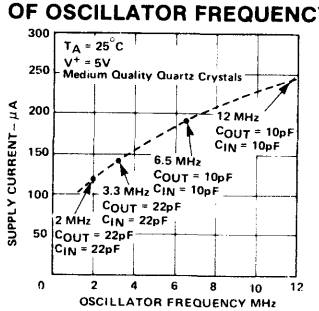
TEST CONDITIONS: f_{OSC} = 6.5536MHz(7207), 5.24288MHz(7207A), V^+ = 5V, T_A = 25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V^+	-20°C to +85°C	4		5.5	V
Supply Current	I^+	All outputs open circuit		260	1000	μA
Output on Resistances	$r_{ds(on)}$	Output current = 5mA All outputs		50	120	Ω
Output Leakage Currents	I_{OLK}	All outputs (STORE only)			50	μA
(Output Resistance Terminals 12,13,14)	(R_{OUT})	Output current = 50μA, 7207A only			33K	Ω
Input Pulldown Current	I_{pd}	Terminal 11 connected to V^+		50	200	μA
Input Noise Immunity			25			% supply voltage
Oscillator Frequency Range	f_{OSC}	Note 2	2		10	MHz
Oscillator Stability	f_{STAB}	C_{IN} = C_{OUT} = 22pF		0.2	1.0	ppm/V
Oscillator Feedback Resistance	r_{OSC}	Quartz crystal open circuit Note 3	3			MΩ

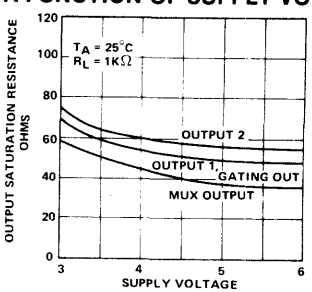
NOTE 2: Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.

NOTE 3: The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

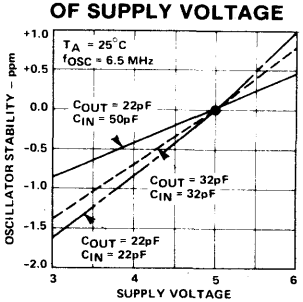
SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



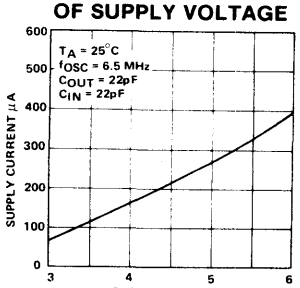
OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

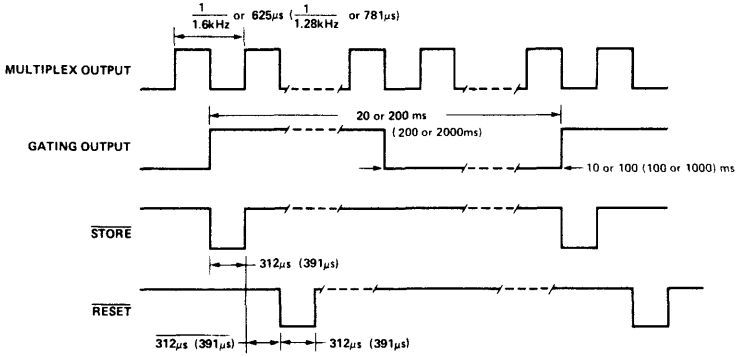


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



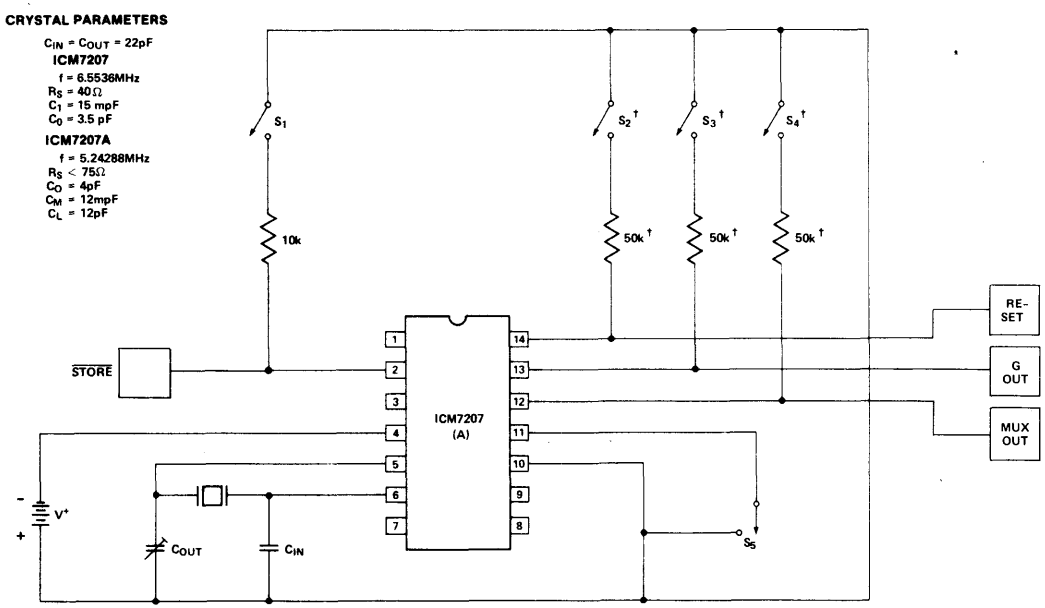
OUTPUT TIMING WAVEFORMS 7207 (7207A)

Crystal Frequency = 6.5536 (5.24288) MHz



Referring to the test circuit, the crystal oscillator frequency is divided by 2^{12} to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to V^+ or GROUND (open circuit).

TEST CIRCUIT



SWITCHES S_1, S_2, S_3, S_4 OPEN CIRCUIT FOR SUPPLY CURRENT MEASUREMENT.
SWITCH S_5 OPEN CIRCUIT FOR SLOW GATING PERIOD.

† SWITCHES S_2, S_3, S_4 and 50k RESISTORS ARE NOT NEEDED WHEN USING THE ICM7207A.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

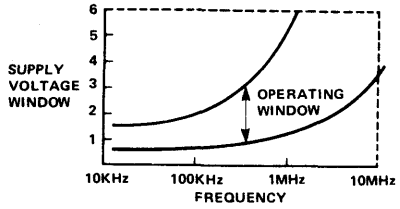
It is recommended that the crystal load capacitance (C_L) be no greater than 15pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10 ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05 ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.



For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet.

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet, and app note A015. Other frequency counters using the ICM7207/A can be constructed using the ICM7224, ICM7225, and ICM7236, for LCD, LED and VF displays. The latter are available as EV/Kits also.

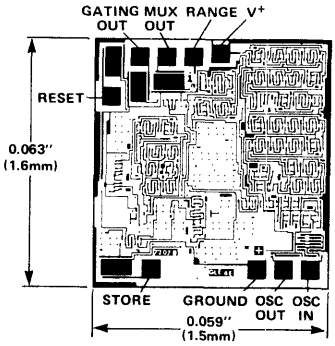
The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

QUARTZ CRYSTAL MANUFACTURERS

The following list of possible suppliers is intended to be of assistance in putting a design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Intersil.

a) CTS Knights, Sandwich, Illinois, (815) 786-8411
b) Motorola Inc., Franklin Park, Illinois (312) 451-1000
c) Sentry Manufacturing Co., Chickasaw, Oklahoma (405) 224-6780
d) Tyco Filters Division, Phoenix, Arizona (602) 272-7945
e) M-Tron Inds., Yankton, South Dakota (605) 665-9321
f) Saronix, Palo Alto, California (415) 856-6900

CHIP TOPOGRAPHY



Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

ICM7208
CMOS
7 Decade Counter

FEATURES
- **Low operating power dissipation < 10mW**
- **Low quiescent power dissipation < 5mW**
- **Counts and displays 7 decades**
- **Wide operating supply voltage range**
  $2V \leq V^{+} \leq 6V$
- **Drives directly 7 decade multiplexed common cathode LED display**
- **Internal store capability**
- **Internal inhibit to counter input**
- **Test speedup point**
- **All terminals protected against static discharge**

DESCRIPTION
The ICM7208 is a fully integrated seven decade counter-decoder-driver and is manufactured using Intersil's low voltage metal gate C-MOS process.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

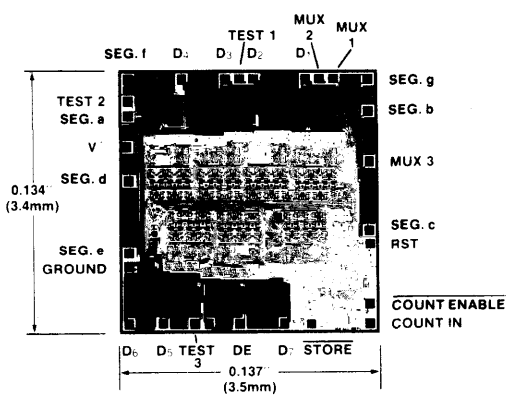
The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signal gating.

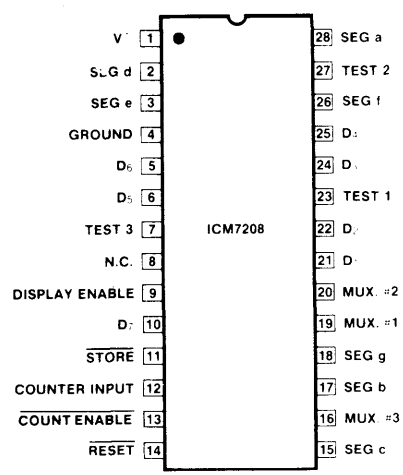
ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	28 LEAD PACKAGE
ICM7208IPI	-20°C to +85°C	PLASTIC
ORDER DICE BY FOLLOWING PART NUMBER: ICM7208D		

CHIP TOPOGRAPHY



PIN CONFIGURATION (OUTLINE DRAWING PI)



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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 1 W
Supply voltage (Note 2) 6V
Output digit drive current (Note 3) 150mA
Output segment drive current ..... 30 mA
Input voltage range (any input terminal) (Note 2) ... Not to exceed the supply voltage
Operating temperature range ..... -20°C to +85°C
Storage temperature range ..... -55°C to +125°C
Lead temperature (soldering, 10 seconds) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATION CHARACTERISTICS

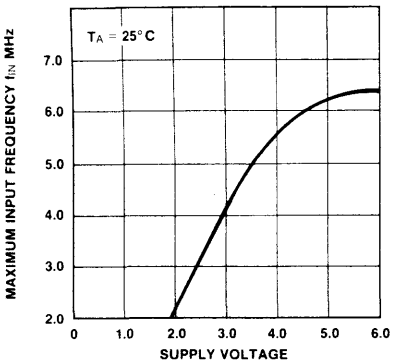
TEST CONDITIONS: (V^+ = 5V, T_A = 25°C, TEST CIRCUIT, display off, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I_Q	All controls plus terminal 19 connected to V^+ No multiplex oscillator		30	300	μA
Quiescent Current	I_Q	All control inputs plus terminal 19 connected to V^+ except STORE which is connected to GROUND		70	350	μA
Operating Supply Current	I^+	All inputs connected to V^+, RC multiplexer osc operating f_{in} < 25KHz		210	500	μA
Operating Supply Current	I^+	f_{in} = 2MHz			700	μA
Supply Voltage Range	V^+	$f_{in} \leq$ 2MHz	3.5		5.5	V
Digit Driver On Resistance	r_{DIG}			4	12	Ω
Digit Driver Leakage Current	I_{DIG}				500	μA
Segment Driver On Resistance	r_{SEG}			40		Ω
Segment Driver Leakage Current	I_{SLK}				500	μA
Pullup Resistance of RESET or STORE Inputs	R_P		100	400		kΩ
COUNTER INPUT Resistance	R_{IN}	Terminal 12 either at V^+ or GROUND			100	kΩ
COUNTER INPUT Hysteresis Voltage	V_{HIN}			25	50	mV

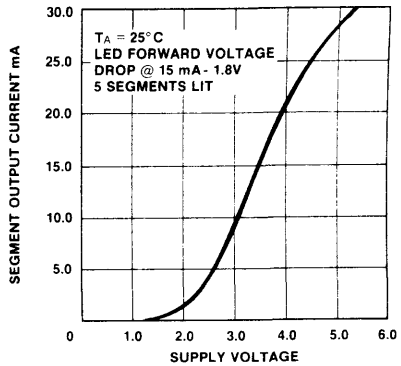
NOTE 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
NOTE 2: The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.
NOTE 3: The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

TYPICAL PERFORMANCE CHARACTERISTICS

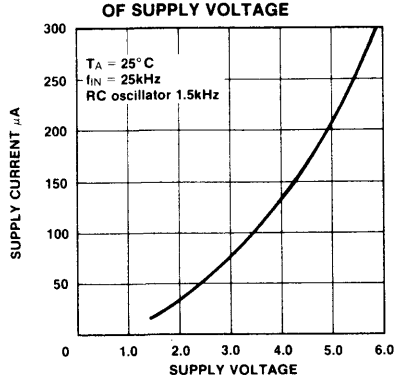
MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



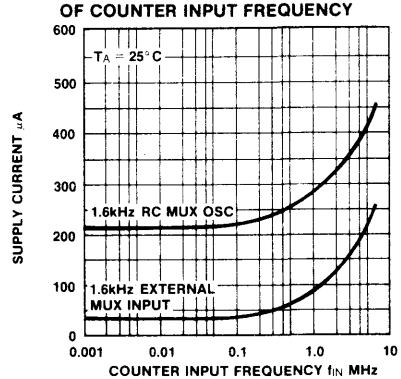
SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



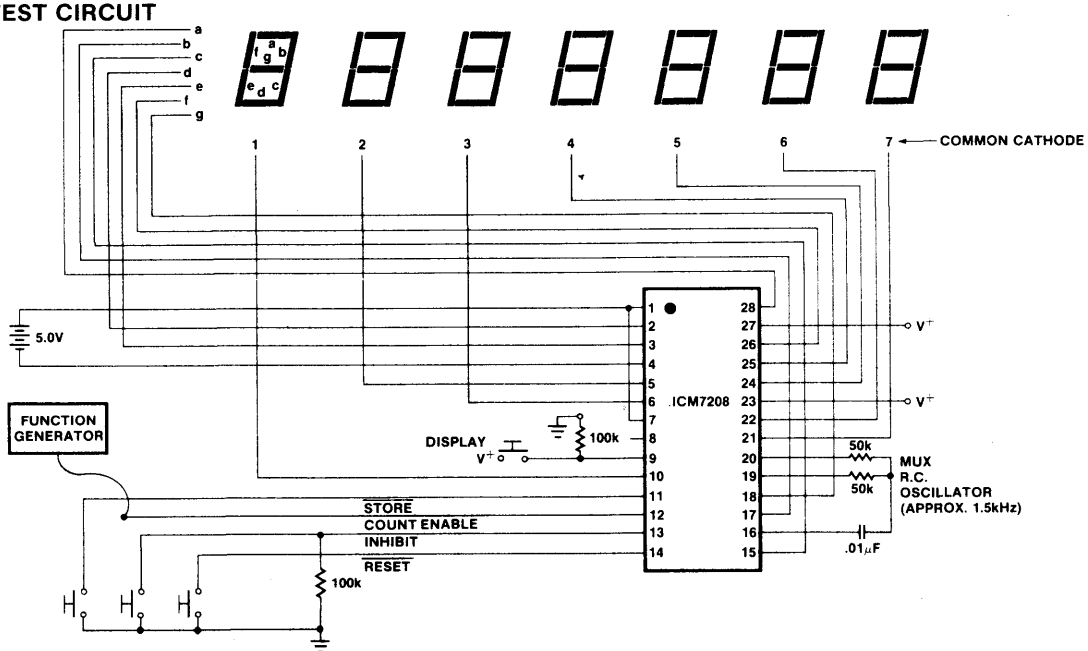
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY



TEST CIRCUIT



TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

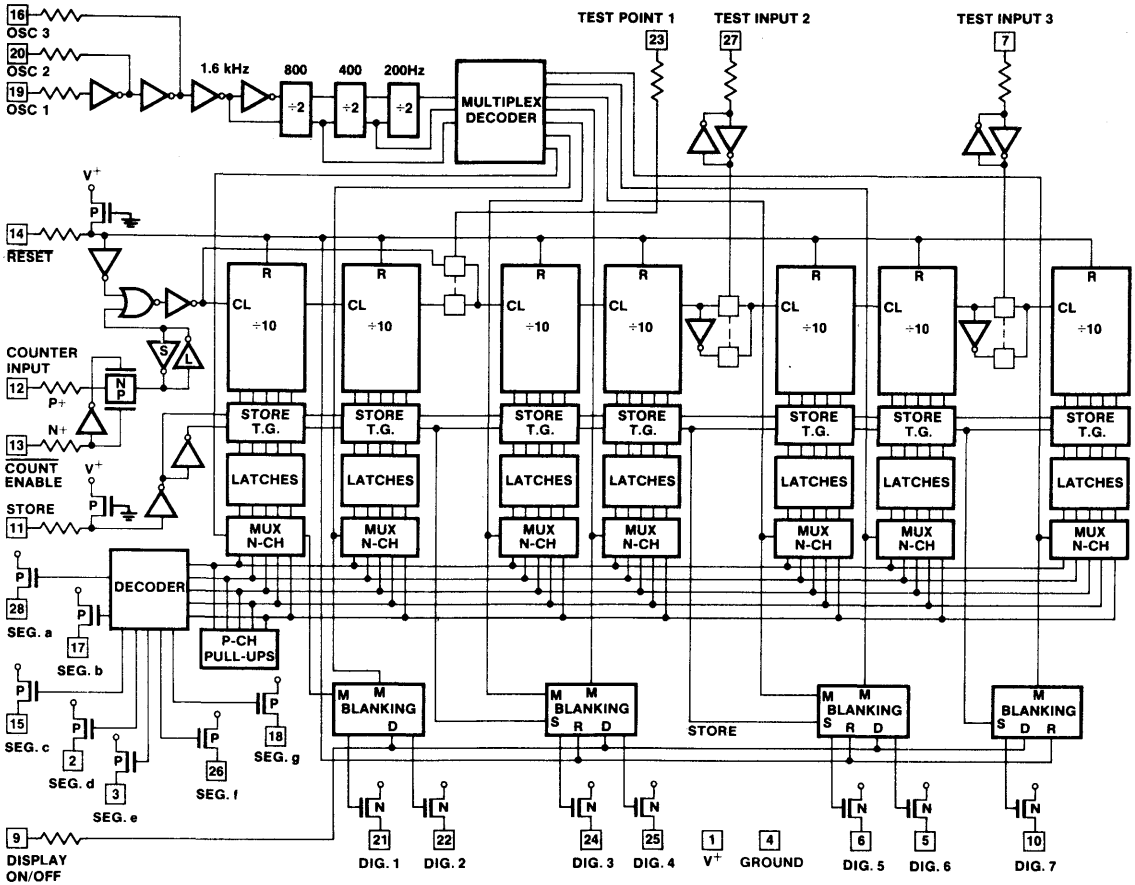
CONTROL INPUT DEFINITIONS

INPUT	TERMINAL	VOLTAGE	FUNCTION
1. DISPLAY	9	V^+	Display On
		Ground	Display Off
2. STORE	11	V^+	Counter Information Latched
		Ground	Counter Information Transferring
3. ENABLE	13	V^+	Input to Counter Blocked
		Ground	Normal Operation
4. RESET	14	V^+	Normal Operation
		Ground	Counters Reset

COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

BLOCK DIAGRAM



APPLICATION NOTES

1. Format of Signal to be Counted

The noise immunity of the COUNTER INPUT Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply. **NOTE: The amplitude of the input signal should not exceed the supply; otherwise, damage may be done to the circuit.**

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately $10^{-4}V/\mu sec$ at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

When driving the input of the ICM7208 from TTL, a 1k-5k ohm pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

2. Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit current exceed 150 mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with 500μA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

3. Display Multiplex Rate

The ICM7208 has approximately 0.5μs overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input.

4. Unit Counter

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.

For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

Figure 1 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4 x 1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

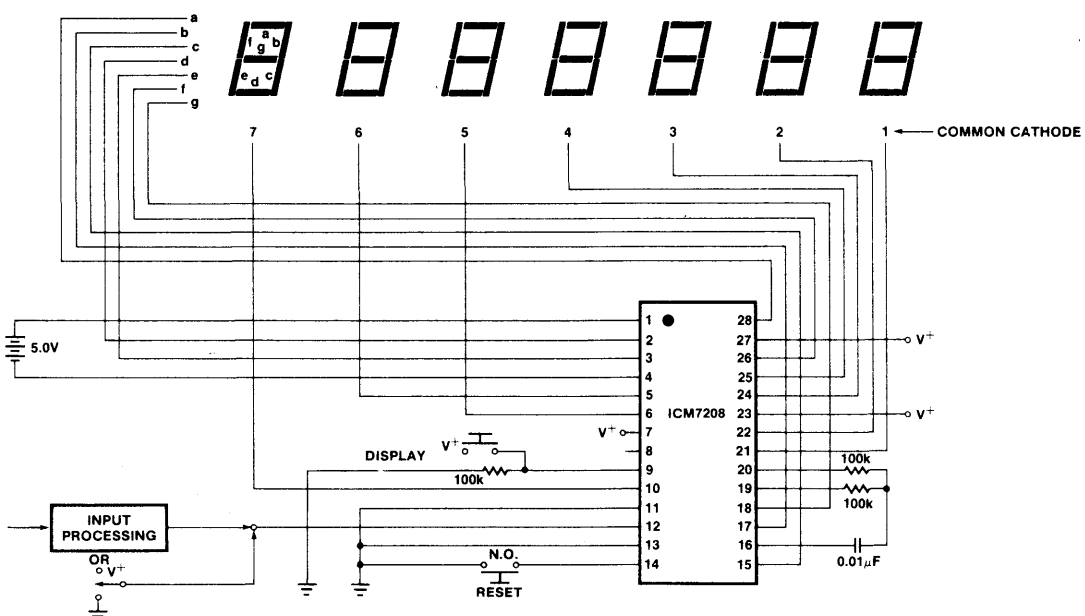


Figure 1: Schematic Unit Counter

5. Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 2). The ICM7207 uses a crystal controlled oscillator to provide the store and reset pulses together with the counting window. Figure 3 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches, and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

Using a 6.5536mHz quartz crystal and the ICM7207 driving the ICM7208, two ranges of counting may be obtained, using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

The ICM7207 provides the multiplex frequency reference of 1.6kHz.

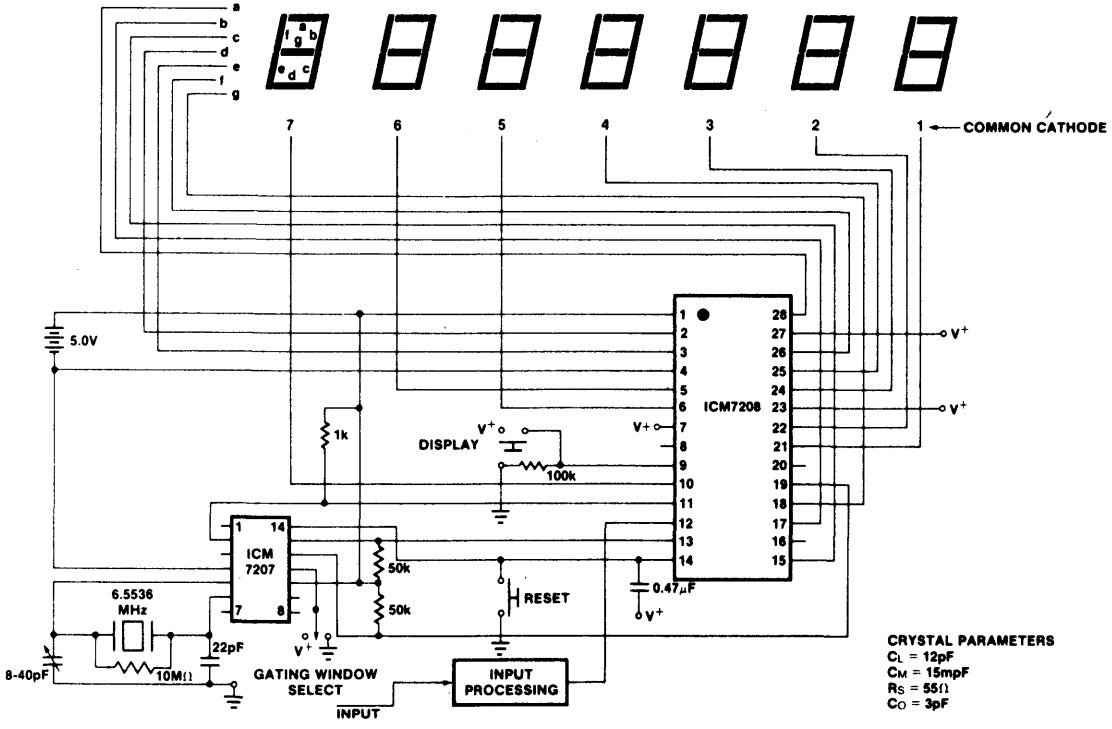


Figure 2: Frequency Counter

Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.

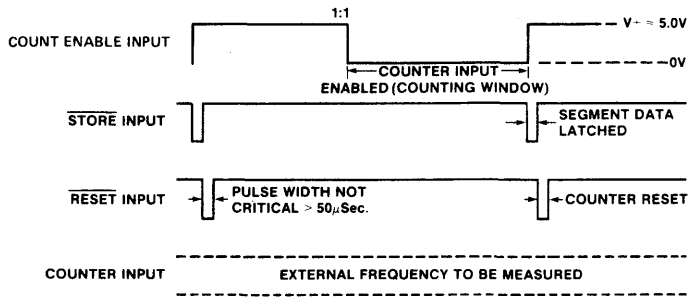


Figure 3: *Frequency Counter Input Waveforms*

6. Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure 5 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 4.

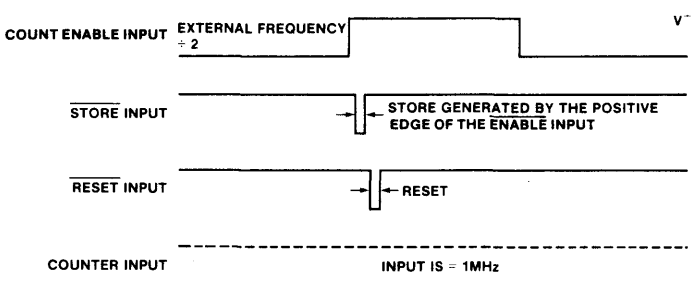


Figure 4: Period Counter Input Waveforms

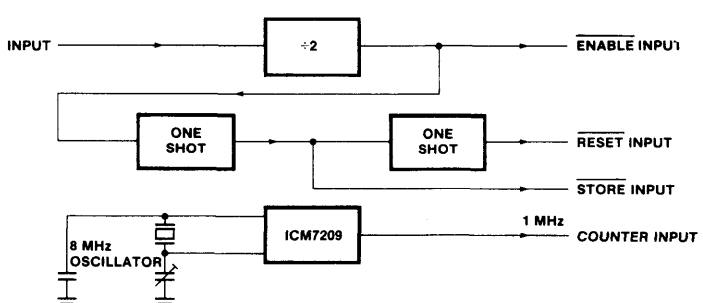


Figure 5: Period Counter Input Generator

ICM7211 (LCD)
ICM7212 (LED)
Four Digit CMOS Display Decoder/Drivers

ICM7211 (LCD) FEATURES

- **Four digit non-multiplexed 7 segment LCD display outputs with backplane driver**
- **Complete onboard RC oscillator to generate backplane frequency**
- **Backplane input/output allows simple synchronization of slave-device segment outputs to a master backplane signal**
- **ICM7211 devices provide separate Digit Select inputs to accept multiplexed BCD input (Pinout and functionally compatible with Siliconix DF411)**
- **ICM7211M devices provide data and digit select code input latches controlled by $\overline{\text{Chip Select}}$ inputs to provide a direct high speed processor interface**
- **ICM7211 decodes binary hexadecimal; ICM7211A decodes binary to Code B (0-9, dash, E, H, L, P, blank)**

ICM7212 (LED) FEATURES

- **28 current-limited segment outputs provide 4-digit non-multiplexed direct LED drive at > 5mA per segment.**
- **Brightness input allows direct control of LED segment current with a single potentiometer. Can function digitally as a display enable.**
- **ICM7212M and ICM7212A devices provide same input configuration and output decoding options as the ICM7211.**

DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs. These outputs provide the zero d.c. component signals necessary for long display life.

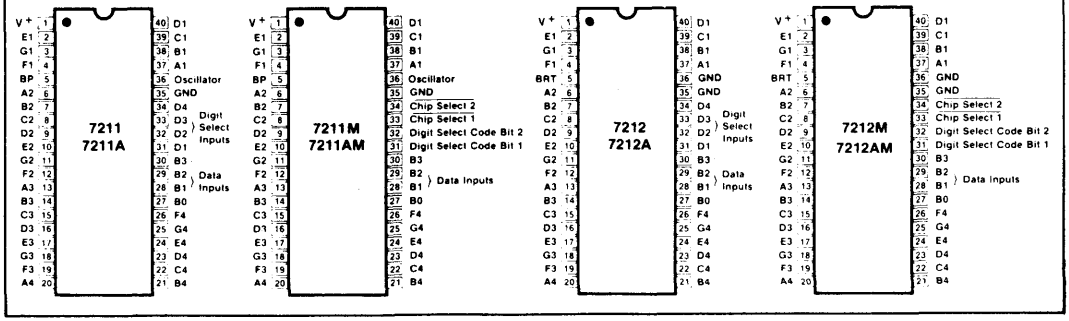
The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled low leakage open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with two input configurations. The basic devices provide four data-Bit inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL71C03. The microprocessor interface (suffix M) devices provide data input latches and Digit Select code latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

PIN CONFIGURATIONS (OUTLINE DRAWING PL)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 70°C
Supply Voltage 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, GROUND −0.3V
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.
NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

TEST CONDITIONS: All parameters measured with $V^+ = 5V$ unless otherwise specified.

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{op}	Test circuit, Display blank		10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36		±2	±10	
Segment Rise/Fall Time	t_{rfs}	C_L = 200pF		0.5		µs
Backplane Rise/Fall Time	t_{rfb}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{osc}	Pin 36 Floating		19		kHz
Backplane Frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{op}	Pin 5 (Brightness), Pins 27-34 - GROUND		10	50	µA
Operating Current	I_{op}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment On Current	I_{SEG}	Segment On, V_O = +3V	5	8		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				2	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	µA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	µA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			
Inter-Digit Select Time	t_{ids}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
$\overline{\text{Chip Select}}$ Active Pulse Width	t_{csa}	other $\overline{\text{Chip Select}}$ either held active, or both driven together	200			ns
Data Setup Time	t_{ds}		100			
Data Hold Time	t_{dh}		10	0		
Inter-$\overline{\text{Chip Select}}$ Time	t_{ics}		2			µs

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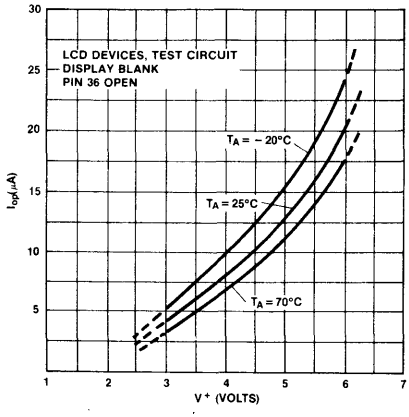
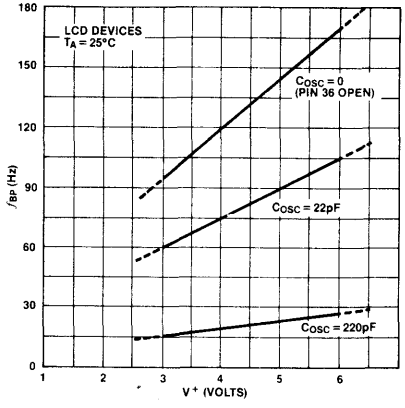
TYPICAL CHARACTERISTICS

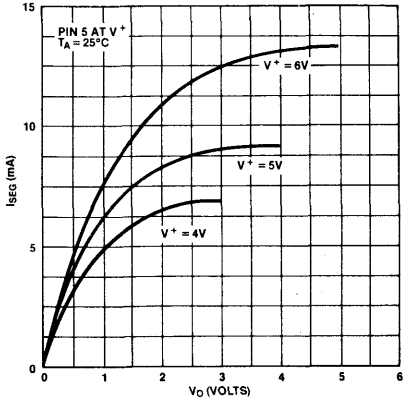
ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



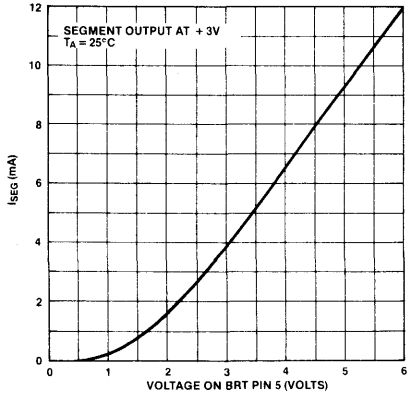
ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



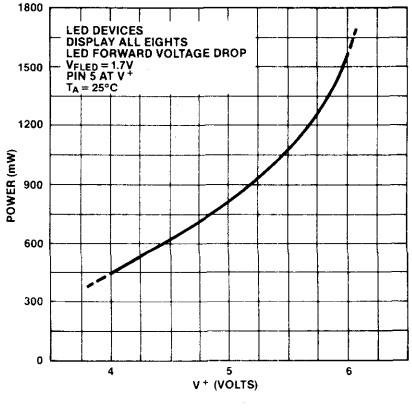
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

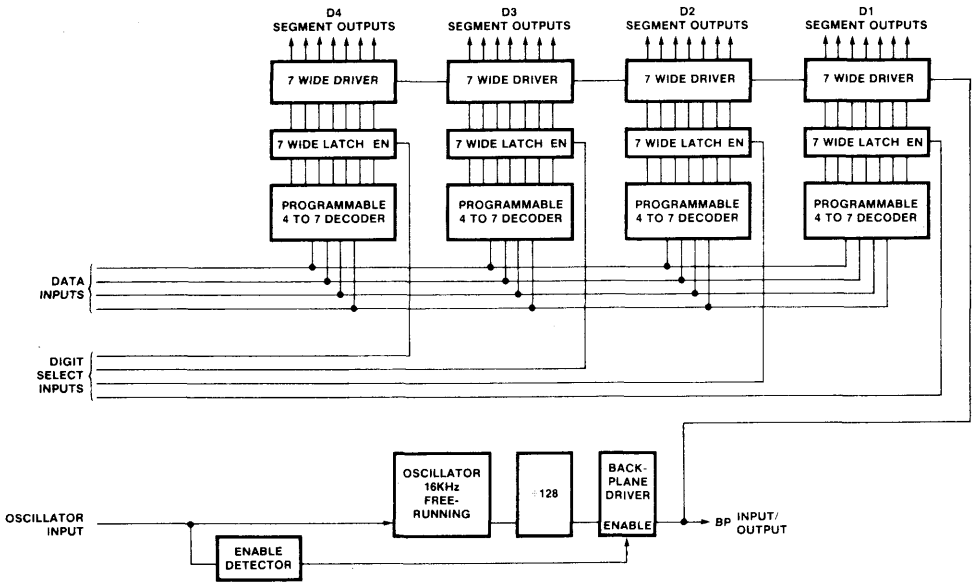


ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

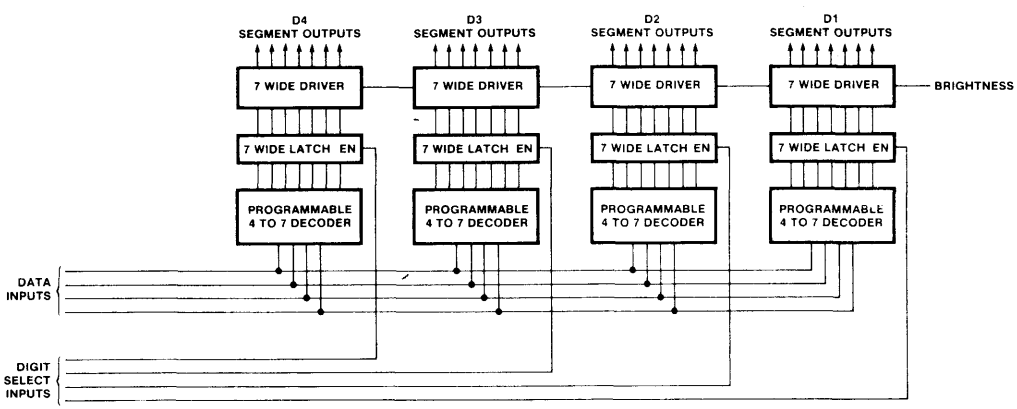


BLOCK DIAGRAMS

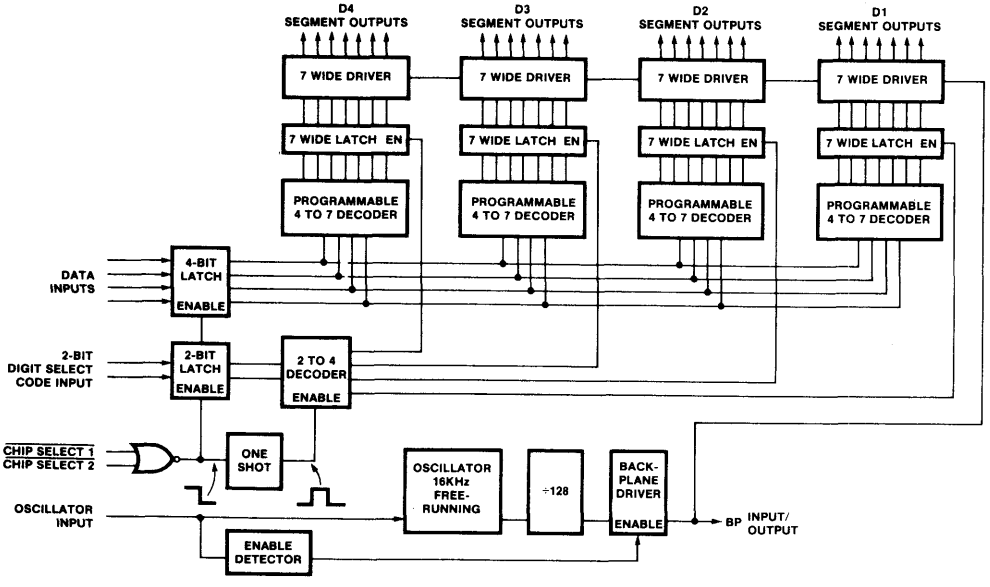
ICM7211 (A)



ICM7212 (A)



ICM7211(A)M



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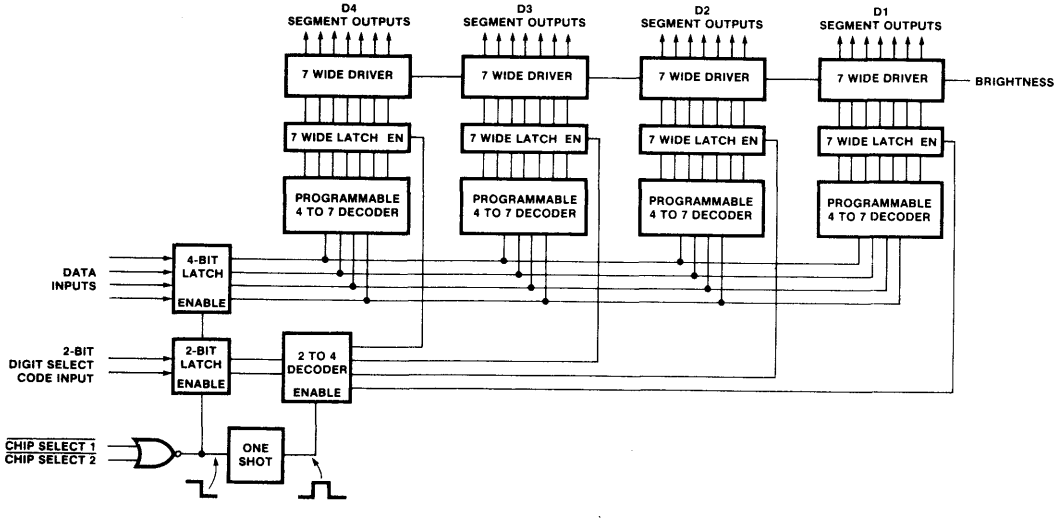
ICM7212(A)M



INPUT DEFINITIONS

In this table, V^+ and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One GND = Logical Zero	Twos	
B2	29	V^+ = Logical One GND = Logical Zero	Fours	
B3	30	V^+ = Logical One GND = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V^+ GROUND	Oscillator input Disables BP output devices, allowing segments to be synced to an external signal input at the BP terminal (Pin 5)	

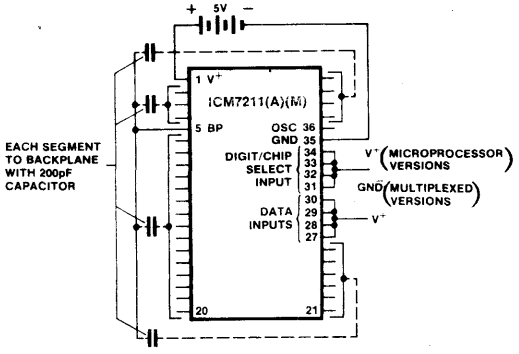
ICM7211/ICM7212
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active GND = Inactive	D1 (Least significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most significant) Digit Select

ICM7211M/ICM7212M
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One GND = Logical Zero	DS1 & DS2 serve as a two bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V^+ = Inactive GND = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

TEST CIRCUIT



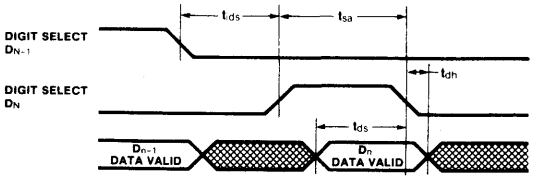


Figure 1: Multiplexed Input Timing Diagram

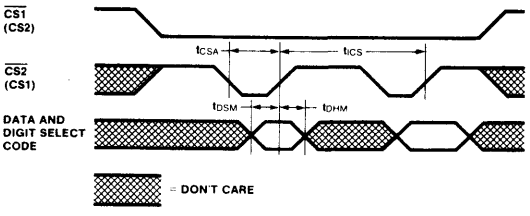


Figure 2: Microprocessor Interface Input Timing Diagram

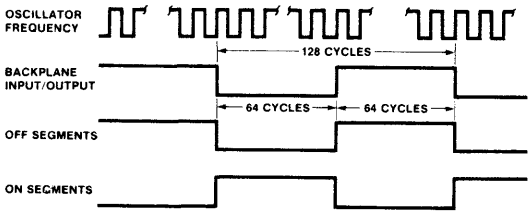
DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit by seven-segment LCD displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to GrouND. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment), thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits; and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters (rise and fall times not exceeding 5μs. ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very



Display Waveforms

large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V^+.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above GrouND). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit by seven-segment common-anode LED displays, including 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100KΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED devices have two connections for GrouND; both of these pins should be connected. The

double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (–15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

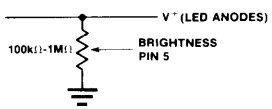


Figure 3: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211M, ICM7212, and ICM7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AM decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E. H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. *minimum*) custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Fig (1) and under Operating Characteristics for data setup, hold, and inter-digit select times must be met to ensure correct output.

The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

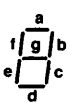
In these devices, the four data input bits and the two-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit select code latches.

A select code of 00 writes into D4, DS2 = 0, DS1 = 1 writes into D3, DS2 = 1, DS1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Fig (2), and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

Table 1: Output Codes

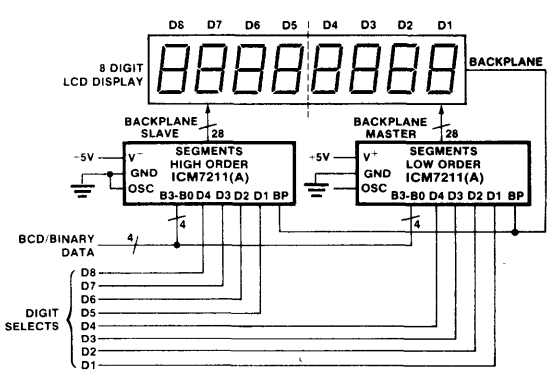
BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	H
1	1	0	0	C	L
1	1	0	1	d	P
1	1	1	0	E	E
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT

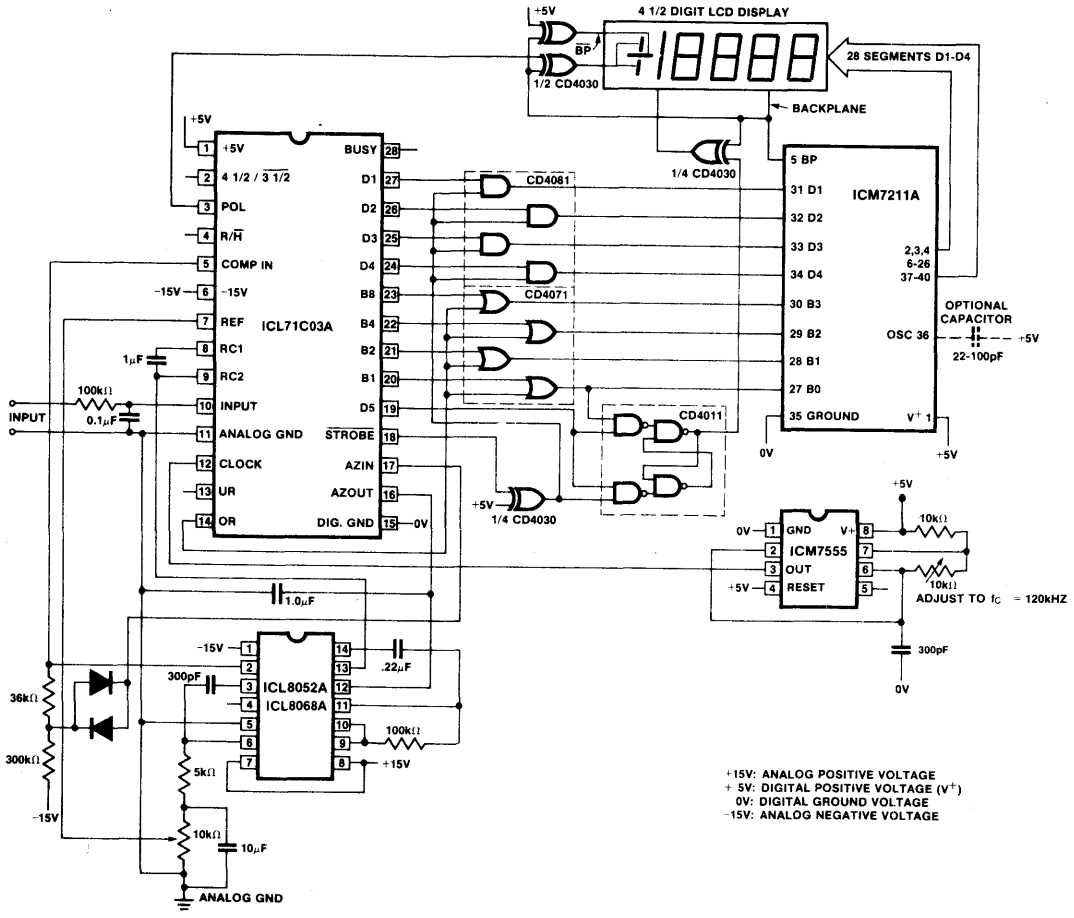


APPLICATIONS

1. Ganged ICM7211's Driving 8-Digit LCD Display.

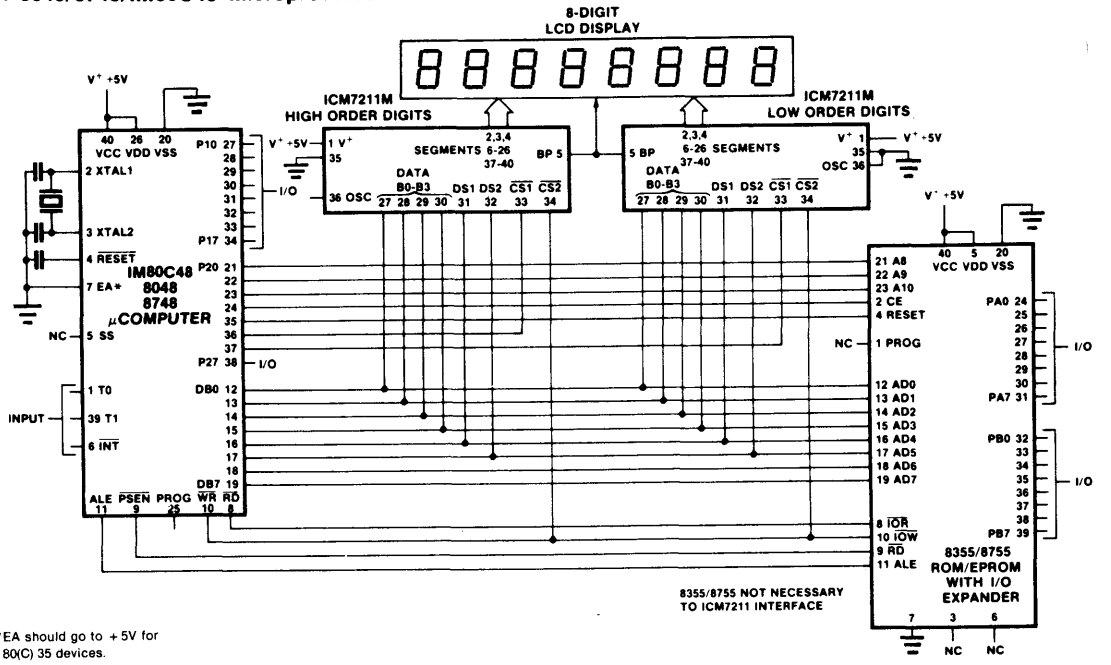


2. 4 1/2 Digit LCD DPM with Digit Blanking on Overrange.



NOTE: See also ICL8052/ICL8068/ICL71C03 and ICL7135 Data Sheets for similar circuits with fewer features.

3. 8048/8748/IM80C48 Microprocessor Interface.



*EA should go to + 5V for 80(C) 35 devices.

ORDERING INFORMATION

ORDER PART NUMBER		OUTPUT CODE	INPUT CONFIGURATIONS
LCD DISPLAY	ICM7211 IPL ICM7211A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT
	ICM7211M IPL ICM7211AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE
LED DISPLAY	ICM7212 IPL ICM7212A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT
	ICM7212M IPL ICM7212AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE

Evaluation Kits are also available. Order ICM7211 EV/Kit or ICM7212 EV/Kit.

ICM7216A/B/C/D 10 MHz Universal/ Frequency Counters

FEATURES

ALL VERSIONS:

- **Functions as a frequency counter. Measures frequencies from DC to 10 MHz**
- **Four internal gate times: 0.01 sec, 0.1 sec, 1 sec, 10 sec in frequency counter mode**
- **Output directly drives digits and segments of large multiplexed LED displays. Common anode and common cathode versions**
- **Single nominal 5V supply required**
- **Stable high frequency oscillator, uses either 1 MHz or 10 MHz crystal**
- **Internally generated decimal points, interdigit blanking, leading zero blanking and overflow indication**
- **Display Off mode turns off display and puts chip into low power mode**
- **Hold and Reset inputs for additional flexibility**

ICM7216A AND B

- **Functions also as a period counter, unit counter, frequency ratio counter or time interval counter**
- **1 cycle, 10 cycles, 100 cycles, 1000 cycles in period, frequency ratio and time interval modes**
- **Measures period from 0.5μs to 10s**

ICM7216C AND D

- **Decimal point and leading zero blanking may be externally selected**

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Universal Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1 Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in μsec. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

ORDERING INFORMATION

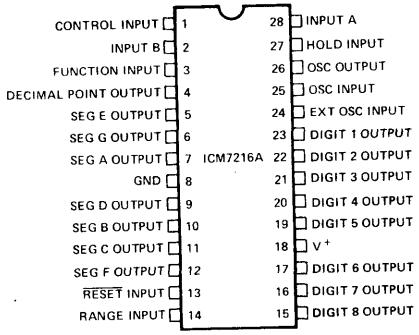
Universal Counter; Common Anode LED	**ICM 7216 A IJI**
Universal Counter; Common Cathode LED	**ICM 7216 B IPI**
Frequency Counter; Common Anode LED	**ICM 7216 C IJI**
Frequency Counter; Common Cathode LED	**ICM 7216 D IPI**

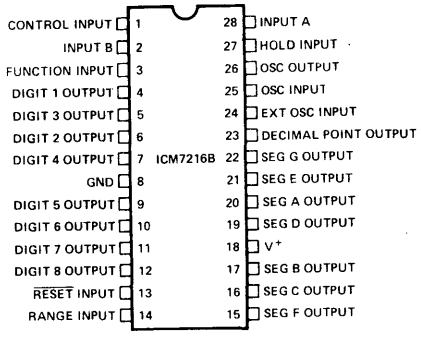
Evaluation Kit:
Use ICM7226 EV/Kit

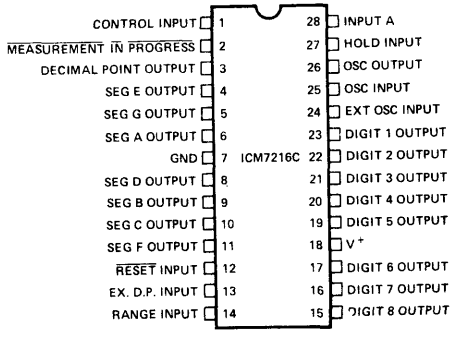
ICM 7216 D IPI

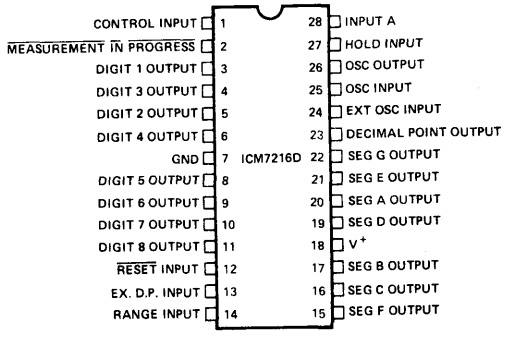
- ICM 7216 D — Type
- IPI — Package: JI — 28 pin CERDIP; PI — 28 pin PLASTIC DIP
- IPI — Temperature Range -20°C to +85°C

PIN CONFIGURATIONS (outline dwgs JI, PI)









EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIJL (Common Anode LED Display), a 10MHz quartz crystal, eight 7 segment 0.3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or Output Terminal[1] ..... $V^+ + 0.3V$ to $-0.3V$
Maximum Power Dissipation at 70°C ..... 1.0W (ICM7216A & C)
0.5W (ICM7216B & D)
Lead Temperature (Soldering, 10 sec) ..... 300°C
Maximum Operating Temperature Range ..... −20°C to +85°C
Maximum Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ to GND by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216A/B						
Operating Supply Current	I^+	Display Off, Unused Inputs to GND		2	5	mA
Supply Voltage Range	V^+	-20°C < T_A < +85°C, INPUT A, INPUT B Frequency at f_{max}	4.75		6.0	V
Maximum Frequency INPUT A, Pin 28	$f_{A(max)}$	-20°C < T_A < +85°C 4.75 < $V^+ \leq$ 6.0V, Figure 1, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5			 MHz MHz
Maximum Frequency INPUT B, Pin 2	$f_{B(max)}$	-20°C < T_A < +85°C 4.75 < $V^+ \leq$ 6.0V, Figure 2	2.5			MHz
Minimum Separation INPUT A to INPUT B Time Interval Function		-20°C < T_A < +85°C 4.75 < $V^+ \leq$ 6.0V, Figure 3	250			ns
Maximum Osc. Freq. and Ext. Osc. Frequency	f_{osc}	-20°C < T_A < +85°C 4.75 < $V^+ \leq$ 6.0V	10			MHz
Minimum Ext. Osc. Freq.	f_{osc}				100	kHz
Oscillator Transconductance	g_m	V^+ = 4.75V, T_A = +85°C	2000			μmhos
Multiplex Frequency	f_{mux}	f_{osc} = 10MHz		500		Hz
Time Between Measurements		f_{osc} = 10MHz		200		ms
Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage	 V_{INL} V_{INH}	-20°C < T_A < +85°C	 3.5		1.0	 V V
Input Resistance to V^+ Pins 13,24	R_{IN}	$V_{IN} = V^+ - 1.0V$	100	400		kΩ
Input Leakage Pin 27,28,2	I_{ILK}				20	μA
Minimum Input Rate of Change	dV_{IN}/dt	Supplies Well Bypassed		15		mV/μs
ICM7216A						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	 I_{OH} I_{OL}	 $V_{OUT} = V^+ - 2.0V$ V_{OUT} = + 1.0V	 -140	 -180 +0.3		 mA mA
SEGment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 V_{OUT} = + 1.5V $V_{OUT} = V^+ - 2.5V$	 20	 35 -100		 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to GROUND	 V_{INL} V_{INH} R_{IN}	 V_{IN} = +1.0V	 2.0 50	 100	0.8	 V V kΩ
ICM7216B						
Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 V_{OUT} = + 1.3V $V_{OUT} = V^+ - 2.5V$	 50	 75 -100		 mA μA
SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	 I_{OH} I_{SLK}	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	 -10	 	 10	 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V^+	 V_{INL} V_{INH} R_{IN}	 $V_{IN} = V^+ - 1.0V$	 $V^+ - 0.8$ 200	 360	 $V^+ - 2.0$ 	 V V kΩ

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP	MAX.	UNITS
ICM7216C/D						
Operating Supply Current	I^+	Display Off, Unused Inputs to GND		2	5	mA
Supply Voltage Range		$-20°C < T_A < +85°C$, INPUT A Frequency at f_{max}	4.75		6.0	V
Maximum Frequency INPUT A, Pin 28	$f_{A(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ < 6.0V$, Figure 1	10			MHz
Maximum Osc. Freq and Ext. Osc. Frequency	f_{osc}	$-20°C < T_A < +85°C$ $4.75 < V^+ < 6.0V$	10			MHz
Minimum Ext. Osc. Freq.	f_{osc}				100	kHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$, $T_A = +85°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		ms
Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage	V_{INL} V_{INH}	$-20°C < T_A < +85°C$	 3.5		1.0	V V
Input Resistance to V^+ Pins 12,24	R_{IN}	$V_{IN} = V^+ - 1.0V$	100	400		kΩ
Input Leakage Pin 27, Pin 28	I_{ILK}				20	μA
Output Current Pin 2	I_{OL}	$V_{OL} = +.4V$	0.36			mA
	I_{OH}	$V_{OH} = V^+ - .8V$	265			μA
Minimum Input Rate of Change	dV_{IN}/dt	Supplies Well Bypassed		15		mV/μs
ICM7216C						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	I_{OH} I_{OL}	$V_{OUT} = V^+ - 2.0V$ $V_{OUT} = 1.0V$	-140	-180 0.3		mA mA
SEGment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	I_{OL} I_{OH}	$V_{OUT} = +1.5V$ $V_{OUT} = V^+ - 2.5V$	20	30 -100		mA μA
Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to GROUND	V_{INL} V_{INH} R_{IN}	 $V_{IN} = +1.0V$	 2.0 50	 100	0.8	V V kΩ
ICM7216D						
Digit Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	I_{OL} I_{OH}	$V_{OUT} = +1.3V$ $V_{OUT} = V^+ - 2.5V$	50	75 100		mA μA
SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	I_{OH} I_{SLK}	$V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	10	15	 10	mA μA
Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V^+	V_{INL} V_{INH} R_{IN}	 $V_{IN} = V^+ - 1.0V$	 $V^+ - 0.8$ 200	 360	$V^+ - 2.0$	V V kΩ

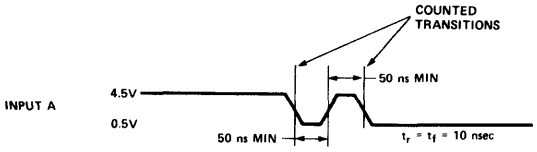


FIGURE 1. Waveform for Guaranteed Minimum $f_{A(max)}$ Function = Frequency, Frequency Ratio, Unit Counter.

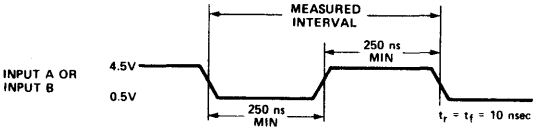


FIGURE 2. Waveform for Guaranteed Minimum $f_{B(max)}$ and $f_{A(max)}$ for Function = Period and Time Interval.

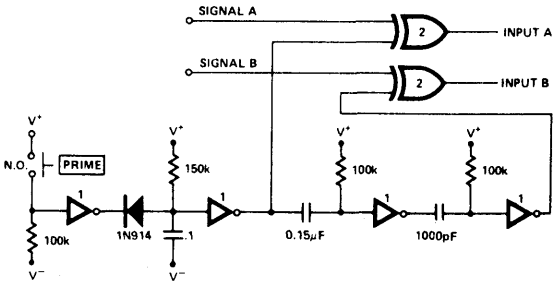
TIME INTERVAL MEASUREMENT

The ICM7216A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7216A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can be easily accomplished with the following circuit: (Figure 3b).



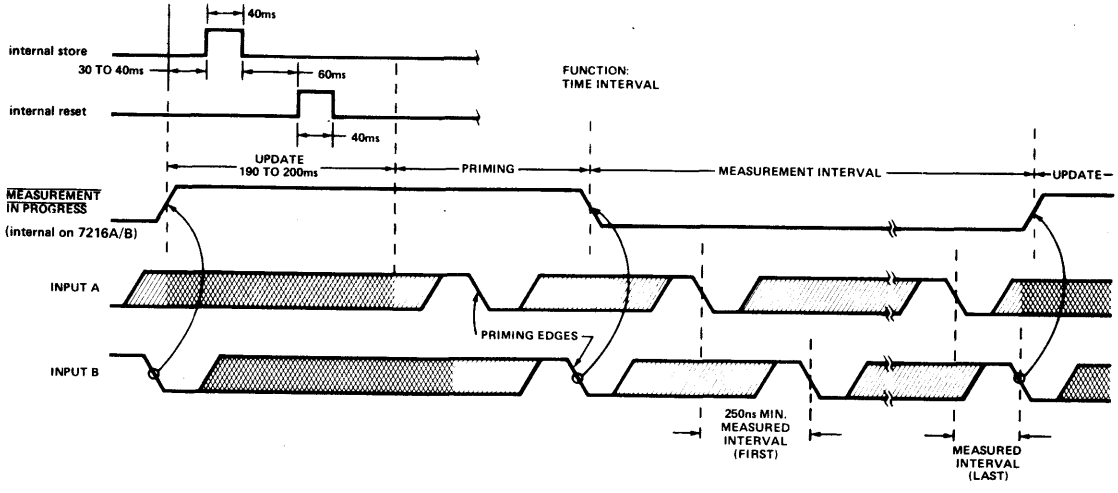
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3b. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A/B as the first alternating signal states automatically prime the device. See Figure 3b.

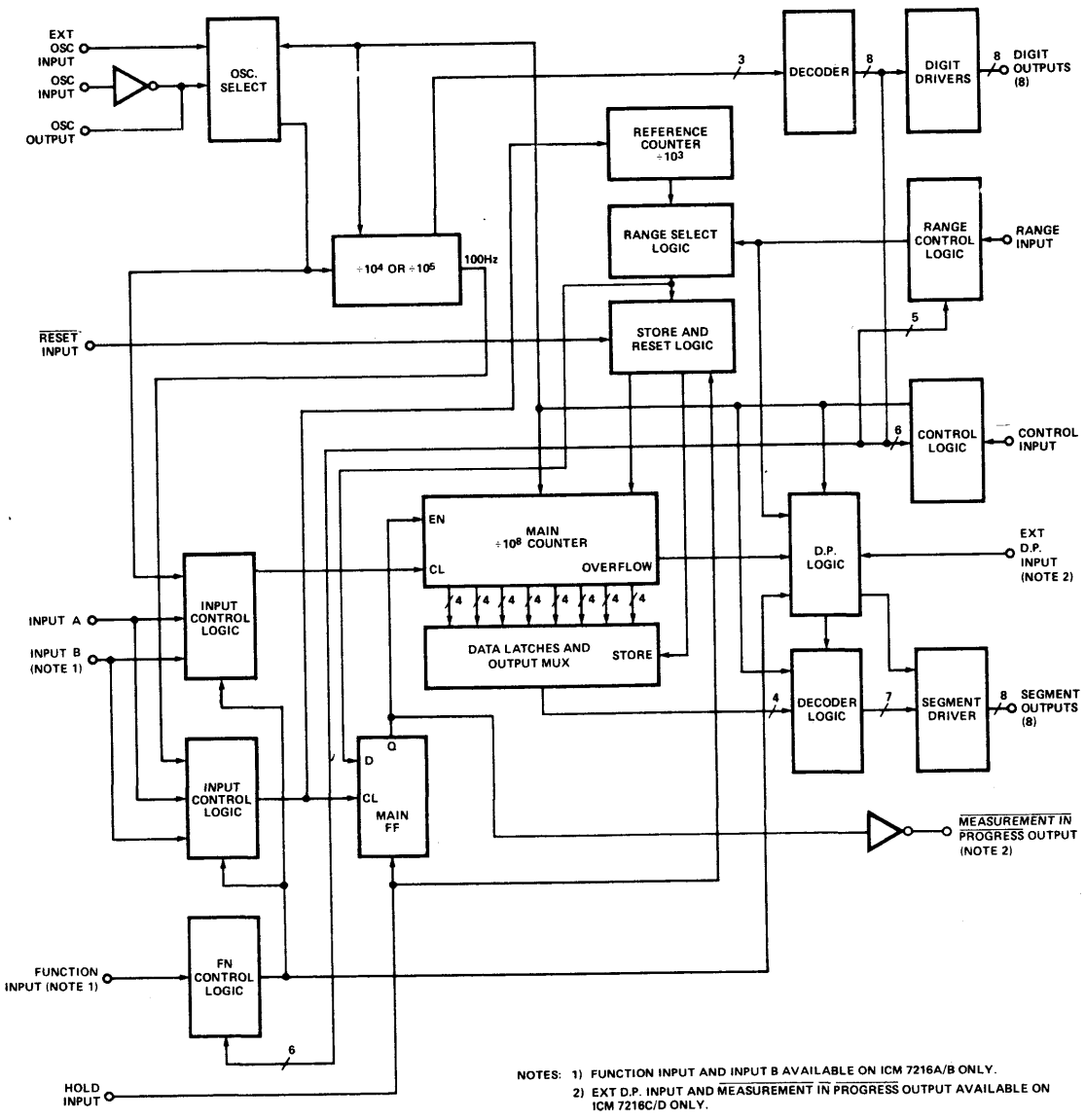
During any time interval measurement cycle, the ICM7216A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

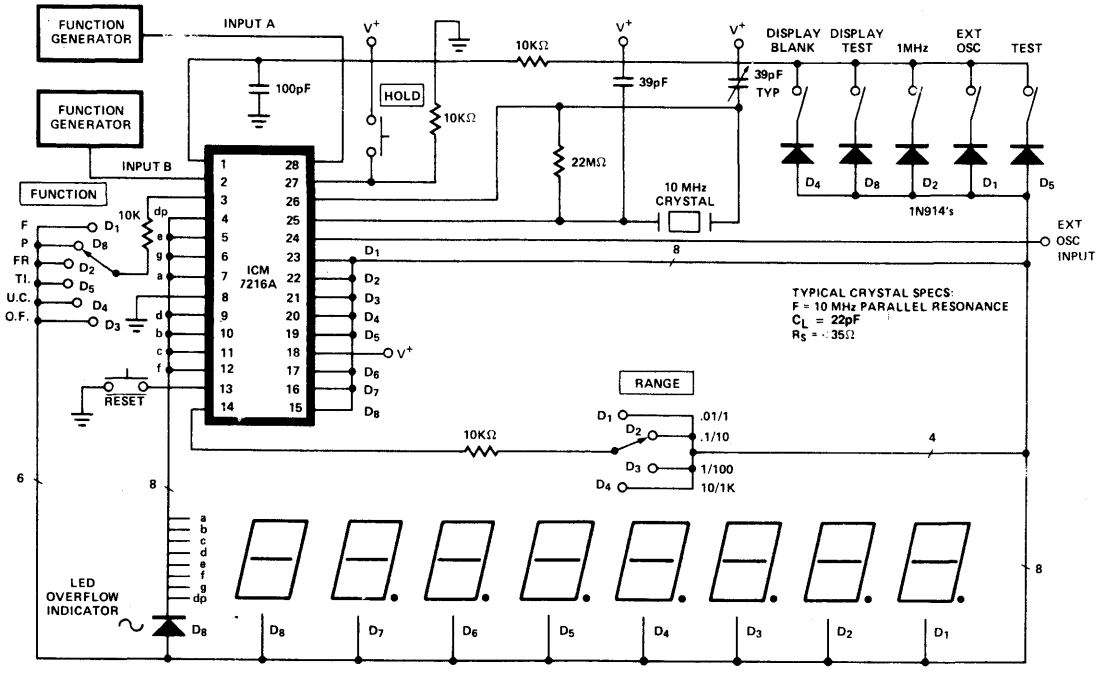
FIGURE 3a. Waveforms for Time Interval Measurement (others are similar, but without priming phase).

BLOCK DIAGRAM

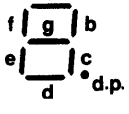


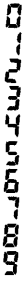
NOTES: 1) FUNCTION INPUT AND INPUT B AVAILABLE ON ICM 7216A/B ONLY.
2) EXT D.P. INPUT AND MEASUREMENT IN PROGRESS OUTPUT AVAILABLE ON ICM 7216C/D ONLY.

TEST CIRCUIT (7216A shown; others similar)



SEGMENT IDENTIFICATION AND DISPLAY FONT





Overflow will be indicated on the decimal point output of digit 8.

A separate LED overflow indicator can be connected as follows:

	CATHODE	ANODE
ICM7216A/C	DEC. PT.	D_8
ICM7216B/D	D_8	DEC. PT.

APPLICATION NOTES

GENERAL

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from T²L logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A/B).

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. Multiplexed Input Functions

	FUNCTION	DIGIT
FUNCTION INPUT Pin 3 (ICM7216A & B Only)	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT Pin 14	.01 sec/1 Cycle	D_1
	.1 sec/10 Cycles	D_2
	1 sec/100 Cycles	D_3
	10 sec/1K Cycles	D_4
CONTROL INPUT Pin 1	Blank Display	D_4 and Hold
	Display Test	D_8
	1 MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	(Test	D_5)
EXT. D.P. INPUT Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

CONTROL INPUT Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Blank Display is selected at the same time.

Blank Display — To disable the drivers, it is necessary to tie D_4 to the CONTROL INPUT and have the HOLD input at V^+. The chip will remain in this "Display Off" mode until HOLD is switched back to GND. While in the "Display Off" mode, the segment and digit driver outputs are open, the oscillator continues to run with a typical supply current of 1.5mA with a 10 MHz crystal, and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to GND. Segment and Digit Drive outputs may thus be bussed to drive a common display (up to 6 circuits).

1 MHz Select — The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable — In this mode the EXTERNAL OSCILLATOR INPUT is used instead of the on-chip oscillator for Timebase input and Main Counter input in **period** and **time interval modes.** The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 kHz or the chip will reset itself to enable the on-chip oscillator. OSCillator INPUT (pin 25) must also be connected to EXT. OSC. input when using EXT. OSC. input.

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to EXTERNAL DECIMAL POINT input is active. Leading Zero Blanking will be disabled for all digits following the decimal point (7216C/D only).

Test Mode — This is a special mode for testing purposes only. Contact factory for details.

RANGE INPUT

The RANGE INPUT selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except **unit counter** a change in the RANGE INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

FUNCTION INPUT

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.** This Input is available on the ICM7216A *and B only.*

These functions select which signal is counted into the Main Counter and which signal is counted by the Reference Counter, as shown in Table 2. In all cases, only 1→0 transitions are counted or timed. In **time interval**, a flip-flop is toggled first by a 1→0 transition of INPUT A and then by a 1→0 transition of INPUT B. The oscillator is gated into the Main Counter from the time INPUT A toggles the flip-flop until INPUT B toggles it. In **unit counter** mode, the main counter contents are continuously displayed. A change in the FUNCTION INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed.

TABLE 2. 7216A/B Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A → B)	Oscillator (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

6

EXTernal DECimal Point INput

When the **external decimal point** is selected this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

HOLD Input — Except in **unit counter** mode, when the HOLD input is at V^+ any measurement in progress (before the "store time", see Figure 3a) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When HOLD is changed to GND a new measurement is immediately initiated. In **unit counter** mode, the counter is not reset; the count is frozen but will continue if HOLD goes low again.

$\overline{\text{RESET}}$ Input — The RESET input is the same as an inverted HOLD Input, except the latches for the Main Counter are enabled, resulting in an output of all zeros, and the pin has a pull-up.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking assume right hand decimal point displays, and zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows. Overflow is indicated by the decimal point on digit 7 turning on.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8$ V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with $V_F = 1.8$V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4,5,6 and 7 show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

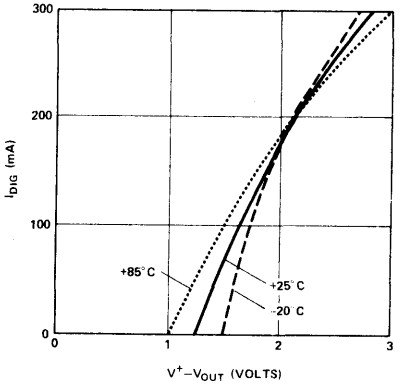


FIGURE 4. ICM7216A & C Typical I_{DIG} vs. $V^+ - V_{OUT}$, 4.5V ≤ V^+ ≤ 6.0V

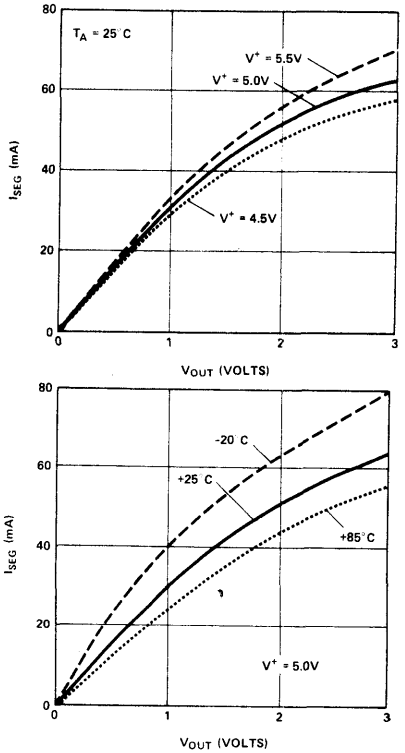
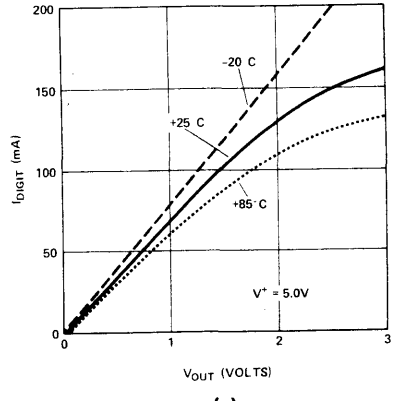
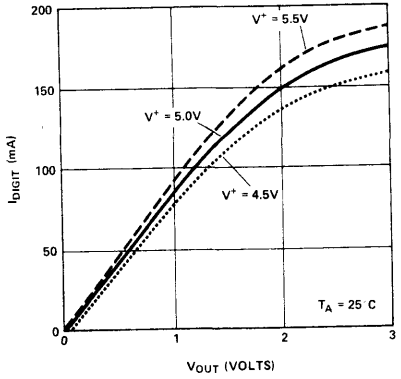


FIGURE 5. ICM7216A & C Typical I_{SEG} vs. V_{OUT}



(a)



(b)

FIGURE 6. ICM7216B & D Typical I_{DIGIT} vs. V_{OUT}

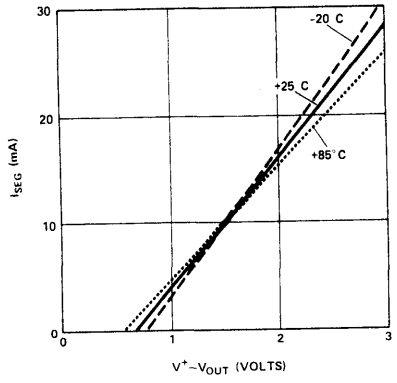


FIGURE 7. ICM7216B & D Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

ACCURACY

In a Universal Counter crystal drift and quantization effects cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ± 1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 8, the least accuracy will be obtained at 10 kHz. In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 9. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 10.

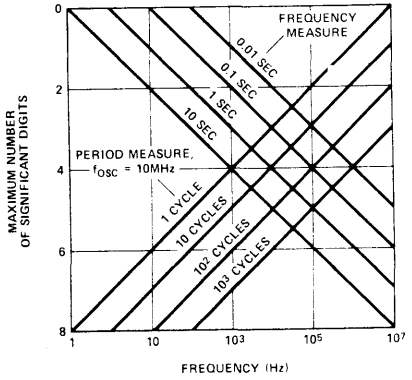


FIGURE 8. Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

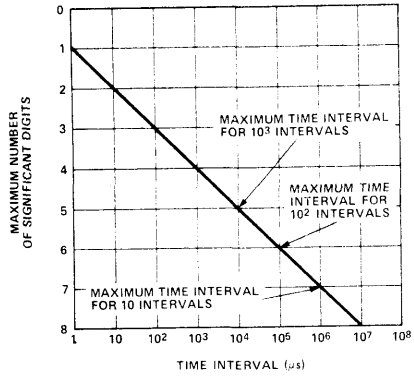


FIGURE 9. Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

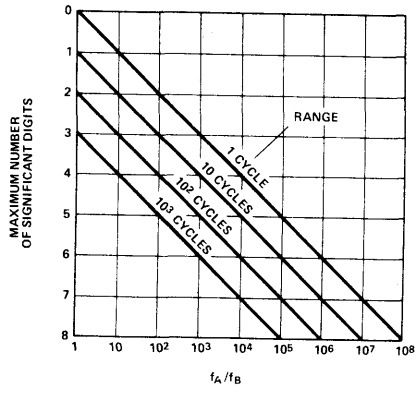


FIGURE 10. Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 11. This circuit can use input frequencies up to 10 MHz at INPUT A and 2 MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ns in duration.

To measure frequencies up to 40 MHz the circuit of Figure 12 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 ms and the display multiplex rate is decreased to 125 Hz.

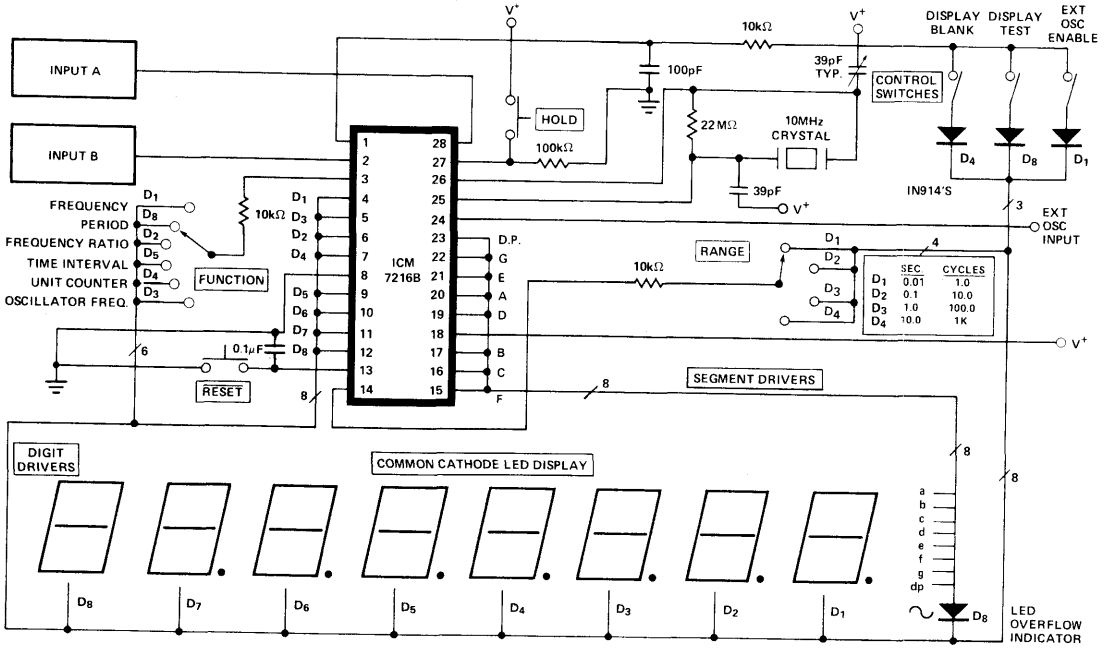


FIGURE 11. 10MHz Universal Counter

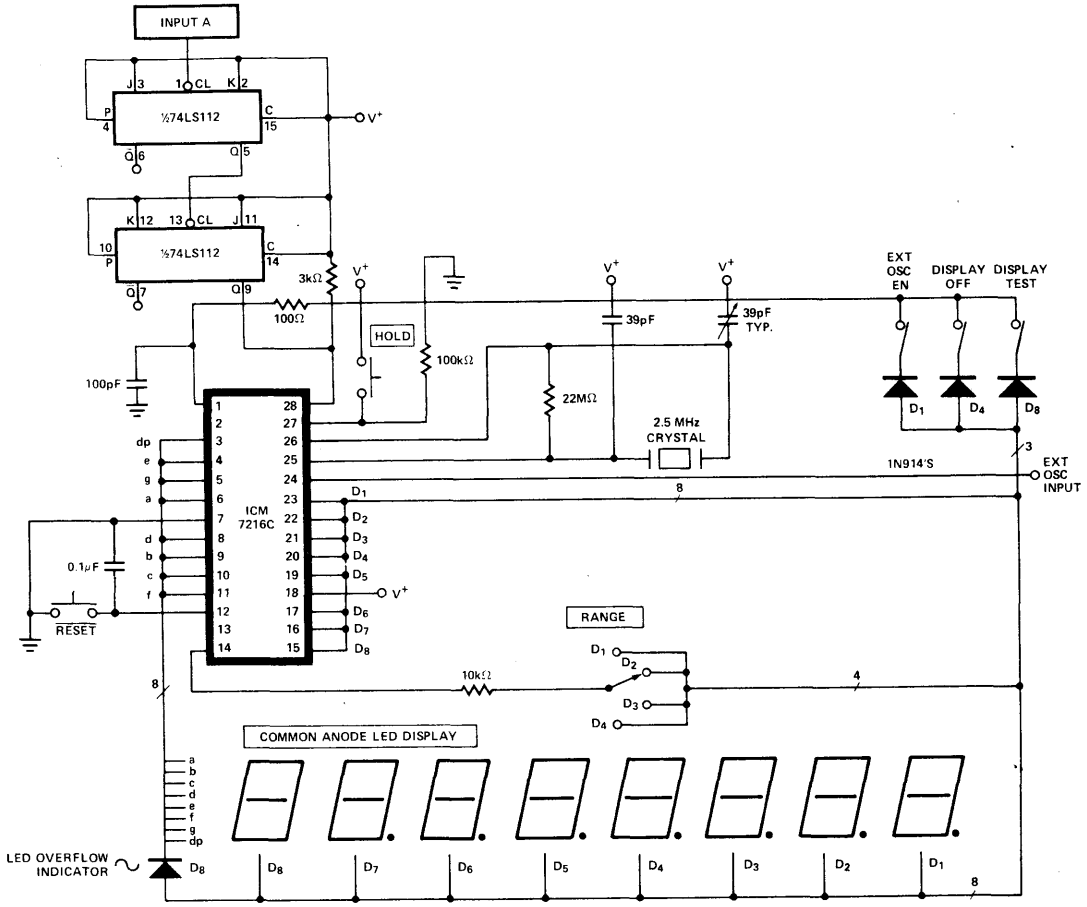


FIGURE 12. 40MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 MHz, but the decimal point must be moved one digit to the right. Figure 13 shows a frequency counter with a ÷10 prescaler and an ICM7216C. Since there is no external decimal point control with the ICM7216A or B, the decimal point may be controlled externally with additional drivers as shown in Figure 14. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 15 additional logic has been added to count the input directly in **period** mode for maximum accuracy. In Figures 13 through 15, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

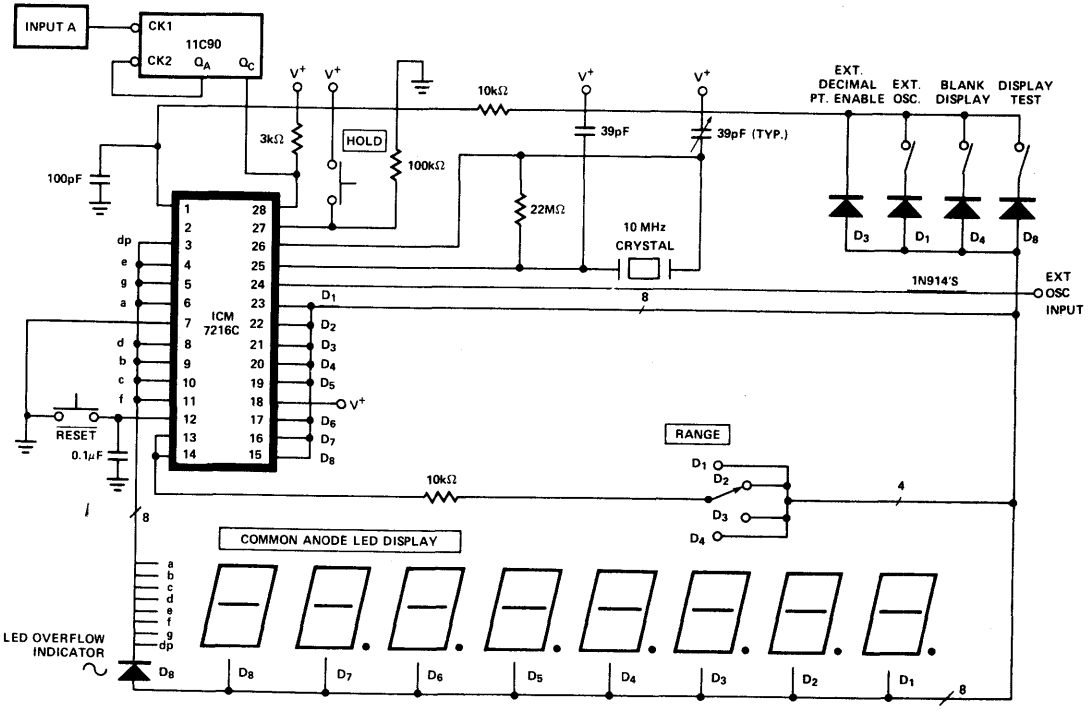


FIGURE 13. 100MHz Frequency Counter

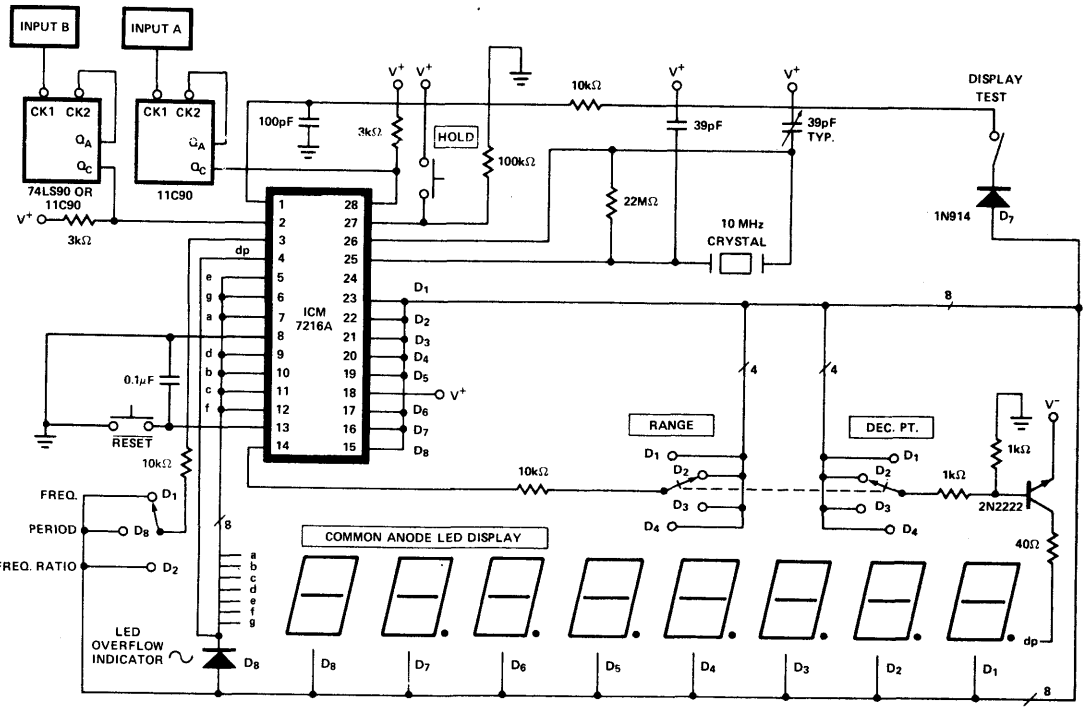


FIGURE 14. 100MHz Multifunction Counter

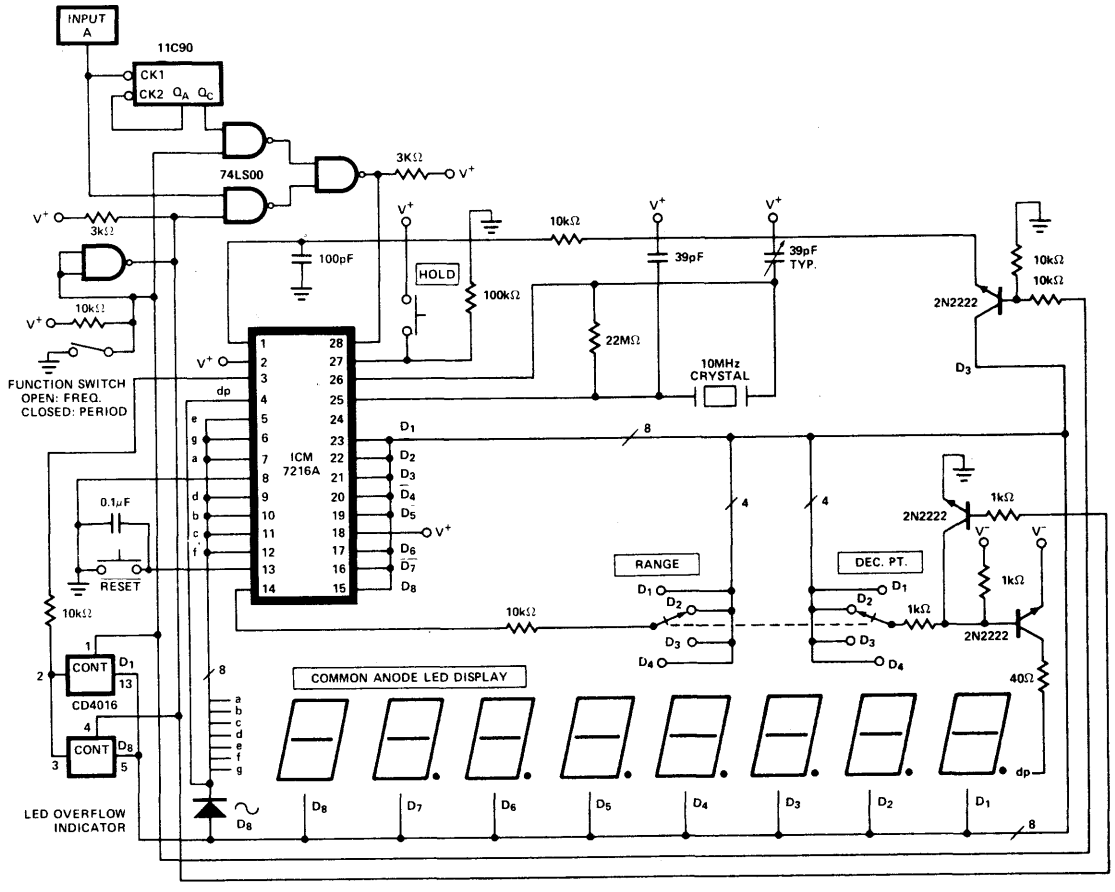


FIGURE 15. 100MHz Frequency, 2MHz Period Counter

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

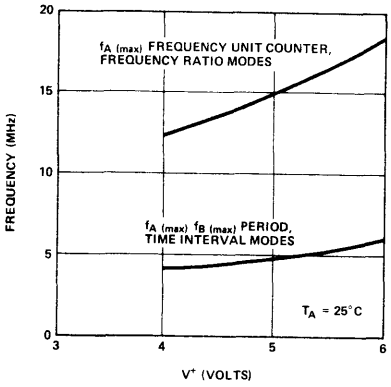
where $C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$

C_O = Crystal Static Capacitance
R_S = Crystal Series Resistance
C_{in} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2 \times 10^4}$ for 10 MHz mode and $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1 MHz mode.

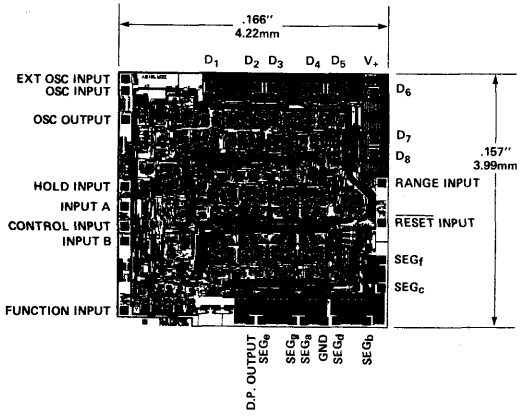
The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.



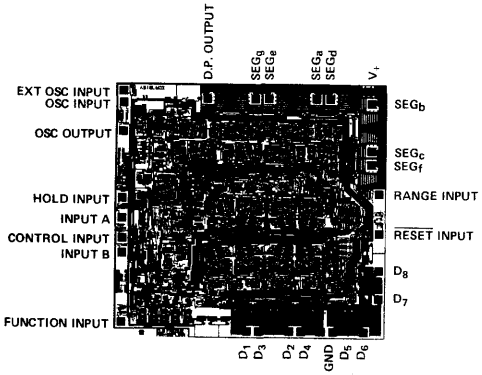
$f_{A(max)}$, $f_{B(max)}$ as a Function of V+

FIGURE 16. Typical Operating Characteristics

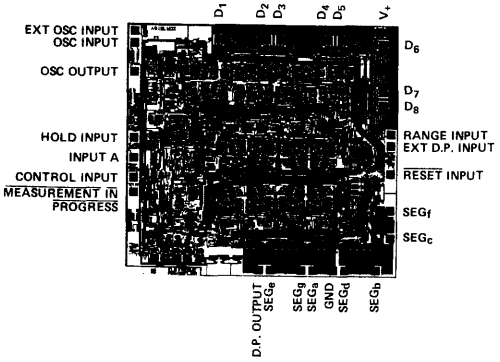
CHIP TOPOGRAPHIES



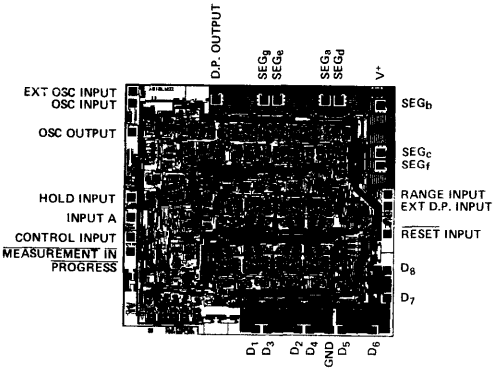
ICM7216A



ICM7216B



ICM7216C



ICM7216D

ICM7217 Series
ICM7227 Series
4-Digit CMOS Up/Down Counter/ Display Driver

FEATURES

- **Four decade, presettable up-down counter with parallel zero detect**
- **Settable register with contents continuously compared to counter**
- **Directly drives multiplexed 7 segment common anode or common cathode LED displays**
- **On-board multiplex scan oscillator**
- **Schmitt trigger on count input**
- **TTL compatible BCD I/O port, carry/borrow, equal, and zero outputs**
- **Display blank control for lower power operation; quiescent power dissipation < 5mW**
- **All terminals fully protected against static discharge**
- **Single 5V supply operation**

DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to .8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

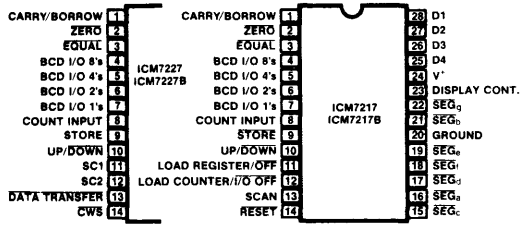
The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

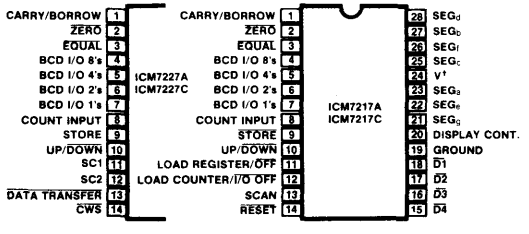
To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2 MHz, although the device will typically run with f_{in} as high as 5 MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750 kHz maximum.

PIN CONFIGURATIONS (outline dwgs JI, PI)



COMMON ANODE



COMMON CATHODE

ORDERING INFORMATION

Display Option	Count Option Max Count	28-LEAD Package	Order Part Number
Common Anode	Decade/9999	CERDIP	ICM7217IJI
Common Cathode	Decade/9999	PLASTIC	ICM7217AIPI
Common Anode	Timer/5959	CERDIP	ICM7217BIJI
Common Cathode	Timer/5959	PLASTIC	ICM7217CIPI
Common Anode	Decade/9999	CERDIP	ICM7227IJI
Common Cathode	Decade/9999	PLASTIC	ICM7227AIPI
Common Anode	Timer/5959	CERDIP	ICM7227BIJI
Common Cathode	Timer/5959	PLASTIC	ICM7227CIPI

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (common anode/Cerdip) ..... 1W Note 1
Power Dissipation (common cathode/Plastic) ... 0.5W Note 1
Supply Voltage $V^+ - V^-$ 6V
Input Voltage
(any terminal) ..... V^+ +0.3V, Ground -0.3V Note 2
Operating temperature range ..... -20°C to +85°C
Storage temperature range ..... -55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

OPERATING CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $T_A = 25°C$, Test Circuit, Display Diode Drop 1.7V, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply current (Lowest power mode)	I^+ (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 3)		350	500	µA
Supply current (Lowest power mode)	I^+ (7227)	Display off (Note 3)		300	500	µA
Supply current OPERATING	I_{OP}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver output current	I_{DIG}	Common anode, $V_{OUT} = V^+ - 2.0V$	140	200		mA peak
SEGment driver output current	I_{SEG}	Common anode, $V_{OUT} = +1.3V$	-25	-40		mA peak
Digit Driver output current	I_{DIG}	Common cathode, $V_{OUT} = +1.3V$	-75	-100		mA peak
SEGment driver output current	I_{SEG}	Common cathode $V_{OUT} = V^+ - 2V$	10	12.5		mA peak
$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	I_P	$V_{OUT} = V^+ - 2V$ (See Note 3)	5	25		µA
3 level input impedance	Z_{IN}			100		kΩ
BCD I/O input high voltage	V_{BIH}	ICM7217 common anode (Note 4) ($V^+ = 5.0V$)	1.3			V
		ICM7217 common cathode (Note 4)	$V^+ - 0.6$			V
		ICM7227 with 50pF effective load	3			V
BCD I/O input low voltage	V_{BIL}	ICM7217 common anode (Note 4) ($V^+ = 5.0V$)			0.8	V
		ICM7217 common cathode (Note 4)			$V^+ - 1.8$	V
		ICM7227 with 50pF effective load			1.5	V
BCD I/O input pullup current	I_{BPU}	ICM7217 common cathode $V_{IN} = V^+ - 2V$ (Note 3)	5	25		µA
BCD I/O input pulldown current	I_{BPD}	ICM7217 common anode $V_{IN} = +1.3V$ (Note 3)	5	25		µA
BCD I/O, CARRY/BORROW, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high current	I_{BOH}	$V_{OH} = V^+ - 1.5V$	100			µA
BCD I/O, CARRY/BORROW, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low current	I_{BOL}	$V_{OL} = +0.4V$	-2			mA
Count input frequency (Guaranteed)	f_{in}	$V^+ = 5V \pm 10\%$, $-20°C < T_A < +70°C$	0	5	2	MHz
Count input threshold	V_{TH}	$V^+ = 5V$		2		V
Count input hysteresis	V_{HYS}	$V^+ = 5V$		0.5		V
Display scan oscillator frequency	f_{ds}	Free-running (SCAN terminal open circuit)		2.5		kHz
Operating Temperature Range	T_A	Industrial temperature range	-20		+85	°C

NOTE 1 These limits refer to the package and will not be obtained during normal operation.

NOTE 2 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

NOTE 3 In the ICM7217 the UP/$\overline{DOWN}$, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 µA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.

NOTE 4 These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.

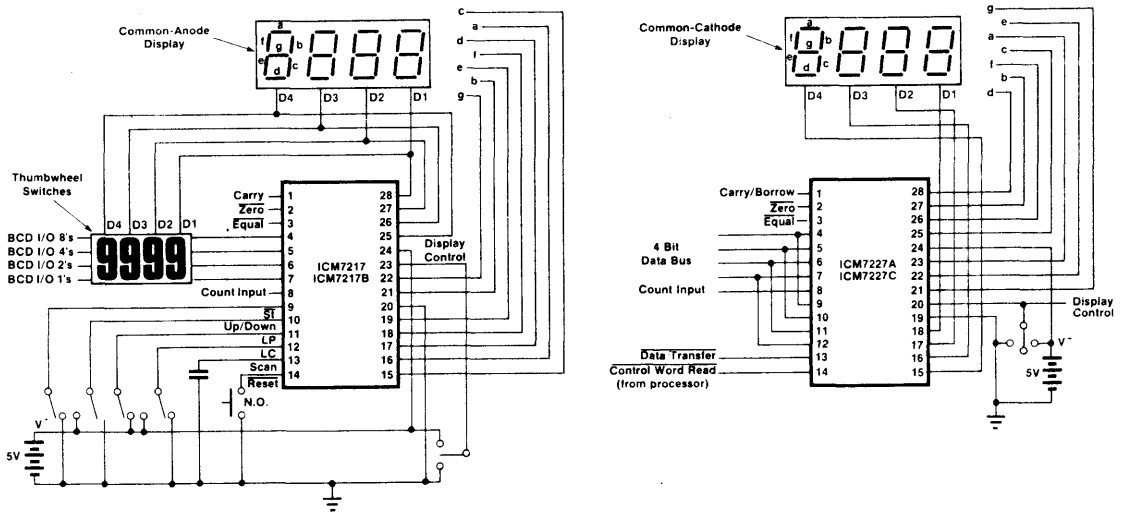


Figure 1: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

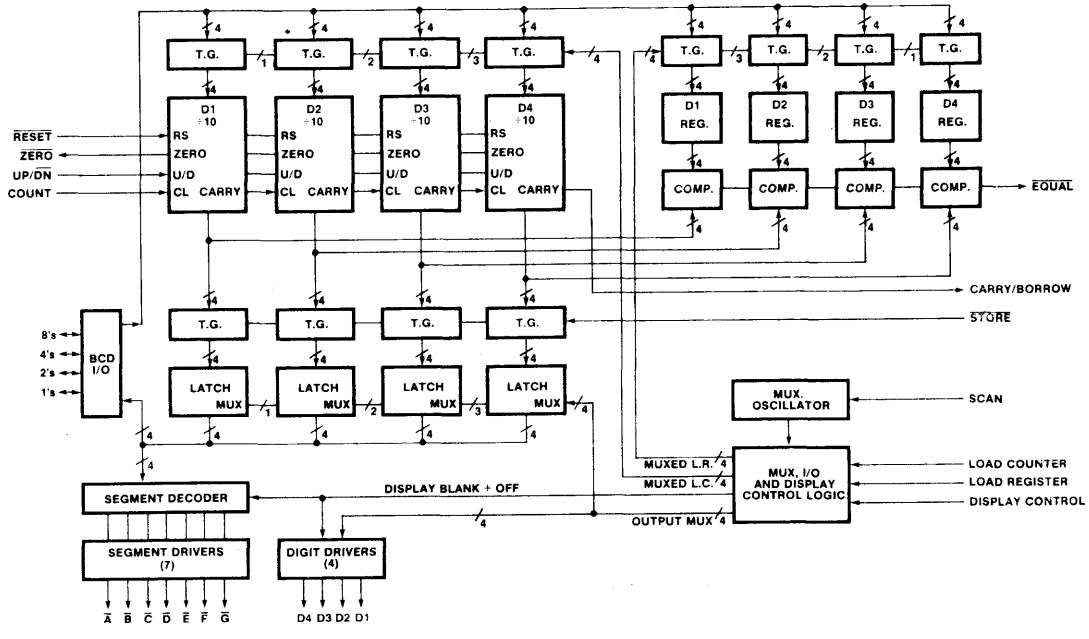


Figure 2: ICM7217 Functional Block Diagram

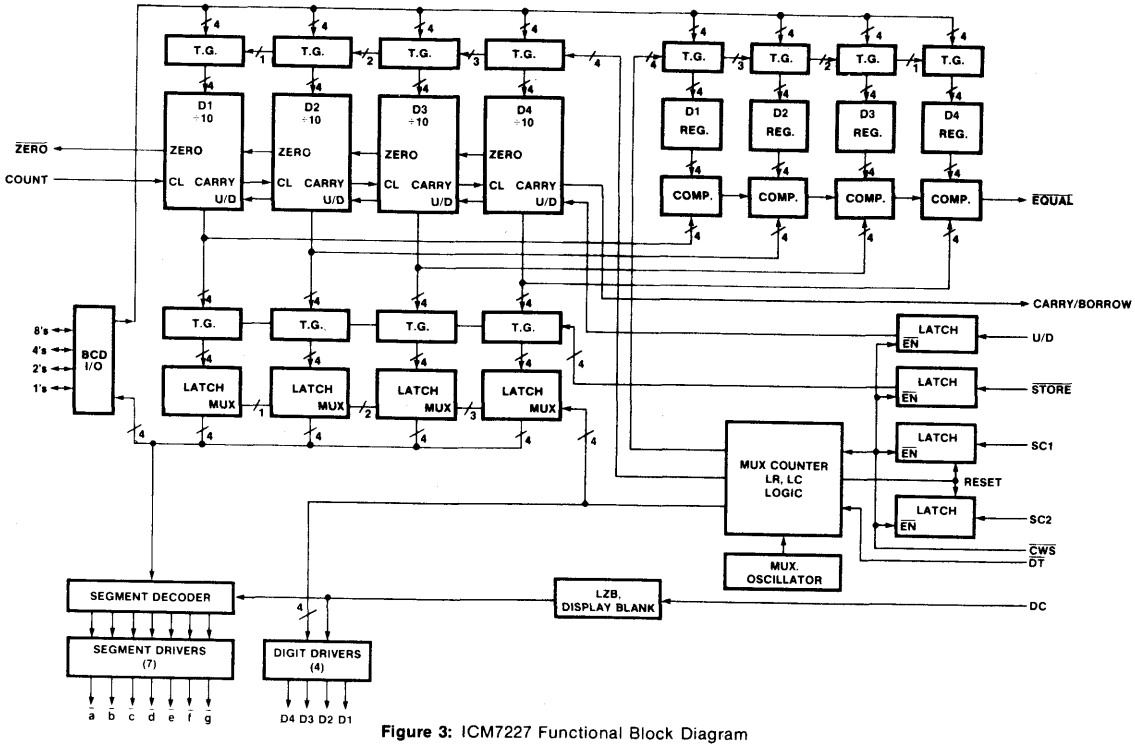


Figure 3: ICM7227 Functional Block Diagram

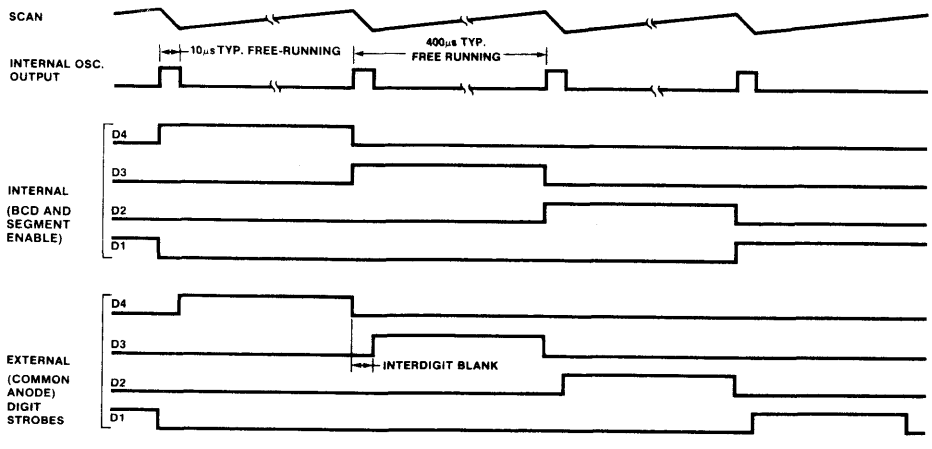


Figure 4: Multiplex Timing

DESCRIPTION OF OPERATION

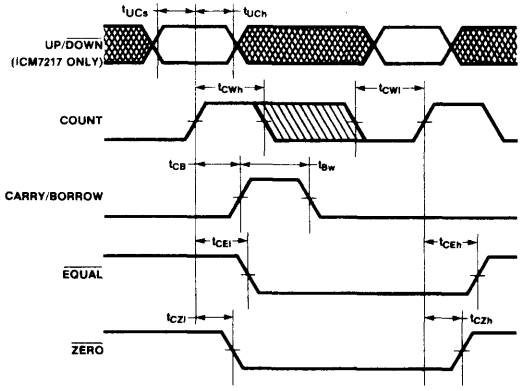
OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 2mA @ 0.4V (on resistance 200 ohms), and for a logic one, the outputs will source >60μA. A 10kΩ pull-up resistor to V+ on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.



SYMBOL	DESCRIPTION	MUX	TYP	MAX	UNITS
t_{UCs}	UP/$\overline{DOWN}$ setup time (min)		300		
t_{UCh}	UP/$\overline{DOWN}$ hold time (min)		0		
t_{CUh}	COUNT pulse high (min)		100	250	ns
t_{CUl}	COUNT pulse low (min)		100	250	
t_{CB}	COUNT to CARRY/BORROW delay		750		
t_{Bw}	CARRY/BORROW pulse width		100		
t_{CEl}	COUNT to $\overline{EQUAL}$ delay		500		
t_{CZl}	COUNT to $\overline{ZERO}$ delay		300		

Figure 5: ICM7217/27 COUNT and Output Timing

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 4 shows the multiplex timing, while Figure 5 shows the Output Timing. Figures 6 through 9 show the output characteristics of the Digit and SEGment drivers. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V^+); this corresponds to normal operation. When this pin is connected to V^+, the segments are inhibited, and when connected to V^-, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 1.

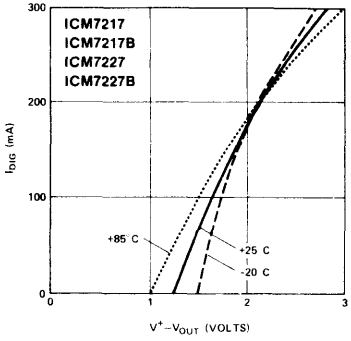
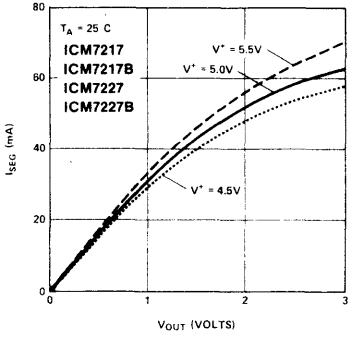


Figure 6: Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ \leq 6.0V$



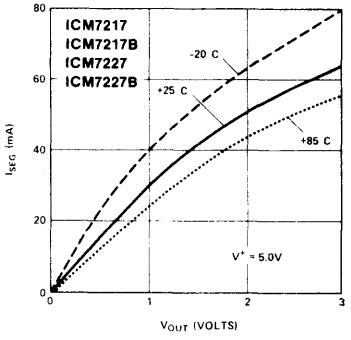
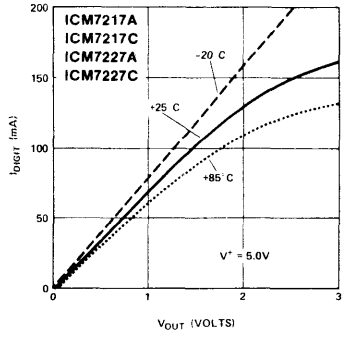


Figure 7: Typical I_{SEG} vs. V_{OUT}



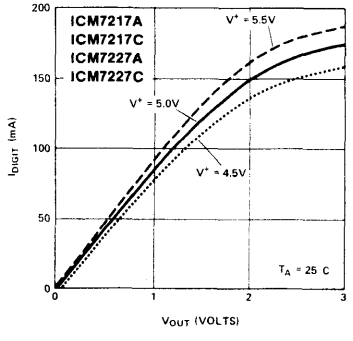


Figure 8: Typical I_{DIGIT} vs. V_{OUT}

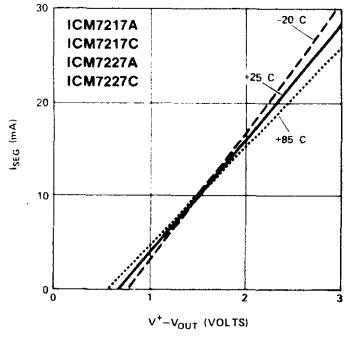


Figure 9: Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5 \leq V^+ - V^- \leq 6.0V$

CONTROL OF ICM7217

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for ICM7217 versions) are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplex Rate Control

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time (4 digits)
None	2.5 kHz	625 Hz	1.6 ms
20 pF	1.25 kHz	300 Hz	3.2 ms
90 pF	600 Hz	150 Hz	8 ms

During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 10 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

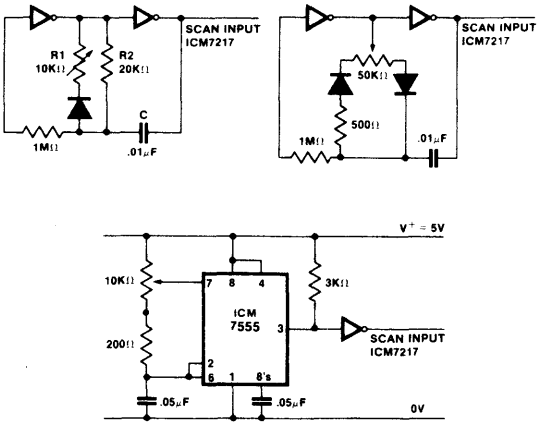


Figure 10: Brightness Control Circuits

Counting Control

As shown in Figure 5, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pullup resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately 1/2 V^+ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V^+, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V^+, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V^+, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 11). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD

I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 12). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Fig. 12. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

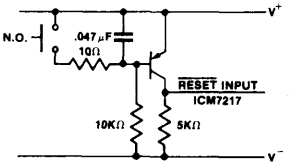
Output and Input Restrictions

The CARRY/BORROW output is not valid during load counter and reset operations.

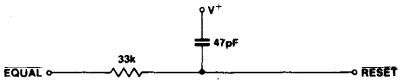
The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below.



When using the circuit as a programmable divider(÷ by n with equal outputs) a short time delay (about 1μs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration.



When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

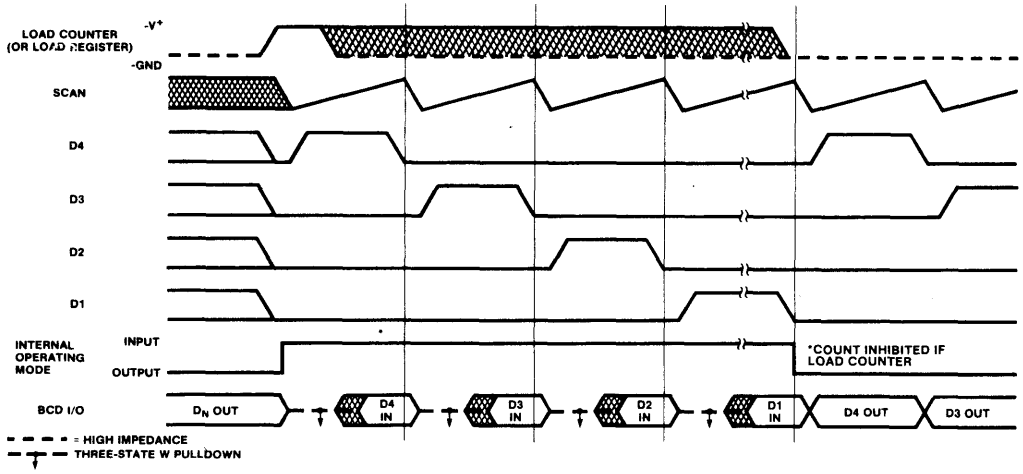
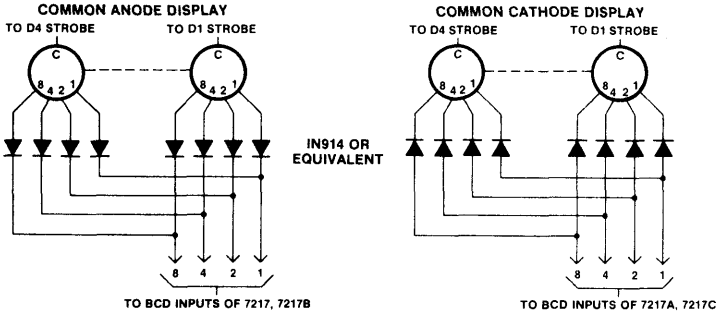


Figure 11: ICM7217 BCD I/O and LOADING TIMING



Note: If the BCD pins are to be used for outputs a 10kΩ resistor should be placed in series with each digit line to avoid loading problems through the switches.

Figure 12: Thumbwheel switch/diode connections

Table 2: Control Input Definitions ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{STORE}}$	9	V^+ (or floating) Ground	Output latches not updated Output latches updated
UP/$\overline{\text{DOWN}}$	10	V^+ (or floating) Ground	Counter counts up Counter counts down
$\overline{\text{RESET}}$	14	V^+ (or floating) Ground	Normal Operation Counter Reset
LOAD COUNTER/ $\overline{\text{I/O OFF}}$	12	Unconnected V^+ Ground	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ $\overline{\text{OFF}}$	11	Unconnected V^+ Ground	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ Ground	Normal operation Segment drivers disabled Leading zero blanking inhibited

Table 3: Control Input Definitions ICM7227

INPUT		TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{DATA TRANSFER}}$		13	V^+ Ground	Normal Operation Causes transfer of data as directed by select code
Control Word Port	STORE	9	V^+ (During $\overline{\text{CWS}}$ Pulse) Ground	Output latches updated Output latches not updated
,,	UP/$\overline{\text{DOWN}}$	10	V^+ (During $\overline{\text{CWS}}$ Pulse) Ground	Counter counts up Counter counts down
,, ,,	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V^+ = "1" Ground = "0"	SC1, SC2 control:– 00 Change store and up/$\overline{\text{down}}$ latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
$\overline{\text{Control Word Strobe}}$ ($\overline{\text{CWS}}$)		14	V^+ Ground	Normal operation Causes control word to be written into control latches
DISPLAY CONTrol (DC)		23 Common Anode 20 Common Cathode	Unconnected V^+ Ground	Normal operation Display drivers disabled Leading zero blanking inhibited

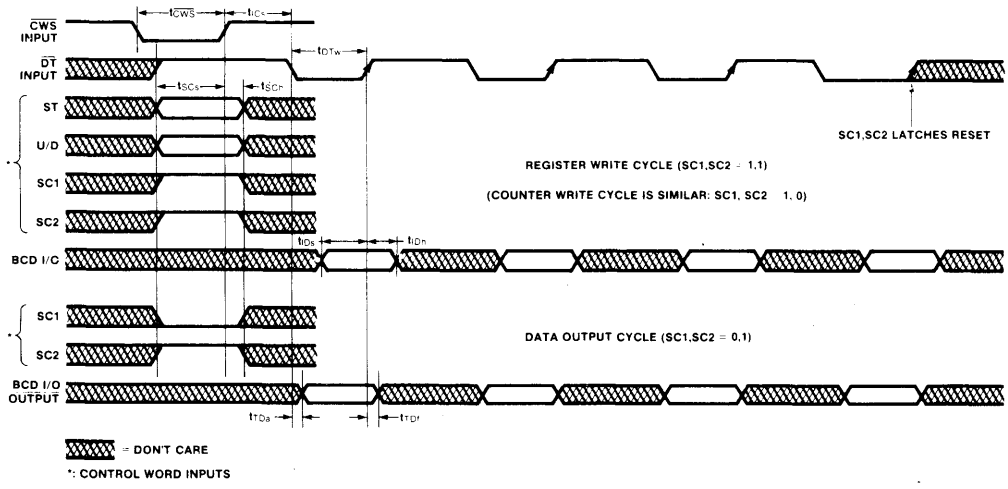


Figure 13: ICM7227 I/O Timing (see Table 4)

CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/$\overline{\text{DOWN}}$, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a **data transfer** operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DATA TRANSFER}}$ pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Fig. 13 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{\overline{CWS}}$	Control Word Strobe Width (min)		275		ns
t_{ICS}	Internal Control Set-up (min)		2.5	3	µs
$t_{\overline{DT}W}$	DATA TRANSFER pulse width (min)		300		ns
t_{SCS}	Control to Strobe setup (min)		300		ns
t_{SCH}	Control to Strobe hold (min)		300		ns
t_{IDS}	Input Data setup (min)		300		ns
t_{IDH}	Input Data hold (min)		300		ns
t_{TDACC}	Output Data access		300		ns
t_{TDF}	Output Transfer to Data float		300		ns

APPLICATIONS

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V^+.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Figure 9 for a similarly operating multi-digit connection.

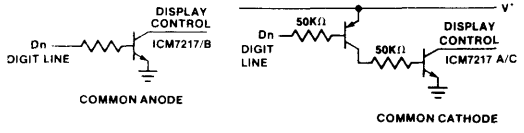


Figure 14: Forcing Leading Zero Display

DRIVING LARGER DISPLAYS

For displays requiring more current than the ICL7217/7227 can provide, the circuits of Figure 15 can be used.

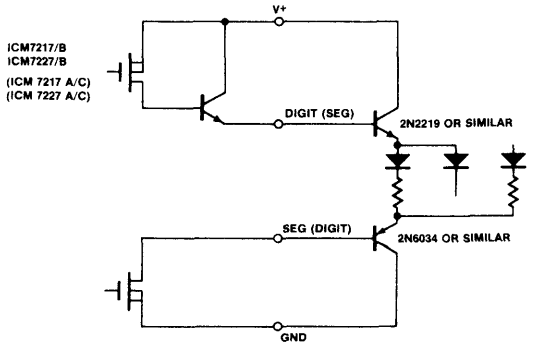


Figure 15: Driving High Current Displays

LCD DISPLAY INTERFACE (Figure 16)

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10—20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

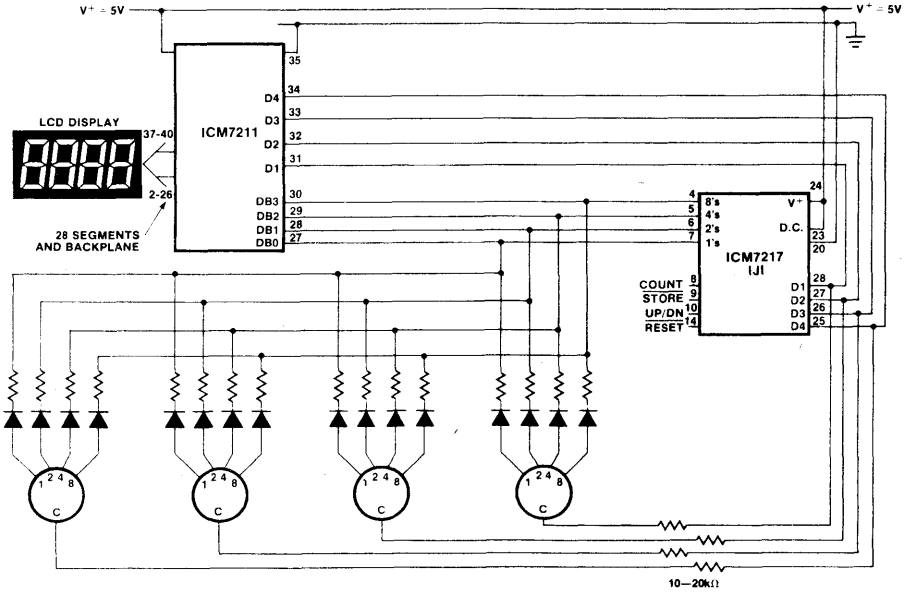


Figure 16: LCD Display Interface (with Thumbwheel Switches)

UNIT COUNTER WITH BCD OUTPUT (Figure 17)

The simplest application of the ICM7217 is a 4 digit unit counter. All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A and a common-cathode calculator-type display, results in the least expensive digital counter/display system available.

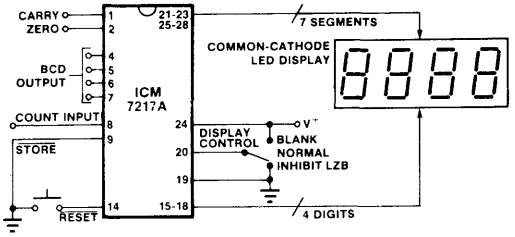
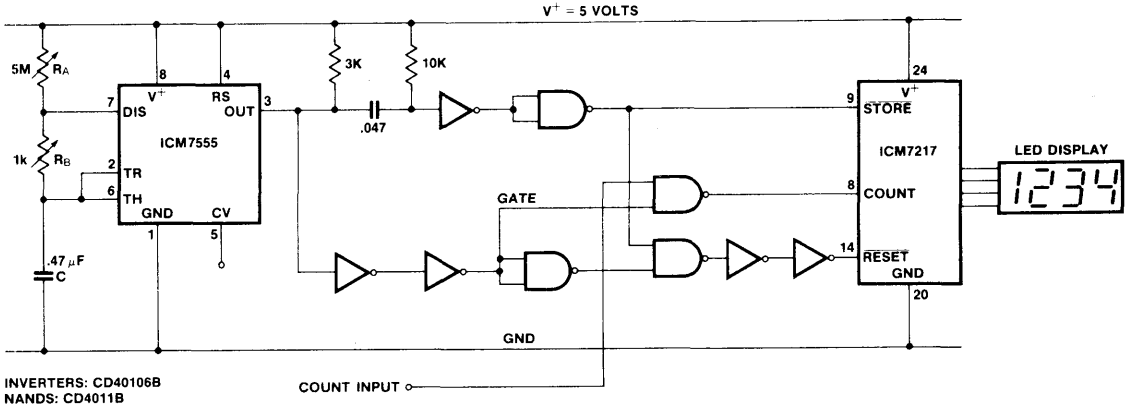


Figure 17: Unit Counter

INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER (Figure 18)

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300-500μs. The positive waveform time is given by $t_{wp} = 0.693 (R_A + R_B) C$ while the negative waveform is given by $t_{wn} = 0.693 R_B C$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1k potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.



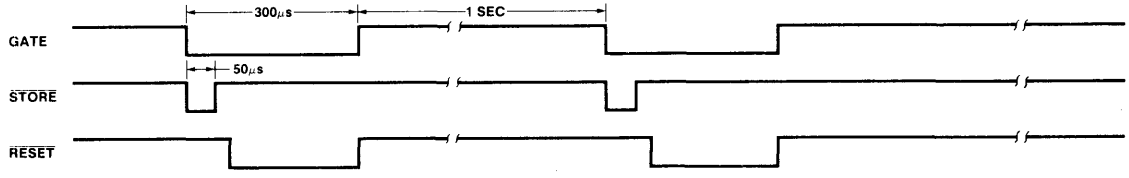


Figure 18: Inexpensive Frequency Counter

TAPE RECORDER POSITION INDICATOR/ CONTROLLER (Figure 19)

This circuit shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047 μF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

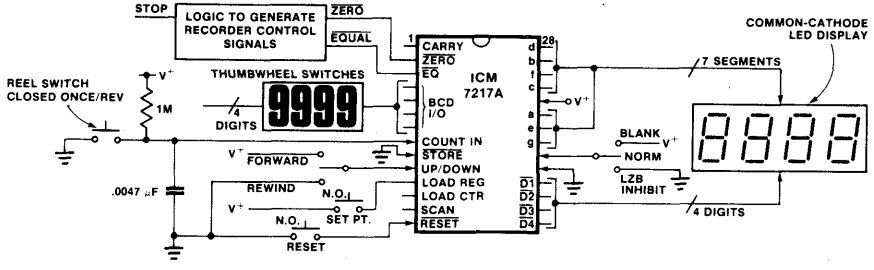


Figure 19: Recorder Indicator

PRECISION ELAPSED TIME/COUNTDOWN TIMER (Figure 20)

This circuit uses an ICM7213 precision one minute/one second timebase generator using a 4.1943 MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used. This technique may be used on any 3-level input. The 100k pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 18 to generate a 1Hz reference.

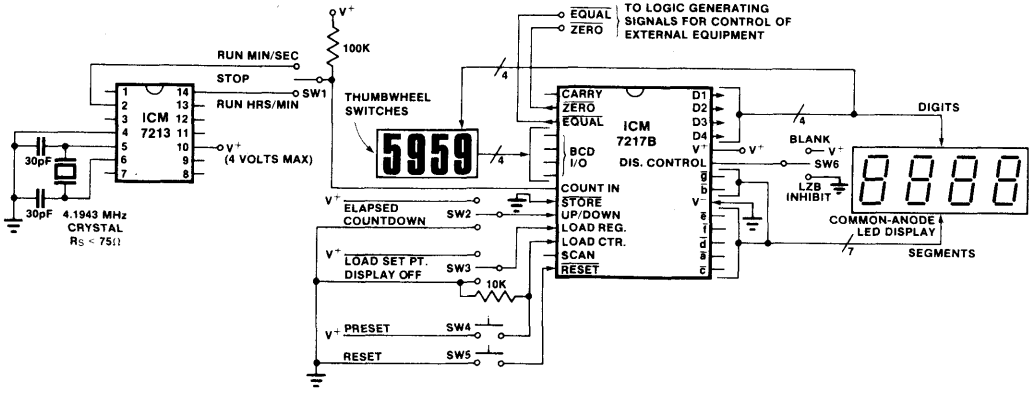


Figure 20: Precision Timer

MICROPROCESSOR INTERFACE-ICM7227
(Figure 21)

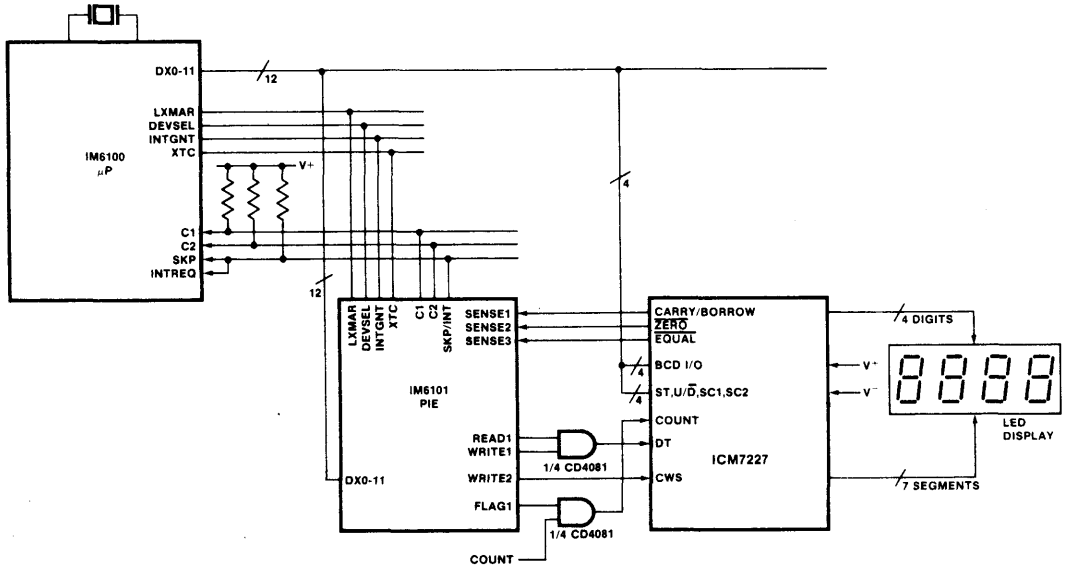


Figure 21: IM6100

This circuit shows the hardware necessary to interface the ICM7227 to an Intersil IM6100 CMOS microprocessor. Using an IM6101 Parallel Interface Element (PIE) allows the addition of one or more ICM7227 devices as generalized peripherals to any IM6100 system, using a *minimum* of external components.

A similar configuration may be used with the MC6800 using the corresponding PIE, while an 8255 can be used to interface 8080 based systems.

The ICM7227 can perform many "accessory" functions that are inefficient or impossible for the processor to perform. For example, by adding a timebase such as an ICM7213, and using an ICM7227C or D, an inexpensive real-time clock/display, directly accessible by the processor, can be constructed.

8-DIGIT UP/DOWN COUNTER (Figure 22)

This circuit shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\bar{a}$ or $\bar{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

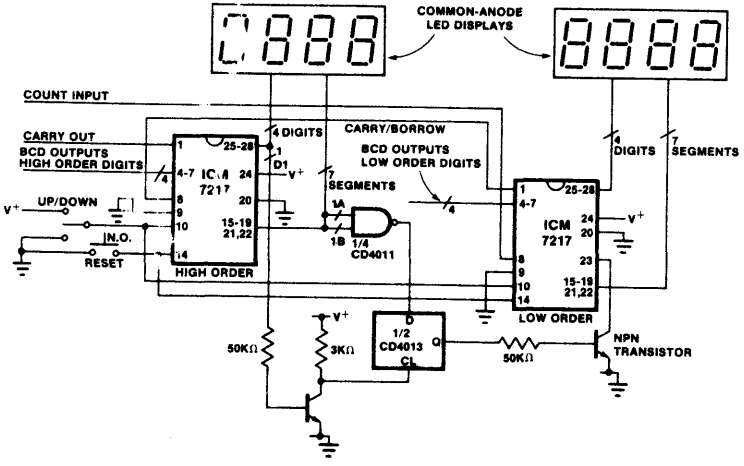


Figure 22: 8 Digit Up/Down Counter

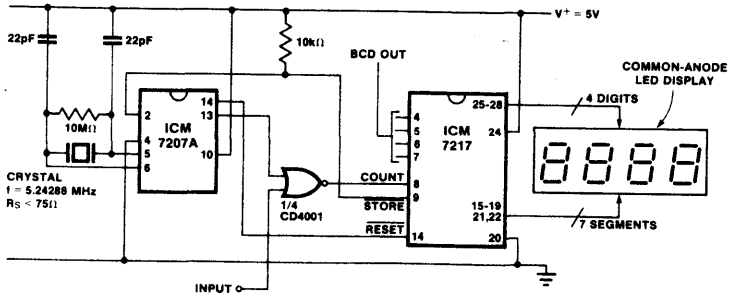


Figure 23: Precision Frequency Counter (~1MHz Maximum)

PRECISION FREQUENCY COUNTER/ TACHOMETER (Figure 23)

This circuit is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{STORE}$ and $\overline{RESET}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V^+, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536 MHz crystal), giving a 0.01 second gating with Pin 11 connected to V^+, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the $\overline{EQUAL}$ and $\overline{ZERO}$ outputs, to count in SYNC with an ICL7109 A/D Converter. By $\overline{RESET}$ing the ICM7217 on a "tare" value conversion, and $\overline{STORE}$-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7019 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.

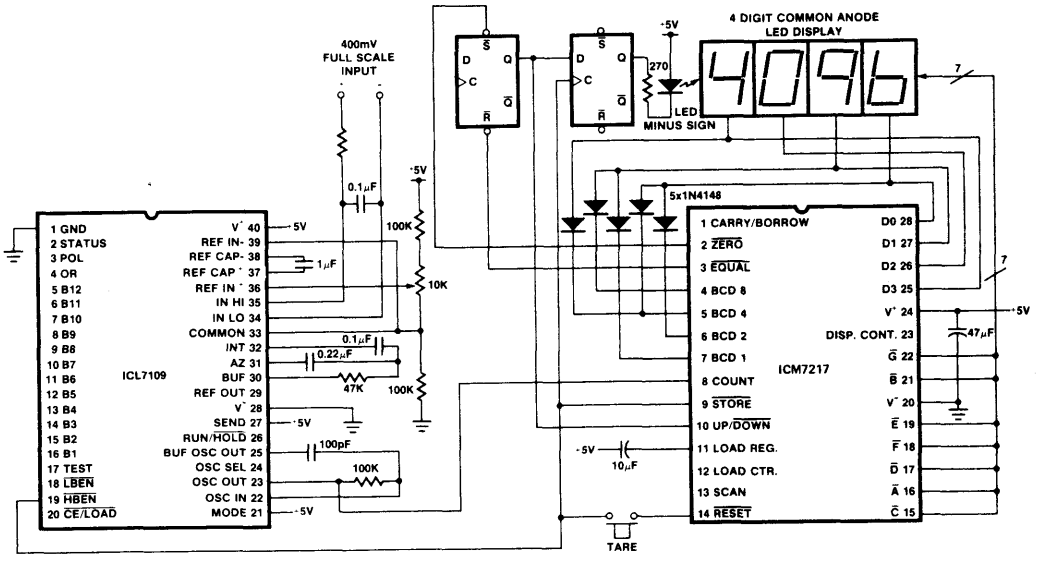
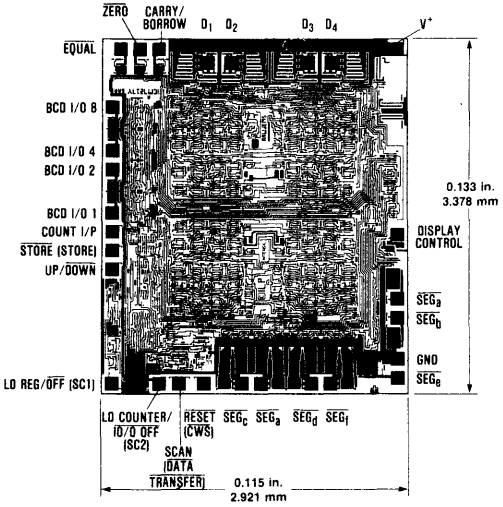
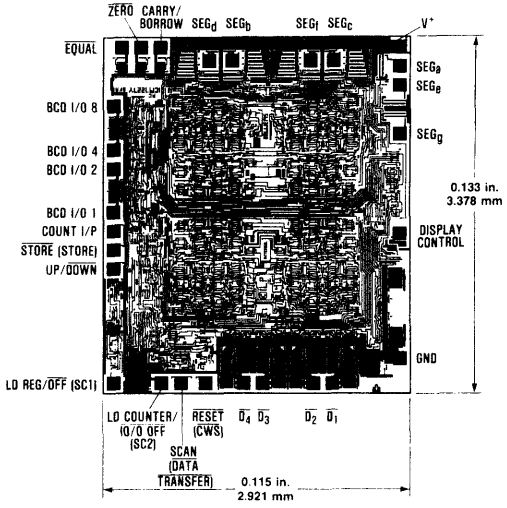


Figure 24: Auto-Tare System for A/D Converter

CHIP TOPOGRAPHY



ICM7217/B (ICM7227/B)



ICM7217A/C (ICM7227A/C)

6

ICM7218 Series
CMOS Universal 8 Digit LED Driver System

FEATURES

- **Total circuit integration on chip includes:**
  - **a) Digit and segment drivers**
  - **b) All multiplex scan circuitry**
  - **c) 8X8 static memory**
  - **d) 7 segment Hexadecimal and Code B decoders**
- **Output drive suitable for large LED displays**
- **Both common anode and common cathode LED drive versions**
- **Single 5 volt supply required**
- **Data retention to 2 volts supply**
- **Shutdown feature - turns off display and puts chip into very low power dissipation mode**
- **Pin selectable choice of 2 seven segment decoders - Hexa or Code B - or no decode**
- **Microprocessor compatible**
- **Serial and random access versions**
- **Decimal point drive on each digit**

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems and an LED display. Included on chip is an 8x8 static memory array providing storage for the displayed information, 2 types of 7 segment decoders, all the multiplex scan circuitry and the high power digit and segment drivers.

The ICM7218A and ICM7218B are intended to be used primarily in microprocessor systems. Data is read directly from the I/O bus line from the microprocessor. 2 Control lines ($\overline{\text{Write}}$, and Mode) define chip select, which reads either 4 bits of control information (Data Coming, $\overline{\text{Shutdown}}$, Decode, Hexa or Code B Decoding) or 8 bits of Display Input Data. Display Input Data (8 words, 8 bits each) is automatically sequenced into the memory on successive positive going $\overline{\text{Write}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218A drives a common anode display while the ICM7218B drives a common cathode display. (See Block Diagram 1)

The ICM7218C and ICM7218D feature 2 lines for control information ($\overline{\text{Write}}$, Three Level Input; Hexa, Code B, $\overline{\text{Shutdown}}$), 4 lines for Input Data and 3 lines for Data Addressing of each of eight data memory locations.

Data is written into memory by setting up a Data Address memory location, defining 4 lines of Input Data and then strobe the $\overline{\text{Write}}$ line low. The Three Level Control Input is independent of the $\overline{\text{Write}}$ instruction. Only Hexadecimal and Code B decoding are available for the Display Outputs. The ICM7218C drives a common anode display, the ICM7218D a common cathode display. (See Block Diagram 2)

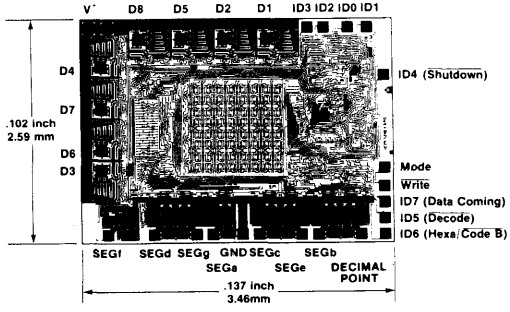
The ICM7218E provides 4 separate lines for control information ($\overline{\text{Write}}$, Hexa-Code B, Decode, $\overline{\text{Shutdown}}$), 8 lines for input data, and 3 lines for digit address. Data is written into the memory by setting up a Data Address memory location, defining 8 lines of Input Data, and then strobe the $\overline{\text{Write}}$ line low. Control information is on separate lines and is independent of the $\overline{\text{Write}}$ instruction. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218E drives a common anode display. (See Block Diagram 3)

6

ORDERING INFORMATION

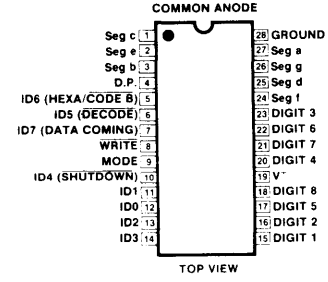
Typical App.	Order Part Number	Display Option	Package
Serial Access	ICM7218A IJI	Common Anode	28 Lead CERDIP
	ICM7218B IPI	Common Cathode	28 Lead Plastic
Random Access	ICM7218C IJI	Common Anode	28 Lead CERDIP
	ICM7218D IPI	Common Cathode	28 Lead Plastic
	ICM7218E IDL	Common Anode	40 Lead Ceramic

CHIP TOPOGRAPHY ICM7218A



PIN CONFIGURATION (OUTLINE DRAWING JI)

ICM7218A



Note: Pins 5, 6, 7, 10 are under control of Mode pin 9. See page 6-60.

See page 6-57 for other device configurations.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 300mA
Segment Output Current 50mA
Input Voltage (any terminal) ..... V^+ +0.3V to V^- −0.3V NOTE 1
Power Dissipation (28 Pin CERDIP) ..... 1 W NOTE 2
Power Dissipation (28 Pin Plastic) ..... 0.5 W NOTE 2
Power Dissipation (40 Pin Ceramic) ..... 1 W NOTE 2
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

SYSTEM ELECTRICAL CHARACTERISTICS

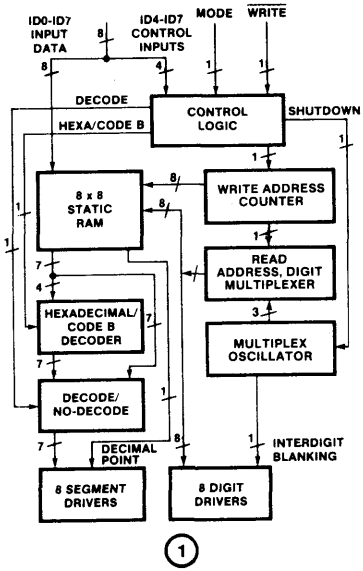
V^+ = 5V ±10%; T_A = 25°C, Test Circuit, Display Diode Drop 1.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+		4		6	V
		Power Down Mode	2		6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	µA
Operating Supply Current	I_{OP}	Decoder On, Outputs Open Ckt	250		950	µA
		No Decode, Outputs Open Ckt	200		450	µA
Digit Drive Current	I_{DIG}	Common Anode Vout = V^+ −2.0	−170			mA
		Common Cathode Vout = V^- +1V	50			mA
Digit Leakage Current	I_{DLK}				100	µA
Peak Segment Drive Current	I_{SEG}	Common Anode Vout = V^- +1.5V	20	25		mA
		Common Cathode Vout = V^+ −2.0V	−10			mA
Segment Leakage Current	I_{SLK}				50	µA
Display Scan Rate	f_{MUX}	Per Digit		250		Hz
Three Level Input						
Logical "1" Input Voltage	V_{INH}	Hexidecimal ICM7218C, D (Pin 9)	4.0			V
Floating Input	V_{INF}	Code B ICM7218C, D (Pin 9)	2.0		3.0	V
Logical "0" Input Voltage	V_{INL}	Shutdown ICM7218C, D (Pin 9)			1.75	V
Three Level Input Impedance	Z_{IN}	Note 3		100		kΩ
Logical "1" Input Voltage	V_{IH}		3.5			V
Logical "0" Input Voltage	V_{IL}				.8	V
Write Pulse Width (Negative)	tw	7218A, B	550	400		ns
Write Pulse Width (Positive)	$t\overline{w}$	7218A, B	550	400		ns
Write Pulse Width (Negative)	tw	7218C, D, E	400	250		ns
Write Pulse Width (Positive)	$t\overline{w}$	7218C, D, E	400	250		ns
Mode Hold Time	t_{mh}	7218A,B		150		ns
Mode Pulse Width	tm	7218A, B	500			ns
Data Set Up Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		25			ns
Digit Address Set Up Time	t_{das}	ICM7218C, D, E	500			ns
Digit Address Hold Time	t_{dah}	ICM7218C, D, E	100			ns
Data Input Impedance	Z_{IN}	5-10 pF Gate Capacitance		10^{10}		Ohms

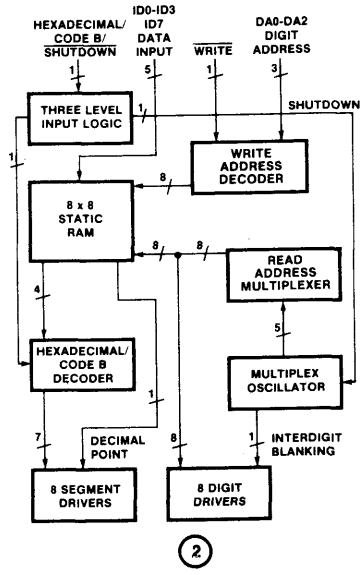
NOTE 3: In the ICM7218C and D (random access versions) the Hexa/Code B/$\overline{\text{Shutdown}}$ Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50µA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

BLOCK DIAGRAMS

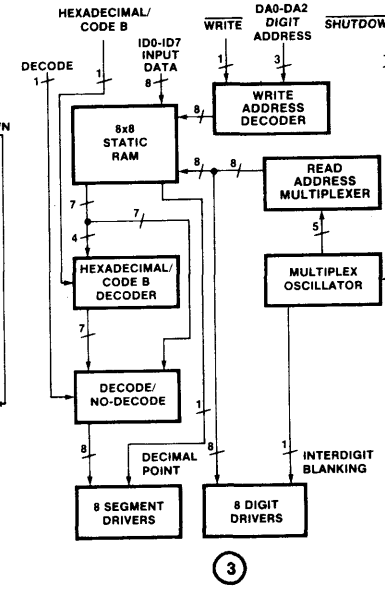
ICM7218A, ICM7218B



ICM7218C, ICM7218D

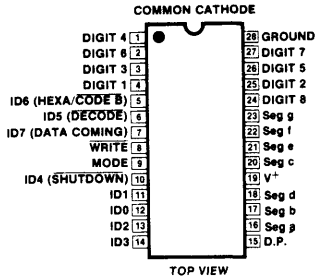


ICM7218E



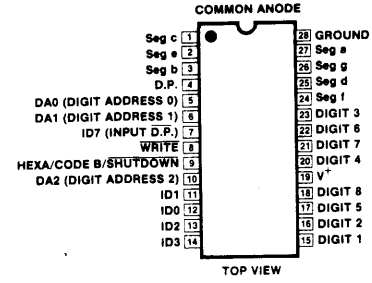
PIN CONFIGURATIONS (See page 6-65 for ICM7218A)

ICM7218B* (OUTLINE DRAWING PI)

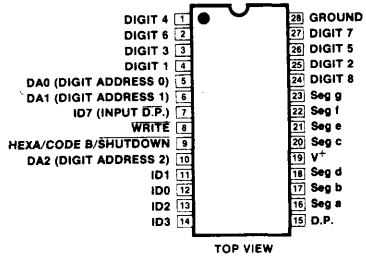


*Note: Pins 5, 6, 7, 10 are under control of Mode pin 9. See page 6-60.

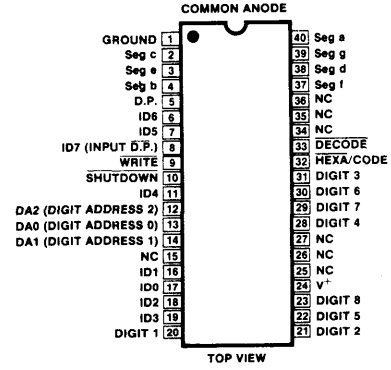
ICM7218C (OUTLINE DRAWING JI)



ICM7218D (OUTLINE DRAWING PI)



ICM7218E (OUTLINE DRAWING DL)



INPUT DEFINITIONS ICM7218A and B

INPUT		TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{WRITE}}$		8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
MODE		9	High Low	Load Control Word on Write Pulse Load Input Data on Write Pulse
ID4 $\overline{\text{SHUTDOWN}}$	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder, and Displays Disabled)
ID5 ($\overline{\text{DECODE}}$/No Decode)	MODE High	6	High Low	No Decode Decode
ID6 (HEXAdecimal/CODE B)	MODE High	5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING - Control Word)	MODE High	7	High Low	Data Coming No Data Coming } Control Word
Input Data ID0-ID7*	MODE Low	11,12,13, 14,5,6 10,7	High Low	Loads "One" (Note 2) Loads "Zero" (Note 2)

*ID0-ID3 = Don't care when writing control word
ID4-ID7 = Don't care when writing Hex/Code B
(The display blanks on ICM7218A/B versions when writing in Data)

INPUT DEFINITIONS ICM7218C and D

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{WRITE}}$	8	High Low	Inputs Not Loaded Into Memory Inputs Loaded Into Memory
Three Level Input (Note 1)	9	High Floating Low	Hexadecimal Decode Code B Decode Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address DA2 (MSB)-DA0 (LSB)	10,6,5	High Low	Loads "Ones" Loads "Zeros"
Input Data ID3 (MSB) - ID0 = Data ID7 = $\overline{\text{D.P.}}$	14,13,11,12 7	High Low	Loads "Ones" (Note 2) Loads "Zeros" (Note 2)

INPUT DEFINITIONS ICM7218E

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{WRITE}}$	9	High Low	Input Latches Not Updated Input Latches Updated
$\overline{\text{SHUTDOWN}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address (0,1,2) DA0-DA2	13,14,12	High Low	Loads "Ones" Loads "Zeros"
$\overline{\text{DECODE}}$/No Decode	33	High Low	No Decode Decode
$\overline{\text{HEX}}$Adecimal/CODE B	32	High Low	Code B Decoding Hexadecimal Decoding
Input Data ID0-ID7	16,17,18,19 6 7,11,8	High Low	Loads "Ones" (Note 2) Loads "Zeros" (Note 2)

NOTE 1 In the ICM7218C and ICM7218D versions, Hexadecimal, Code B and Shutdown are controlled with a three level input on Pin 9. Pulling Pin 9 high decodes Hexadecimal. Floating Pin 9 decodes Code B and pulling Pin 9 low puts the ICM7218 in a Shutdown mode.

NOTE 2 In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents "on" segments, (i.e. segments are positive true, decimal point is negative true).

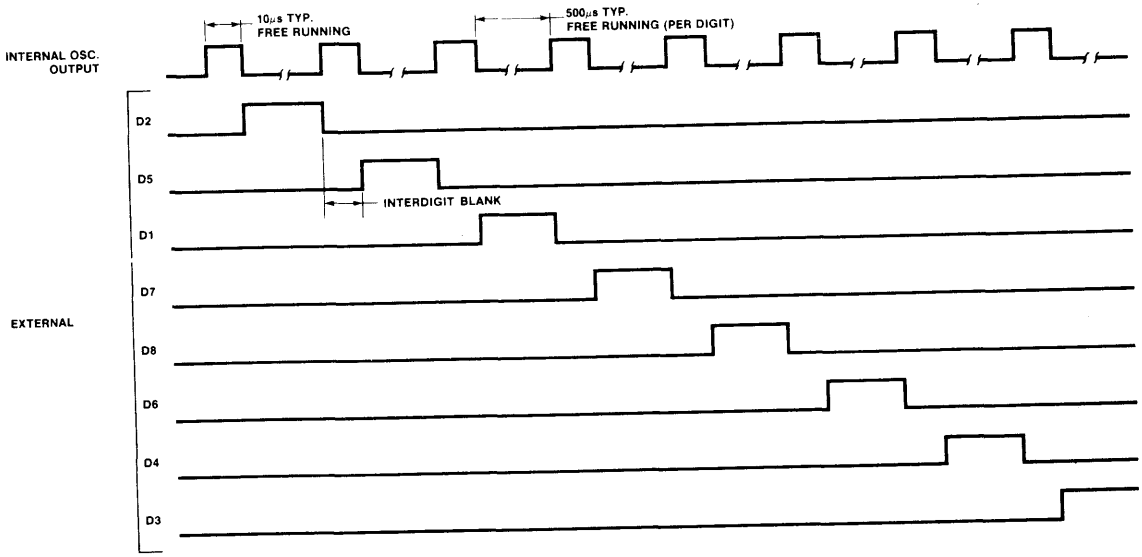


Figure 1: Multiplex Timing

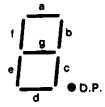


Figure 2: Segment Assignments

DECODE/No Decode

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or 2 Binary codes plus decimal point (5 bits per digit). The 7 segment decoder on chip may be disabled if direct segment information is inputted.

In the No Decode format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: $\overline{D.P.}$ a b c e g f d

In this format, "Ones" represents on segments for all inputs except for the Decimal Point, where "zero' represents on segments.

HEXAdecimal or CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (—), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Binary Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexa Code	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
Code B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(Blank)

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically 10μA at $V^+ = 5$), turns off both the digit and segment drivers, stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown - only the output and read sections of the device are disabled.

6

Powerdown

In a Shutdown Mode, the supply voltage may be reduced to 2 volts without data being lost in memory. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With 5 segments being driven, this is equal to about 40mA per segment peak drive or 5mA average drive. The common cathode drive is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes to ensure that segment information is correct before the next digit drive thereby avoiding ghosting.

Leading Zero Blanking

This may be programmed into chip memory in the no-decode operation (each segment programmed for a zero for the blanked digits) or by using the 16th state (binary 15) with the Code B decoder.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to parallel connect digit drives together. For example, by paralleling pairs of digit drives together to drive a 4 digit display 10 mA average segment drive can be obtained.

APPLICATIONS, continued

Power Dissipation Considerations

Assuming common anode drive at $V^{+} = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will, therefore, be 640mW rising to about 900mW for all '8"s displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Serial Input Drive Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and $\overline{\text{WRITE}}$ low. The instructions occur on 4 lines and are - Decode/no Decode, type of Decode (if desired), $\overline{\text{SHUTDOWN}}$/no Shutdown and DATA COMING/not Coming. After the control instructions have been read (with Data Coming instruction) display data can be written into memory with each following negative going pulse of $\overline{\text{WRITE}}$, MODE being low. After all 8 words or digit memory locations have been written, additional transitions of the state of $\overline{\text{WRITE}}$ are ignored. It is not possible to change one individual digit without refreshing the data for all the other digits. (This can, however, be achieved with the ICM7218C/D/E where the digits are individually addressed.)

Random Access Input Drive Considerations (ICM7218C/D/E)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{WRITE}}$ pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs (which define the digit where the data is to be written into the memory) and apply a negative going WRITE pulse. For example, it is possible to change only digit 7 without refreshing the data for all the other digits. (However, this cannot be achieved with the ICM7218A/B.)

Supply Capacitor

A 0.1μF capacitor is recommended between V^{+} and GROUND to bypass multiplex noise.

SWITCHING WAVEFORMS ICM7218

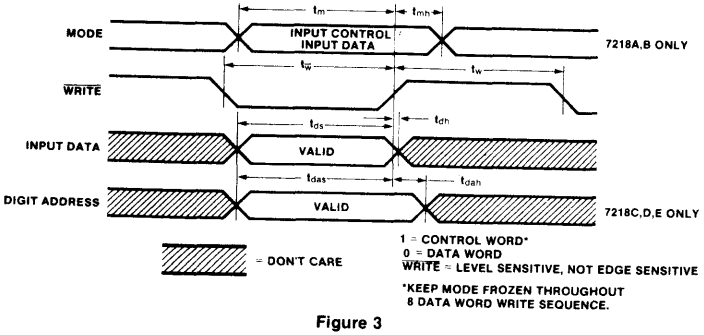


Figure 3

CHIP ADDRESS SEQUENCE ICM7218A and B

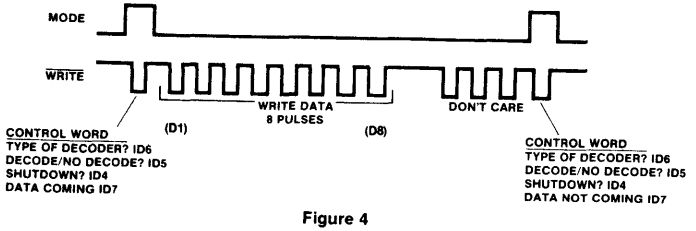


Figure 4

CHIP ADDRESS SEQUENCE EXAMPLE ICM7218C/D/E

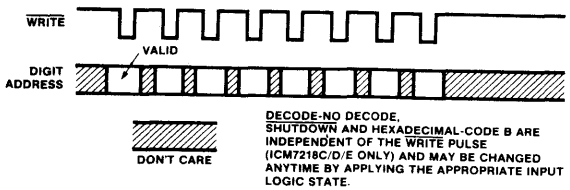
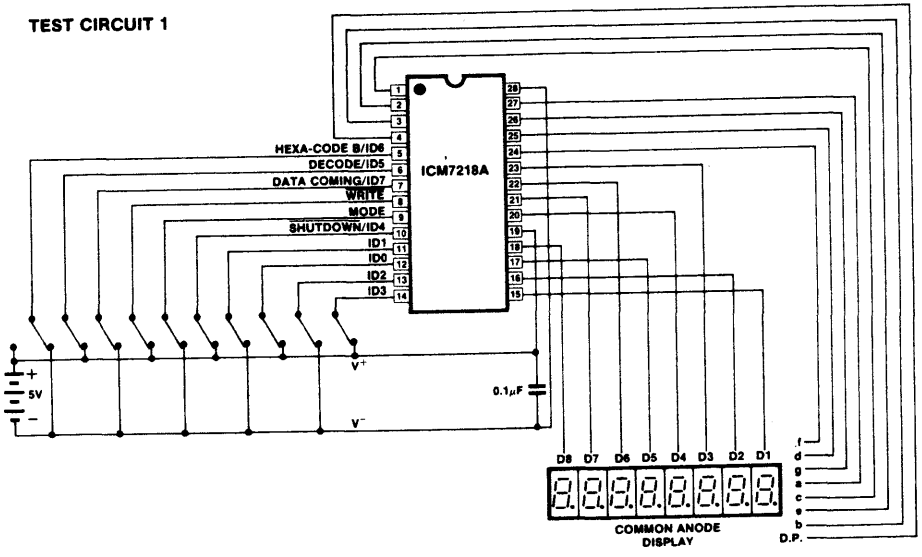


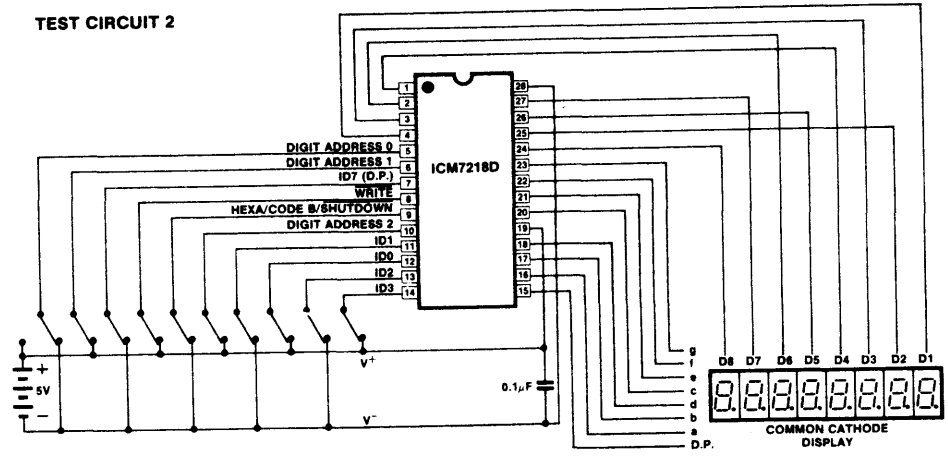
Figure 5

TEST CIRCUITS

TEST CIRCUIT 1

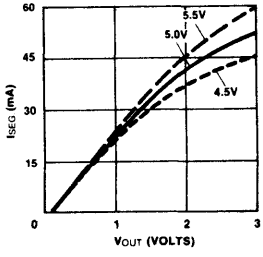


TEST CIRCUIT 2

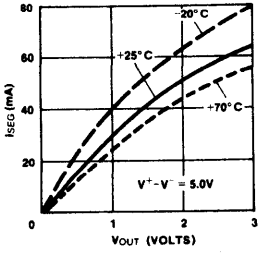


TYPICAL CHARACTERISTICS

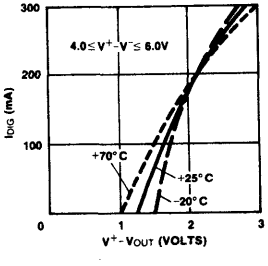
COMMON ANODE SEG. DRIVER
ISEG vs. VOUT
AT 25°C



COMMON ANODE SEG. DRIVER
ISEG. vs. VOUT

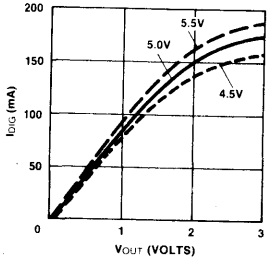


COMMON ANODE DIGIT DRIVER
IDIG vs. (V+-VOUT)

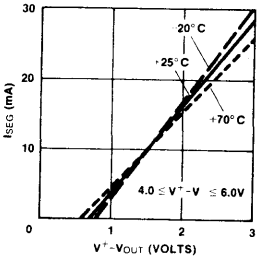


TYPICAL CHARACTERISTICS, CONTINUED

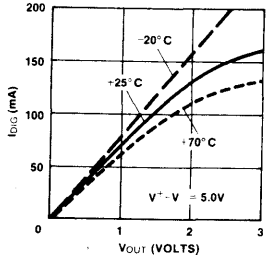
COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT} AT 25°C



COMMON CATHODE SEG. DRIVER
I_{SEG} vs. $(V^+ - V_{OUT})$



COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}



APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

The display interface (ICM7218) is shown with an MCS-48 family microprocessor. The 8 bit data bus DB0/DB7-ID0/ID7 transfers control and data information to the 7218 display interface on successive $\overline{WRITE}$ pulses. When MODE is high a control word is transferred. MODE low allows data transfer on a $\overline{WRITE}$ pulse. Eight memory address locations in the 8 x 8 static memory are automatically sequenced on each successive $\overline{WRITE}$ pulse. After eight $\overline{WRITE}$ pulses have occurred, further pulses are ignored and the display interface returns to normal display operation until a new control word is transferred. See Figure 4. This also allows writing to other peripheral devices without disturbing the ICM7218 A/B.

Decoding of the stored data in memory is defined by the control word and may be decoded in Hexadecimal, Code B, or No-Decode formats.

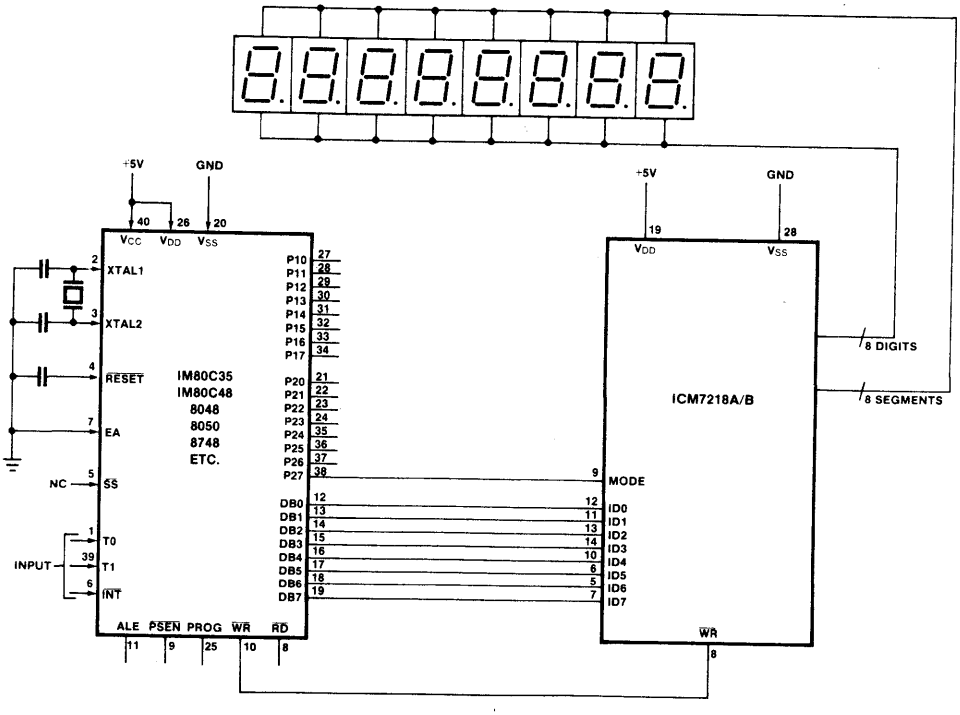


Figure 6: 8 Digit Microprocessor Display

16 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the MCS-48 I/O bus (DB7-DB0) is transferred to both ICM7218 (ID3-ID0) simultaneously, 4 bits + 4 bits on $\overline{\text{WRITE}}$ enable.

Display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded sequentially on a single 8 bit data bus, ie D0 D1, D2 D3, D4 D5, etc..

Decimal point information (from the processor, P26-P27) is supplied to the ICM7218 on bus lines ID7 to both devices.

Choice of decoding is available in either Hexadecimal or Code-B format by hardwiring or decoding to a Three Level format on Pin 9 of the ICM7218.

Multiplexing is asynchronous with respect to the microprocessor and is completely performed by the ICM7218.

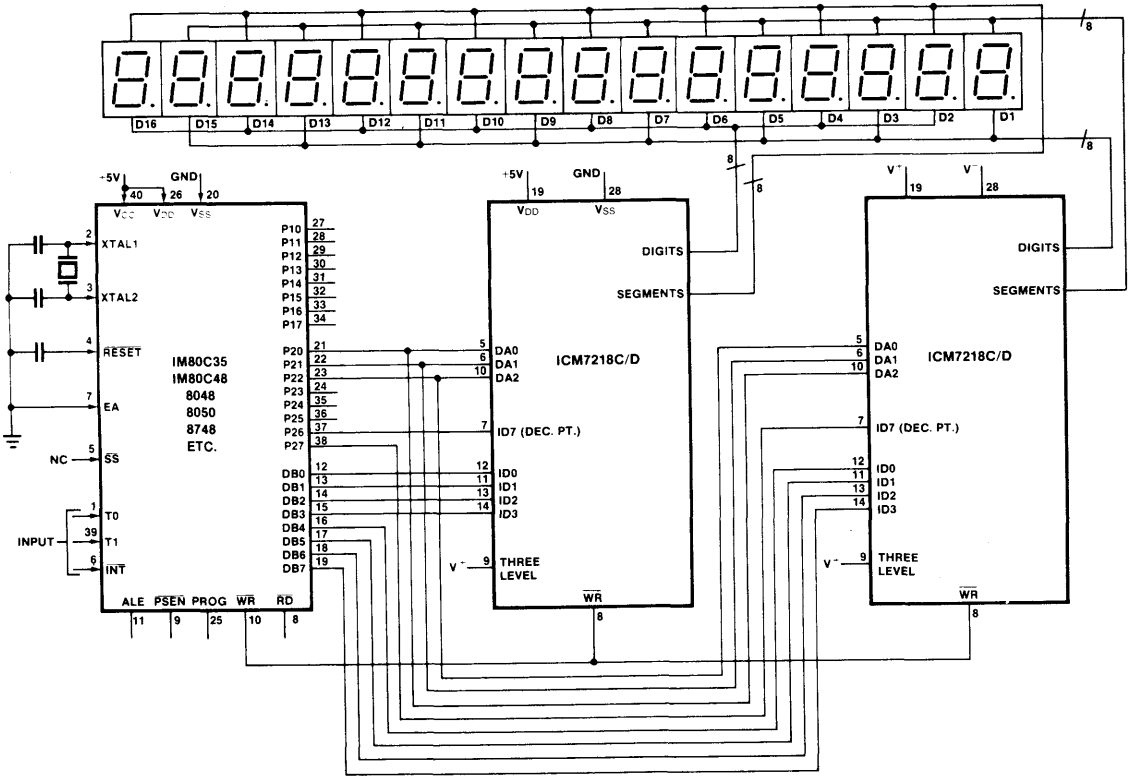


Figure 7: 16 Digit Display

NO DECODE APPLICATION

The ICM7218 can be used as a microprocessor based LED status panel driver. The microprocessor selected control word would include "No Decode" and "Data Coming". The computer then outputs word oriented "Ones" and "Zeroes" to indicate on-off states. This data is read into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 "segments" x 8 digits = 64 dots ÷ 2 per red or green = 32 channels). With red, yellow and green, 21 channels can be accommodated.

Additional ICM7218's may be bussed and addressed (see Figures 6 and 7) to expand the status panel capacity. Note per figure 4 that after the ICM7218A/B has been read in its data (8 $\overline{\text{WRITE}}$ pulses), it ignores additional information on the data lines. A new control word must be received before the next write sequence can be accommodated. Consequently, by address decoding and $\overline{\text{WRITE}}$ pulse enabling, numerous ICM7218's can be bussed together to allow a large number of indicator channels.

ICM7224 (LCD)
ICM7225 (LED)
4½-Digit Counter/ Decoder/Drivers

FEATURES

- High frequency counting—guaranteed 15MHz, typically 25MHz at 5V
- Low power operation—less than 100μW quiescent
- STORE and RESET inputs permit operation as frequency or period counter
- True COUNT INHIBIT disables first counter stage
- CARRY output for cascading four-digit blocks
- Schmitt-trigger on the COUNT input allows operation in noisy environments or with slowly changing inputs
- Leading Zero Blanking INput and OUTput for correct leading zero blanking with cascaded devices
- LCD devices provide complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal
- LED devices provide BRighTness input which can function digitally as a display enable or with a single potentiometer as a continuous display brightness control

GENERAL DESCRIPTION

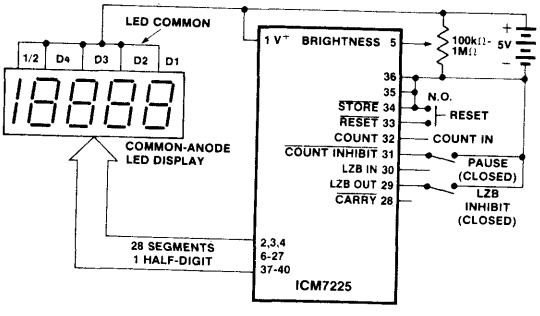
The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry, which allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

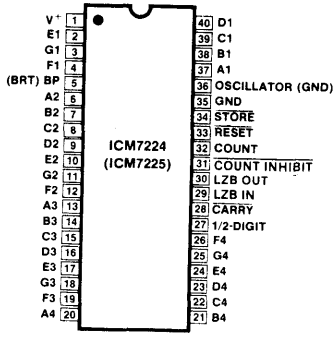
These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In LED systems, the BRighTness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic package.

TYPICAL APPLICATION (UNIT COUNTER)



PIN CONFIGURATION (outline dwg PL)



ORDERING INFORMATION

	ORDER PART NUMBER	COUNT OPTION
LCD DISPLAY	ICM7224 IPL	19999
	ICM7224A IPL	15959
LED DISPLAY	ICM7225 IPL	19999
	ICM7225A IPL	15959

Evaluation Kits, order ICM7224 EV/Kit or ICM7225 EV/Kit

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 70°C
Supply Voltage (V^+) 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, −0.3V
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.
NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

(All Parameters measured with $V^+ = 5V$ unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	μA
Operating supply voltage range	V^+		3	5	6	V
OSCILLATOR input current	I_{OSCI}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
BackPlane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		
Oscillator frequency	f_{osc}	Pin 36 Floating		19		KHz
Backplane frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

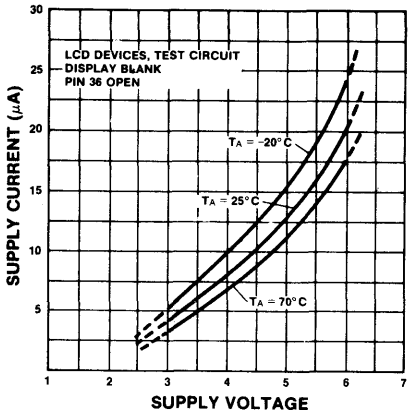
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (BRighTness) at GROUND Pins 29, 31-34 at V^+		10	50	μA
Operating supply voltage range	V^+		4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment on current	I_{SEG}	Segment On, Vout = + 3V	5	8		mA
Half-digit on current	I_H	Half-digit on, Vout = + 3V	10	16		

FAMILY CHARACTERISTICS

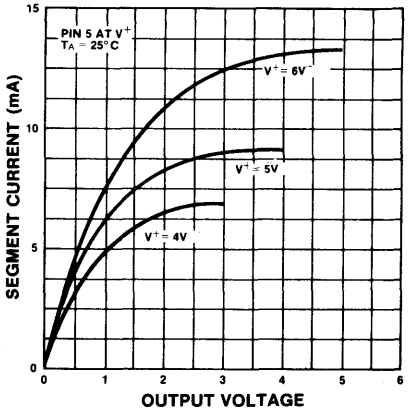
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 Vout = V^+ - 3V		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			1	
$\overline{\text{COUNT}}$ Input Threshold	V_{CT}			2		
$\overline{\text{COUNT}}$ Input Hysteresis	V_{CH}			0.5		
Output High Current	I_{OH}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = V^+ − 3V	350	500		μA
Output Low Current	I_{OL}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = + 3V	350	500		
Count Frequency	f_{count}	4.5V < V^+ < 6V	0	DC-25	15	MHz
$\overline{\text{STORE}}$, $\overline{\text{RESET}}$ Minimum Pulse Width	t_S,t_R		3			μs

TYPICAL CHARACTERISTICS

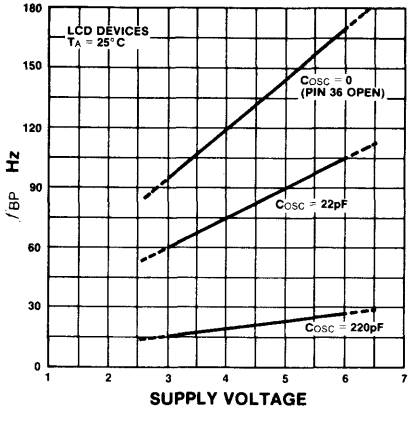
7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



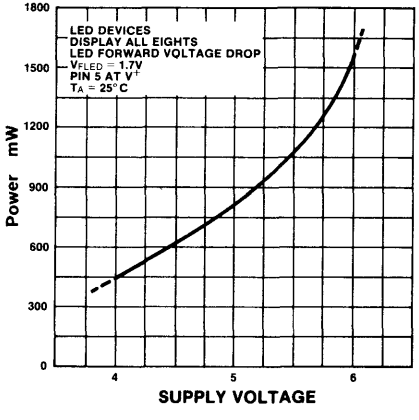
7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



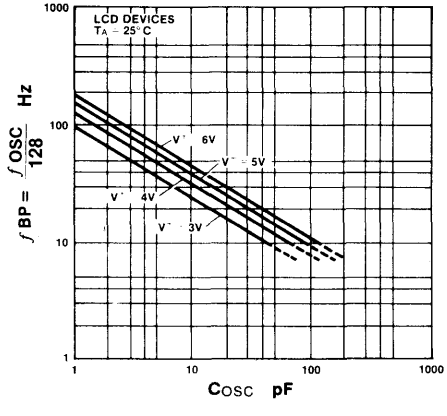
7224 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



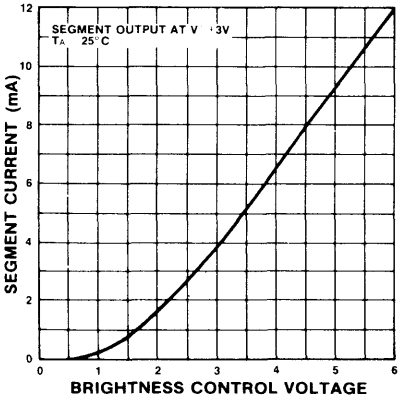
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



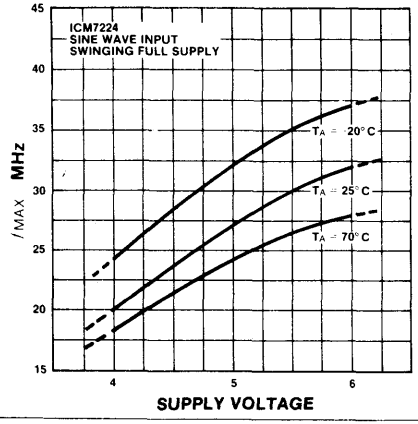
7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}



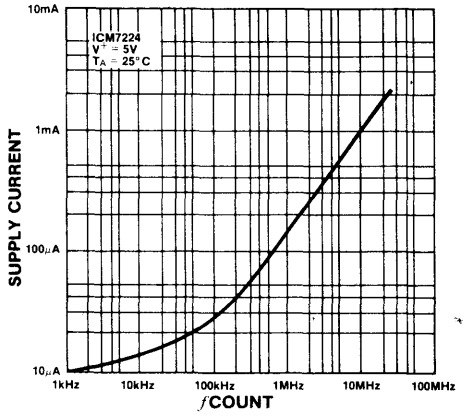
7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



MAXIMUM COUNT FREQUENCY (TYPICAL)
AS A FUNCTION OF SUPPLY VOLTAGE

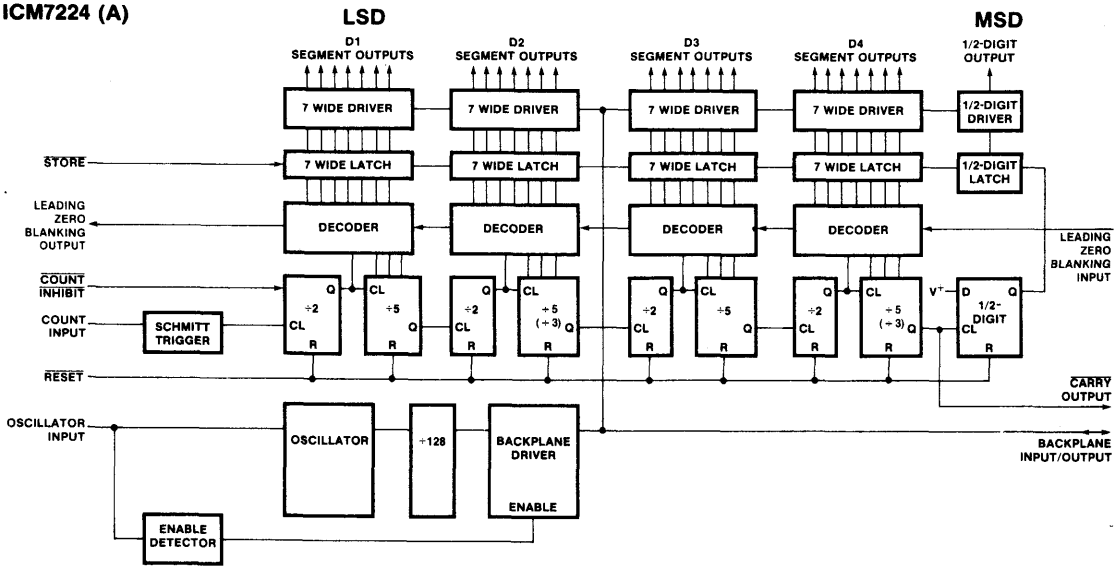


SUPPLY CURRENT AS A FUNCTION
OF COUNT FREQUENCY

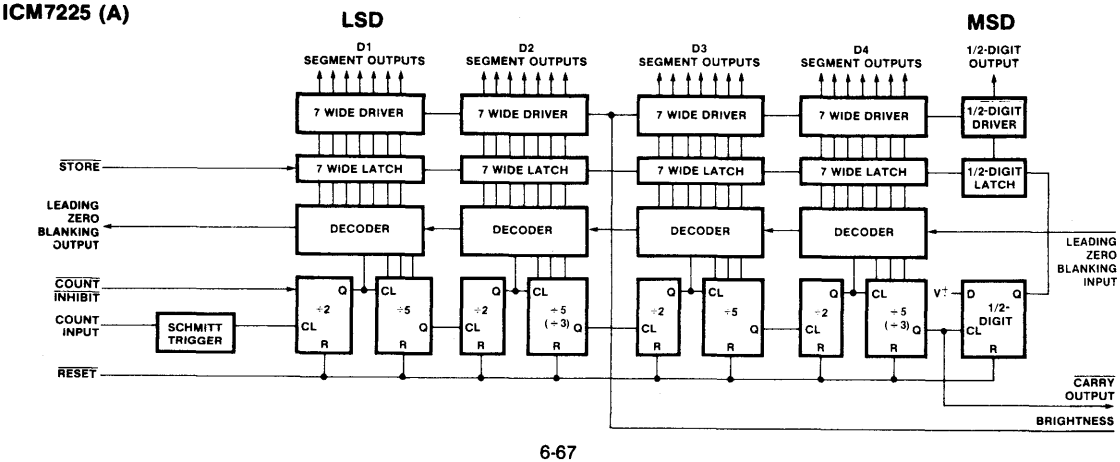


BLOCK DIAGRAMS

ICM7224 (A)



ICM7225 (A)



CONTROL INPUT DEFINITIONS

In this table, V^+ and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking INput	29	V^+ or Floating GROUND	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V^+ or Floating GROUND	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V^+ or Floating GROUND	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V^+ or Floating GROUND	Output Latches not Updated Output Latches Updated

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional 4½-digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to GROUND. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19KHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V^+; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving 4½-digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at ground, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for ground; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

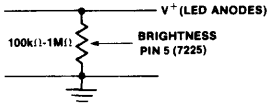


Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the $\overline{\text{CARRY}}$ signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, while the $\overline{\text{CARRY}}$ output provides a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

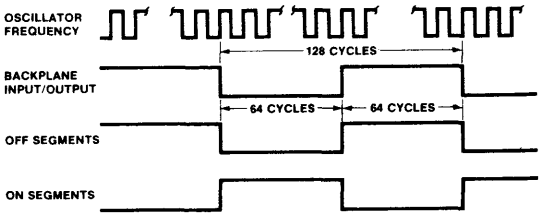
Each decade of counter drives directly into a four-to-seven decoder which develops the seven-segment output code. The output data is latched at the driver; when the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes; when low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

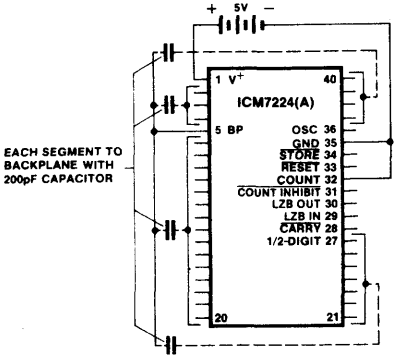
For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit device would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 or ICM7225 devices in four-digit blocks.

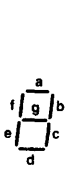
DISPLAY WAVEFORMS

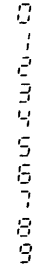


TEST CIRCUIT



SEGMENT ASSIGNMENT AND DISPLAY FONT

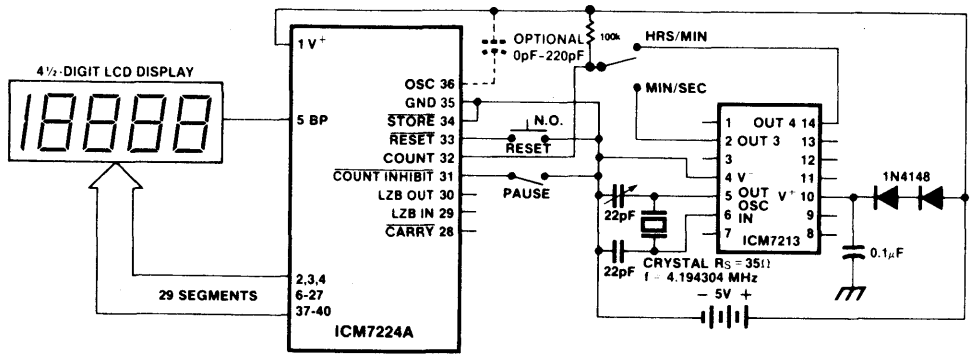




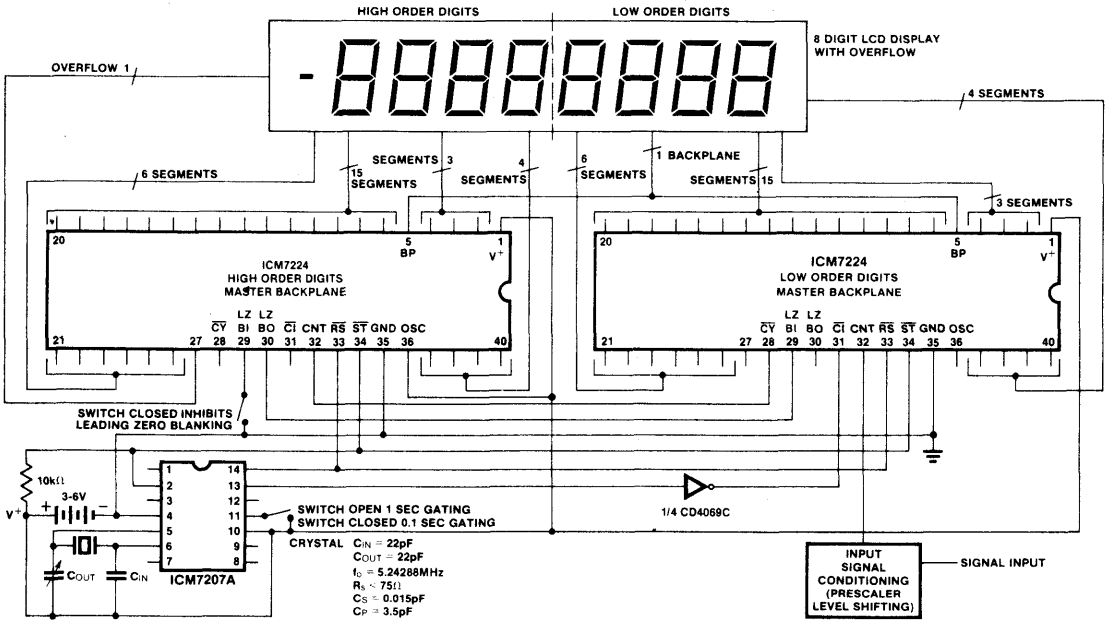
(BLANK)

APPLICATIONS

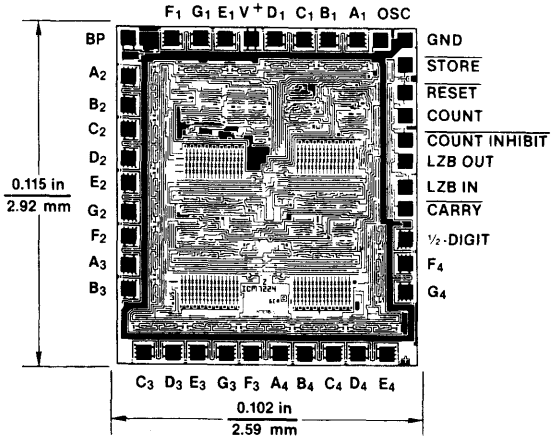
1. Two-Hour Precision Timer



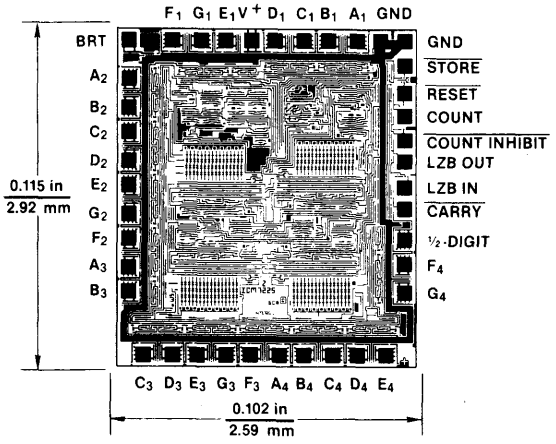
2. Eight-Digit Precision Frequency Counter



CHIP TOPOGRAPHIES



ICM7224



ICM7225

ICM7226A/B

10MHz Universal Counter System for LED Displays

FEATURES

- **CMOS design for very low power**
- **Output drivers directly drive both digits and segments of large 8 digit LED displays. Both common anode and common cathode versions are available**
- **Measures frequencies from DC to 10MHz; periods from 0.5μs to 10s**
- **Stable high frequency oscillator uses either 1MHz or 10MHz crystal**
- **Control signals available for external systems operation**
- **Multiplexed BCD outputs**

APPLICATIONS

- **Frequency Counter**
- **Period Counter**
- **Unit Counter**
- **Frequency Ratio Counter**
- **Time Interval Counter**

ORDERING INFORMATION

DISPLAY	DEVICE	PACKAGE	ORDER NUMBER
Common Anode	ICM7226A	CERDIP	ICM7226AIJL
		DICE	ICM7226A/D
Common Cathode	ICM7226B	Plastic	ICM7226BIPL
		DICE	ICM7226B/D

NOTE: An evaluation kit is available for these devices — order ICM7226AEV/KIT.

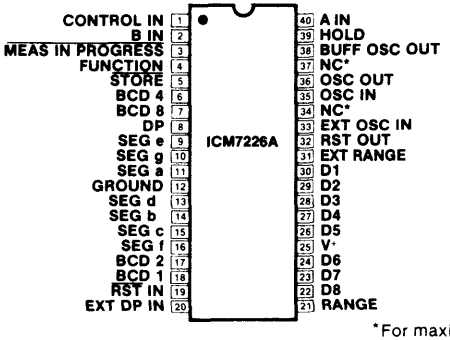
GENERAL DESCRIPTION

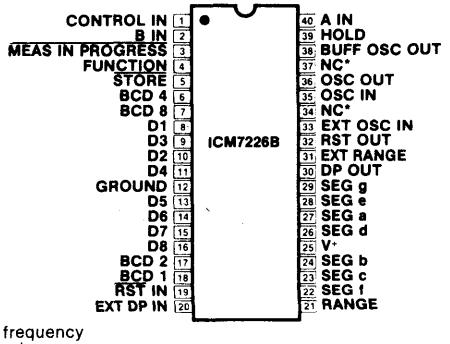
The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in **frequency** and **unit counter** modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval**, the 10MHz timebase gives a 0.1μsec resolution. In **period average** and **time interval average**, the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode display with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

PIN CONFIGURATION (outline dwgs JL, PL)





*For maximum frequency stability, connect to V^+ or GROUND

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
*Voltage on any Input or
Output Terminal (Note 1) ..... Not to exceed V^+ or GND by more than 0.3V
Maximum Power Dissipation at 70°C (Note 2)
ICM7226A 1.0W
ICM7226B 0.5W
Maximum Operating Temperature Range ..... −20°C to +85°C
Maximum Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

***Note 1:** Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V^+ or GROUND by 0.3V.

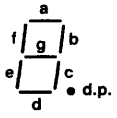
Note 2: Assumes all leads soldered or welded to PC board and free air flow.

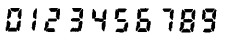
ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Supply Current	I^+_{OP}	Display Off Unused inputs to GROUND		2	5	mA
Supply Voltage Range	V_{SUPP}	-20°C < T_A < 85°C Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
Maximum Guaranteed Frequency Input A, Pin 40	$f_{A(max)}$	-20°C < T_A < 85°C 4.75V < V^+ < 6.0V Figure 1 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5	14		MHz
Maximum Frequency Input B, Pin 2	$f_{B(max)}$	-20°C < T_A < 85°C 4.75V < V^+ < 6.0V Figure 2	2.5			
Minimum Separation Input A to Input B Time Interval Function		-20°C < T_A < 85°C 4.75V < V^+ < 6.0V Figure 3	250			ns
Maximum osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	f_{OSC}	-20°C < T_A < 85°C 4.75V < V^+ < 6.0V	(0.1)	10		MHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$ $T_A = +85°C$	2000			μS
Multiplex Frequency	f_{mux}	f_{osc} = 10 MHz		500		Hz
Time Between Measurements		f_{osc} = 10 MHz		200		ms
Minimum Input Rate of Charge	dV_{in}/dt	Inputs A, B		15		mV/μs

SEGMENT IDENTIFICATION AND DISPLAY FONT





LED overflow indicator connections:
Overflow will be indicated on the decimal point output of digit 8.

	CATHODE	ANODE
ICM7226A	d.p.	D_8
ICM7226B	D_8	d.p.

ELECTRICAL CHARACTERISTICS (Continued)

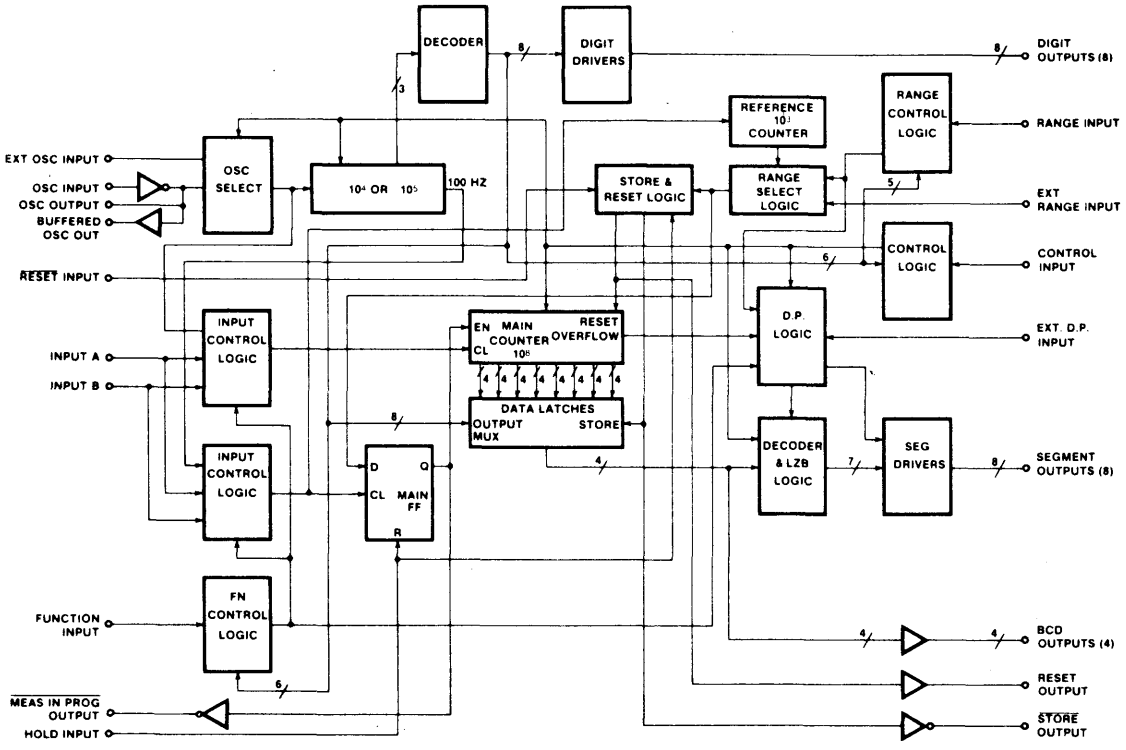
TEST CONDITIONS: $V^+ = 5.0V$, test circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT VOLTAGES PINS 2,19,33,39,40,35						
input low voltage	V_{IL}	$-20°C < T_A < +70°C$	1.0			V
input high voltage	V_{IH}				3.5	
PIN 2, 39, 40 INPUT LEAKAGE, A,B	I_{ILK}				20	µA
Input resistance to V^+ PINS 19,33	R_{IN}	$V_{IN} = V^+ -1.0V$.	100	400		kΩ
Input resistance to GROUND PIN 31	R_{IN}	$V_{IN} = +1.0V$	50	100		
Output Current PINS 3,5,6,7,17,18,32,38	I_{OL}	$V_{OL} = +0.4V$	400			µA
PINS 5,6,7,17,18,32	I_{OH}	$V_{OH} = +2.4V$	100			µA
PINS 3,38	I_{OH}	$V_{OH} = V^+ -0.8V$	265			
ICM7226A PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER						
high output current	I_{OH}	$V_O = V^+ -2.0V$	150	180		mA
low output current	I_{OL}	$V_O = +1.0V$		-0.3		
SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16						
low output current	I_{OL}	$V_O = +1.5V$	25	35		mA
high output current	I_{OH}	$V_O = V^+ -1.0V$		100		µA
MULTIPLEX INPUTS PINS 1,4,20,21						
input low voltage	V_{IL}				0.8	V
input high voltage	V_{IH}		2.0			
input resistance to GROUND	R_{IN}	$V_{IN} = +1.0V$	50	100		kΩ
ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16						
low output current	I_{OL}	$V_O = +1.0V$	50	75		mA
high output current	I_{OH}	$V_O = V^+ -2.5V$		100		µA
SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30						
high output current	I_{OH}	$V_O = V^+ -2.0V$	10	15		mA
leakage current	I_L	V_O = GROUND			10	µA
MULTIPLEX INPUTS PINS 1,4,20,21						
input low voltage	V_{IL}				$V^+ -2.0$	V
input high voltage	V_{IH}		$V^+ -0.8$			
input resistance to V^+	R_{IN}	$V_{IN} = V^- -1.0V$	200	360		kΩ

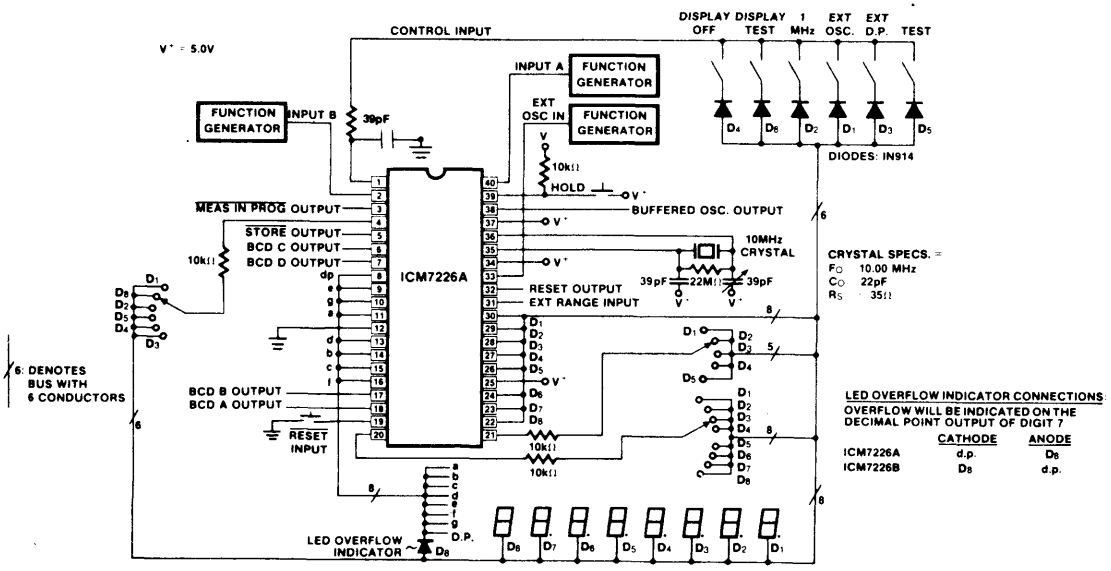
EVALUATION KIT

An evaluation kit is available for the ICM7226. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226. With the help of this kit, an engineer or technician can have the ICM7226 "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIJL, a 10MHz quartz crystal, eight each 7-segment 0.3" LEDs, PC board, resistors, capacitors, diodes, switches and IC socket. Order Number ICM7226AEV/Kit.

BLOCK DIAGRAM



TEST CIRCUIT



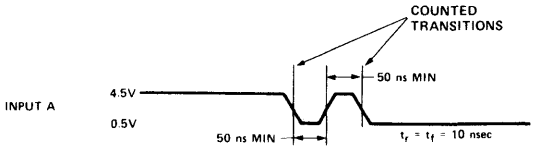


FIGURE 1. Waveform for Guaranteed Minimum $f_{A(max)}$ Function = Frequency, Frequency Ratio, Unit Counter.

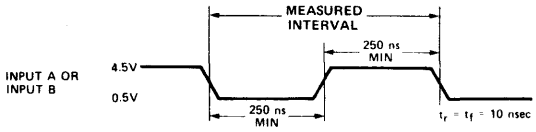


FIGURE 2. Waveform for Guaranteed Minimum $f_{B(max)}$ and $f_{A(max)}$ for Function = Period and Time Interval.

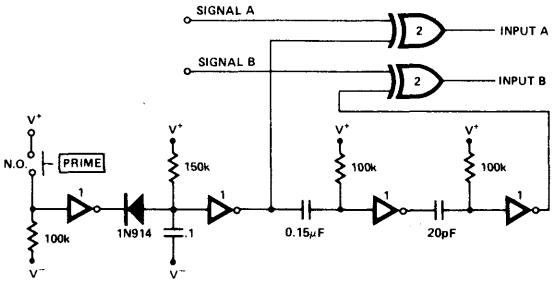
TIME INTERVAL MEASUREMENT

The ICM7226A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can be easily accomplished with the following circuit: (Figure 3b).



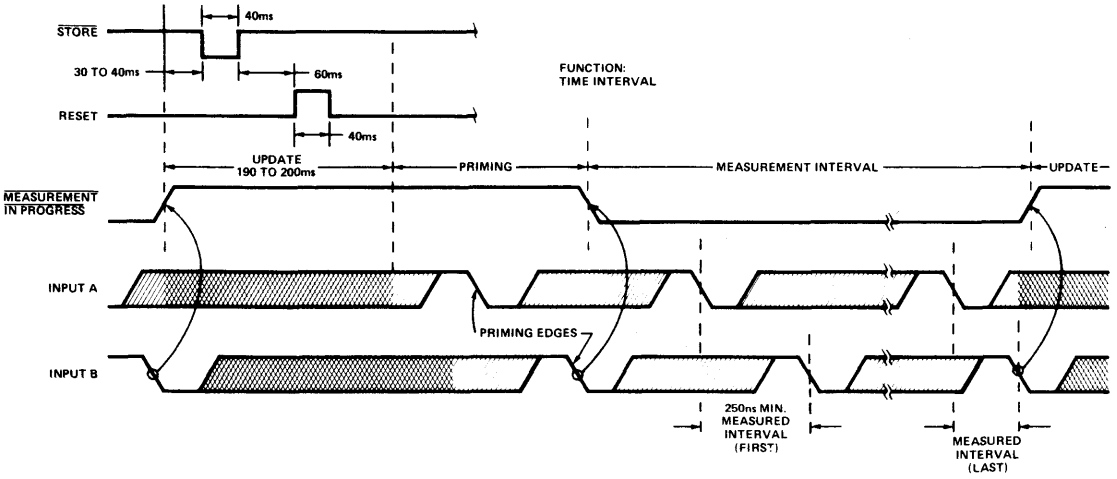
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3b. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A/B as the first alternating signal states automatically prime the device. See Figure 3a.

During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

FIGURE 3a. Waveforms for Time Interval Measurement (Others are similar, without priming phase)

APPLICATION NOTES

GENERAL

INPUTS A & B

The signal to be measured is applied to INPUT A in **frequency period, unit counter, frequency ratio** and **time interval** modes. The other input signal to be measured is applied to INPUT B in **frequency ratio** and **time interval**. f_A should be higher than f_B during **frequency ratio**.

Both inputs are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$ and input impedance of 250kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. Multiplexed Input Control

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	0.01 Sec/1 Cycle	D_1
	0.1 Sec/10 Cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1k Cycles	D_4
PIN 31	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Blank Display	D_4&Hold
	Display Test	D_8
	1MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	Test	D_5
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

CONTROL INPUTS

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if **display off** is selected at the same time.

Display Off - To enable the **display off** mode it is necessary to tie D_4 to the CONTROL input and have the HOLD input at V^+. The chip will remain in this mode until HOLD is switched low. While in the **display off** mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5mA with a 10MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter.)

1MHz Select - The **1MHz select** mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in **period** and **time interval**, since the least significant digit will be in 1μs increments rather than 0.1μs.

External Oscillator Enable - In this mode, the EXTernal OSCillator INput is used, rather than the on-chip oscillator, for the Timebase and Main Counter inputs in **period** and **time interval** modes. The on-chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to **both** OSC IN (pin 35) and EXT OSC IN (pin 33), or provide crystal for "default" oscillation, to avoid hang-up problems.

External Decimal Point Enable - When **external decimal point** is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode - This is a special mode used only in high speed production testing, and serves no other purpose.

RANGE INPUT

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter, or if the EXTernal RANGE INput determines the measurement time. In all functional modes except **unit counter**, a change in the RANGE input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

FUNCTION INPUT

Six functions can be selected. They are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.**

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In **time interval**, a flip flop is set first by a 1→0 transition at INPUT A and then reset by a 1→0 transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow indication is output on the Decimal Point Output during D_8.

TABLE 2. Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Osc ON Gate	Osc OFF Gate
Unit Counter(Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100Hz (Osc ÷ 10^5 or 10^4)

EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input - Except in the **unit counter** mode, when the HOLD Input is at V^+, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD Input is at V^+, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

$\overline{\text{RESET}}$ Input - The $\overline{\text{RESET}}$ Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTernal RANGE Input - The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure 4 shows the relationship between $\overline{\text{MEASurement IN PROGRESS}}$ and EXTernal RANGE Input.

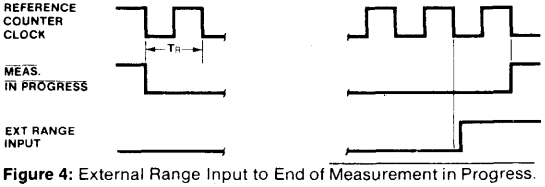


Figure 4: External Range Input to End of Measurement in Progress.

$\overline{\text{MEASUREMENT IN PROGRESS}}$, $\overline{\text{STORE}}$ AND RESET Outputs - These Outputs are provided to facilitate external interfacing. Figure 5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The $\overline{\text{MEASUREMENT IN PROGRESS}}$ output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.

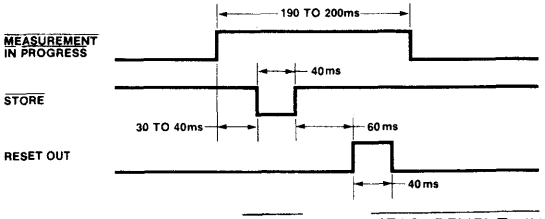


Figure 5: RESET OUT, $\overline{\text{STORE}}$, and $\overline{\text{MEASUREMENT IN PROGRESS}}$ Outputs Between Measurements.

BCD Outputs - The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A - Common Anode) or negative going (ICM7226B - Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load and when interfacing low power Schottky TTL latches, it is necessary to use 1kΩ pull down resistors on the TTL inputs for optimum results. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

TABLE 3 Truth Table BCD Outputs

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFFered OSCillator OUTput - The BUFFered OSCillator OUTput has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244μs, and an interdigit blanking time of 6μs to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the Main Counter overflows. The internal decimal point control displays frequency in kHz and time in μs.

The ICM7226A is designed to drive common anode LED displays at a peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 6, 7, 8 and 9 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

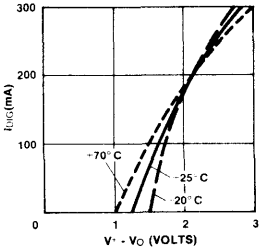


Figure 6: ICM7226A Typical I_{DIG} vs. V^+-V_O $4.5 \leq V^+ \leq 6.0V$

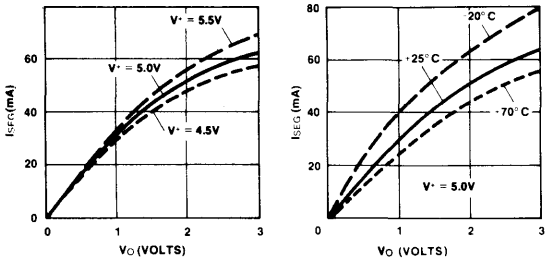


Figure 7: ICM7226A Typical I_{SEG} vs. V_O

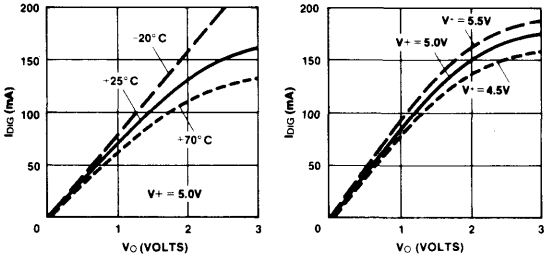


Figure 8: ICM7226B Typical I_{DIG} vs. V_O

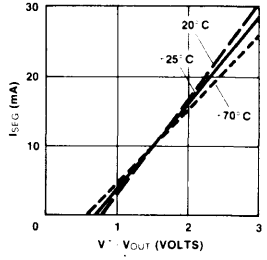


Figure 9: ICM7226B Typical I_{SEG} vs. (V^+-V_O) $4.5V \leq V^+ \leq 6.0V$

To increase the light output from the displays, V^+ may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

ACCURACY

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode, maximum accuracy is obtained with high frequency inputs, and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10, the least accuracy will be obtained at 10kHz. In **time interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 11. In **frequency ratio** measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 12.

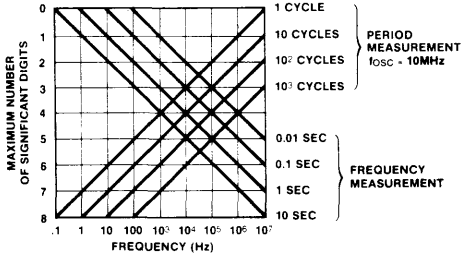


Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

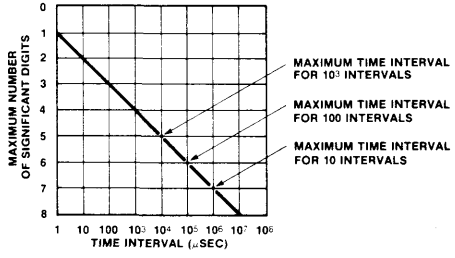


Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

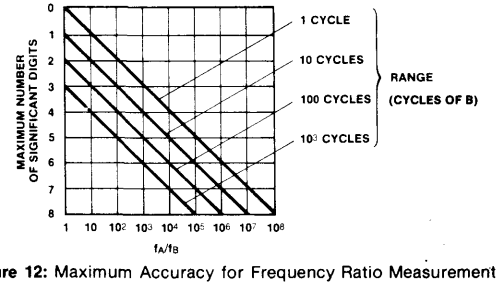


Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and

hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V+ should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in figure 13.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **frequency and period counter.** To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 15 shows use of a ÷10 prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy. Note that A IN comes from Q_C rather than Q_D, to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.

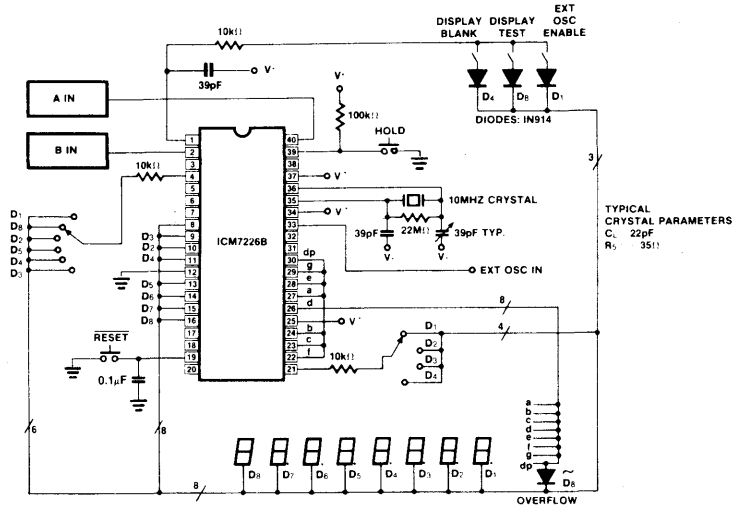
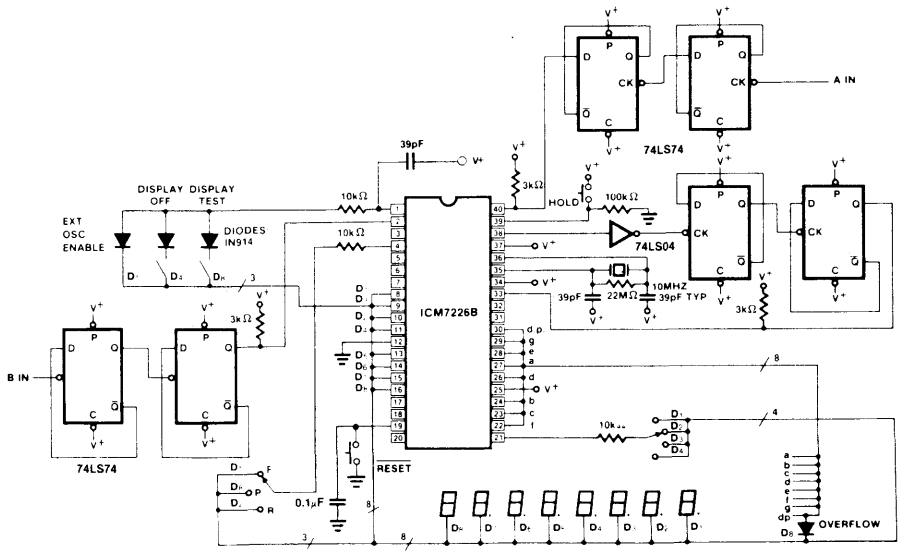


Figure 13: 10MHz Universal Counter



Notes: 1) If a 2.5MHz crystal is used, diode D1 and I.C.'s 1 and 2 can be eliminated.

Figure 14: 40MHz Frequency, Period Counter

Figure 16 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74153 or 74251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

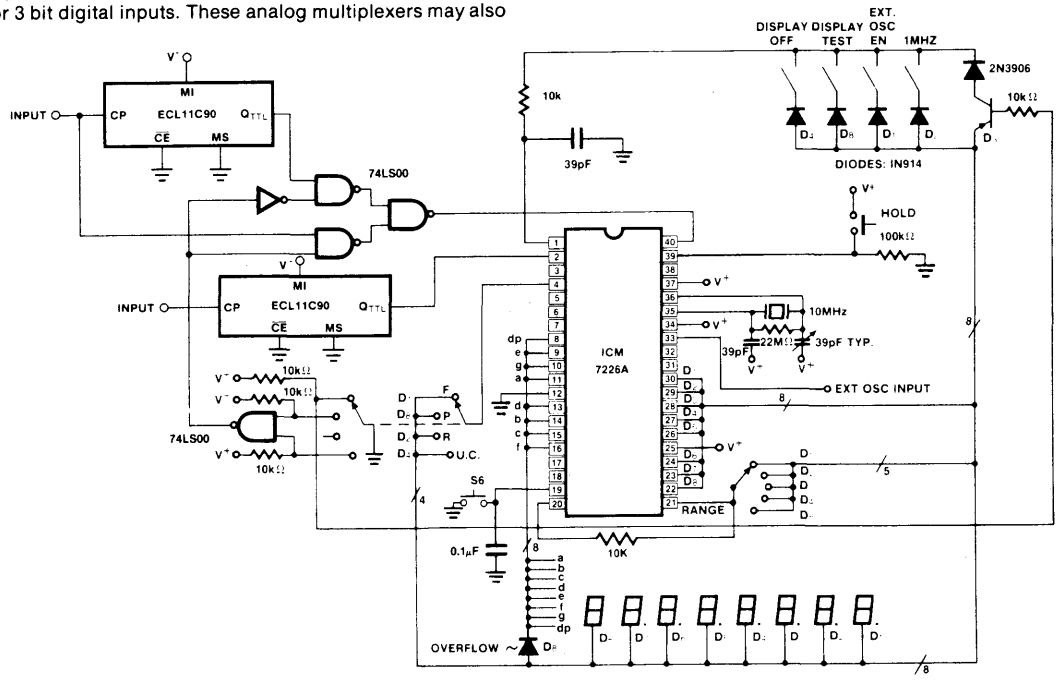


Figure 15: 100MHz Multi Function Counter

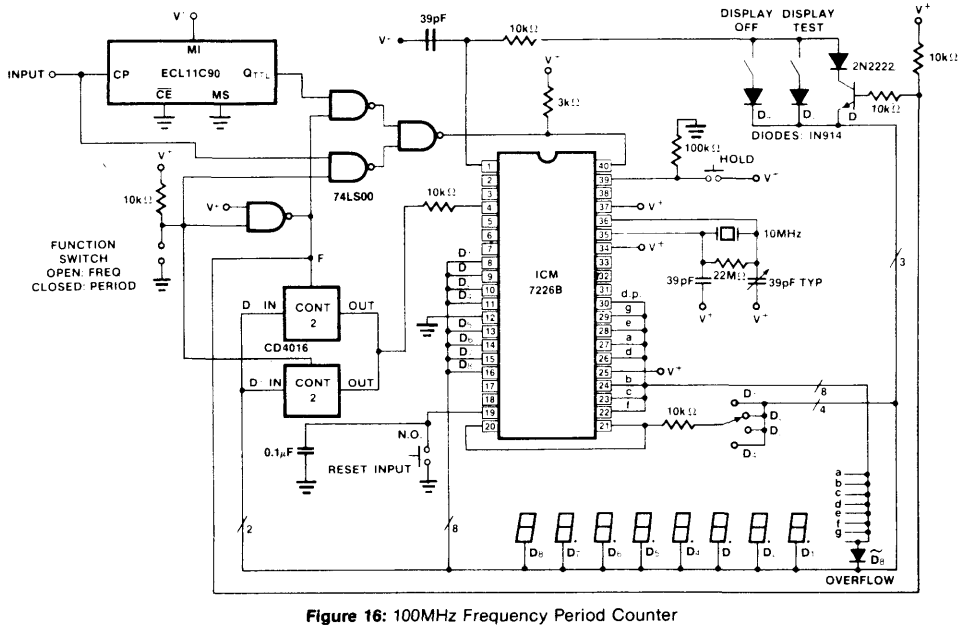
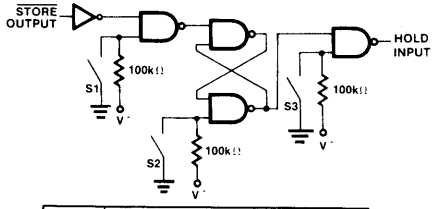


Figure 16: 100MHz Frequency Period Counter

The circuit shown in figure 17 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in figure 18 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 18 on the circuit shown in Figure 14 will reduce the time between measurements from 1600ms to 800ms.



SWITCH	FUNCTION
S1	OPEN SINGLE MEAS MODE ENABLED
S2	CLOSED INITIATE NEW MEASUREMENT
S3	CLOSED HOLD INPUT

Figure 17: Single Measurement Circuit for Use With ICM7226

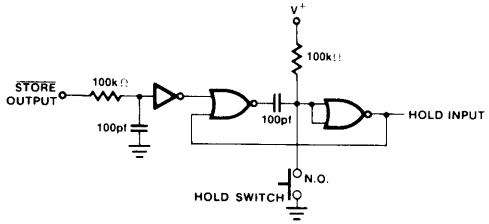
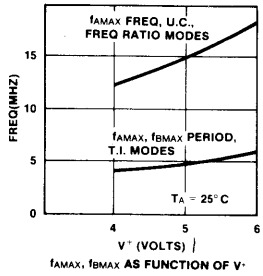


Figure 18: Circuit for Reducing Time Between Measurements



fAMAX, fBMAX AS FUNCTION OF V⁺

Figure 19: Typical Operating Characteristics

Figure 20 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive 2 ICM7211 display drivers. The ICM7226 EV/Kit may easily be interfaced to 2 ICM7211 EV/Kits in this way. A similar arrangement can be used for driving vacuum fluorescent displays with the ICM7235.

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a load capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{CinCout}{Cin+Cout}\right)$

C_O = Crystal static capacitance
R_S = Crystal Series Resistance
Cin = Input Capacitance
Cout = Output Capacitance
$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4pF to C_{IN} and C_{OUT} . For maximum frequency stability, C_{IN} and C_{OUT} should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10MHz nor 1MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2 \times 10^4}$ for 10MHz mode and $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1MHz mode. The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to V^+.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFfered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator iNput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V^+ or GROUND and these two signals should be kept away from the oscillator circuit.

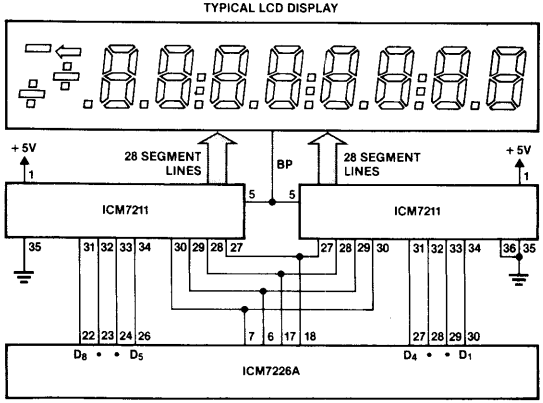
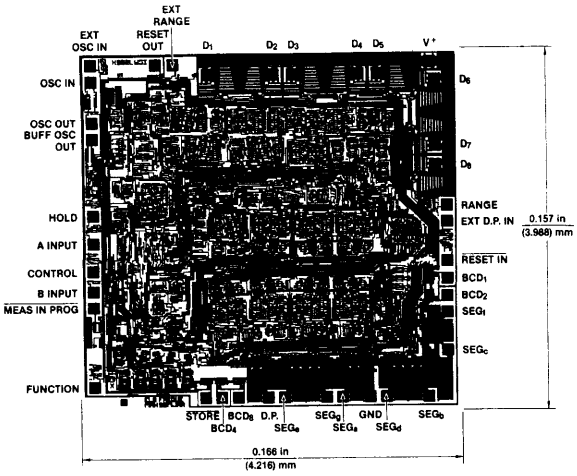
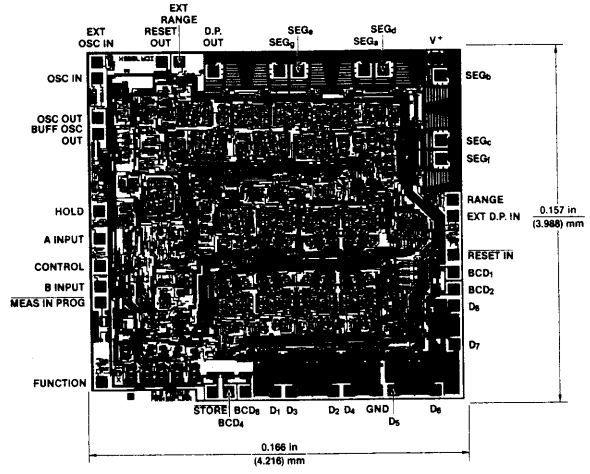


Figure 20: 10MHz Universal Counter System with LCD Display

CHIP TOPOGRAPHIES



ICM7226A



ICM7226B

ICM7231/32/33/34 Display Decoder/Drivers for Triplexed Liquid Crystal Displays

FEATURES

- **ICM7231: Drives 8 digits of 7 segments with two independent annunciators per digit. Address and data input in parallel format.**
- **ICM7232: Drives 10 digits of 7 segments with two independent annunciators per digit. Address and data input in serial format.**
- **ICM7233: Drives 4 characters of 18 segments. Address and data input in parallel format.**
- **ICM7234: Drives 5 characters of 18 segments. Address and data input in serial format.**
- **Chips provide all signals required to drive rows and columns of triplexed LCD display.**
- **Display voltage independent of power supply, allows user control of display operating voltage and temperature compensation if desired.**
- **On-chip oscillator provides all display timing.**
- **Total power consumption typically 200μW, maximum 500μW at 5V.**
- **Low-power shutdown mode retains data with 5μW typical power consumption at 5V, 1μW at 2V.**
- **Direct interfacing to high-speed microprocessors and microcomputers.**

6

GENERAL DESCRIPTION

The ICM7231/7234 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry and contain a mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

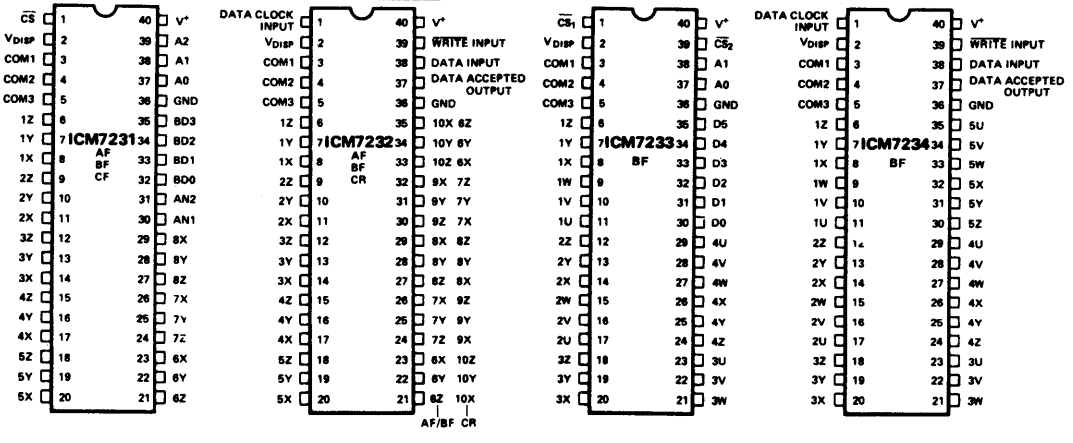
The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits. The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

The ICM7234 uses a serial input structure like that of the ICM7232, and drives five 18-segment characters. Again, the input bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static discharge. Devices are packaged in a 40 pin plastic DIP.

PIN CONFIGURATIONS (outline dwg PL)



OPTION TABLE AND ORDERING INFORMATION

ORDER PART* NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231AFIPL	Hexadecimal	Both Annunciators on COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
ICM7231BFIPL	Code B			
ICM7231CFIPL	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7232AFIPL	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data 2 bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
ICM7232BFIPL	Code B			
ICM7232CRIPL	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7233AFIPL	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7233BFIPL	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Four Characters
ICM7234AFIPL	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Five Characters
ICM7234BFIPL	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

*Dice versions also available (ICM7231AF/D, ICM7233AF/D, etc.) Introductory parts may be available only in CERDIP package. Change suffix to IJL if necessary.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] ..... 0.5 W @ 70°C
Supply Voltage (V^+) ..... 6.5 V
Input Voltage[2] ..... $-0.3 \le V_{IN} \le 6.5$
Display Voltage[2] ..... $-0.3 \le V_{DISP} \le +0.3$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. This limit refers to that of the package and will not be obtained during normal operation.
2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V^+ but not more than 6.5 volts above GND.

ELECTRICAL CHARACTERISTICS $V^+ = 5V \pm 10\%$, $T_A = -20°C$ to $+85°C$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Power Supply Voltage	V^+		4.5	>4	5.5	V
Data Retention Supply Voltage	V^+	Guaranteed Retention at 2V	2	1.6		V
Logic Supply Current	I^+	Current from V^+ to Ground excluding Display. $V_{DISP} = 2V$		30	100	µA
Shutdown Total Current	I_S	V_{DISP} Pin 2 Open		1	10	µA
Display Voltage Range	V_{DISP}	Ground $\le V_{DISP} \le V^+$	0		V^+	V
Display Voltage Setup Current	I_{DISP}	$V_{DISP} = 2V$ Current from V^+ to V_{DISP} On-Chip		15	25	µA
Display Voltage Setup Resistor Value	R_{DISP}	One of Three Identical Resistors in String	40	75		kΩ
DC Component of Display Signals		(Sample Test only)		1/4	1	% (V^+ - V_{DISP})
Display Frame Rate	f_{DISP}	See Figure 2	60	90	120	Hz
Input Low Level	V_{IL}	ICM7231, ICM7233 Pins 30-35, 37-39, 1			0.8	V
Input High Level	V_{IH}		2.0			V
Input Leakage	I_{ILK}	ICM7232, ICM7234 Pins 1, 38, 39		0.1	1	µA
Input Capacitance	C_{IN}			5		pF
Output Low Level	V_{OL}	Pin 37, ICM7232, ICM7234, $I_{OL} = 1mA$,			0.4	V
Output High Level	V_{OH}	$V^+ = 4.5V$, $I_{OH} = -500\mu A$	4.1			V
Operating Temperature Range	T_{OP}	Industrial Range	-20		+85	°C

AC CHARACTERISTICS $V^+ = 5V \pm 10\%, -20°C \leq T_A \leq +85°C$

PARALLEL INPUT (ICM7231, ICM7233) See Figure 12

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
$\overline{\text{Chip Select}}$ Pulse Width	t_{cs}		500	350		ns
Address/Data Setup Time	t_{ds}		200			ns
Address/Data Hold Time	t_{dh}		0	-20		ns
Inter-Chip Select Time	t_{ics}		3			μs

SERIAL INPUT (ICM7232, ICM7234) See Figures 15, 16, 17

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Data Clock Low Time	$t_{\overline{cl}}$		350			ns
Data Clock High Time	t_{cl}		350			ns
Data Setup Time	t_{ds}		200			ns
Data Hold Time	t_{dh}		0	-20		ns
$\overline{\text{Write}}$ Pulse Width	t_{wp}		500	350		ns
$\overline{\text{Write}}$ Pulse to Clock at Initialization	t_{wll}		1.5			μs
Data Accepted Low Output Delay	t_{odl}			200	400	ns
Data Accepted High Output Delay	t_{odh}			1.5	3	μs
Write Delay After Last Clock	t_{cws}		350			ns

6

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF	See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant 4 Bit Binary Data Inputs	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant 3 Bit Digit Address Inputs	Input Address (See Table 2)	
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	

Note:

3. $\overline{CS}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

ICM7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant Most Significant 6 Bit (ASCII) Data Inputs	Input Data See Table 4	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1	37 38	Least Significant Most Significant Address Inputs	Input Add. See Table 5	
$\overline{CS1}$ $\overline{CS2}$	39 1	Chip Select Inputs (Note 3)	Both inputs LOW load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.	

Note:
3. $\overline{CS1}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided either by pulling it high when inactive, or ensuring frequent activity.

ICM7232 and ICM7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic. ICM7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits ICM7234 9 bits

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V^+) chip is shutdown; oscillator stops, all display pins to V^+.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On ICM7231/33) (On ICM7232/34)	Drive display segments, or columns.
V^+	40	Chip Positive Supply	
GND	36	Chip Ground	

TRIPLEXING (1/3 MULTIPLEXING) LIQUID CRYSTAL DISPLAYS

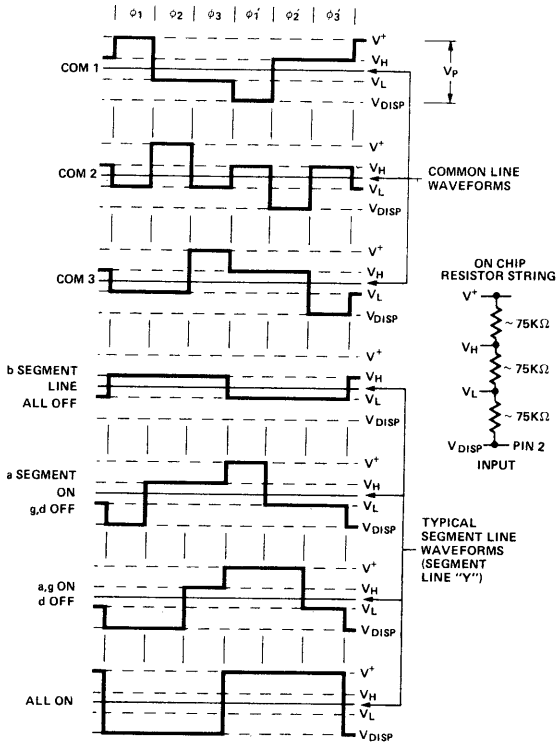
Figure 1 shows the connection diagram for a typical 7-segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 2 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 2 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunicator) acts as a capacitance from segment line to common line, shown schematically in Figure 3. Figure 4 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments in Figure 2.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 4 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always $1.92\ V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 5 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7234 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V^+ and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V^+ - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below ground. This can cause device latchup and destruction of the chip.



NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.
$\phi_1', \phi_2', \phi_3'$ – COMMON LOW WITH RESPECT TO SEGMENT.
COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'
COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'
COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

Figure 2. Display Voltage Waveforms

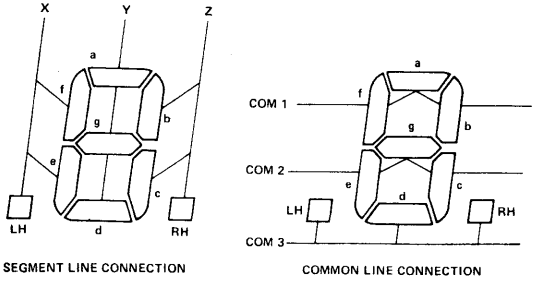


Figure 1. Connection Diagrams for Typical 7-Segment Displays

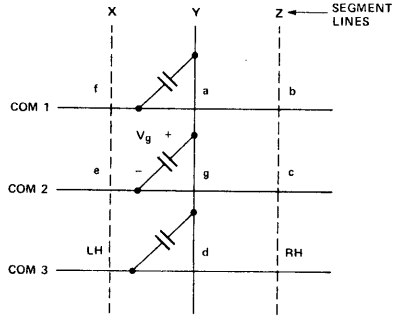


Figure 3. Display Schematic

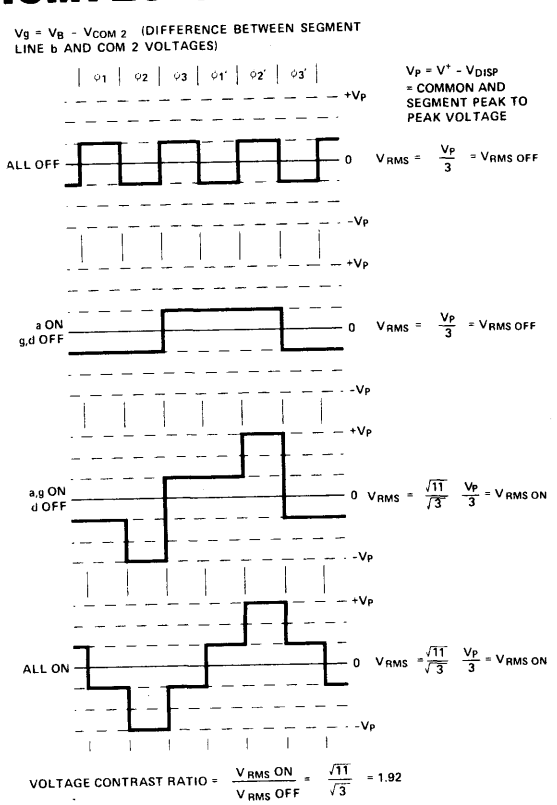


Figure 4. Voltage Waveforms on Segment g (V_g)

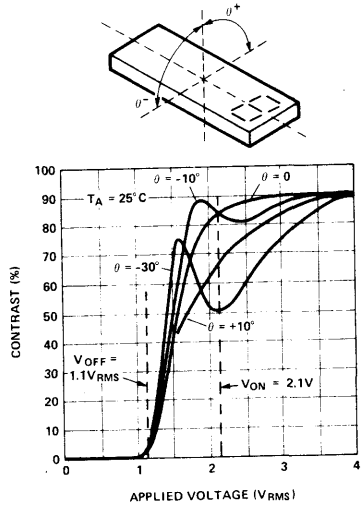


Figure 5. Contrast vs. Applied RMS Voltage

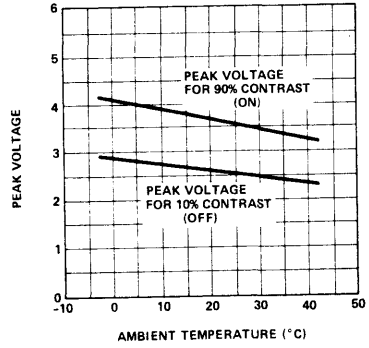


Figure 6. Temperature Dependence of LC Threshold

TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change to a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 6 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 5.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to GND as shown in Figure 7. A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

Figure 8(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 5 and 6. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of -2 mV/°C; five in series gives -10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 8(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about -2 mV/°C) is also multiplied. The transistor should have a beta of at least 100 with a collector current of 10 μA. The inexpensive 2N2222 shown in the figure is a suitable device.

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to GND. The inputs of the chip are designed such that they may be driven above V^+ without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663, as shown in Figure 9. This circuit allows independent adjustment of both voltage and temperature compensation.

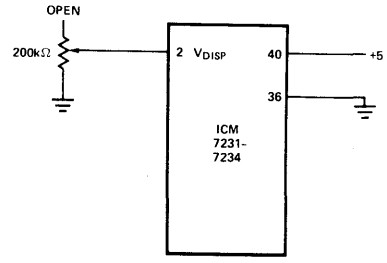


Figure 7 Simple Display Voltage Adjustment

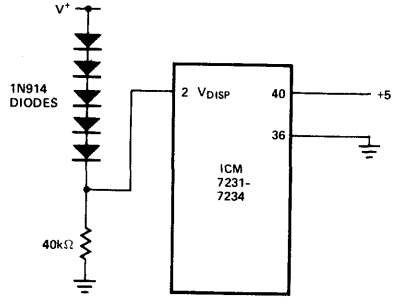


Figure 8(a) String of Diodes

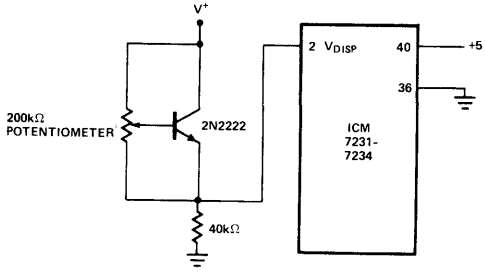


Figure 8(b) Transistor-Multiplier

Figure 8 Diode-based Temperature Compensation

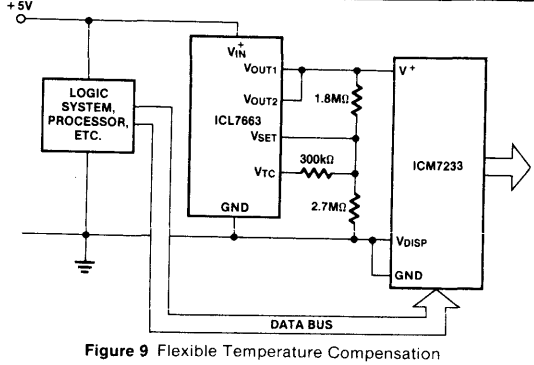


Figure 9 Flexible Temperature Compensation

DESCRIPTION OF OPERATION

PARALLEL INPUT OF DATA AND ADDRESS (ICM7231, ICM7233)

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, see block diagrams Figures 10 and 11. In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input. In the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input devices are shown in Figure 12, with the values for setup, hold, and pulse width times shown in AC Characteristics on page 3. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

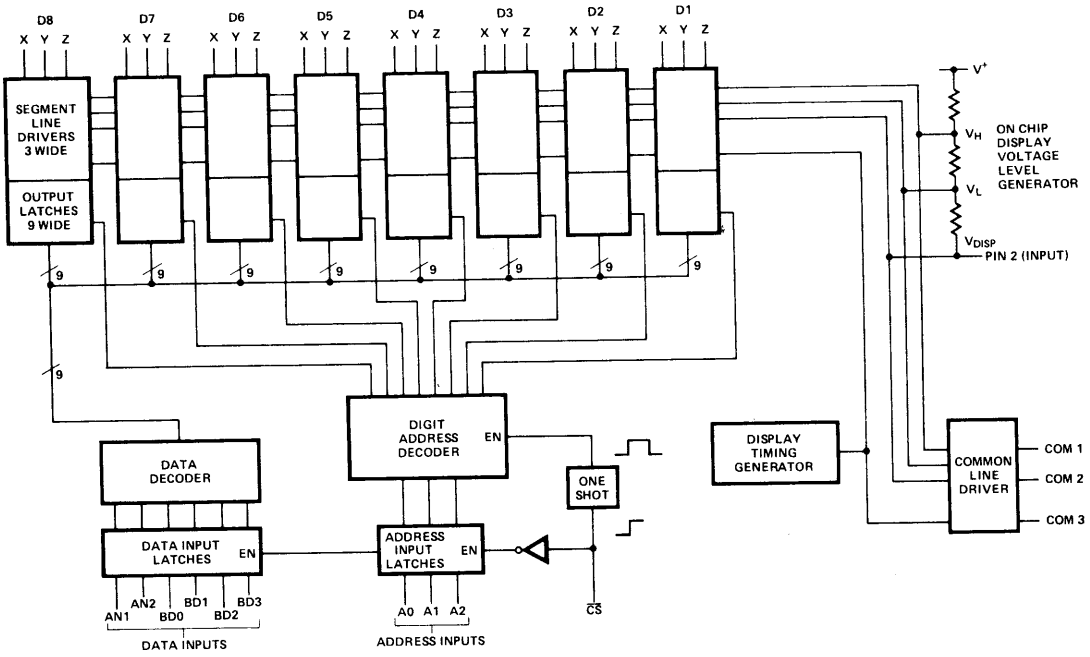


Figure 10. ICM7231 Block Diagram

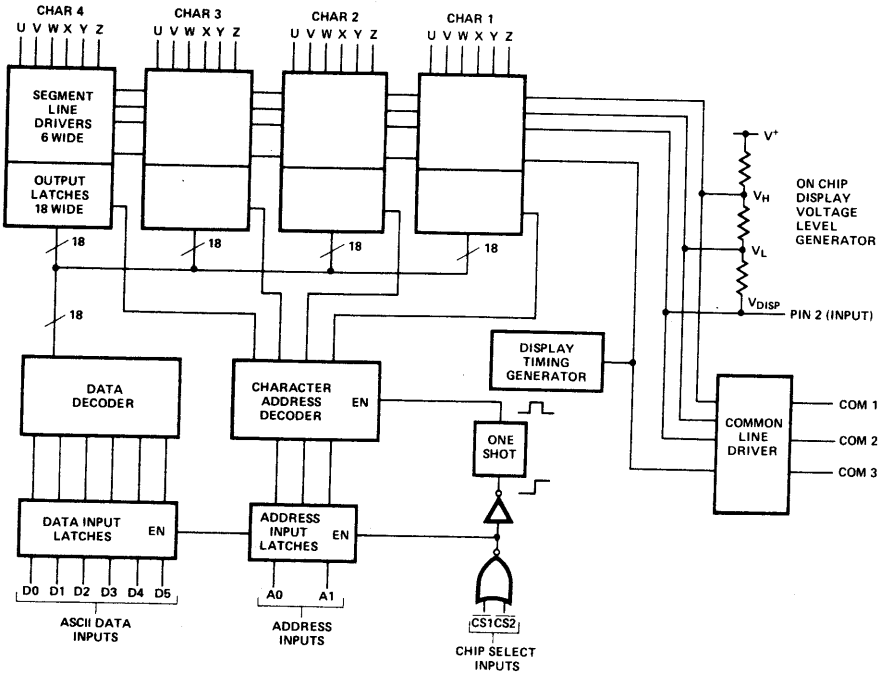
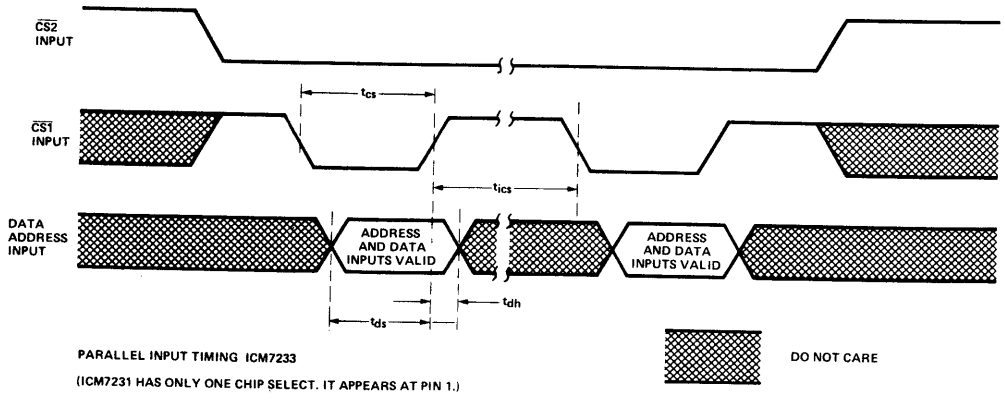


Figure 11. ICM7233 Block Diagram



PARALLEL INPUT TIMING ICM7233

(ICM7231 HAS ONLY ONE CHIP SELECT. IT APPEARS AT PIN 1.)

Figure 12. Parallel Input Timing

SERIAL INPUT OF DATA AND ADDRESS (ICM7232, ICM7234)

The ICM7232 and ICM7234 trade six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits (ICM7232) or one more 18-segment character (ICM7234). This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to block diagrams, Figures 13 and 14 and timing diagrams, Figures 15, 16, and 17. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232, 9 in the ICM7234), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the $\overline{\text{WRITE}}$ input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

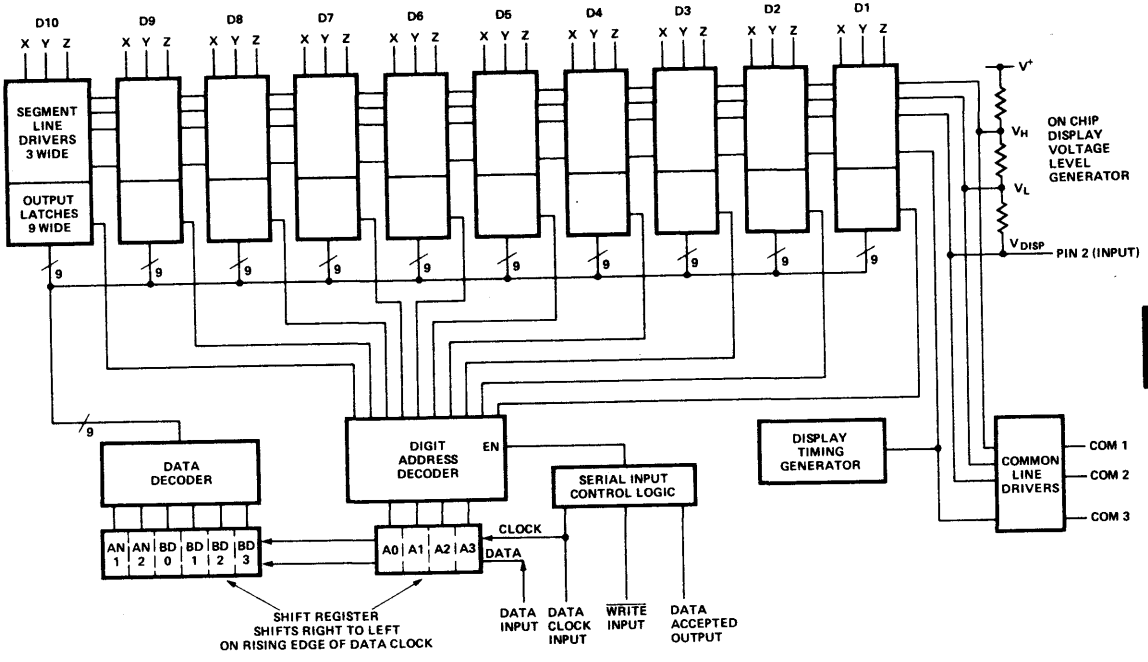


Figure 13. ICM7232 Block Diagram

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic, while in the ICM7234 it is the tenth.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 15. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunicators off, as shown in Figure 16.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

In the ICM7234, nine bits are always required; the control logic is similar, but allows only a $\overline{\text{WRITE}}$ (DATA ACCEPTED Low) with nine bits entered in the shift register, as shown in Figure 17.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

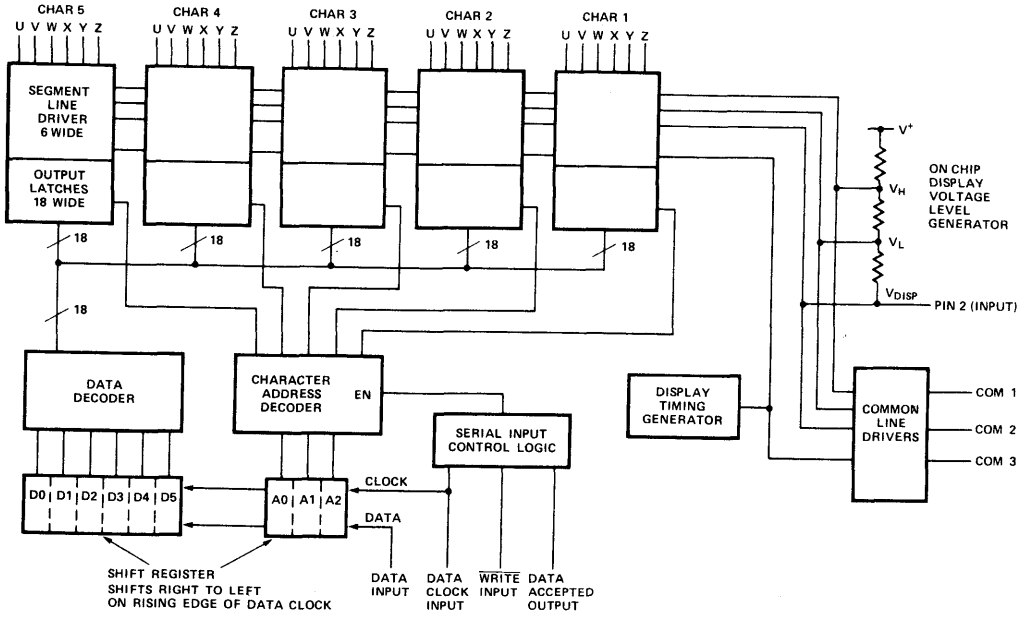


Figure 14. ICM7234 Block Diagram

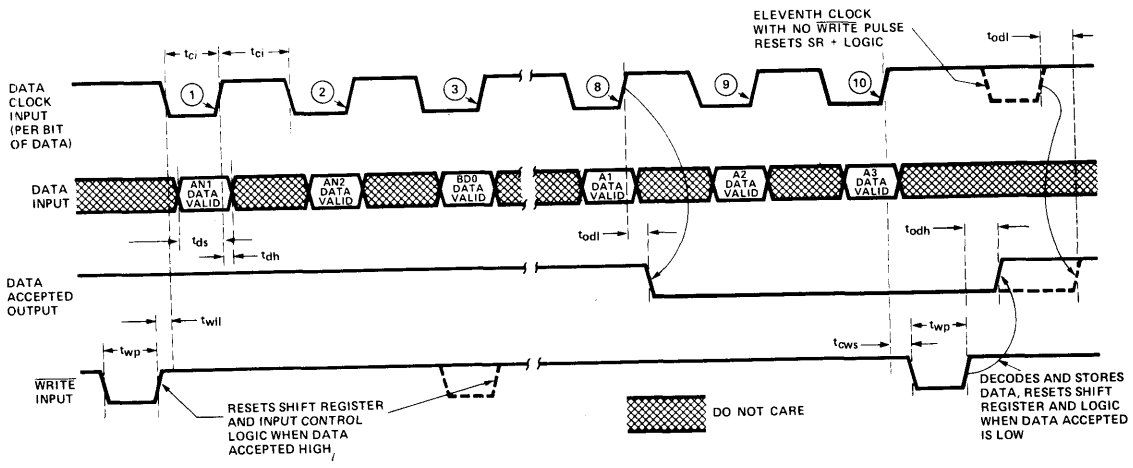


Figure 15. ICM7232 One Digit Input Timing Diagram, Writing Both Annunicators

AN1 ENTER FIRST	AN2	BD0	BD1	BD2	BD3	A_0	A_1	A_2	A_3 ENTER LAST

ICM7232 WRITE ORDER

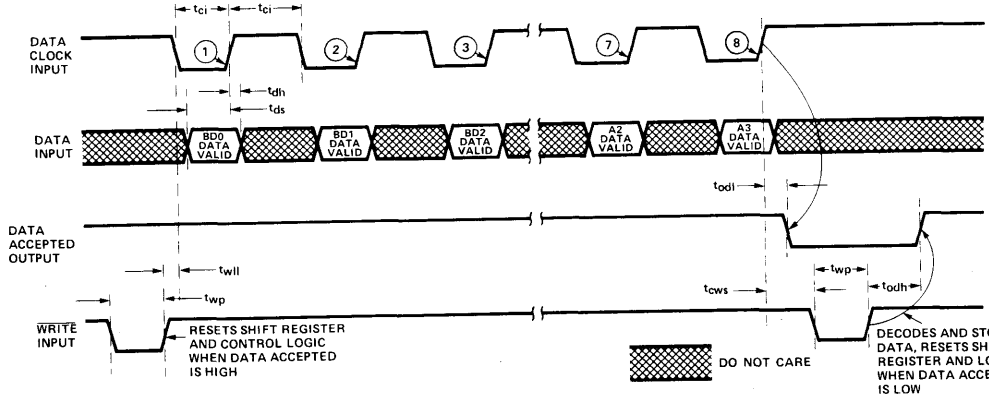


Figure 16. ICM7232 Input Timing Diagram, Leaving Both Annunciators OFF

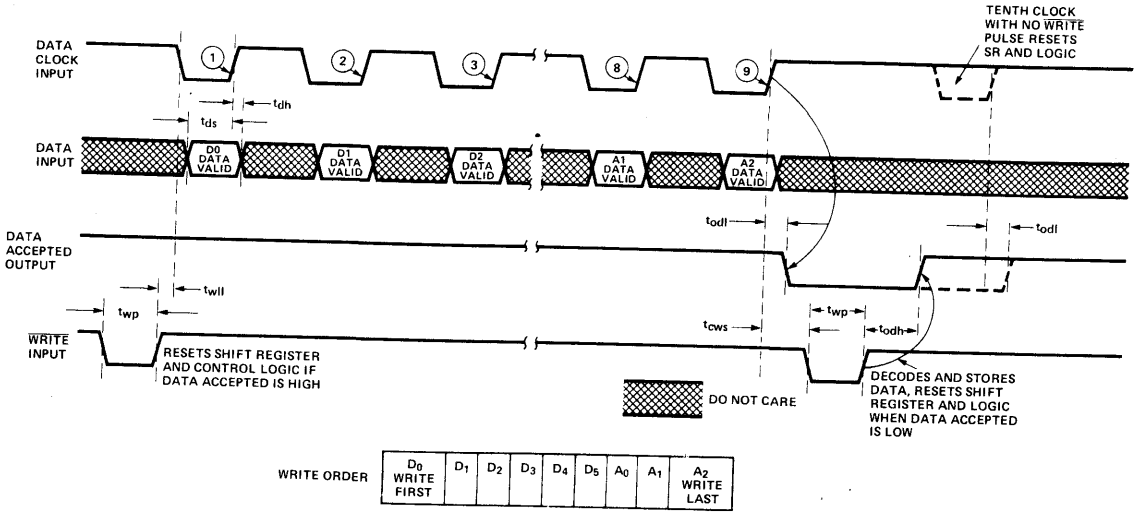


Figure 17. ICM7234 One Character Input Timing Diagram

DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 18. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1) (see Figure 19). The "C" devices provide only a "Code B" output for the 7-segments.

The ICM7233 and ICM7234 are supplied in "A" and "B" versions. Both versions decode an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and two "dots". The "A" devices have numbers which are half width and the "B" devices have full width numbers. The layout for a single character is shown in Figure 20 with output decoding shown in Table 4.

The data decoder is a mask programmable ROM. For large quantity orders custom decoder programs can be arranged. Contact the factory for details

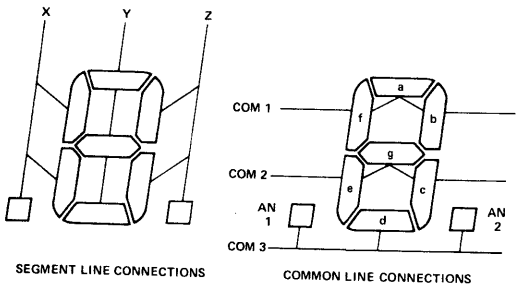


Figure 18. ICM7231 and ICM7232 Display Fonts ("A" and "B" Suffix Versions)

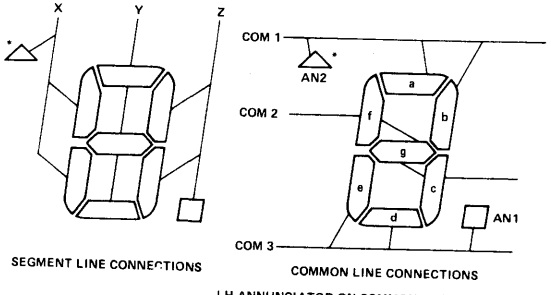


Figure 19. ICM7231 and ICM7232 Display Fonts ("C" Suffix Versions)

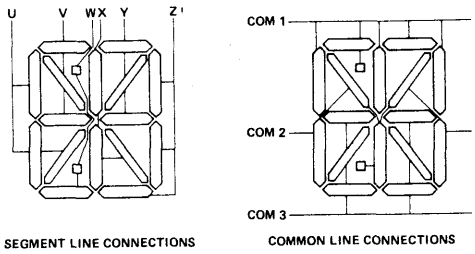


Figure 20. ICM7233 and ICM7234 Display Font (18-Segment Alphanumeric)

Table 1

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

BINARY DATA DECODING (ICM7231/32)

Table 2

CODE INPUT				DISPLAY OUTPUT
ICM 7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

ADDRESS DECODING (ICM7231/32)

Table 3

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0		
0	1		
1	0		
1	1		

ANNUNCIATOR DECODING

EVALUATION KITS

After purchasing a sample of the ICM7231/32/33/34, the majority of users will want to build a sample display. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering kits which contain all the necessary components to build 8 character or 8 digit displays. With the help of such a kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICM7231EV/KIT and the ICM7233 EV/KIT. Both contain the appropriate ICs, a circuit board, a Multiplexed LCD display (7/9 segment for 7231EV/KIT, 16/18 segment for ICM7233EV/KIT), passive components, and miscellaneous hardware.

COMPATIBLE DISPLAYS

Compatible displays are manufactured by:

G.E. Displays Inc., Beechwood, Ohio
(216) 831-8100 (#356E3R99HJ)

Epson America Inc., Torrance, CA
(Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA
(Custom Displays)

Crystaloid, Hudson, OH

Table 4

CODE INPUT				DISPLAY OUTPUT				
				D5, D4			A	B
D3	D2	D1	D0	0, 0	0, 1	1, 0	1, 1	
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

DATA DECODING
6 - BIT ASCII→18 SEGMENT
(ICM7233/34)

Table 5

CODE INPUT			DIGIT SELECTED
ICM 7234 ONLY			
A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

ADDRESS
DECODING
(ICM7233/34)

TYPICAL APPLICATIONS

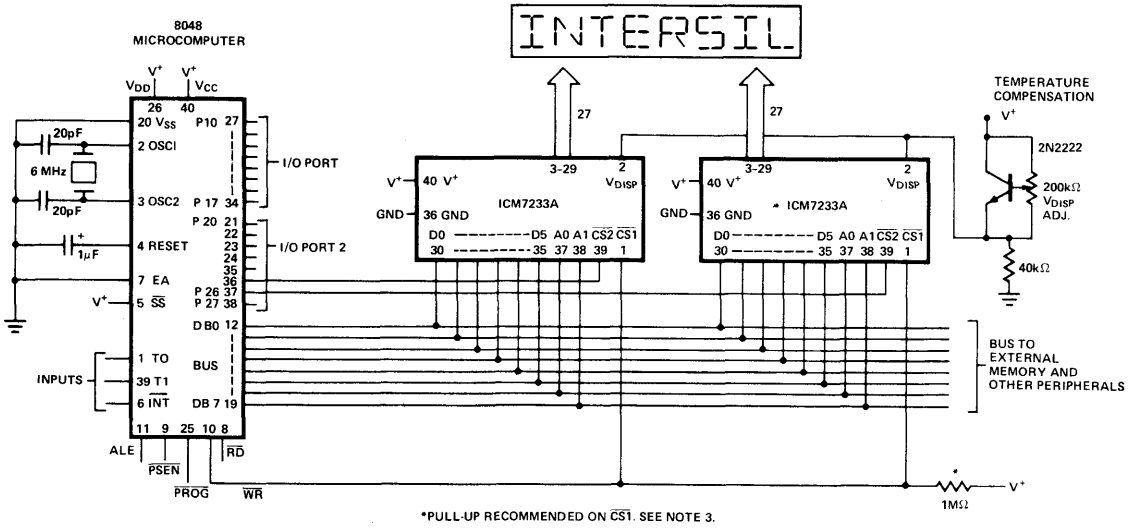


Figure 21. 8048/IM80C48 Microcomputer with 8 Character 16 Segment ASCII Triplex Liquid Crystal Display. The two bit character address is merged with the data and written to the display driver under the control of the $\overline{WR}$ line. Port lines are used to either select the target driver, or deselect all of them for other bus operations.

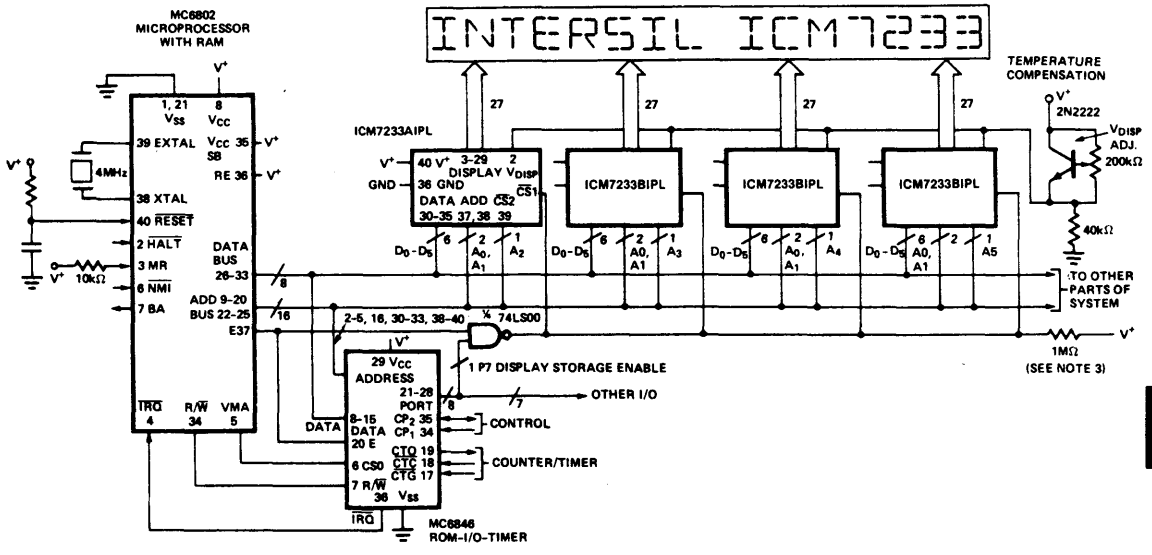


Figure 22. MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display. The peripheral device provides ROM and Timer functions in addition to port line control of the display bank. Individual character locations are addressed via the address bus. Note that VMA is not decoded on these lines, which could cause problems with the TST instruction.

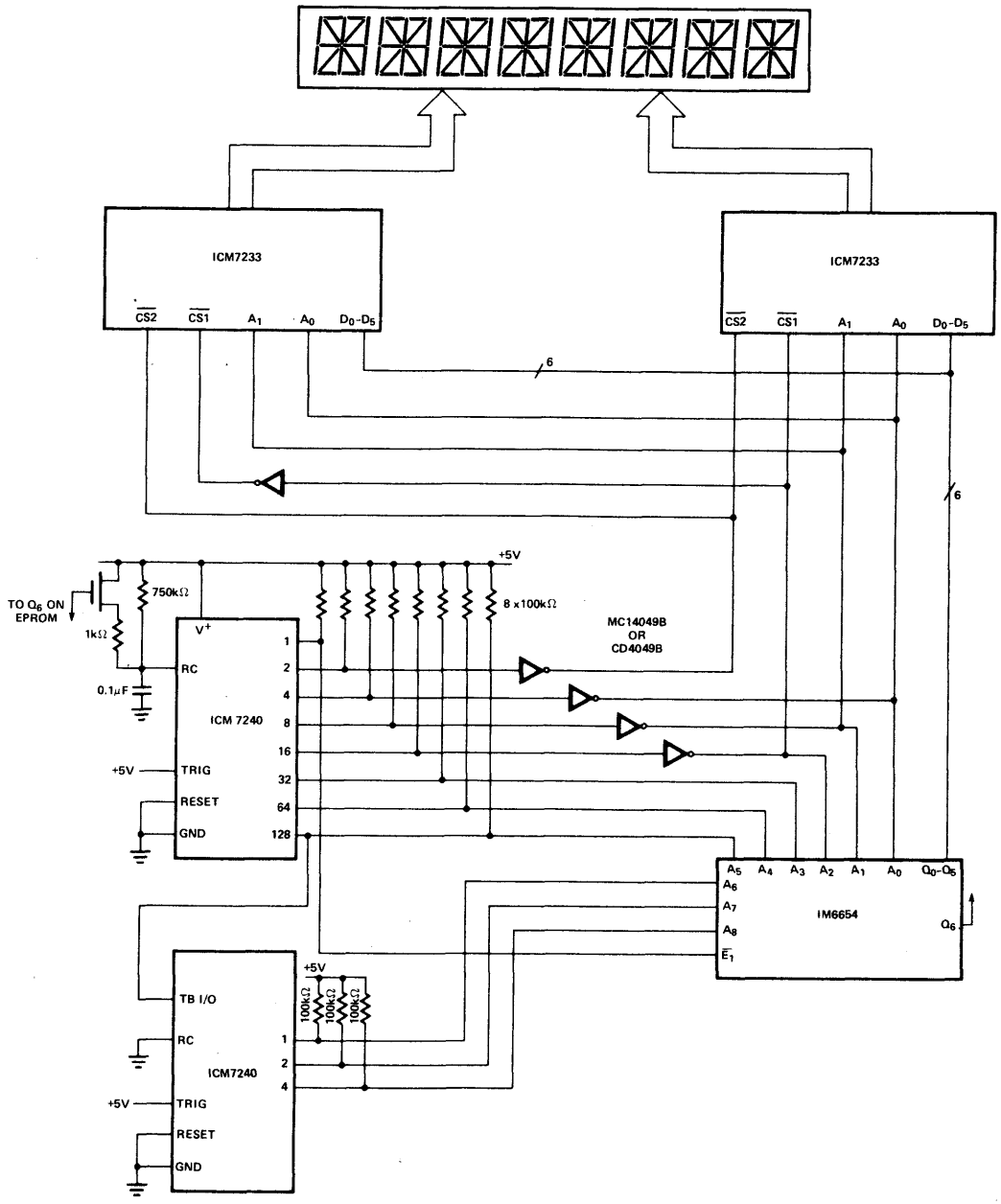


Figure 23. EPROM-Coded Message System. This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

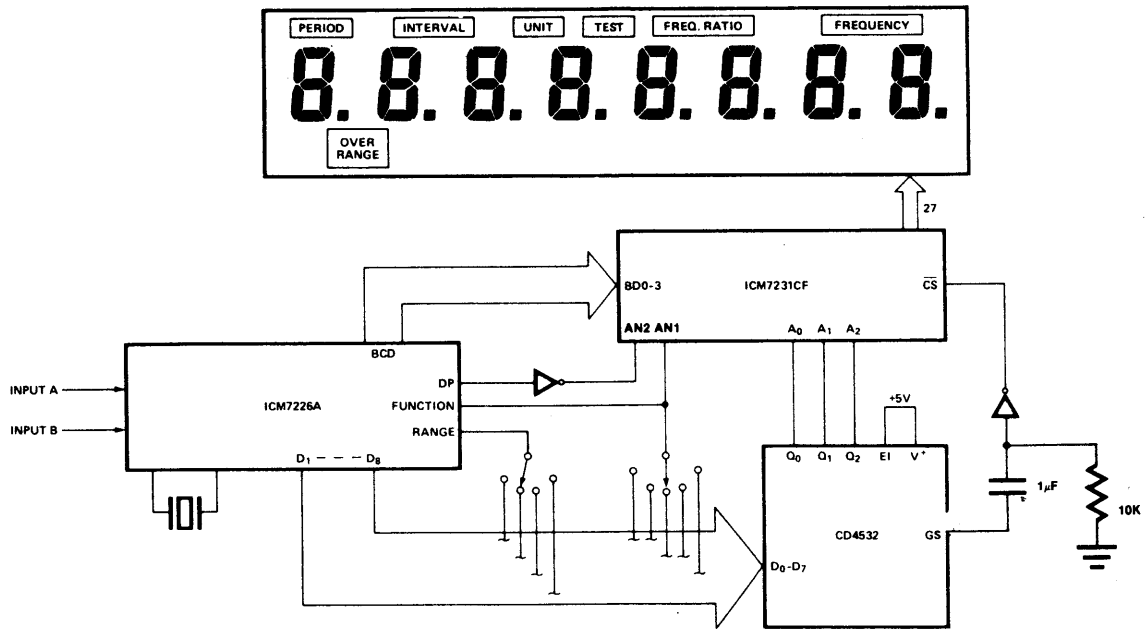


Figure 24. 10 MHz Frequency/Period Pointer with LCD Display. The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.

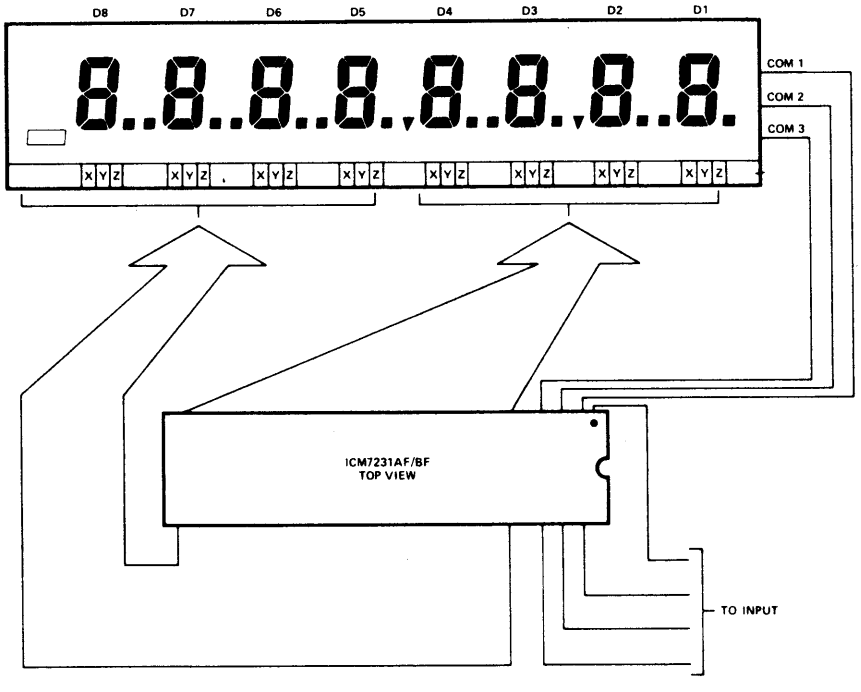


Figure 25. "Forward" Pin Orientation and Display Connections.

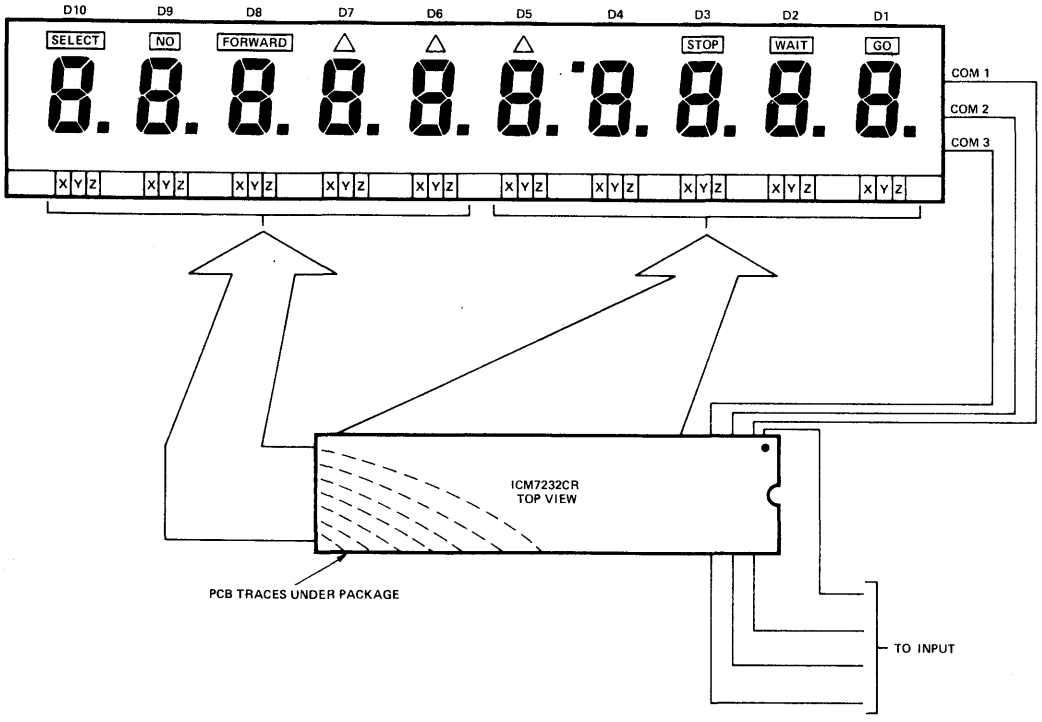


Figure 26. "Reverse" Pin Orientation and Display Connections

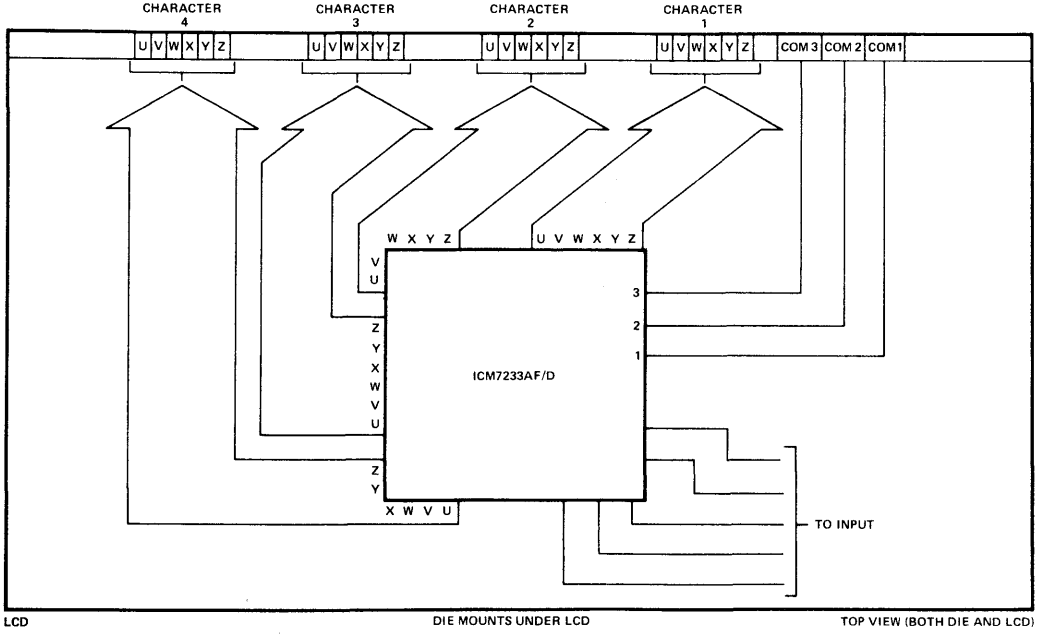
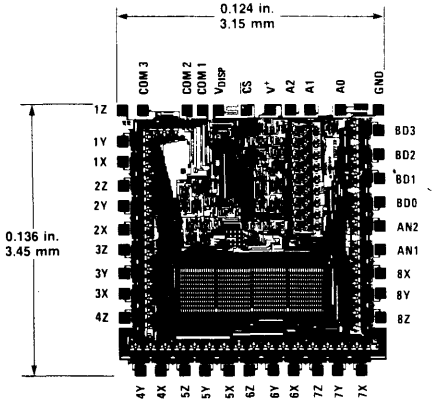
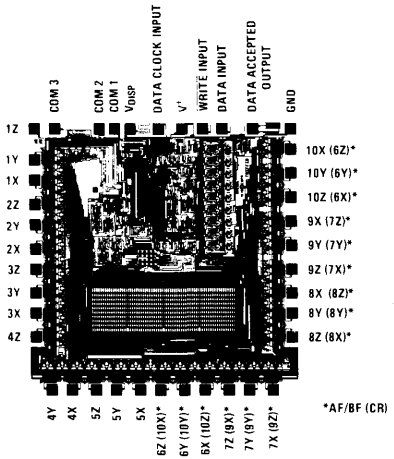


Figure 27. "Forward" Die Pad Orientation and Typical Triplex Alphanumeric Display Connections

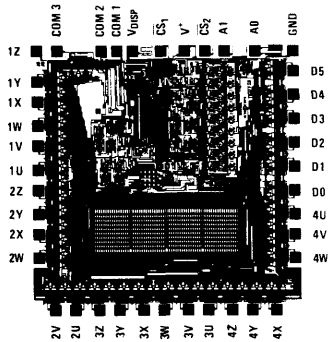
CHIP TOPOGRAPHY



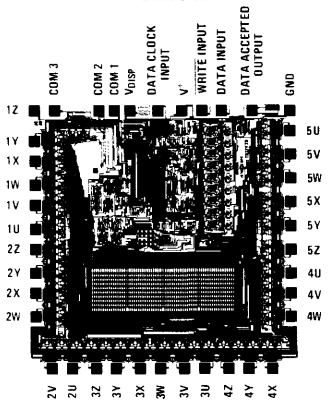
ICM7231



ICM7232



ICM7233



ICM7234

6

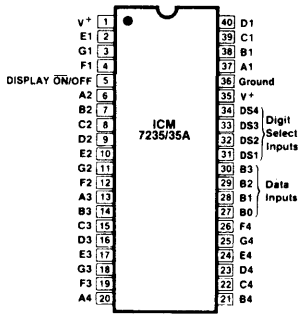
ICM7235

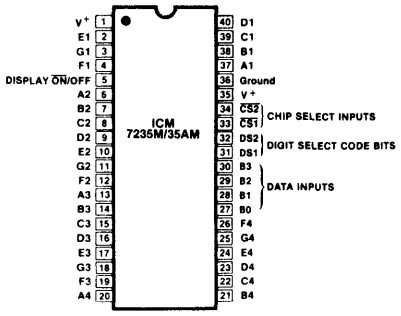
Four Digit Non-Multiplexed Vacuum Fluorescent Display Decoder/Drivers

FEATURES

- **28 high voltage segment drivers provide four 7-segment digits**
- **Multiplexed BCD input (7235)**
- **High speed processor interface (7235M)**
- **7-segment hex (0-9, A-F) or Code-B (0-9, dash, E, H, L, P, blank) output versions available**
- **Display blanking input**
- **All devices fabricated using high density MAX-CMOS™ LSI technology for very low-power, high-performance operation**
- **All inputs fully protected against static discharge**

PIN CONFIGURATIONS (outline dwg PL)





DESCRIPTION

The ICM7235 family of display driver circuits provides the user with a single chip interface between digital logic or microprocessors to non-multiplexed 7-segment vacuum fluorescent displays.

The chips provide 28 high voltage open drain P-channel transistor outputs organized as four 7-segment digits.

The devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the Intersil ICM7217, ICM7226 and ICL7135. The microprocessor interface devices (suffix M) provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output (0-9, A-F). The "A" versions provide the same output code as the ICM7218 Code "B" (0-9, dash, E, H, L, P, blank). Either device will correctly decode true BCD to seven-segment decimal outputs.

All devices in the ICM7235 family are packaged in a standard 40-pin plastic dual-in-line package.

The ordering information shows the four standard devices of the ICM7235 family and their markings, which serve as part numbers for ordering purposes.

ORDERING INFORMATION

Order Part Number	Output Code	Input Configuration
ICM7235 IPL	Hexadecimal	Multiplexed 4-Bit
ICM7235A IPL	Code B	Multiplexed 4-Bit
ICM7235M IPL	Hexadecimal	Microprocessor Interface
ICM7235AM IPL	Code B	Microprocessor Interface

An Evaluation Kit is available for this part.
Order number ICM7235 EV/Kit.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ +70°C
Supply Voltage (V^+ -Ground) ..... 6.5 Volts
Input Voltage (Note 2) ..... V^+ +0.3V, Ground −0.3V
Output Voltage (Note 3) ..... V^+ −35V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

All parameters measured with $V^+ = 5V$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Supply Current	I^+	Measured V^+ to Ground Test circuit; display blank or OFF		10	50	μA
Supply Current	I^+	Measured V^+ to Display			100	mA
Segment OFF Output Voltage	V_{SEG}	$I_{SLK} = 10\mu A$	30			V
Segment OFF Leakage Current	I_{LS}	$V_{SEG} = V^+ - 30V$		0.1	10	μA
Segment ON Current	I_{SEG}	$V_{SEG} = V^+ - 2V$	1.5	2.5		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}	Referred to Ground	3			V
Logical "0" Input Voltage	V_{IL}	Referred to Ground			1.5	V
Input Leakage Current	I_{ILK}	Pins 27-34		±0.1	±1	μA
Input Capacitance	C_{IN}	Pins 27-34		5		pF
$\overline{ON}$/OFF Input Leakage	$I_{ILK(\overline{ON}/OFF)}$	All Devices		±0.1	±1	μA
$\overline{ON}$/OFF Input Capacitance	$C_{IN(\overline{ON}/OFF)}$	All Devices		200		pF
AC CHARACTERISTICS — MULTIPLEXERD INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			ns
Inter-Digit Select Time	t_{ids}		2			μs
AC CHARACTERISTICS — MICROPROCESSOR INTERFACE						
$\overline{C}$hip $\overline{S}$elect Active Pulse Width	t_{csa}	Other $\overline{C}$hip $\overline{S}$elect either held active, or both driven together	200			ns
Data Setup Time	t_{dsm}		100			ns
Data Hold Time	t_{dhm}		10	0		ns
Inter-$\overline{C}$hip $\overline{S}$elect Time	t_{ics}		2			μs

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any input terminal to a voltage in excess of V^+ or ground may cause destructive device latch-up. For this reason, it is recommended that inputs from external sources operating on a different power supply be applied only after the device's own power supply has been established, and that on multiple supply systems the supply to the ICM7235 be turned on first.

NOTE 3: This value refers to the display outputs only.

INPUT DEFINITIONS

In this table, V^+ and ground are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One Ground = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One Ground = Logical Zero	Twos	
B2	29	V^+ = Logical One Ground = Logical Zero	Fours	
B3	30	V^+ = Logical One Ground = Logical Zero	Eights (Most Significant)	
$\overline{ON}$/OFF	5	V^+ = OFF, Ground = ON		Display $\overline{ON}$/OFF Input

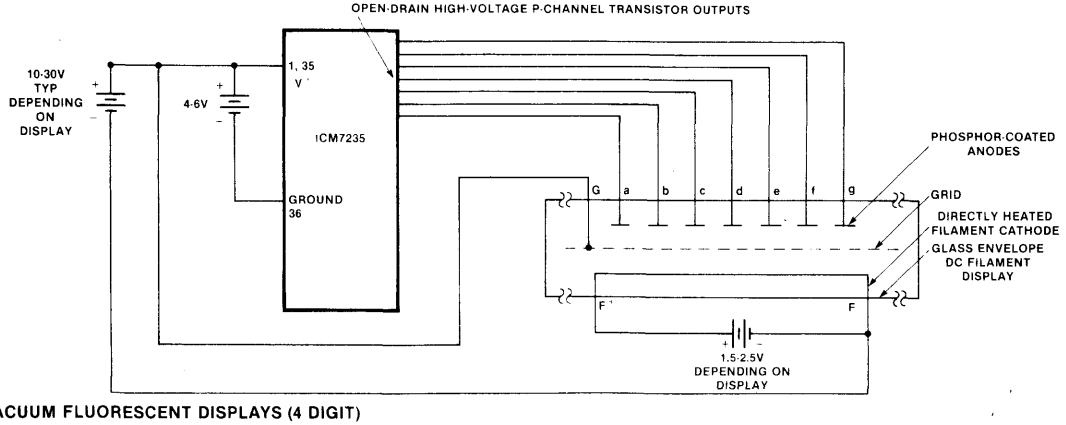
ICM7235, ICM7235A
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active Ground = Inactive	D1 (Least Significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most Significant) Digit Select

ICM7235M, ICM7235AM
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One Ground = Logical Zero	DS2 & DS1 serve as a two-bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V^+ = Inactive Ground = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken to ground, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

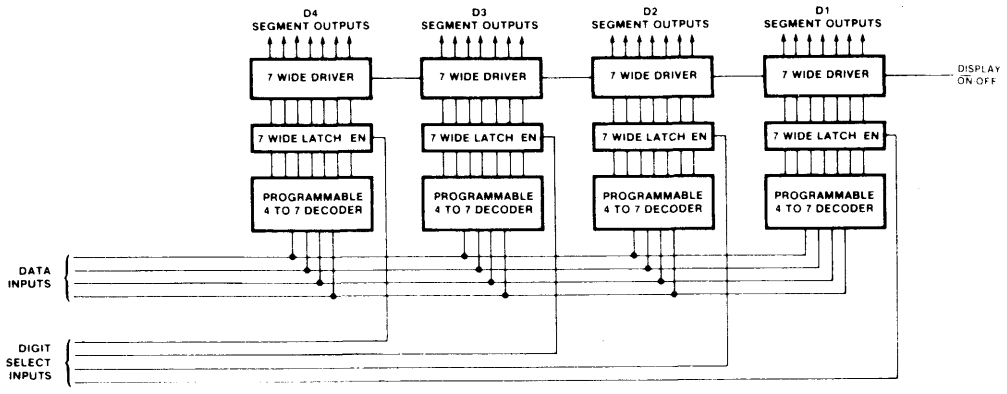
ICM7235 TYPICAL DC VACUUM FLUORESCENT DISPLAY CONNECTION



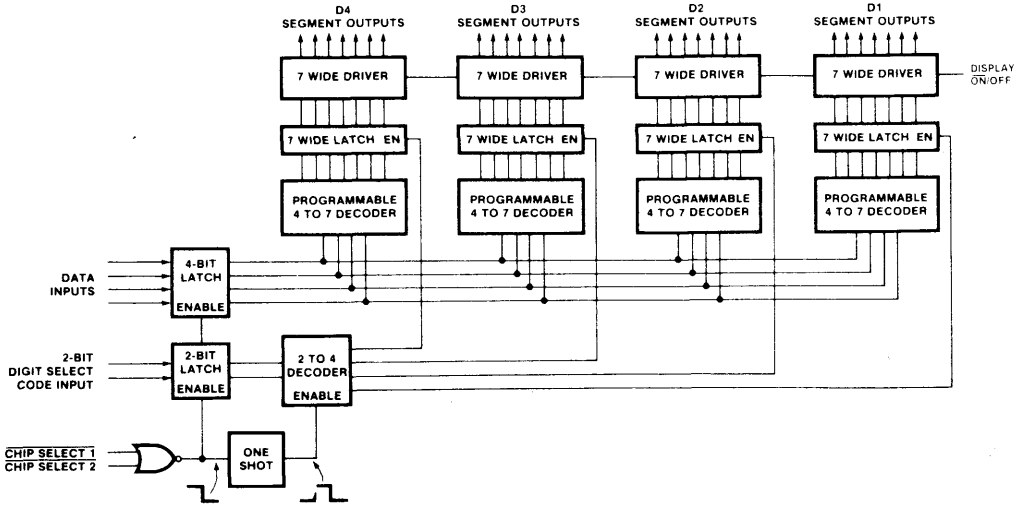
VACUUM FLUORESCENT DISPLAYS (4 DIGIT)

N.E.C. Electronics, Inc.
Models FIP4F8S and FIP5F8S

ICM7235/35A



ICM7235M/35AM



CIRCUIT DESCRIPTION

Each device in the ICM7235 family provides signals for directly driving the anode terminals of a four-digit, 7-segment non-multiplexed vacuum fluorescent display. The outputs are taken from the drains of high-voltage, low-leakage P-channel FETs, each capable of withstanding $> -35V$ with respect to V^+. In addition, the inclusion of an $\overline{ON}$/OFF input allows the user to disable all segments by connecting pin 5 to V^+; this same input may also be used as a brightness control by applying a signal swinging between V^+ and ground and varying its duty cycle.

The ICM7235 may also be used to drive non-multiplexed common cathode LED displays by connecting each segment output to its corresponding display input, and tying the common cathode to ground. Using a power supply of 5V and an LED with a forward drop of 1.7V results in an "ON" segment current of about 3mA, enough to provide sufficient brightness for displays of up to 0.3" character height.

Note that these devices have two V^+ terminals; each should be connected to the positive supply voltage. This double connection is necessary to minimize the effects of bond wire resistance, which could be a problem due to the high display currents.

Input Configurations and Output Codes

The standard devices in the ICM7235 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 through 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7235 and ICM7235M decode this binary input into a 7-segment alphanumeric hexadecimal output, while the ICM7235A and ICM7235AM decode the binary input into the same 7-segment output as the ICM7218 "Code B," i.e., 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a 7-segment decimal output.

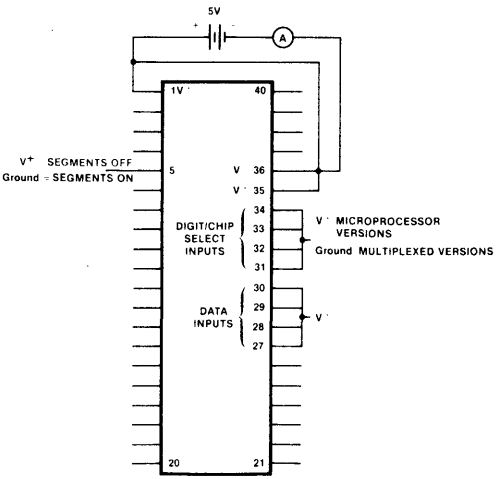
These devices are actually mask-programmable to provide any 16 combinations of the 7-segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact your Intersil Sales Office for details.

The ICM7235 and ICM7235A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate Digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one Digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Figure 2 and under Operating Characteristics for data setup, hold, and inter-digit select times must be met to ensure correct output.

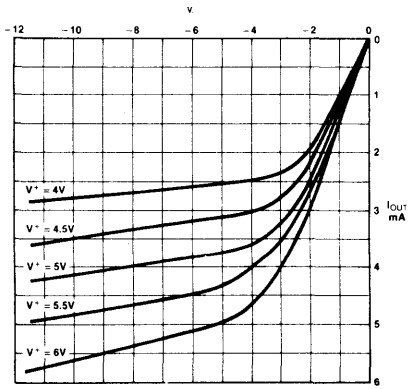
The ICM7235M and AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the 2-bit Digit Select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both Chip Select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken to ground. On the rising edge of either Chip Select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches. A select code of 00 writes into D4, 01 writes into D3, 10 writes into D2 and 11 writes into D1. The timing relationships for inputting data are shown in Figure 3, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS



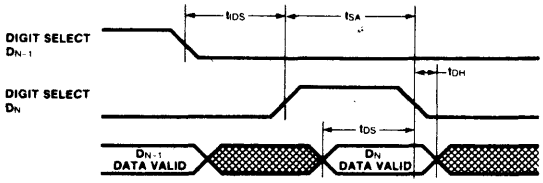


Figure 2. Multiplexed Input Timing Diagram

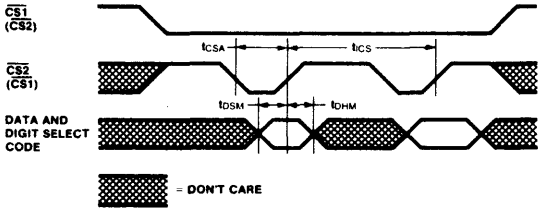


Figure 3. Microprocessor Interface Input Timing Diagram

Table 1: Output Codes

BINARY				HEXADECIMAL ICM7235 ICM7235M	CODE B ICM7235A ICM7235AM
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT

ICM7236
4½-Digit Counter With Vacuum Fluorescent Static Display Drivers

FEATURES

- **High frequency counting—guaranteed 15MHz, typically 25MHz at 5V**
- **Low power operation—less than 100μW quiescent**
- **Direct 4½-digit seven-segment display drive for non-multiplexed Vacuum Fluorescent displays**
- **$\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ inputs permit operation as frequency or period counter**
- **True $\overline{\text{COUNT INHIBIT}}$ disables first counter stage**
- **$\overline{\text{CARRY}}$ output for cascading four-digit blocks**
- **Schmitt-trigger on COUNT input allows operation in noisy environments or with slowly changing inputs**
- **Leading Zero Blanking INput and OUTput for correct leading zero blanking with cascaded devices**
- **All inputs fully protected against static discharge—no special handling precautions necessary**
- **Devices fabricated using MAXCMOS™ process for high-performance, low power operation**

DESCRIPTION

The ICM7236 and ICM7236A devices are high-performance CMOS 4½-digit counters, including decoders, output latches, count inhibit, reset, and leading zero blanking circuitry, and twenty-nine high-voltage open drain P-channel transistor outputs suitable for driving non-multiplexed (static) vacuum fluorescent displays.

The ICM7236 is a decade counter, providing a maximum count of 19999, while the ICM7236A is intended for timing purposes, providing a maximum count of 15959.

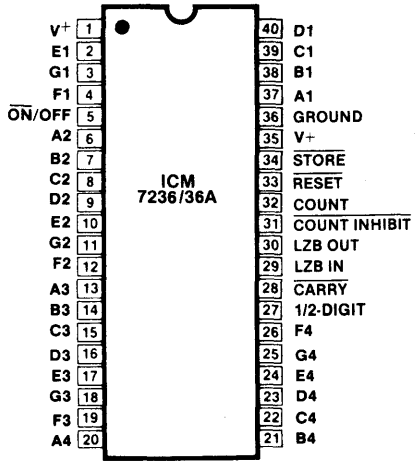
The counter section of the two devices in the ICM7236 family provides direct static counting from DC to 15MHz guaranteed (with a 5V ± 10% supply) over the operating temperature range. At normal room temperatures, the device will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allows a direct interface with the ICM7207 devices to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate features intended to simplify cascading in four-digit blocks. The $\overline{\text{CARRY}}$ output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allow correct leading zero blanking between four-decade blocks.

The ICM7236 and ICM7236A are packaged in a standard 40-pin dual-in-line plastic package.

6

PIN CONFIGURATION (outline dwg PL)



ORDERING INFORMATION

ORDER PART NUMBER	COUNT OPTION
ICM7236IPL	19999
ICM7236AIPL	15959
ICM7236 EV/KIT	(Evaluation Kit)

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ +70°C
Supply Voltage (V^+) ..... 6.5 V
Display Voltage (Note 3) ..... V^+ −35V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

(All parameters measured with $V^+ = 5V$ unless otherwise indicated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}	V^+	3	5	6	V
Operating Current	I_{OP}	Test circuit, Display blank		10	50	μA
Display Voltage	V_{DISP}				30	V
Display Output Leakage	I_{DLK}	Output OFF, $V = V^+ - 30V$		0.1	10	μA
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 $V = V^+ - 3V$		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			2	V
COUNT Input Threshold	V_{CT}			2		V
COUNT Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	$\overline{CARRY}$ (Pin 28), LZB OUT (Pin 30) $V_{OUT} = V^+ - 3V$.	350	500		μA
Output Low Current	I_{OL}	$\overline{CARRY}$ (Pin 28), LZB OUT (Pin 30) $V_{OUT} = +3V$.	350	500		μA
Count Frequency	f_{count}	$4.5V < V^+ < 6V$	0	25	15	MHz
$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width	t_S, t_W		3			μs

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than ground may cause destructive device latch-up. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7236/7236A be turned on first.

NOTE 3: This limit refers to the display output terminals only.

DESCRIPTION OF OPERATION

All of the chips in the ICM7236 family provide twenty-nine outputs suitable for directly driving the anode terminals of 4½ digit seven-segment non-multiplexed (static) vacuum-fluorescent displays. Each display output is the drain of a high-voltage low-leakage P-channel transistor, capable of withstanding typically greater than −35 volts with respect to V^+. The output characteristics are shown graphically under "Typical Characteristics."

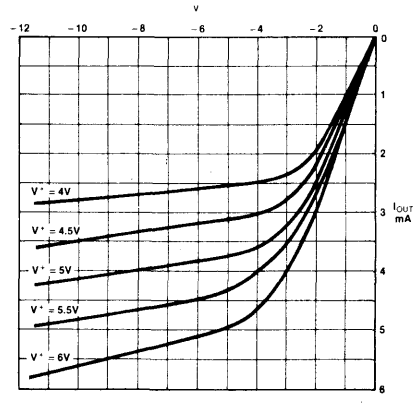
These chips also provide a dislay $\overline{ON}$/OFF input which may be used to disable all the segment outputs and thus blank the display. This input may also be used to control the display brightness by varying the duty cycle of a signal at the input swinging between V^+ and ground.

NOTE that these circuits have two terminals for V^+; both of these pins should be connected to the power supply positive terminal. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

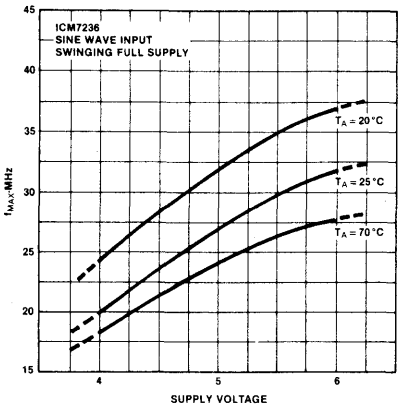
These chips may also be used to directly drive non-multiplexed common-cathode LED displays, where each segment of the display is driven by one ICM7236 output, and the common cathode is connected to ground. With a 5V power supply and a 1.7V LED diode forward voltage drop, the current in an "ON" segment will be typically 3mA. This should provide sufficient brightness in displays up to about 0.3" character height.

TYPICAL CHARACTERISTICS

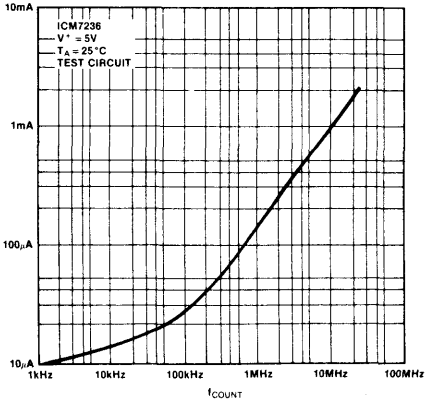
Output Characteristics



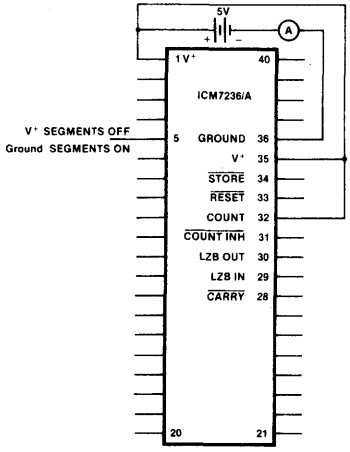
Maximum Count Frequency (Typical) as a Function of Supply Voltage



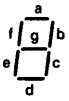
Supply Current as a Function of Count Frequency



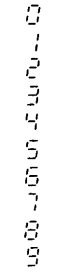
TEST CIRCUIT



SEGMENT ASSIGNMENT



DISPLAY FONT



COUNTER SECTION

The devices in the ICM7236 family implement a four-digit ripple-carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the carry signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, and the $\overline{\text{CARRY}}$ output will provide a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ disables the first divide-by-two in the counter chain without affecting its clock. This provides a true **count** inhibit which is not sensitive to the state of the COUNT input, preventing false counts which can result from using a normal logic gate forcing the state of the clock to prevent counting.

Each decade drives directly into a four-to-seven decoder which derives the seven-segment output code. Each decoder output corresponds to the one-segment terminal of the device. The output data is latched at the driver; when the $\overline{\text{STORE}}$ pin is at a negative level, these latches are updated, and when the pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating, or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the Leading Zero Blanking INput is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, which can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, on an eight-decade counter with overflow using two ICM7236 devices, the Leading Zero Blanking OUTput of the high-order digit device would be connected to the Leading Zero Blanking INput of the low-order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7236 devices in four-digit blocks.

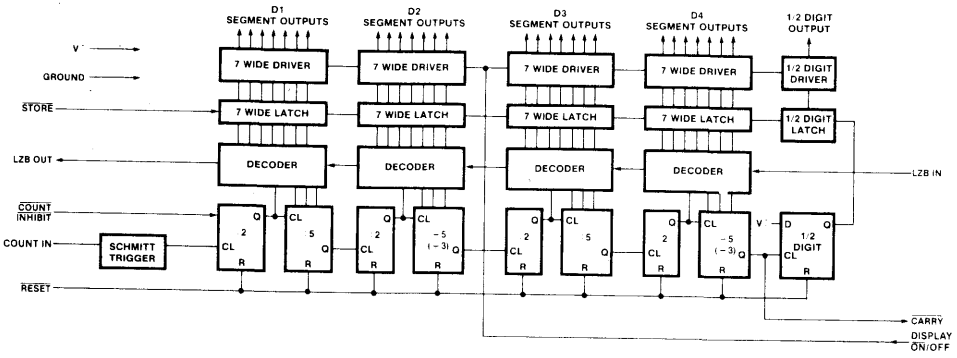
CONTROL INPUT DEFINITIONS

In this table, V^+ and ground are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

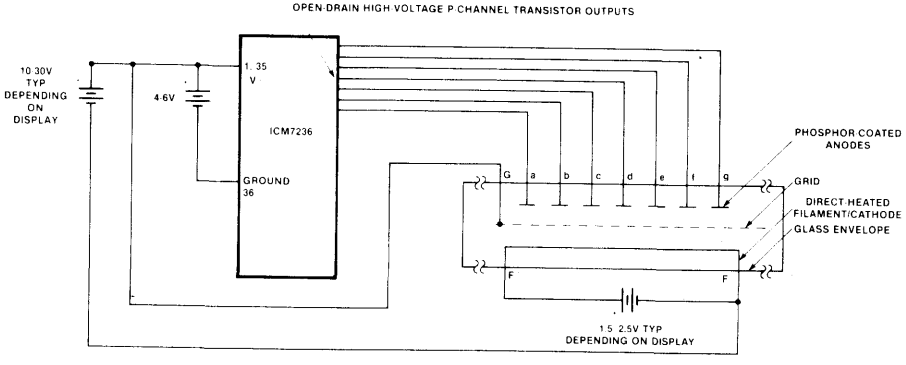
OPERATING CHARACTERISTICS

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking Input (LZB IN)	29	V^+ or Floating Ground	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V^+ or Floating Ground	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V^+ or Floating Ground	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V^+ or Floating Ground	Output Latches Not Updated Output Latches Updated
Display $\overline{\text{ON}}$/OFF	5	V^+ Ground	Display Outputs Disabled Display Outputs Enabled

BLOCK DIAGRAM



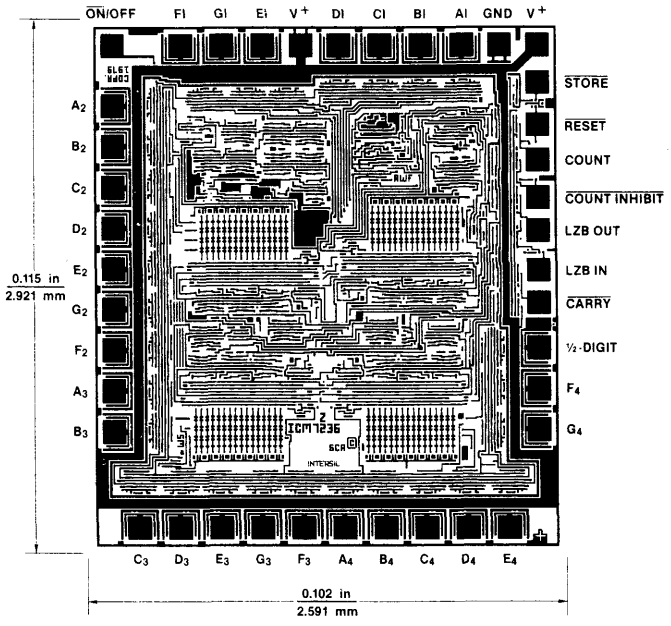
TYPICAL DC VACUUM FLUORESCENT DISPLAY CONNECTION



VACUUM FLUORESCENT DISPLAYS (4½-DIGIT):
N.E.C. Electronics, Inc.
Model FIP5F8S

ICM7236

CHIP TOPOGRAPHY



6

ICM7240/50/60 CMOS Programmable Timers/Counters

FEATURES

- **Replaces 8240/50/60, 2240 in most applications**
- **Timing from microseconds to days**
- **May be used as fixed or programmable counter**
- **Programmable with standard thumbwheel switches**
- **Select output count from**
  1RC to 255RC (ICM7240)
  1RC to 99RC (ICM7250)
  1RC to 59RC (ICM7260)
- **Monostable or astable operation**
- **Low supply current: 115μA @ 5 volts**
- **Wide supply voltage range: 2-16 volts**
- **Cascadeable**

GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICL 8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

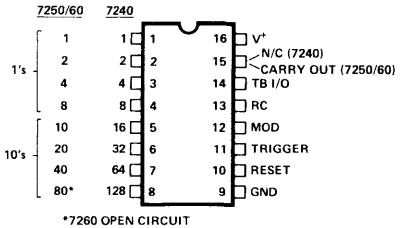
6

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240/D		Dice Only
ICM7250/D		Dice Only
ICM7260/D		Dice Only

PIN CONFIGURATION (OUTLINE DRAWING JE)

ICM7240, 7250, 7260



*7260 OPEN CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage[1]
Terminals 10,11,12,13,14 ..... GND -0.3V to $V^+ + 0.3V$

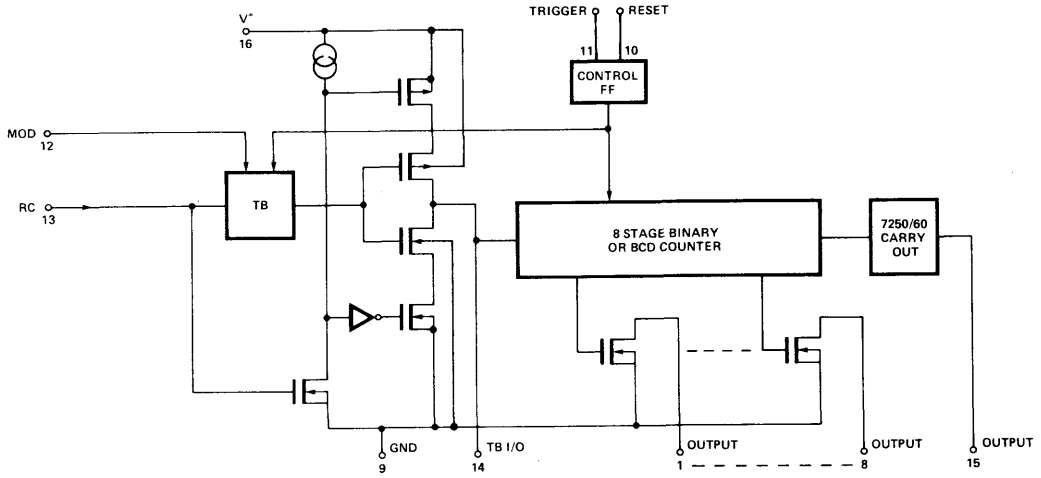
Maximum continuous output current (each output) ..... 50 mA
Power Dissipation[2] ..... 200 mW
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50/60 be turned on first.
2. Derate at -2 mW/°C above 25°C.

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM

ICM7240/50/60



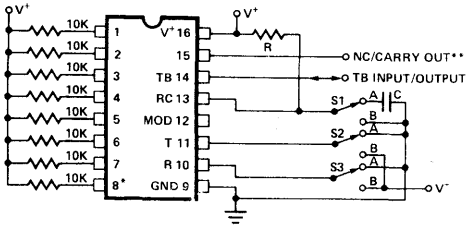
ELECTRICAL CHARACTERISTICS

Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, $R = 10K\Omega$, $C = 0.1\mu F$		300	700	μA
		Operating, $R = 1M\Omega$, $C = 0.1\mu F$		120	500	μA
		TB Inhibited, RC Connected to GND		125		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	$I_{SOURCE} = 1$ mA	3.5	4.2		V
		$I_{SINK} = 3.2$ mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level	V_{MOD}	$V^+ = 5V$		3.5		V
		$V^+ = 15V$		11.0		V
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Max Count Toggle Rate 7240	f_t	$V^+ = 2V$ (Counter/Divider Mode)	2	1		MHz
		$V^+ = 5V$ (Counter/Divider Mode)		6		MHz
		$V^+ = 15V$ (Counter/Divider Mode)		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Max Counter Toggle Rate 7250, 7260	f_t	$V^+ = 5V$ (Counter/Divider Mode)	1.5	5		MHz
Max Count Toggle Rate 7240, 7250, 7260	f_t	Programmed Timer — Divider Mode			100	KHz
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, $I_{OUT} = 3.2$ mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	$V^+ = 5V$, per Output			1	μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$	1K		22M	Ω
		$V^+ \leq 16V$	1K		22M	Ω

TEST CIRCUIT

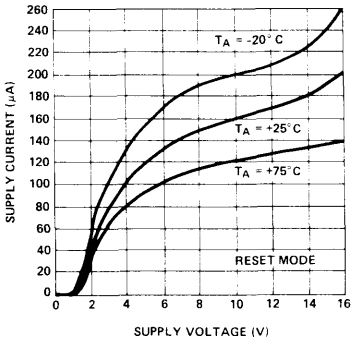


S1–A = RC RUN, B = T. B. INPUT RUN
S2–A = INACTIVE, B = TRIGGER
S3–A = INACTIVE, B = RESET

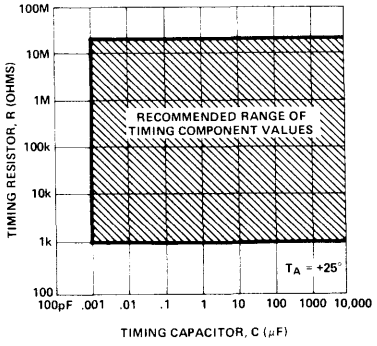
NOTE: S1-B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.
* * TERMINAL 15 IS CARRY OUTPUT FOR 7250/60 DEVICES.
* TERMINAL 8 IS OPEN CIRCUIT FOR 7260.

TYPICAL PERFORMANCE CHARACTERISTICS

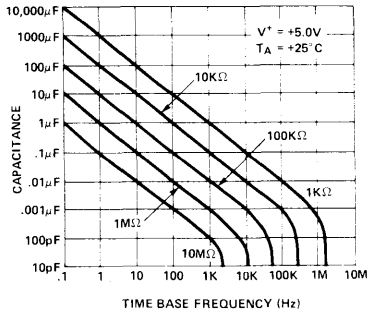
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



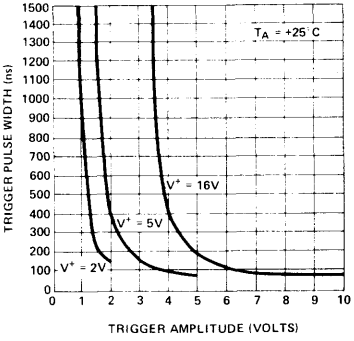
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



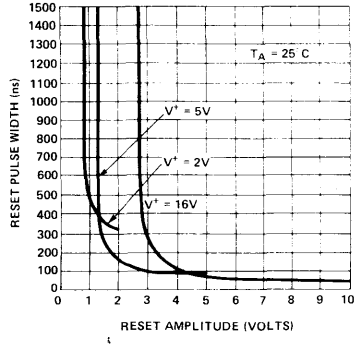
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



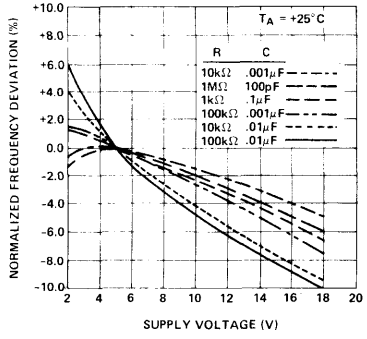
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE

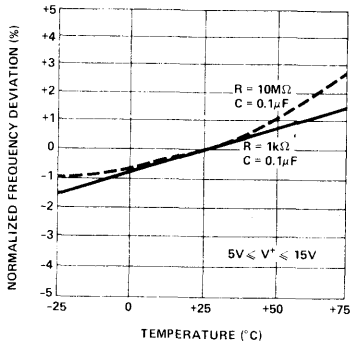


NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE

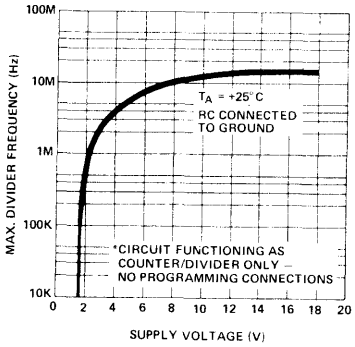


TYPICAL PERFORMANCE CHARACTERISTICS

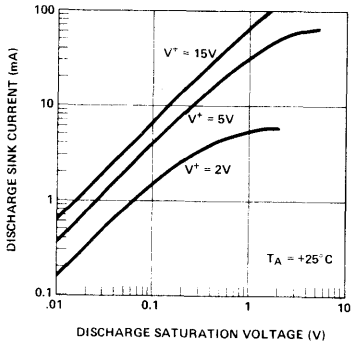
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



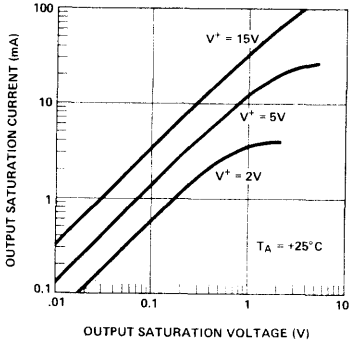
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE*



DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



DESCRIPTION OF PIN FUNCTIONS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 1). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.

GROUND (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by positive going control pulses applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

MODULATION AND SYNC INPUT (PIN 12)

The period t of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12.

TIMEBASE INPUT/OUTPUT PIN (TERMINAL 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input terminal if terminal 13 (RC) is connected to GND.

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50/60 is used to replace an 8240/50/60 or 2240.

CARRY OUTPUT (TERMINAL 15, ICM7250/60 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 or 7260 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50/60 are shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. See Figure 3.

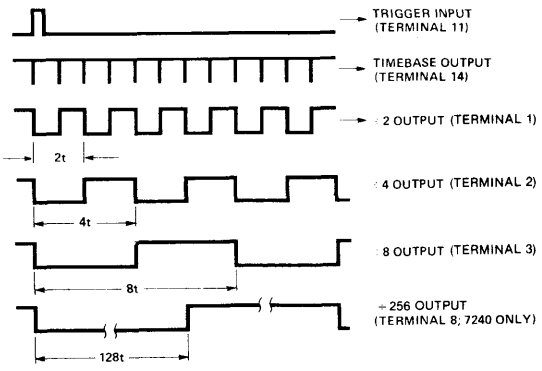


Figure 1. Timing Diagram for ICM7240/50/60

CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state, and starts the time base oscillator. Then, external C is charged through external R from 20% to 70% of V^+, generating a timing waveform with period t, equal to 1_{RC}. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250/60. The timing cycle terminates when a positive-going reset pulse is applied to pin 10. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carrry-out is also HIGH.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal; the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit operates in its astable, or free-running mode, after initial triggering.

PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain N-channel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as **any one** of the outputs is low. Each output is capable of sinking ≈5 mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) t_o would be 32t for a 7240 and 20t for a 7250/60. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $t_o = (1 + 16 + 32)t$ for the 7240 or $(1 + 10 + 20)t$ for the 7250/60. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

$1t \leq t_o \leq 255t$ (7240)
$1t \leq t_o \leq 99t$ (7250)
$1t \leq t_o \leq 59t$ (7260)

Note that for the 7250 and 7260, invalid count states (BCD values ≥ 10) will not be recognized and the counter will not stop.

The 7240/50/60 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see figure 2. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 2, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 1, which shows the phase relations between the counter outputs. Figure 3 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 and ICM7260 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of 1_{RC} to 99_{RC}. Cascading two ICM7250's (using the carry out gate) would expand selection to 9999_{RC}. For a ICM7260, there are standard BCD thumbwheel switches for the 0 through 5 digit (twelve position 0 to 5 repeated).

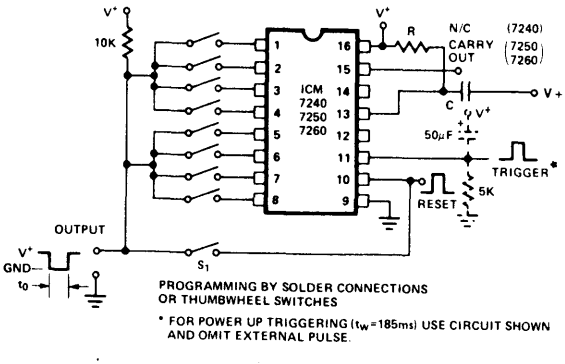


Figure 2. Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

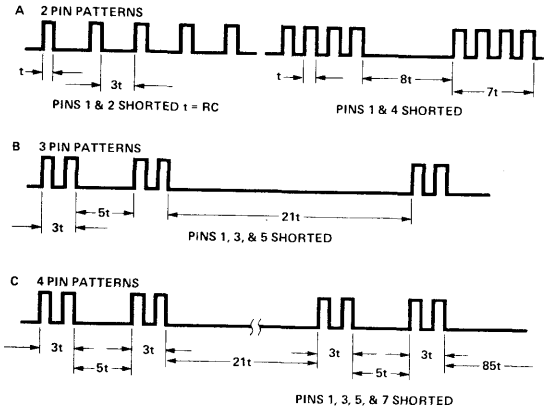


Figure 3. Pulse Patterns Obtained by Shorting Various Counter Outputs

NOTES ON THE COUNTER SECTION

Used as a straight binary counter (ICM7240), as a ÷100 (ICM7250), or ÷60 (ICM7260) all devices are significantly faster than their bipolar equivalents. However, when using these devices as *programmable* counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), 100 (ICM7250), or 60 (ICM7260) the maximum input frequency must be limited to approximately 100 KHz or less (with V+ equal to +5 volts). The reason for this is two-fold:

a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter (8 counters for the ICM7240/50 and 7 for the ICM7260). Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the Reset/Trigger signal.

b. There must be a delay of the positive going output to the Reset terminal, (pin 10) and the Trigger terminal (pin 11). The Reset signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The trigger overrides Reset.

The delay between Trigger and Reset is generated by the signal RC network consisting of the 56kΩ resistor and the 330pF capacitor.

The delay caused by the counter Ripple delays can be as long as 2μs (5 volt supply), and the delay between Reset and Trigger should be at least 2 μs. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 4 and 5.

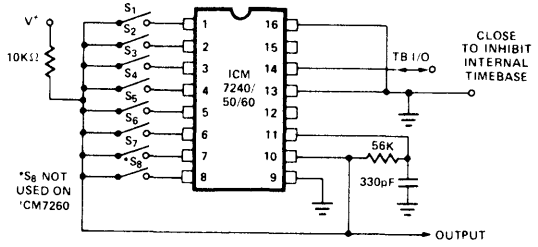


Figure 4. Programming the Counter Section of the ICM7240/50/60

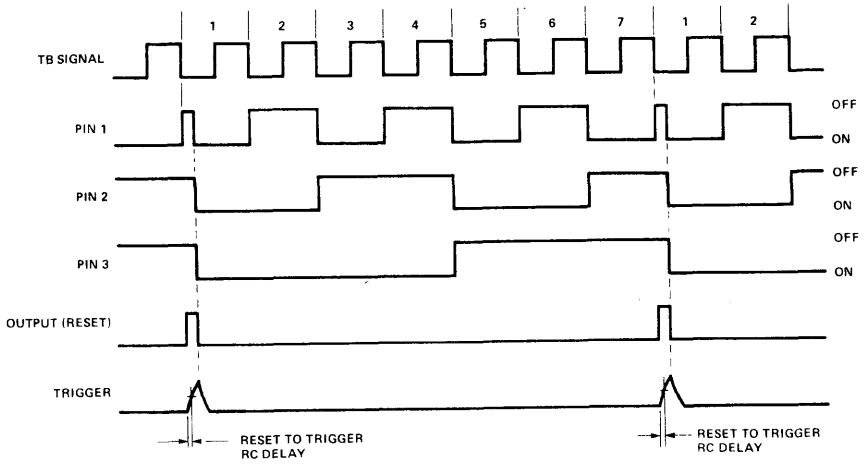


Figure 5. Waveforms for Programming the Counter Section for a Division Ratio of 7 (S_1, S_2, S_3 Closed)

APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V^+ may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200 KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time $\leq 1\mu s$); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50/60.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C , a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

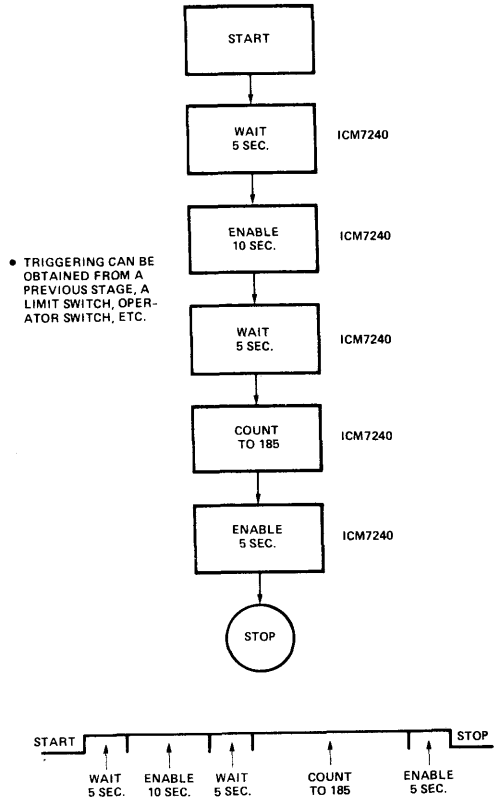


Figure 6.

CMOS PRECISION PROGRAMMABLE 0-99 SECONDS/MINUTES LABORATORY TIMER

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown, the timer can accurately measure preselected time intervals of 0-99 seconds or 0-99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0-99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the pre-programmed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.

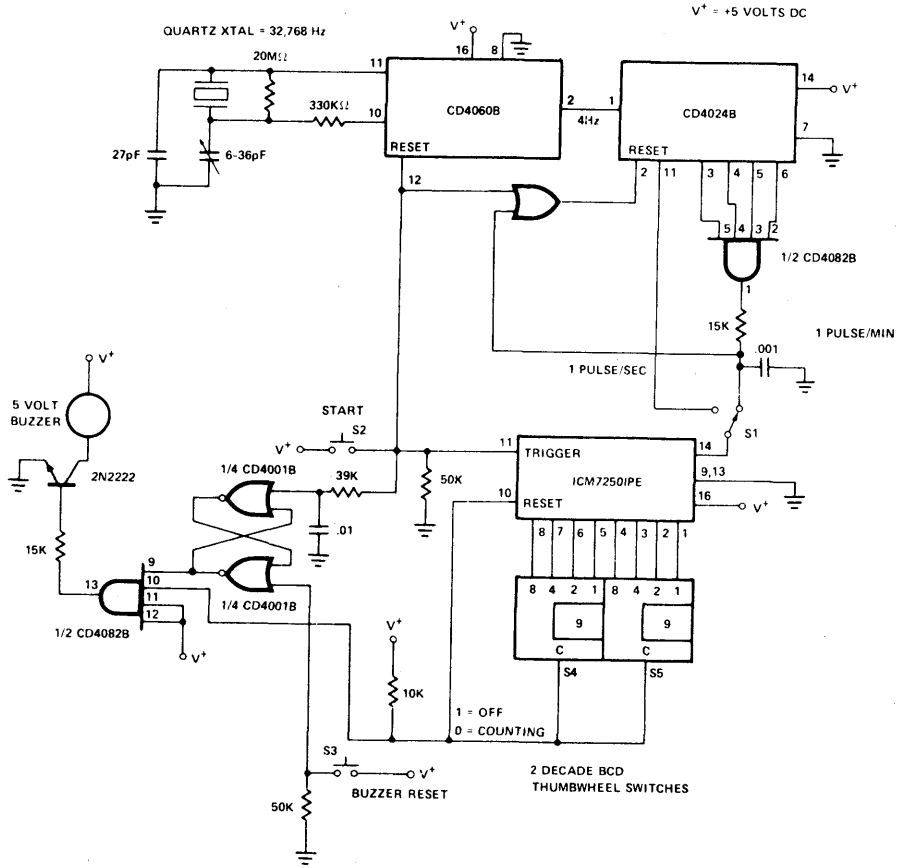


Figure 7.

LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four $\overline{\text{WRITE}}$ pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

With a resistor of approximately 10 MΩ and capacitor of 0.1 μF, the time base of the ICM7240 is one second. Thus, a time of 1-255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.

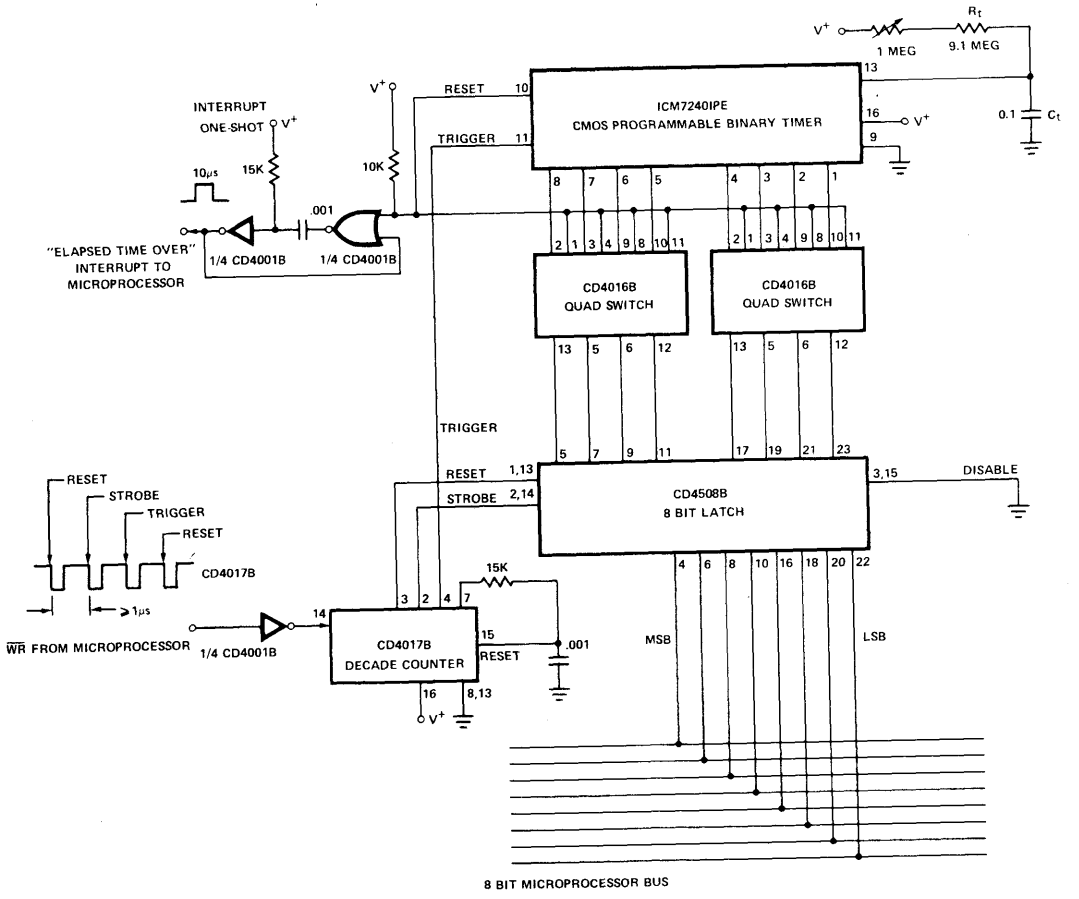
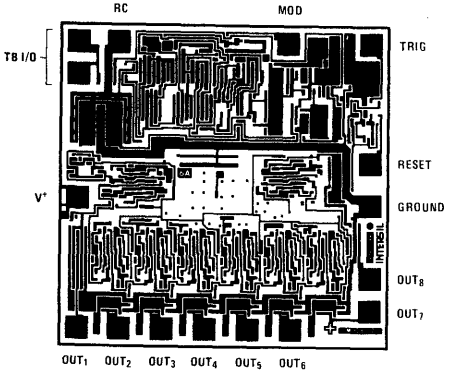
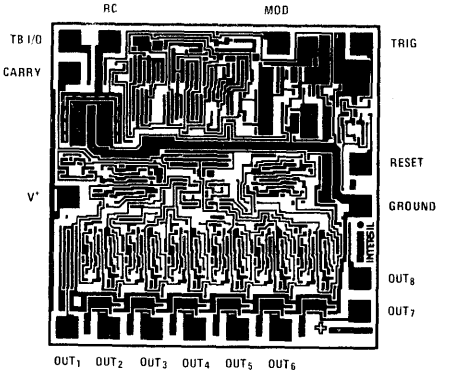


Figure 8.

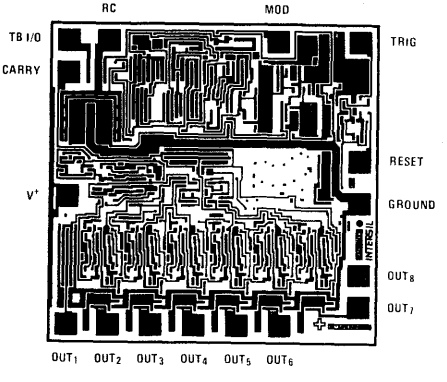
CHIP TOPOGRAPHY



ICM7240



ICM7250



ICM7260

ALL CHIPS 68 x 69 mils

ICM7242
Long Range
Fixed Timer/Counter

FEATURES

- **Replaces the 2242 in most applications**
- **Timing from microseconds to days**
- **Cascadeable**
- **Monostable or astable operation**
- **Wide supply voltage range: 2-16 volts**
- **Low supply current: 115μA @ 5 volts**
- **Extended temperature range: -20° C to +85° C**

GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in 95% of the applications, with a significant reduction in the number of external components.

Three outputs are provided. They are, the oscillator output, and buffered outputs from the first and eighth counters.

The ICM7242 is packaged in an 8-pin CERDIP.

ABSOLUTE MAXIMUM RATINGS

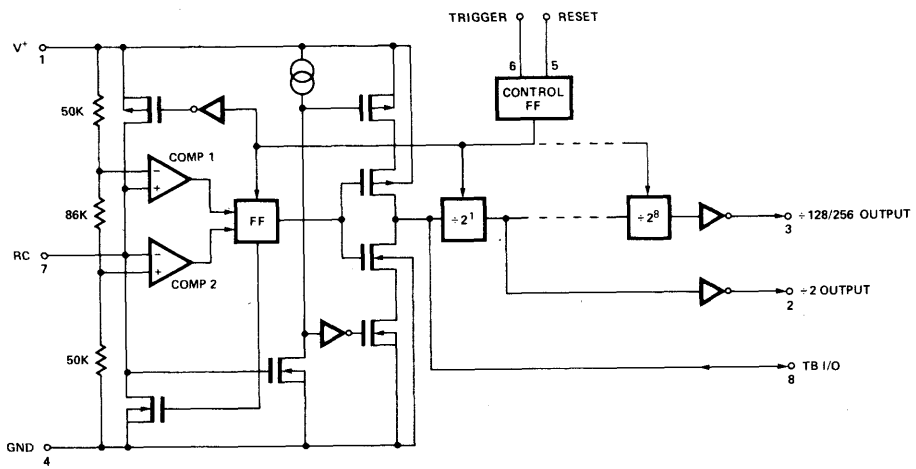
Supply Voltage 18V
Input Voltage[1]
Terminals (Pins 5, 6, 7, 8) ..... GND -0.3V to V^+ + 0.3V
Maximum continuous output current (each output) ..... 50 mA
Power Dissipation[2] ..... 200 mW
Operating Temperature Range ..... -20° C to +85° C
Storage Temperature Range ..... -55° C to +125° C

NOTES:
1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply by applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. Derate at -2 mW/° C above 25° C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

6

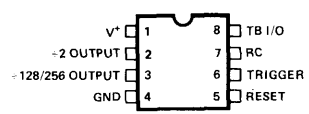
BLOCK DIAGRAM



ORDERING INFORMATION

Device: ICM7242IJA
Dice: ICM7242/D

PIN CONFIGURATION (OUTLINE DRAWING JA)

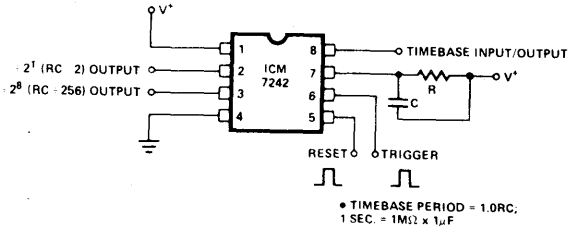


ELECTRICAL CHARACTERISTICS

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, $R = 10K\Omega$, $C = 0.1\mu F$		340	800	μA
		Operating, $R = 1M\Omega$, $C = 0.1\mu F$		220	600	μA
		TB Inhibited, RC Connected to GND		225		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	Independent of RC Components		250		ppm/°C
Time Base Output Voltage	V_{OTB}	$I_{SOURCE} = 1$ mA	3.5	4.2		V
		$I_{SINK} = 3.2$ mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Trigger/Reset Input Current	I_{TRIG}, I_{RST}			10		μA
Max Count Toggle Rate	f_t	$V^+ = 2V$	2	1		MHz
		$V^+ = 5V$ Counter/Divider Mode		6		MHz
		$V^+ = 15V$		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, $I_{OUT} = 3.2$ mA		0.22	0.4	V
Output Sourcing Current 7242	I_{SOURCE}	$V^+ = 5V$ Terminals 2 & 3, $V_{OUT} = 1V$		300		μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ = 2 - 16V$	1K		22M	Ω

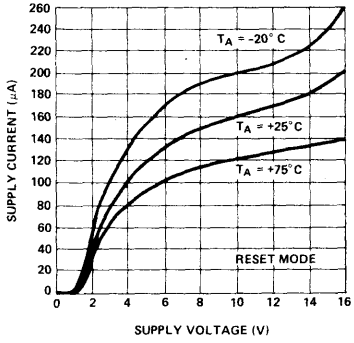
TEST CIRCUIT



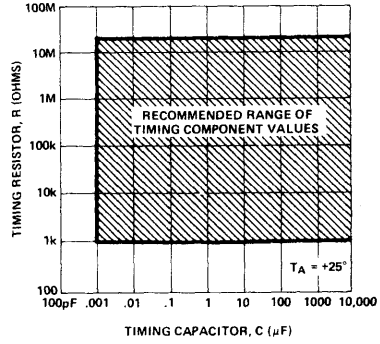
NOTE: OUTPUTS $\div 2^1$ AND $\div 2^8$ ARE INVERTERS AND HAVE ACTIVE PULLUPS.

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

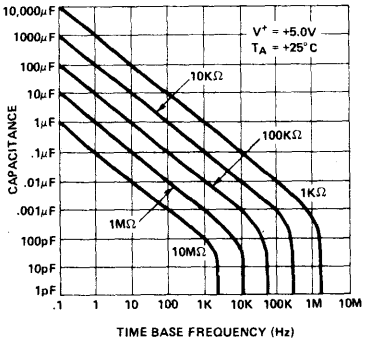


RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

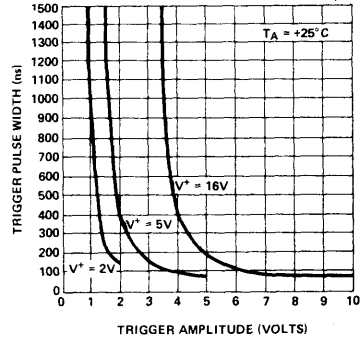


DIMENSIONS IN INCHES AND MILLIMETERS

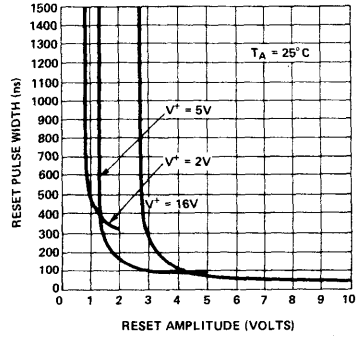
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



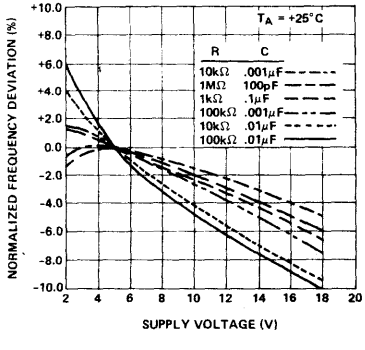
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE

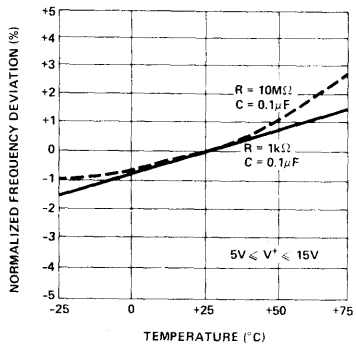


NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

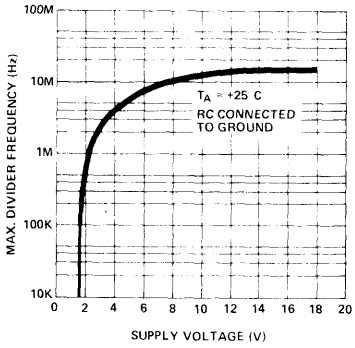


TYPICAL PERFORMANCE CHARACTERISTICS

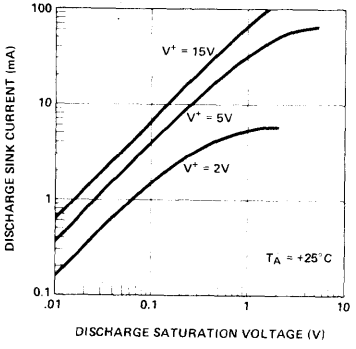
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



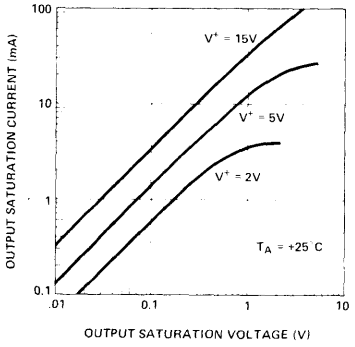
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V^+ may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

OPERATING LIMITS

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200 KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge

on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\div 2^8$ output returns to the high state.

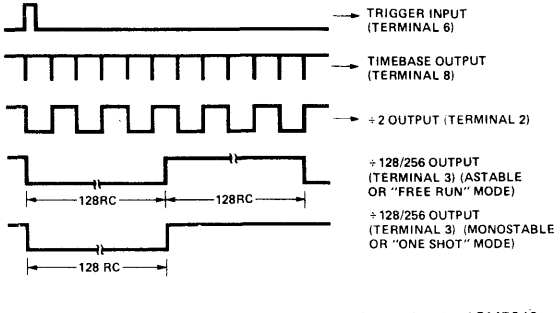


Figure 1. Timing Diagrams of Output Waveforms for the ICM7242. (Compare with Figure 5)

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.

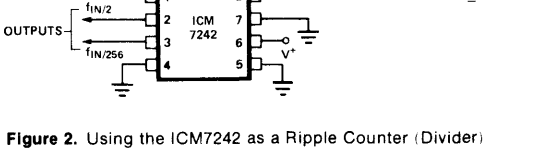


Figure 2. Using the ICM7242 as a Ripple Counter (Divider)

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 3).

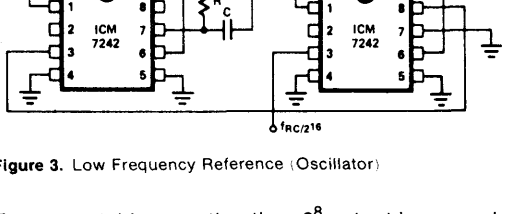


Figure 3. Low Frequency Reference (Oscillator)

For monostable operation the $\div 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p⁻resistors have been used on the ICM7242 to provide the comparator timing points.

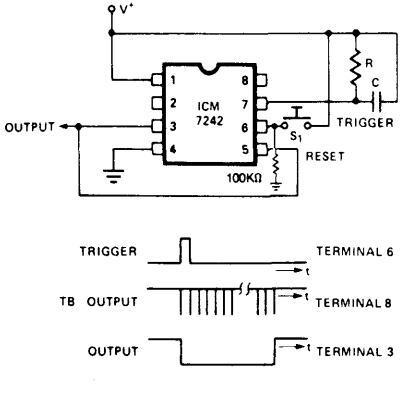


Figure 4. Monostable Operation

COMPARING THE ICM7242 WITH THE 2242

		ICM7242	2242
a.	Operating Voltage	2-16V	4-15V
b.	Commercial Temp. Range	-20° C to +75° C	0° C to +75° C
c.	Supply Current $V^+ = 5V$	0.7 mA Max.	7 mA Max.
d.	Pullup Resistors		
	TB Output	No	Yes
	÷2 Output	No	Yes
	÷256 Output	No	Yes
e.	Toggle Rate	3.0 MHz	0.5 MHz
f.	Resistor to Inhibit Oscillator	No	Yes
g.	Resistor in Series with Reset for Monostable Operation	No	Yes
h.	Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C , a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

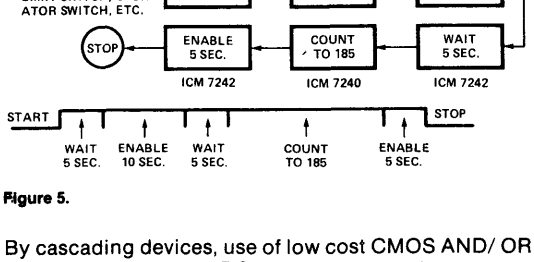


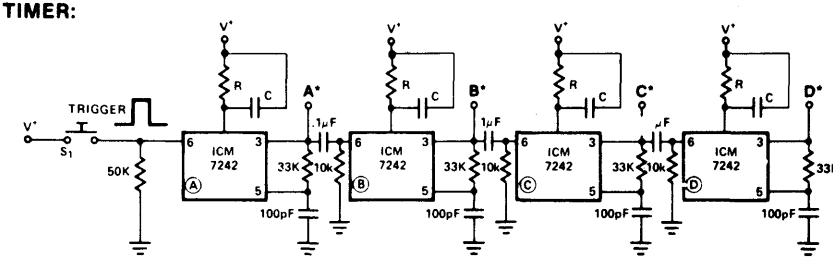
Figure 5.

By cascading devices, use of low cost CMOS AND/ OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

SEQUENCE TIMING

- Process Control
- Machine Automation
- Electro-pneumatic Drivers
- Multi-operation (Serial or Parallel controlling)

SEQUENCE TIMER:



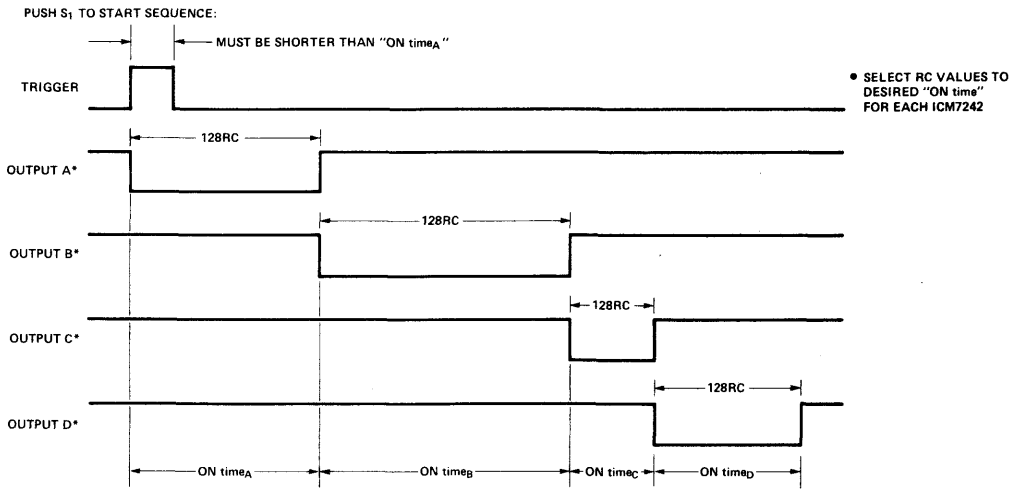
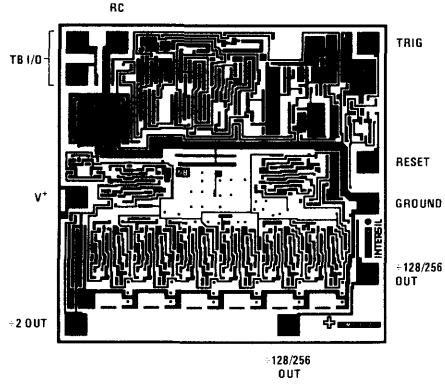


Figure 6.

CHIP TOPOGRAPHY (.068" × .069")



ICM7243

8-Character 14-/16-Segment Alphanumeric LED Display Driver

FEATURES

- **14- and 16-segment fonts with decimal point**
- **Mask programmable for other font-sets up to 64 characters**
- **Microprocessor compatible**
- **Directly drives small common cathode displays**
- **Cascadable without additional hardware**
- **Standby feature turns display off; puts chip in low power mode**
- **Serial entry or random entry of data into display**
- **Single +5V operation**
- **Character and segment drivers, all MUX scan circuitry, 8 x 6 static memory and 64-character ASCII font generator included on-chip**

GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it offloads the processor and minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, an 8 x 6 memory, the high power character and segment drivers, and the multiplex scan circuitry.

Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Serial** (MODE = 1) or **Random** (MODE = 0). In the **Serial Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

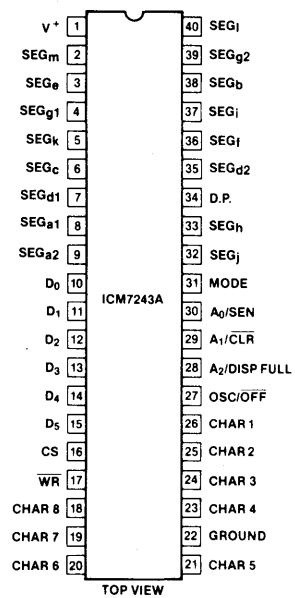
The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

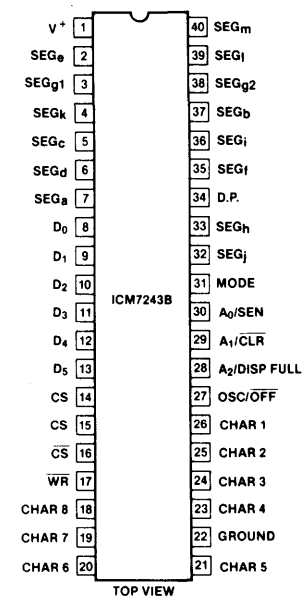
ORDERING INFORMATION

Part Number	Display Segments	Package	Order Number
ICM7243A	16 + d.p.	40 Pin CERDIP	ICM7243AIJL
ICM7243B	14 + d.p.	40 Pin CERDIP	ICM7243BIJL
ICM7243B EV/KIT	Kit with Display		ICM7243B EV/KIT

6

PIN CONFIGURATIONS





ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
CHARacter Output Current 300mA
SEGment Output Current 30mA
Input Voltage (Any Terminal) ..... $(V^+ + 0.3V)$ to $-0.3V$
Power Dissipation 1W
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Voltage	V^+		4.75	5.0	5.25	V
Operating Supply Current	I^+_{OP}	$V^+ = 5.25V$, 10 Segments ON, All 8 Characters		180		mA
Quiescent Supply Current	$I_Q{}^+$	$V^+ = 5.25V$, OSC/$\overline{OFF}$ Pin < 1V		30	250	μA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	$V^+ = 5.25V$, $V_{IH} = 5V$			+1	μA
		$V_{IL} = 0V$	−1			
CHARacter Drive Current	I_{CHAR}	$V^+ = 5V$, $V_{OUT} = 1V$	140	190		mA
CHARacter Leakage Current	I_{CHLK}					μA
SEGment Drive Current	I_{SEG}	$V^+ = 5V$, $V_{OUT} = 2.5V$	14	19		mA
SEGment Leakage Current	I_{SLK}			0.01		μA
DISPlay FULL Output Low	V_{OL}	$I_{OL} = 1.6mA$			0.4	V
DISPlay FULL Output High	V_{OH}	$I_{IH} = 100\mu A$	2.4			V
Display Scan Rate	f_{ds}			400		Hz

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AC CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V)

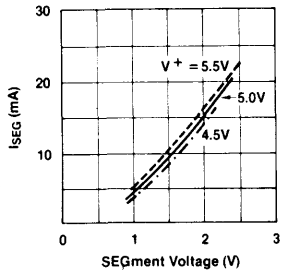
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low	t_{WPl}		250			ns
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High	t_{WPh}		250			
Data Hold Time	t_{Dh}		0	−20		
Data Setup Time	t_{Ds}		250	150		
Address, SEN, MODE Hold Time	t_{Ah}		125	80		
Address, SEN, MODE Setup Time	t_{As}		−20			
CS, $\overline{CS}$ Setup Time	t_{Cs}		0			
Pulse Transition Time	t_t				100	

CAPACITANCE

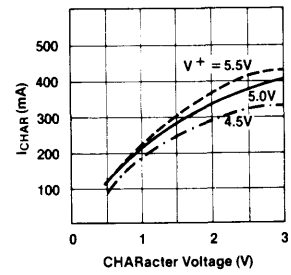
SYMBOL	TEST	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance				pF
C_O	Output Capacitance				pF

TYPICAL PERFORMANCE CURVES

SEGment Current vs Output Voltage

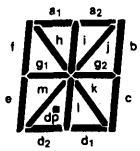


CHARacter Current vs Output Voltage



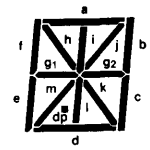
ICM7243A/B DISPLAY FONT, SEGMENT ASSIGNMENTS

Note: Some display manufacturers use different designations for some of the segments. Check data sheets carefully.



D5, D4		0 0	0 1	1 0	1 1
	D3	0	0	1	1
	D2	0	1	0	1
	D1	0	1	0	1
	D0	0	1	0	1

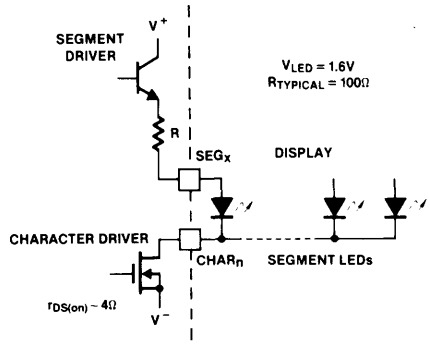
ICM7243A
16-Segment Character Font with Decimal Point



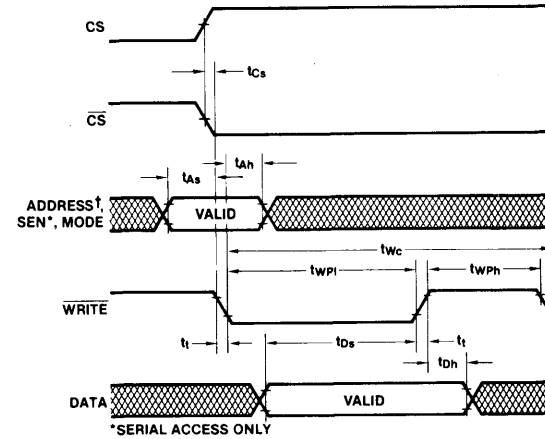
D5, D4		0 0	0 1	1 0	1 1
	D3	0	0	1	1
	D2	0	0	1	1
	D1	0	1	0	1
	D0	0	1	0	1

NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

ICM7243B
14-Segment Character Font with Decimal Point



Segment and Character Drivers Output Circuit

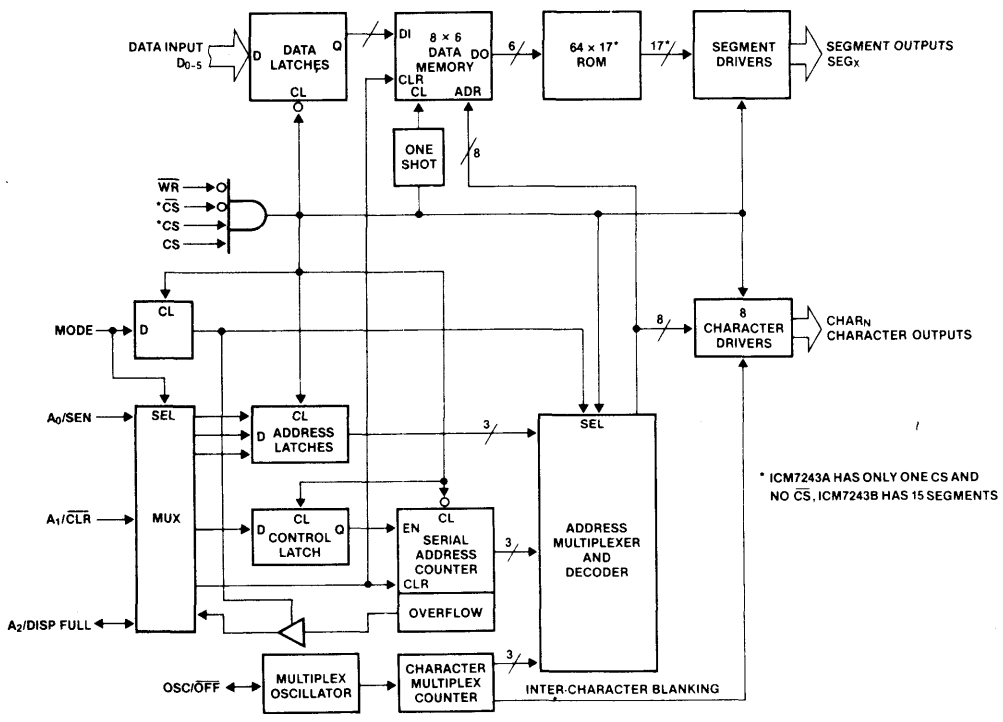


Data Entry Timing

PIN DESCRIPTIONS, ICM7243A *(B)*

SIGNAL	PIN	FUNCTION
D_0-D_5	10-15 *(8-13)*	Six-Bit ASCII Data input pins (active high).
CS, $\overline{CS}$	16 *(14-16)*	Chip Select for decoding from μP address bus, etc.
$\overline{WR}$	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and $\overline{WR}$ can be used as $\overline{CS}$.
MODE	31	Selects data entry MODE. High selects **Serial Access (SA)** mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the **Random Access (RA)** mode where data is displayed on the character addressed via A_0-A_2 Address pins.
A_0/SEN	30	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading display driver/controllers for displays of more than 8 characters (active high enables driver controller).
A_1/$\overline{CLeaR}$	29	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A_2/DISPlay FULL	28	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	27	OSCillator input pin. Adding capacitance to V^+ will lower the internal oscillator frequency. An external oscillator is also applied to this pin. A low puts the display controller/driver into a quiescent mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG_a-SEG_m, D.P.	2-9 *(7)*, 32-40	SEGment driver outputs.
CHARacter 1-8	18-21, 23-26	CHARacter driver outputs.

BLOCK DIAGRAM



DETAILED DESCRIPTION OF OPERATION

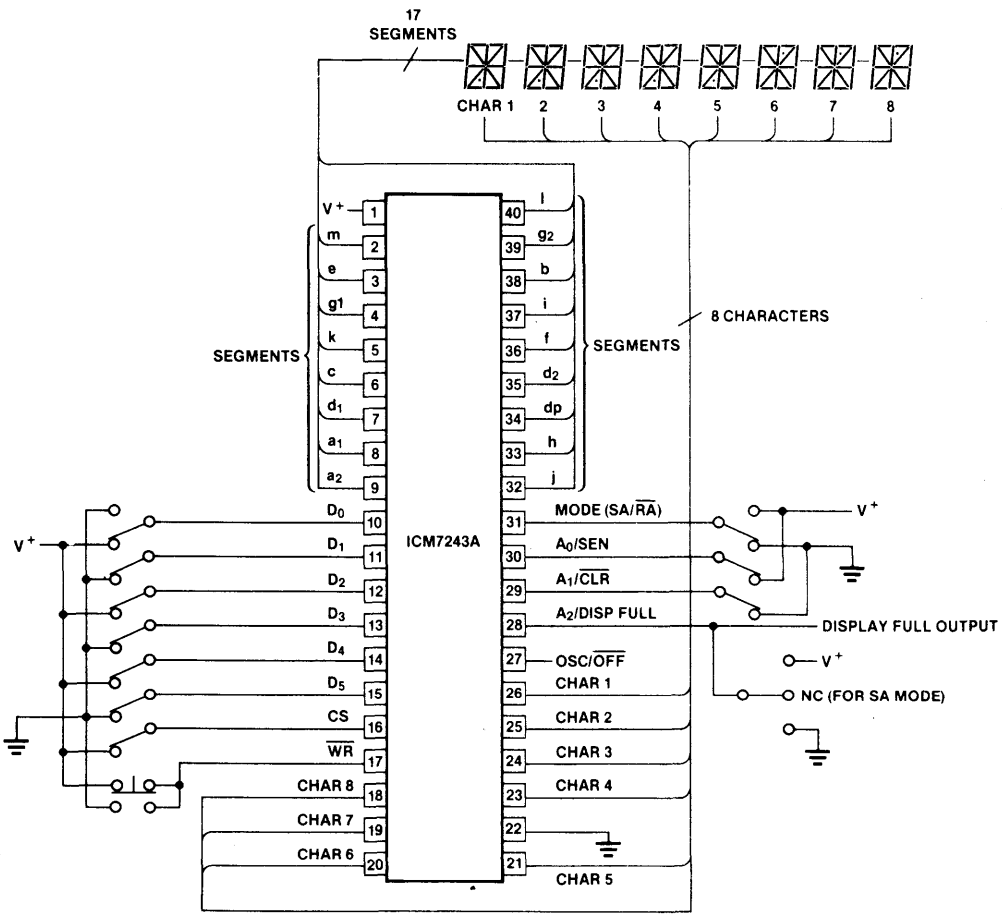
$\overline{WR}$, $\overline{CS}$, CS. These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS and $\overline{CS}$ enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5nsecs) greater than from $\overline{WR}$ or $\overline{CS}$ due to the additional inverter required on the former.

MODE. The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see above). The location in Data Memory where incoming data will be placed is determined either from the Address pins or the Serial Address Counter, under control of this latch, which also controls the function of A_0/SEN, $A_1/\overline{CLR}$, and A_2/DISPlay FULL.

Random Access Mode. When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A_0, A_1, and A_2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Serial Access Mode. If the internal latch is set for **Serial Access (SA),** (MODE latched high), the Serial ENable input on SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Serial Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output is always active in **SA** mode also, and indicates the overflow status of the Serial Address Counter. If this output is low, and SEN is (latched as) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur. This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Serial Access** mode.

TEST CIRCUIT (ICM7243A SHOWN)



Changing Modes. Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of $\overline{WR}$ (or its equivalent). When changing mode from **Serial Access** to **Random Access,** note that A_2/DISPlay FULL will be an output until $\overline{WR}$ has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Serial Access**, $A_1/\overline{CLR}$ should be high to avoid inadvertent clearing of the Data Memory and Serial Address Counter. DISPlay FULL will become active immediately after the falling edge of $\overline{WR}$.

Data Entry. The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/$\overline{OFF}$. The device includes a one-pin relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V^+ at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter strobe lines (see **Display Output**). An inter-character blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Multiplex Counter. This puts the circuit in a low-power-dissipation passive condition in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output. The address output of the Multiplex Counter is multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in **Serial Access** mode, with SEN high and DISPlay FULL low), to control display operations. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5μsec). Each CHARacter output lasts nominally about 300μsec, and is repeated nominally every 2.5msec, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL low for **Serial Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

6 APPLICATIONS

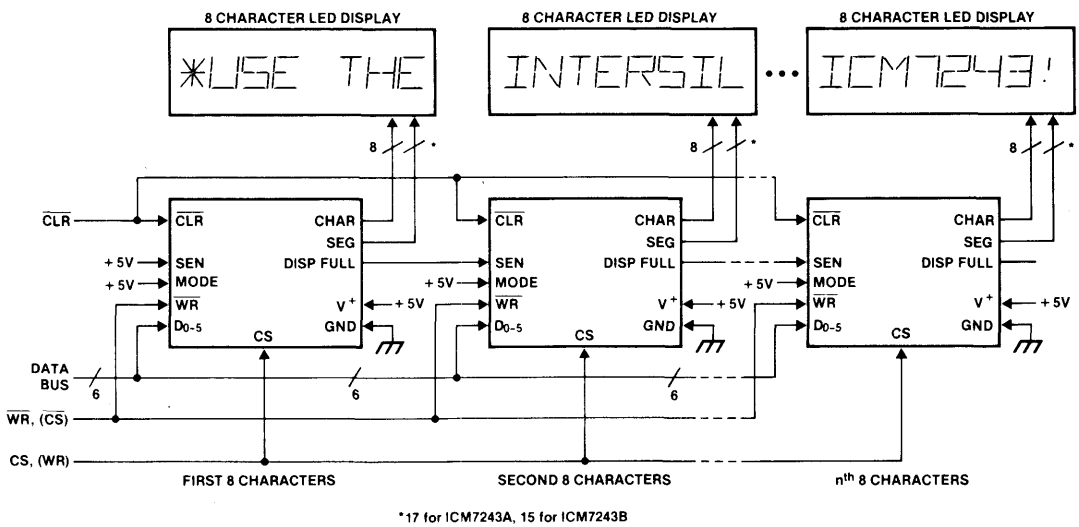


Figure 1. Multicharacter Display using Serial Access Mode

APPLICATIONS (Continued)

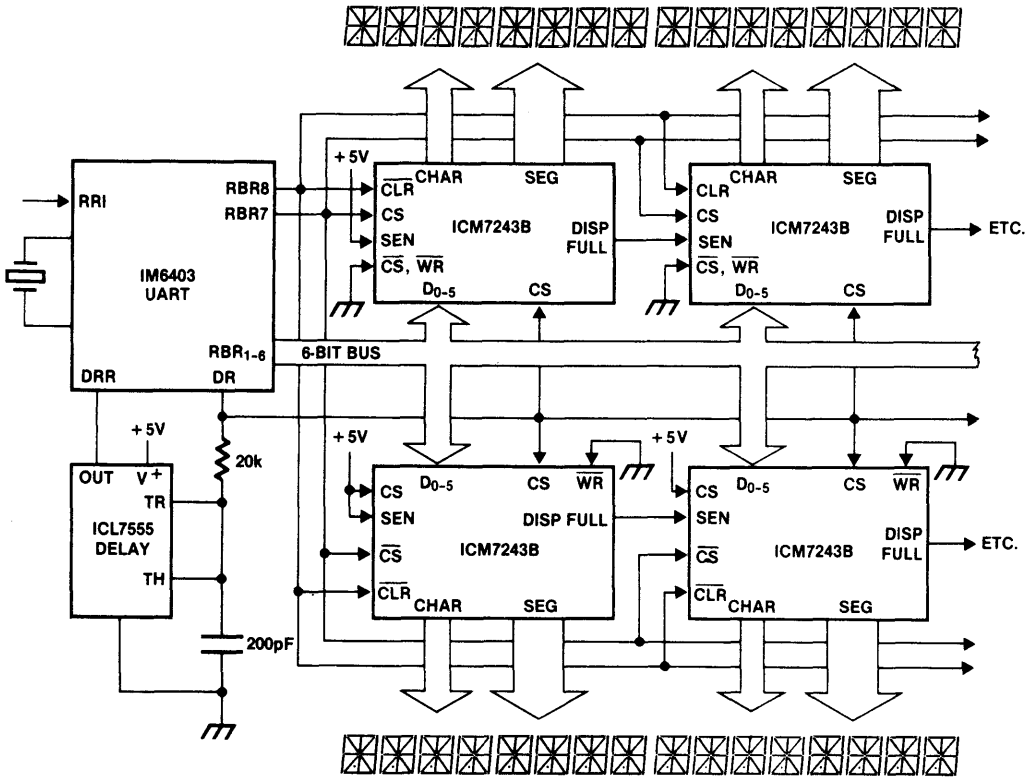


Figure 2. Driving Two Rows of Characters from a Serial Input. UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

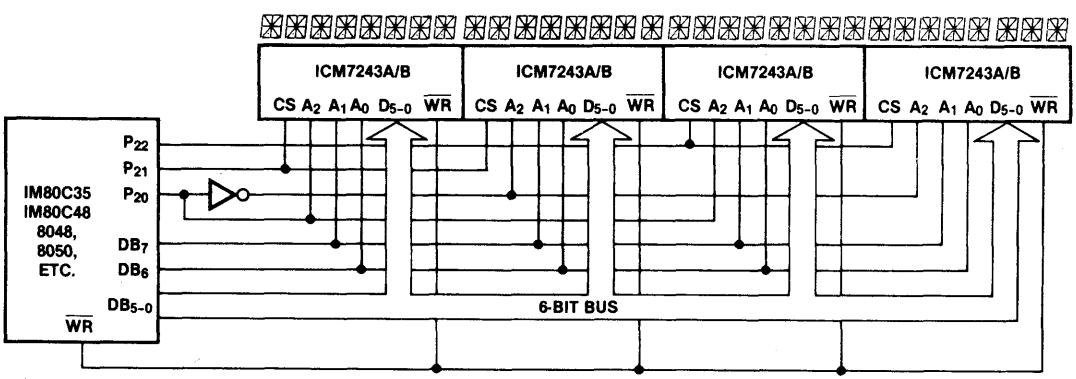


Figure 3. Random Access 32-Character Display in MCS-48 system. One port line controls A_2, other two are CS lines. 8-bit data bus drives 6 data and 2 address lines. MODE should be GrouNDed on each part.

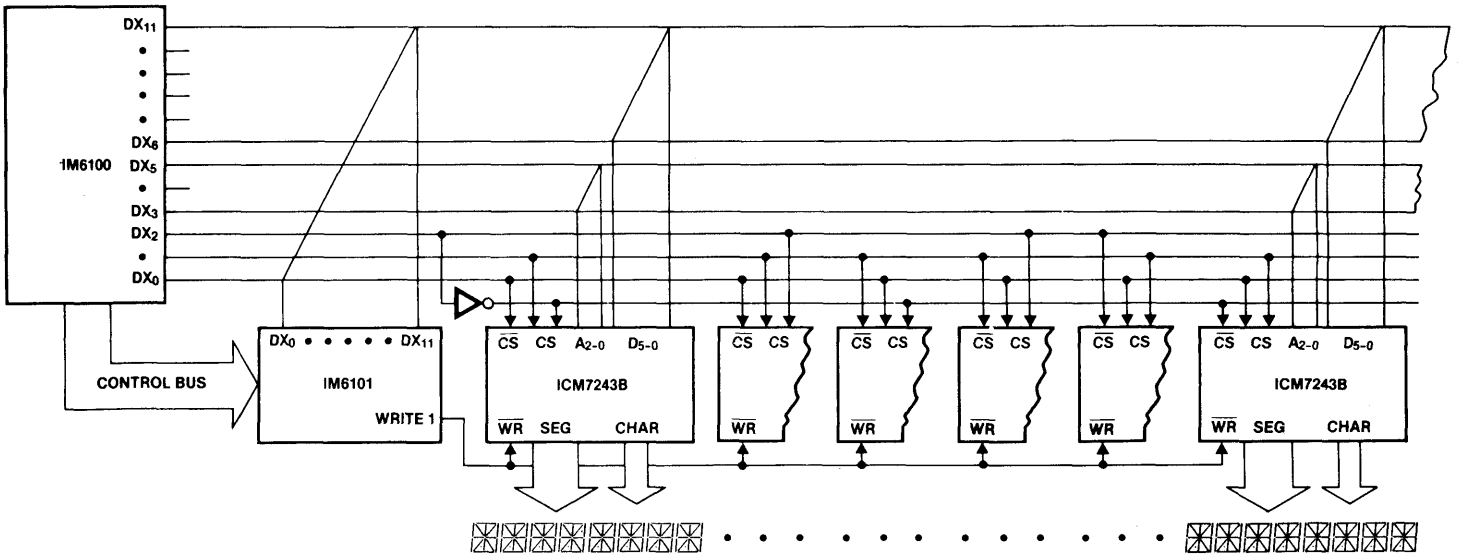
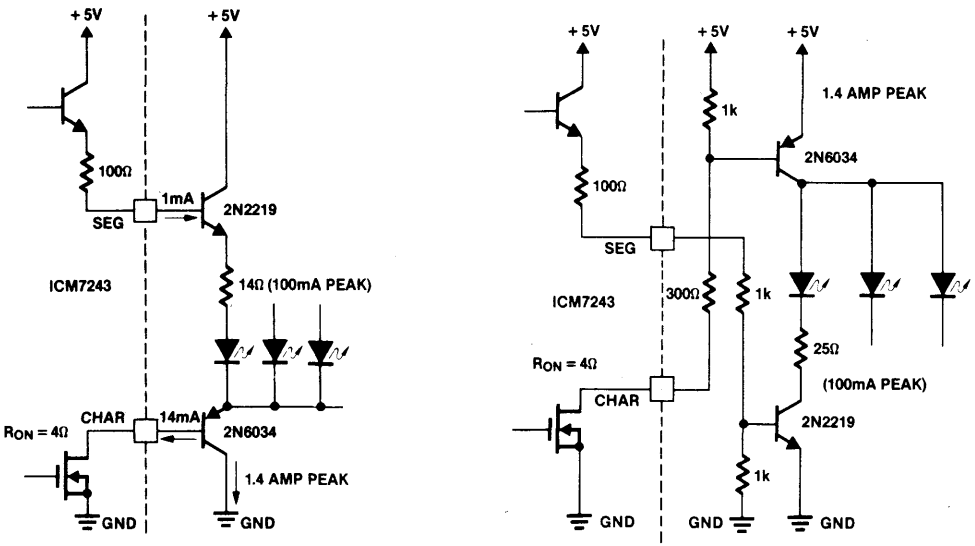


Figure 4. A 48-Character Random Access Display. 12-bit bus split into 6 bits data, 3 bits address within chip, and 3 bits chip address. Inverting one of these chip address lines allows selection of one of 6 chips without decode, using CS and $\overline{CS}$ lines on ICM7243B. Standard 1-of-8 decoder can select 64-character array using ICM7243A/B. WRITE 2 can be used for another row in either case.

APPLICATIONS (Continued)



(5a.) Common Cathode Displays

(5b.) Common Anode Displays

Figure 5. Driving Large Displays. The circuits of Figures 5a and 5b can be used to drive 0.5″ or larger alphanumeric displays, either common cathode (5a) or common anode (5b).

6

COMPONENT SELECTION

Displays suitable for use with the ICM7243 may be obtained from the following manufacturers; among others:

Hewlett Packard Components, Palo Alto, California
(415) 857-6620 (part #HDSP6508, HDSP6300)

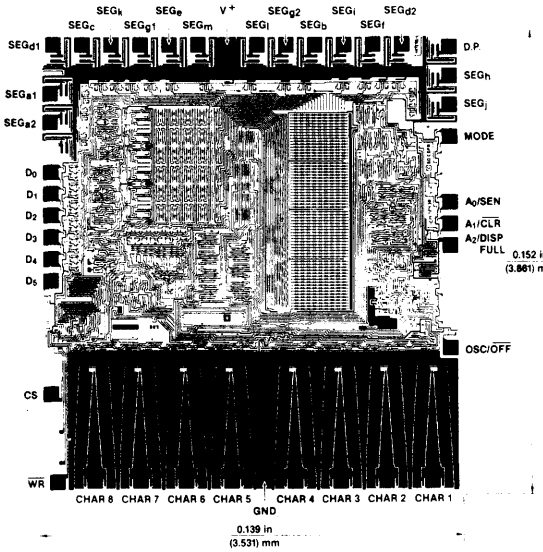
General Instruments Inc., Palo Alto, California
(415) 493-0400 (part #MAN2815)

Texas Instruments Inc., Dallas, Texas
(214) 995-6611 (part #HDSP6508)

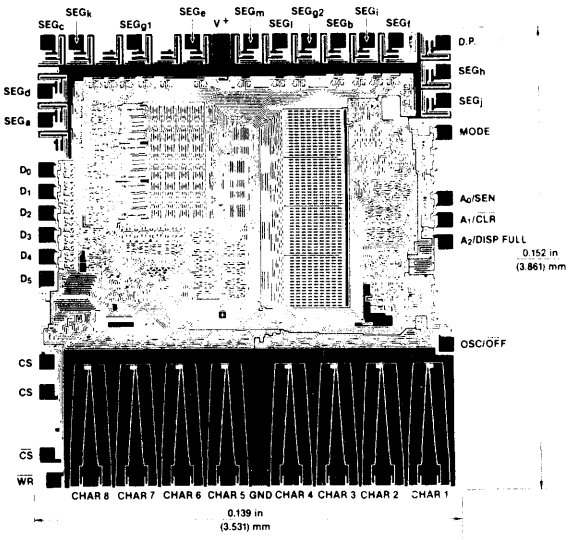
A.N.D., Burlingame, California
(415) 347-9916 (part #AND370R)

IEE Inc., Van Nuys, California
(213) 787-0311 (part #LR3784R)

CHIP TOPOGRAPHIES



ICM7243A



ICM7243B

6

ICM7281
LCD Column Driver

FEATURES

- LCD Dot Matrix Column Driver
- 40 High Voltage LCD Column Drive Outputs For Up to 8 5xN Characters per IC
- Easy Interface
  —Serial Input Shift Register With parallel latch and carry outputs
- Directly Compatible with ICM7280 Row Driver
  —Up to 10 ICM7281's can be driven by an ICM7280 with no external components
- Low Resistance Outputs
  —Can drive both columns and rows of LCD graphics displays
- Will Drive 1.5V Threshold LCDs with Only Single 5V Supply
  —Can drive up to 4.5V threshold LCDs with 15V V_{DISP}

GENERAL DESCRIPTION

The ICM7281 LCD Dot Matrix Column Driver is designed to convert a serial data stream into drive signals for a multiplexed dot matrix LCD. Easily cascadable, up to 10 ICM7281's can be driven by one ICM7280 Intelligent Row Driver to make an 80 character dot matrix display. The ICM7281 also serves as both a Row Driver and Column Driver in LCD dot matrix graphics displays. The low output resistance and the 15V drive capability make it well suited for graphics displays with up to 256 x 256 dots (with 10pF/dot capacitance).

The ICM7281 consists of a 40 bit shift register, a 40 bit latch and 40 level-shifters/drivers. The 4 display drive voltages are generated externally, usually by a Row Driver. A serial data interface is used to minimize the number of pins needed for digital interfacing. Two data Carry Outputs are included for cascading several ICM7281's to drive large LCD displays.

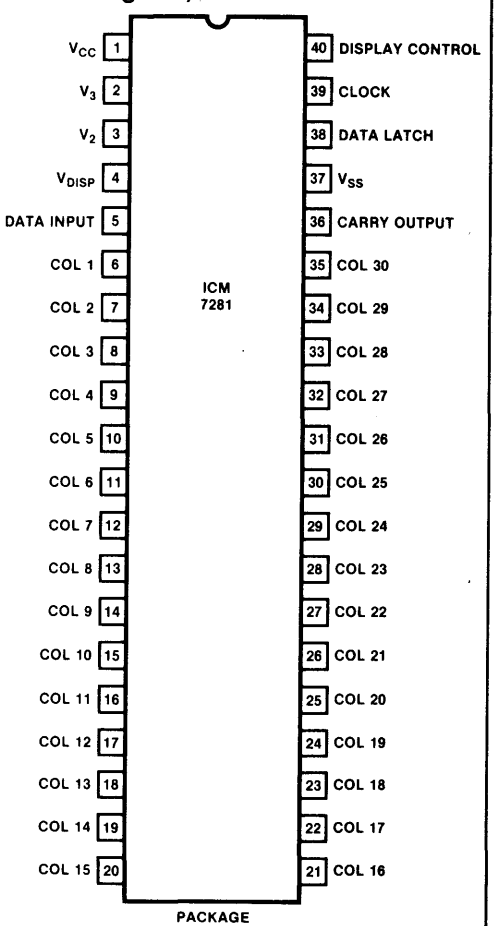
ORDERING INFORMATION

No. Of Columns	Package	Order Number
30	40 Pin Plastic	ICM7281IPL
40	Dice	ICM7281I/D
40	52-64 Pin Plastic Flatpack	—

TYPICAL APPLICATIONS

- Column Drivers for Dot Matrix Alpha-numeric Displays using ICM7280 Row Driver
- Row and Column Drivers for LCD Dot Matrix Graphics Displays
- Segment Driver for LCD Bargraphs and Annunciators
- Serial Input I/O Expander

PIN CONFIGURATIONS
(Outline dwg. PL)



6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} — V_{SS}) 6V

Display Voltage (V_{CC} — V_{DISP}) 18V

Input Voltage (Note 1) . . . . V_{CC} + 0.3V to V_{SS} − 0.3V

Power Dissipation (Note 2) . . . . . 0.3W @ + 85°C

Operating Temperature Range . . . . − 20°C to + 85°C

Storage Temperature Range . . . . . − 65°C to + 150°C

V_2, V_3 . . . . . V_{DISP} to V_{CC}

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in any junction isolated CMOS device, connecting an input to any voltage greater than V_{CC} or less than ground may cause destructive device latch-up. If the input voltage can exceed the recommended range, the input should be limited to less than 1 mA to avoid latch-up.

NOTE 2: This limit refers to that of the package and will not occur during normal operation.

OPERATING CHARACTERISTICS

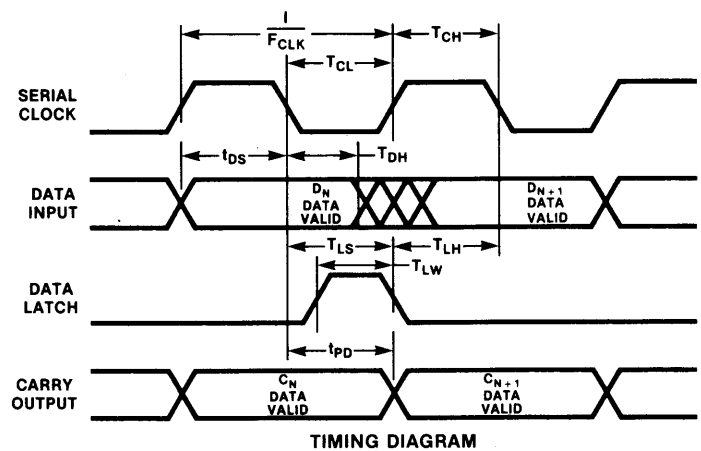
(V_{CC} = 5V ± 10%, V_{DISP} = − 10V, V_2 = 1/3 (V_{CC}-V_{DISP}). V_3 = 2/3 (V_{CC} - V_{DISP}), V_{SS} = 0V, T_A = − 20 to + 85°C) Unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SUPPLY CHARACTERISTICS						
Operating Supply Range	V_{SUPP}	V_{SS} = 0V	4.5	5.0	5.5	V
Display Voltage	V_{DISP}	V_{CC} = 5V, $V_{DISP} < (V2,V3) < V_{CC}$	− 10		V_{CC}	V
Supply Current Quiescent Dynamic	 I_{CC} I_{CC}	 F_{CLK} = 0 F_{CLK} = 500KHz		 .1 450	 10 1000	uA
INPUT CHARACTERISTICS						
Logic 1 Input Range	V_{IH}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	0.7V_{CC}		V_{CC}	V
Logic 0 Input Voltage	V_{IL}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	0		0.3V_{CC}	V
Input Current	I_{IN}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL $0 < V_{IN} < V_{CC}$	− 5	0.01	5	uA
Input Capacitance	C_{IN}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL Dice Plastic Packaged Parts		 3 5		pF
OUTPUT CHARACTERISTICS, CARRY OUTPUTS						
Output High Voltage	V_{OH}	No Load I_{OH} = 400μA	V_{CC} − 0.05 2.4	V_{CC} 4.9		
Output Low Voltage	V_{OL}	No Load I_{OL} = 1.6mA		0 0.16	0.05 0.4	V

OPERATING CHARACTERISTICS (continued)

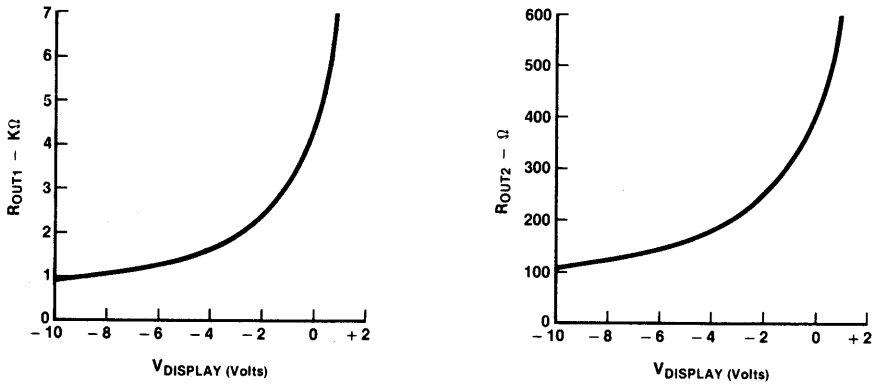
(V_{CC} = 5V ± 10%, V_{DISP} = −10V, V_2 = 1/3 (V_{CC}-V_{DISP}), V_3 = 2/3 (V_{CC} - V_{DISP}), V_{SS} = 0V, T_A = −20 to +85°C) Unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
OUTPUT CHARACTERISTICS, COLUMN OUTPUTS						
Output Resistance	R_{OUT1}	V_{CC}-V_{DISP} = 10V, I_{OUT} = 0.1mA, V_{COL} = 0V, 1 Column ON		1	2	K Ohm
Output Resistance	R_{OUT2}	V_{CC}-V_{DISP} = 10V, V_{COL} = 0V I_{OUT} = 0.05mA per Column All Columns ON		150	250	Ohm
Column Rise Time	T_R	V_{CC}-V_{DISP} = 10V, C_L = 150pF per Column, 0-63% V3 to V_{CC} or 0-63% V2 to V_{DISP} One Column ON All Columns ON		0.3 1.5		µS
Column Fall Time	T_F	V_{CC}-V_{DISP} = 10V, C_L = 150pF per Column, 0-63% V_{CC} to V3 or 0-63% V_{DISP} to V2 One Column ON All Columns ON		0.3 1.5		µS
AC CHARACTERISTICS (See Timing Diagram)						
Data Setup	T_{ds}		150	90		ns
Data Hold	T_{dh}		0	−20		ns
Data Latch Width	T_{lw}		250	100		ns
Data Latch Setup	T_{ls}		625	250		ns
Data Latch Hold	T_{lh}		100			ns
Clock Frequency	F_{clk}		0	2	1	MHz
Clock High Period	T_{ch}		500			ns
Clock Low Period	T_{cl}		500			ns
Carry Prop Delay	T_{pd}	C_L = 15pF		200	350	ns

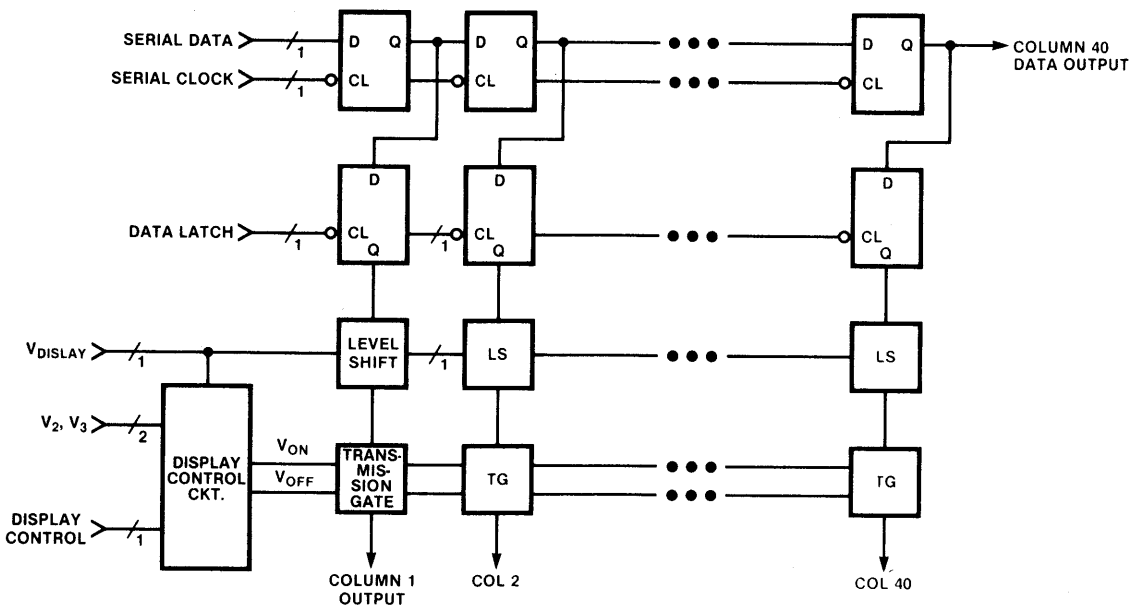


TIMING DIAGRAM

TYPICAL PERFORMANCE CURVES, 25°C



OUTPUT RESISTANCE vs. $V_{DISPLAY}$



ICM7281 COLUMN DRIVER BLOCK DIAGRAM

DETAILED DESCRIPTION

Data Interface

To reduce the pincount, the data interface is serial. The data on DATA INPUT is shifted into the shift register with each falling edge of CLOCK. The data in the shift register is also shifted one bit with each falling edge of CLOCK. The data in the 20th and 40th registers is available as COL 20 OUTPUT and COL 40 OUTPUT on the ICM7281 dice. The packaged part has only one CARRY OUTPUT, which is the 30th column. These outputs are normally used as the DATA INPUT for an adjacent ICM7281.

The DATA LATCH input is used to transfer data from the shift register to the 40 bit latch, which consists of 40 negative edge-triggered D flip-flops. The data in the shift register is stored by the falling edge of DATA LATCH and this latched data will be held until the next falling edge of DATA LATCH.

The DISPLAY CONTROL pin is used to convey multiplex timing information to the Column Drivers. This input is used as one of the two control inputs to the 1 of 4 analog multiplexer that drives each column output.

Figure 1 shows a typical interface between an array of ICM7281's and the ICM7280 Intelligent Row Driver. The Column Driver also readily interfaces with microprocessors, as shown in the block diagram of a graphics display, Figure 2.

LCD Interface

The ICM7281 uses a modified Alt and Pleshko multiplexing scheme, in which the Column Driver uses 4 voltages: V_{CC}, V2, V3, and V_{DISP}. These drive voltages are generated externally, usually by the ICM7280 Intelligent Row Driver. Each column output is driven by an analog multiplexer. The truth table and a schematic of this multiplexer are shown in Figure 3. The column data is the data that is serially loaded into the shift register, then parallel loaded into the data latch. The DISPLAY CONTROL signal, generated by the ICM7280 Row Driver, tells the ICM7281 which half of the mux cycle is occuring.

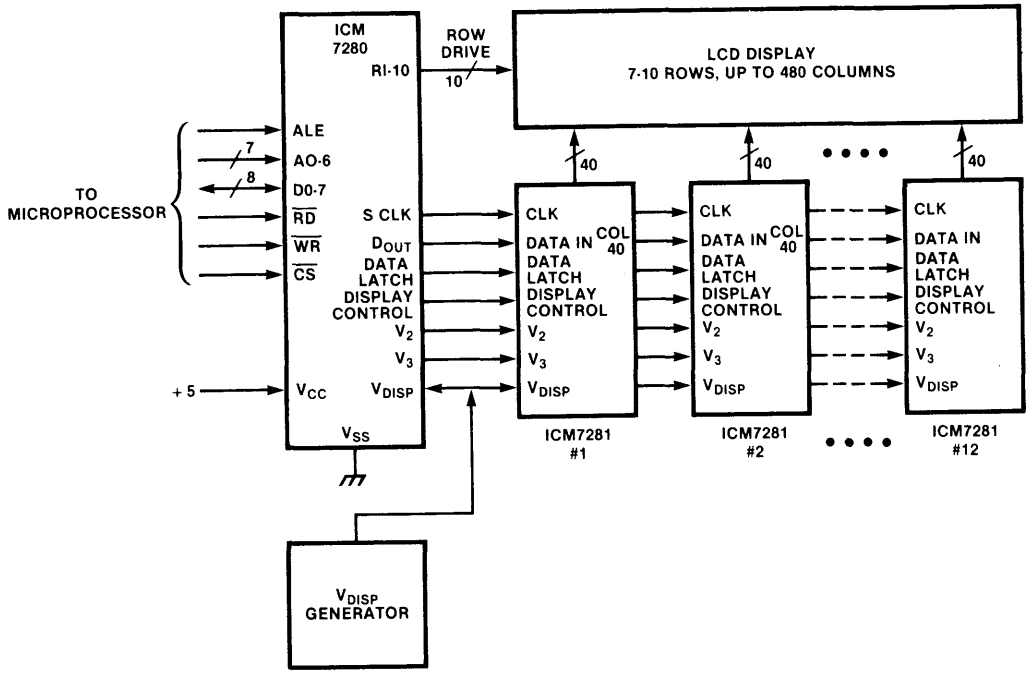


Figure 1. Alphanumeric LCD Display System

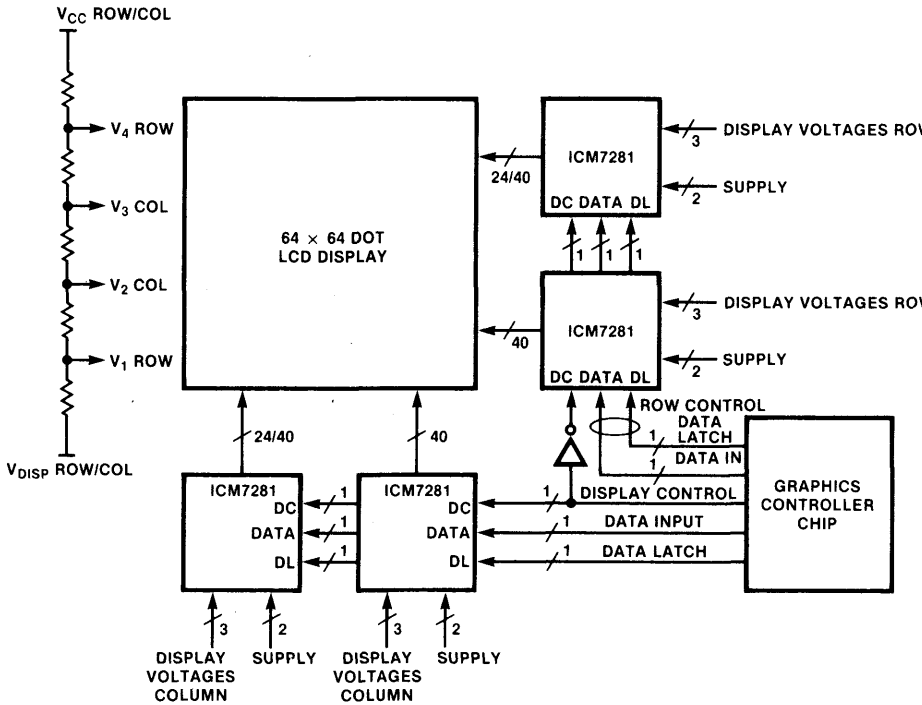
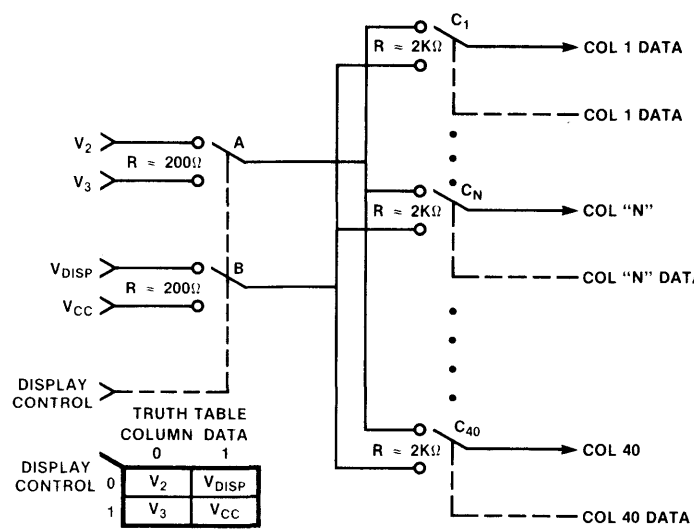


Figure 2. ICM7281 Column Driver Used in a Graphics Application



COLUMN OUTPUT MULTIPLEXER AND TRUTH TABLE

Figure 3. Column Output Multiplexer and Truth Table

LCD MULTIPLEXING

Multiplexing Schemes

The goal in LCD multiplexing is to increase the number of segments a given number of column lines can drive, while not unacceptably degrading the viewability of the LCD display. Increasing the number of rows driven by a column decreases the ratio between the voltage across an ON segment and the voltage across an OFF segment. This ON/OFF voltage ratio is critical since the contrast of an LCD segment is determined by the RMS voltage across that segment. Figure 4 shows a typical curve of RMS voltage vs. contrast. For an acceptable display, the RMS OFF voltage must be below the 10% contrast point and the RMS ON voltage must be above the 50% contrast point. The RMS on voltages for different multiplex ratios are also shown in figure 4. Note that as the number of rows or backplanes goes up, the RMS on voltage decreases.

The ICM7281 can drive either columns or rows using the modified Alt and Pleshko waveforms as shown in figure 5. The ON/OFF voltage ratio formula and the calculated values for common multiplex ratios are shown in table 1. Table II shows the optimum voltages for V1 to V5 for different multiplex ratios.

Temperature Effects and Temperature Compensation of V_{DISP}

The performance of LCD fluids is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures some displays may take several seconds to change to a new character after the new information appears at the LCD driver outputs. However, for most applications above 0°C this will not be a problem, and for low temperature applications, high-speed liquid crystal materials are available. High temperature operation is generally limited by long term degradation of the polarizer and the sealing materials above 70°C or 85°C.

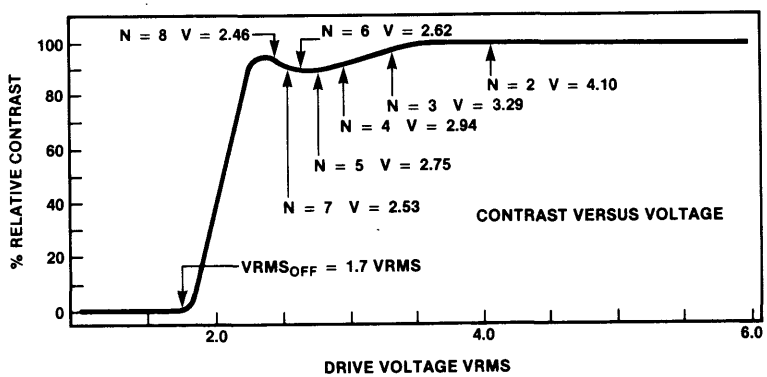
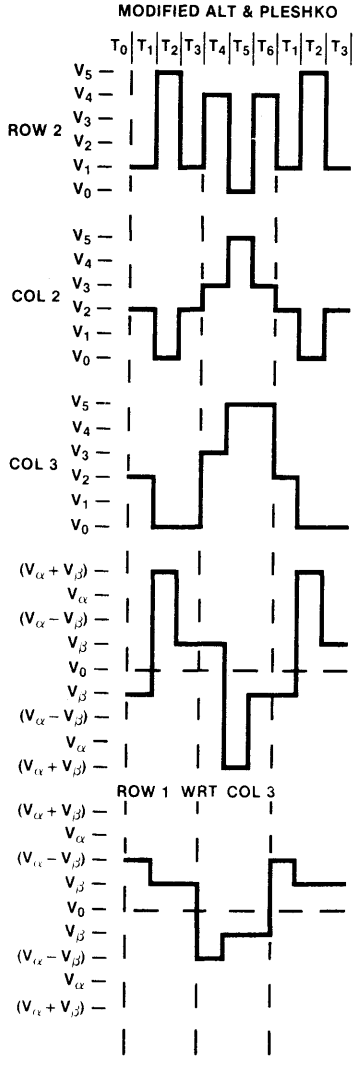
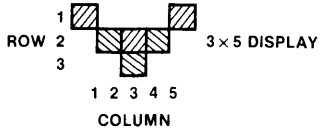


Figure 4.

Table 1. OPTIMUM MULTIPLEX DRIVE

Rows	$V_{ON/OFF}$	Alt and Pleshko V_{CC}-V Display/V_T	ICM7280/ICM7281 V_{CC}-V Display/V_T
4	1.73	4	3
7	1.488	4.74	3.27
8	1.447	4.97	3.37
9	1.414	5.20	3.46
10	1.387	5.41	3.56
12	1.346	5.81	3.74
14	1.315	6.18	3.917
16	1.290	6.532	4.08
32	1.196	8.817	5.19
64	1.134	12.01	6.804





WITH

$V_0 = 0$
$V_1 = V_\beta$
$V_2 = 2V_\beta$
$V_3 = V_\alpha - V_\beta$
$V_4 = V_\alpha$
$V_5 = V_{DISPLAY} = V_\alpha + V_\beta$

$$V_\alpha = \frac{\sqrt{(K+1)^3}}{2(K-1)} V_{TH}, \quad V_\beta = \frac{\sqrt{K+1}}{2} V_{TH}$$

WHERE: $K = \frac{\sqrt{N}+1}{\sqrt{N}-1}$

V_{TH} = THRESHOLD VOLTAGE OF LCD

$$V_{ON\ RMS} = \sqrt{\frac{(V_\alpha + V_\beta)^2 + (N-1)V_\beta^2}{N}}$$

$$V_{OFF\ RMS} = \sqrt{\frac{(V_\alpha - V_\beta)^2 + (N-1)V_\beta^2}{N}}$$

$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{(M+1)^2 + (N-1)}{(M-1)^2 + (N-1)}}$$

$$M = \frac{V_\alpha}{V_\beta}$$

FOR OPTIMUM CONTRAST $M = \sqrt{N}$ $N \geq 4$

Figure 5.

Table II. Optimum Drive Voltages

N	V1	V2	V3	V4	V5	ON/OFF VOLTAGE RATIO
4	1.000	2.000	1.000	2.000	3.000	1.732
5	0.951	1.902	1.176	2.127	3.078	1.618
6	0.919	1.838	1.332	2.252	3.171	1.543
7	0.897	1.793	1.476	2.372	3.269	1.488
8	0.879	1.759	1.608	2.488	3.367	1.447
9	0.866	1.732	1.732	2.598	3.464	1.414
10	0.855	1.710	1.849	2.704	3.559	1.387
11	0.846	1.692	1.960	2.806	3.652	1.365
12	0.838	1.677	2.066	2.904	3.743	1.346
16	0.816	1.633	2.449	3.266	4.082	1.291
20	0.802	1.605	2.786	3.589	4.391	1.255
24	0.793	1.585	3.090	3.883	4.676	1.23
30	0.782	1.564	3.502	4.284	5.066	1.203
32	0.779	1.559	3.629	4.409	5.188	1.196
40	0.771	1.541	4.103	4.874	5.645	1.173
48	0.764	1.529	4.332	5.296	6.061	1.156
54	0.761	1.522	4.830	5.590	6.351	1.147
64	0.756	1.512	5.292	6.047	6.803	1.134

6

The temperature effect most important in the 0-70°C range is the variation of threshold voltage with temperature. For typical liquid crystal materials, the threshold voltage, V_{THRESH}, has temperature coefficient of -7 to -14mV/°C. Since the V_{DISP} is 3.27 times V_{THRESH} (for 7 row multiplex, see Table 1), the V_{DISP} has a tempco of about -25 to -50 mV/°C, depending on LCD fluid tempco. As can be seen in Figure 4, for optimum viewability and contrast ratio, the driving voltage must be accurately matched to the LCD threshold voltage. If a significant variation is temperature is expected, a method of adjusting the V_{DISP} must be provided. Figure 6 uses the ICL7663 voltage regulator to independently set V_{DISP} and the tempco of V_{DISP}. The Vbe multiplier circuit of Figure 7 can be used with some displays. Since the Vbe multiplier's voltage and tempco cannot be independently adjusted, the Vbe multiplier is suitable only for use over a limited temperature range or with a display whose V_{DISP} tempco matches the Vbe multiplier tempco.

With the fluids now available for 32 and 64 multiplex operation it is quite common to have a "Contrast" adjustment accessible to the user. This "Contrast" adjustment varies the V_{DISP} to compensate for both temperature variations and for variations in the viewing angle.

Multiplex Rate and Maximum Drive Capability

The minimum multiplex rate is determined by the response time of the LCD. To avoid flicker, the mux rate should be above 30Hz. The maximum multiplex rate is determined by power dissipation limits and the drive capability of the ICM7281.

The drive capability of the ICM7281 indirectly sets the upper limit of the mux rate. The absolute maximum limit of DC voltage across an LCD is usually specified as 50mV. As the multiplex rate increases, any asymmetry in the rise and fall times will cause a DC offset, in addition to any offset caused by V2 and V3 not being exactly symmetrical with respect to V_{DISP} and V_{CC}. The ICM7281 was designed to have equal rise and fall times, as well as low resistance drivers which make the rise and fall times short. This allows the ICM7281 to drive over 2000pF at mux rate of 100Hz. Normally an LCD dot matrix display will have less than 1000pF capacitance per 40 columns (each ICM7281 drive 40 columns).

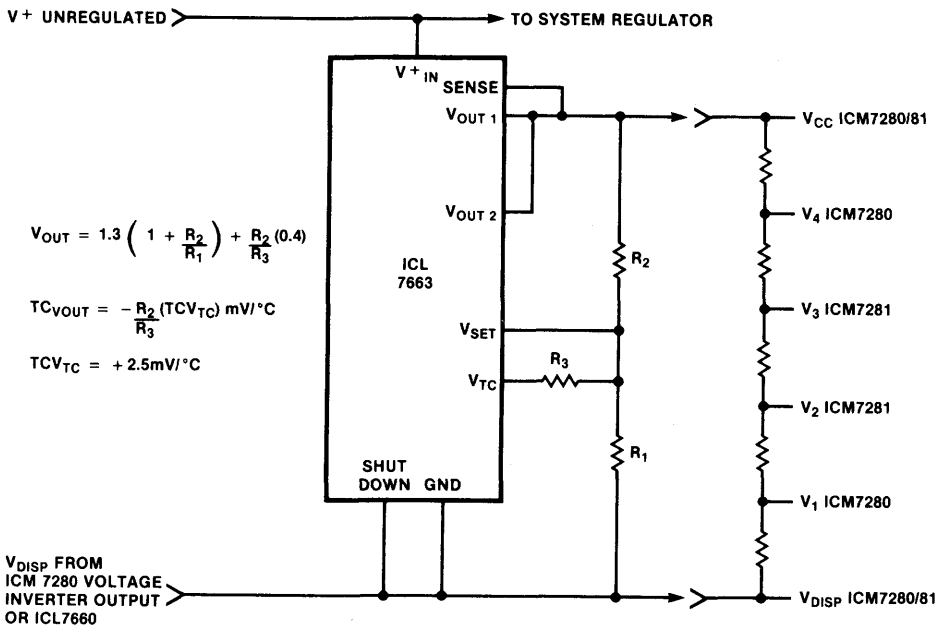


Figure 6. V_{DISP} Generator

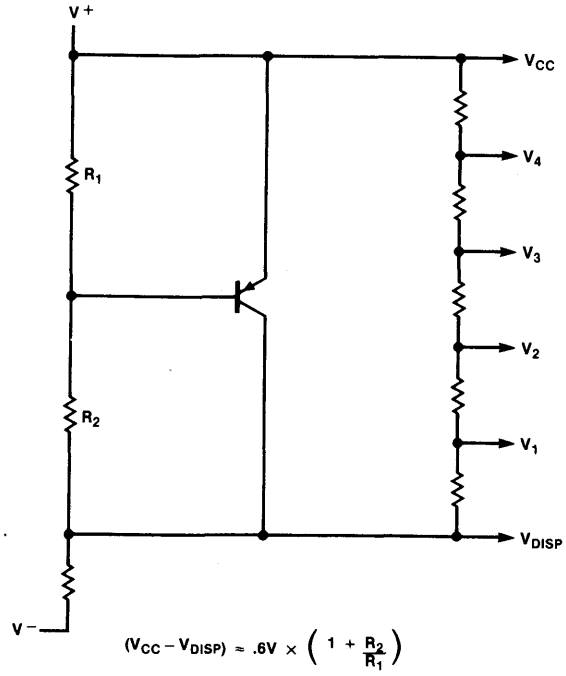


Figure 7. V_{BE} Multiplier

POWER DISSIPATION

The power dissipation of a display system driven by the ICM7281 has several components:

1) Quiescent or DC power dissipation of the ICM7281
2) Dynamic or AC power dissipation of the ICM7281
3) Power consumed in driving the LCD display.

ICM7281 Power Dissipation

The quiescent current of the ICM7281 is very low, typically less than 1μA, and can generally be ignored. The dynamic current is proportional to the clock frequency, with a typical value of 1.0 mA per MHz. This means that at a 500 KHz clock the dynamic current will be 0.5 mA.

LCD Display Drive Dissipation

Since the LCD has very low leakage currents, most of the power used to drive the LCD is used to charge and discharge the LCD capacitance. The power is

$$P_{LCD} = C V^2 F_{EFF}$$

Where:

P_{LCD} is the power dissipated in driving the display

C is the display capacitance

V is Voltage across the display

F is the effective multiplex frequency

The effective multiplex frequency ranges from F_{MUX} to N x F_{MUX}, where F_{MUX} is the multiplex rate and N is the number of rows. The actual effective multiplex frequency is dependent on which characters or bit pattern is being displayed and is typically about N/3 x F_{MUX}

Low Power Shutdown

If the data clock is stopped and the voltages across the LCD are not changing, the power consumption will drop to the 5 to 50 microwatt range. Set V_{DISP}, V2 and V3 equal to V_{CC} to prevent permanent damage to the LCD display by a DC bias. An easy way to shutdown the display voltages is to use the SHUTDOWN pin of an ICL7663, as shown in Figure 6.

APPLICATIONS

Alphanumeric Display Using ICM7280 Intelligent Row Driver

The ICM7280 Intelligent Row Driver is specifically designed to drive multiple ICM7281 LCD Column Drivers. Figure 1 shows a typical 80 character display. The ICM7280 and ICM7281's will drive either 7, 8, 9 or 10 row displays, with the characters having either 5 or 6 columns. The Row Driver receives ASCII data, converts that data to bit-by-bit column data for the ICM7281's and serially shifts data into the ICM7281's. This process is repeated for each phase of the multiplex cycle. The ICL7663 provides a temperature compensated V_{DISP} to the ICM7280 voltage divider, which generates the other voltage needed to drive the LCD display. For further details refer to the ICM7280 Intelligent LCD Row Driver data sheet.

LCD Graphics Display

In this circuit, ICM7281's are used to drive both the rows and columns of the LCD dot matrix. An external controller is used to generate the row and column data that is serially transferred into the ICM7281's.

The display drive voltages are generated in a resistor divider network, with the ICL7663 providing the temperature compensated V_{DISP}. The optimum voltages for V1 through V5 can be calculated using the equations of figure 5. Optimum voltages for common multiplex ratios are shown in Table II.

The LCD shown in Figure 2 is a 32 row display, divided into two sections of 16 rows to increase the ON/OFF RMS voltage ratio, thereby improving the contrast of the display. As LCD fluids improve it will become practical to use 32 or 64 row multiplexing, reducing the number of column drivers by a factor of 2 or 4.

As the number of rows increases, the V_{DISP} required by the ICM7281's modified Alt and Pleshko multiplex scheme increases less than the V_{DISP} required by a classic Alt and Pleshko multiplex scheme. For example: a 64 row display with a 1.45V threshold would require + 5V and − 12.4V supplies using standard Alt and Pleshko multiplexing. The ICM7281 would require only + 5V and − 4.9V to drive this same display with 64 row multiplexing. This means that the negative voltage could easily be generated using a charge pump such as the ICL7660 or the onboard charge pump of the ICM7280.

Serial Input I/O Expander

In addition to driving LCD's, the ICM7281 can be used as an I/O expander as shown in Figure 8. In this case, the data can be serially entered into the ICM7281 shift register using the 80C51 serial port. The 80C51 then transfers the data to the output latch by pulsing the DATA LATCH input with an I/O port line. Note that multiple ICM7281's can be cascaded to get more than 30 output lines. This cascading does not require any additional logic since the ICM7281 CARRY OUTPUTs are used.

DISPLAY CONTROL is tied to V+ so that the data on the column outputs is the same as the data that was entered. If DISPLAY CONTROL is grounded, the column outputs will be inverted data. With V_3 grounded, the logic level at the column outputs will be CMOS compatible, swinging from ground to V+. The output resistance of the column outputs is about 2K ohms.

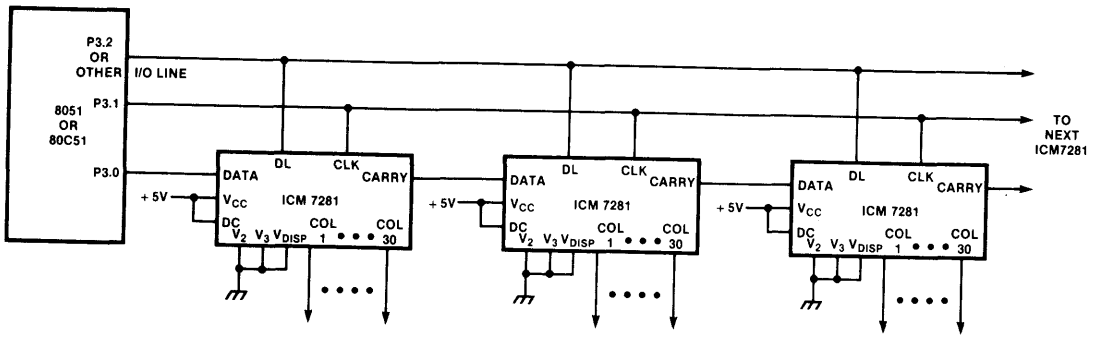
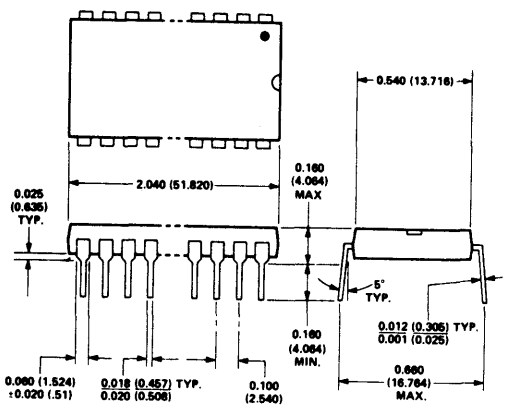


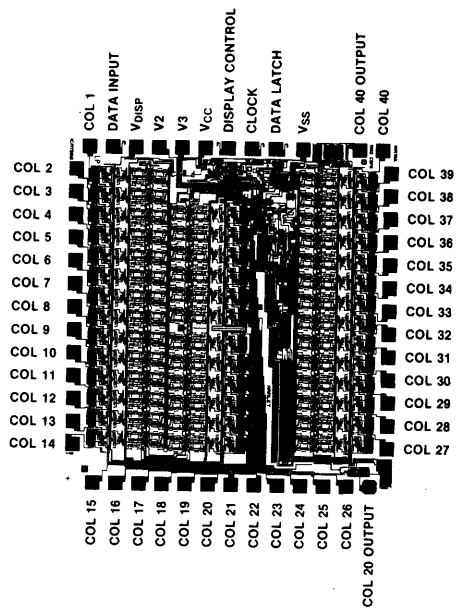
Figure 8. Serial I/O Expander 7281

PACKAGE OUTLINES

All dimensions given in inches and (millimeters).



40 LEAD PLASTIC (PL)



DIE

CHIP TOPOGRAPHY

ICM7555/7556 CMOS General Purpose Timers

FEATURES

- **Exact equivalent in most cases for SE/NE555/556 or the 355.**
- **Low Supply Current — 80μA Typ. (ICM7555) 160μA Typ. (ICM7556)**
- **Extremely low trigger, threshold and reset currents - 20pA Typical**
- **High speed operation - 500 kHz guaranteed**
- **Wide operation supply voltage range guaranteed 2 to 18 volts**
- **Normal Reset function - No crowbarring of supply during output transition.**
- **Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005% per °C at 25°C**
- **Outputs have very low offsets, HI and LO**

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

6

APPLICATIONS

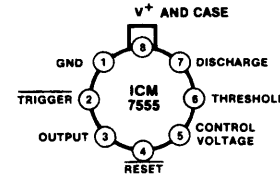
- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555IPA	−20 to +85°C	8 Lead MiniDip
ICM7555ITV	−20 to +85°C	TO-99 Can
ICM7555MTV	−55 to +125°C*	TO-99 Can
ICM7556IPD	−20 to +85°C	14 Lead Plastic DIP
ICM7556MJD	−55 to +125°C*	14 Lead CERDIP
ICM7555/D		DICE
ICM7556/D		DICE

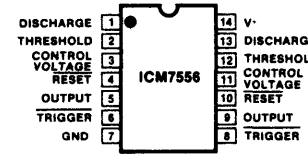
*Add /883B to order number if 883B processing is desired.

PIN CONFIGURATIONS (Top View)



(OUTLINE DRAWING TV)

(OUTLINE DRAWING PA)



(OUTLINE DRAWING JD, PD)

INTERSIL

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage ..... +18 Volts
Input Voltage Trigger, Threshold, Reset ..... ≤ V⁺ + 0.3V to ≥ V⁻ − 0.3V
Output Current 100mA
Power Dissipation [2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Operating Temperature Range [2]
ICM7555IPA .....–20°C to +85°C
ICM7555ITV .....–20°C to +85°C
ICM7556IPD .....–20°C to +85°C
ICM7555MTV ..... –55°C to +125°C
ICM7556MJD ..... -55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 60 Seconds) ..... +300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS (T_A = 25°C, V^+ = +2 to +15 Volts unless other specified)

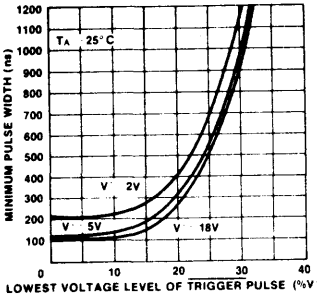
PARAMETER	SYMBOL	TEST CONDITIONS			VALUE MIN	VALUE TYP	VALUE MAX	UNITS
Supply Voltage	V^+	−20°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C			2 3		18 16	V V
Supply Current [3]	I^+	ICM7555	V^+ = 2V V^+ = 18V			60 120	200 300	µA µA
		ICM7556	V^+ = 2V V^+ = 18V			120 240	400 600	µA µA
Timing Error		R_A, R_B = 1k to 100k, C = 0.1µF	5V ≤ V^+ ≤ 15V					
Initial Accuracy		Note 4				2.0	5.0	%
Drift with Temperature		Note 4	V^+ = 5V V^+ = 10V V^+ = 15V			50 75 100		ppm/°C
Drift with Supply Voltage		V^+ = 5V				1.0	3.0	%/V
Threshold Voltage	V_{TH}		V^+ = 5V		0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}		V^+ = 5V		0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	V^+ = 18V V^+ = 5V V^+ = 2V				50 10 1		pA pA pA
Threshold Current	I_{TH}	V^+ = 18V V^+ = 5V V^+ = 2V				50 10 1		pA pA pA
Reset Current	I_{RST}	V_{RESET} = Ground	V^+ = 18V V^+ = 5V V^+ = 2V			100 20 2		pA pA pA
Reset Voltage	V_{RST}	V^+ = 18V V^+ = 2V			0.4 0.4	0.7 0.7	1.0 1.0	V V
Control Voltage Lead	V_{CV}		V^+ = 5V		0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo	V^+ = 18V V^+ = 5V	I_{SINK} = 3.2mA I_{SINK} = 3.2mA		0.1 0.15	0.4 0.4	V V
		Output Hi	V^+ = 18V V^+ = 5V	I_{SOURCE} = 1.0mA I_{SOURCE} = 1.0mA	17.25 4.0	17.8 4.5		V V
Rise Time of Output	t_r	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Fall Time of Output	t_f	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Guaranteed Max Osc Freq	f_{max}	Astable Operation			500			kHz

NOTES:

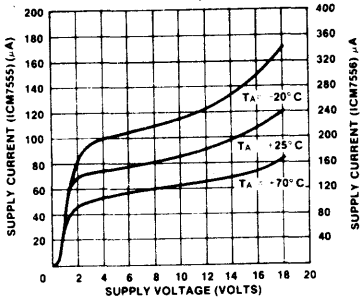
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V⁻ −0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
2. Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).
3. The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.
4. Parameter is not 100% tested, Majority of all units meet this specification.

TYPICAL CHARACTERISTICS

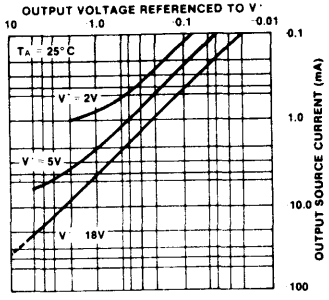
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



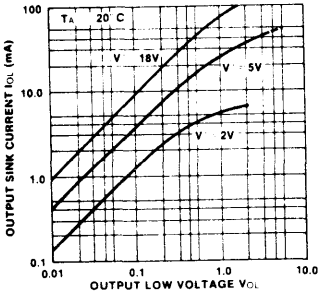
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



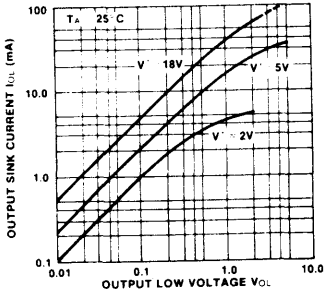
OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



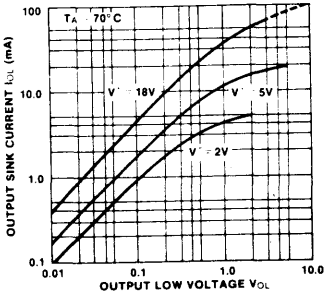
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



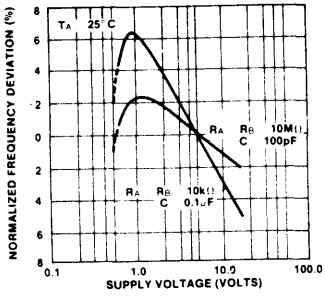
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



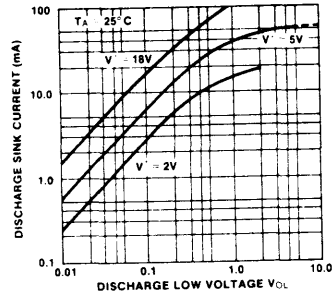
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



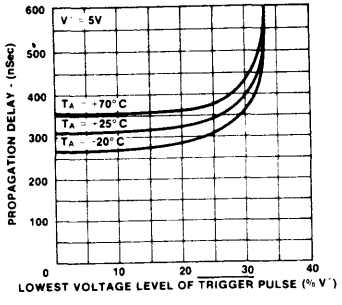
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



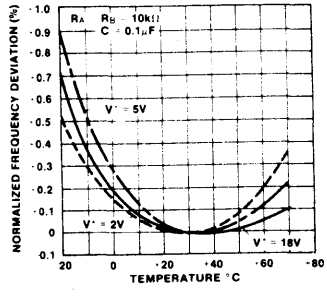
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



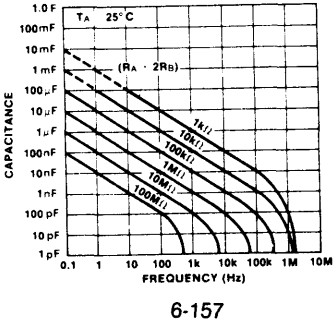
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



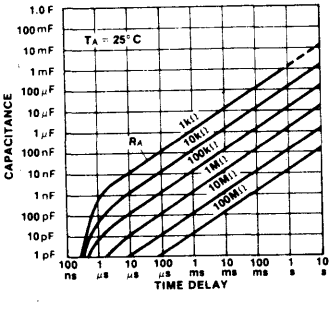
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



FREE RUNNING FREQUENCY AS A FUNCTION OF RA, RB and C



TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C



6

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 2.

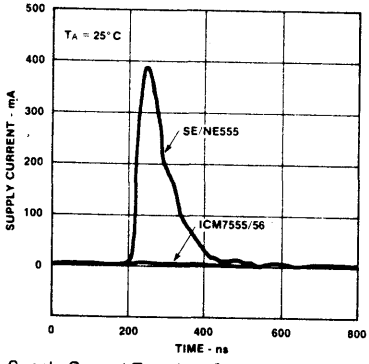


Figure 2. Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2-3 mA instead of 300-400 mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 3 and 4.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 3. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4\,RC}$$

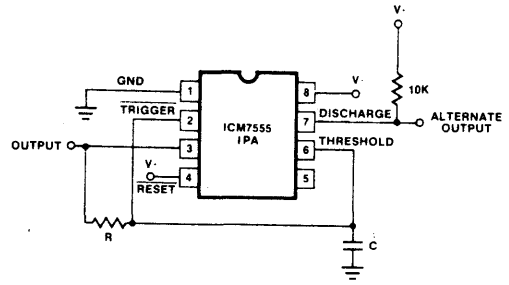


Figure 3: Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

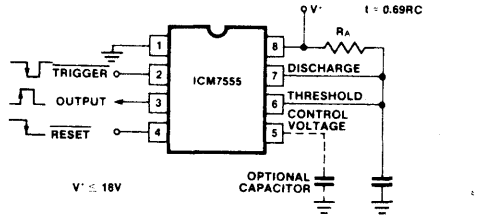


Figure 4: Monostable Operation

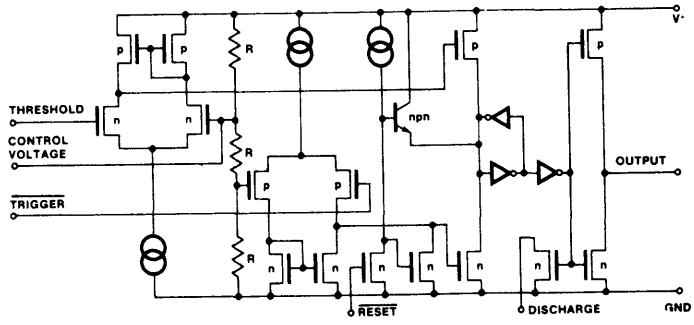
CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

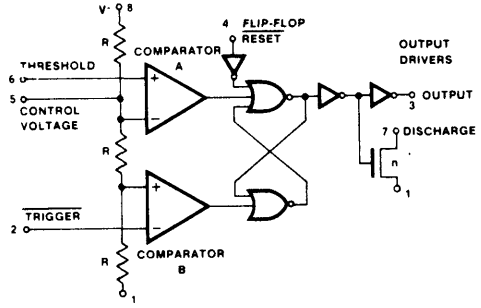
$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

EQUIVALENT CIRCUIT



BLOCK DIAGRAM



This block diagram reduces the circuitry down to its simplest equivalent components.
Tie down unused inputs.
R = 100kΩ, ± 20% typ.

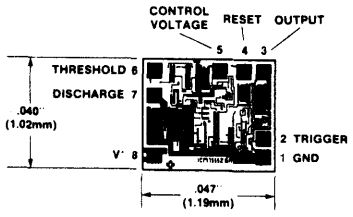
TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V+)	>1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V+)	HIGH	HIGH	OFF

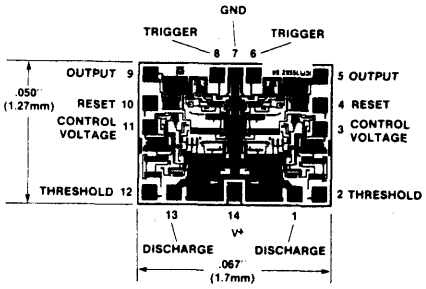
NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

CHIP TOPOGRAPHIES

ICM7555



ICM7556



Timekeeping, DTMF Circuits

Stopwatches

	Page
ICM7045	7-10
ICM7215	7-47

Display Watches/Clocks

ICM7223	7-53
ICM7223A	7-59
ICM7223VF	7-67

Analog Watches/Clocks

ICM1115	7-19
ICM7038	7-5
ICM7050	7-19
ICM7051	7-23
ICM7070	7-27
ICM7245	7-77

Clock Generators

ICM7209	7-39
ICM7213	7-42

Frequency Divider

ICM7241	7-75

Touch Tone Encoder

ICM7206	7-31

Watches

Part Number	Circuit Description	Typical Current at 1.55 VDC
ICM7245B/D/E/F ICM7245U	Analog quartz watch/clock circuit. ICM7245B/D/E/F for bipolar stepper motors. ICM7245U for unipolar stepper motors. Ultra high accuracy: 0.1 ppm.	0.4μA

Notes: All Intersil watch circuits are designed for use with a 32.768Hz quartz crystal. All provide a rapid advance setting.
Watch circuits are normally sold in die form. The ICM7245B/D/E/F and ICM7245U are available in either an 8 pin plastic DIP or mini-flatpack as well as dice.
All Intersil watch circuits have a fixed on-chip oscillator capacitor. The above circuits show typical current at 1.55 Volts LCD units in doubler mode.

Dual Tone (Touch Tone) Encoders

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7206	Touch-tone encoder; requires single contact per key.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206A	Touch-tone encoder; requires one contact per key with common line connected to + supply.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206B	Touch-tone encoder; requires 2 contacts per key with common line connected to negative supply; oscillator enabled when key is pressed.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206C	Touch-tone encoder requires single contact per key; oscillator enabled only when key is depressed. Disable line tied to V^-	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206D	Touch tone encoder; requires single contact per key; oscillator enabled only when key is depressed. DISABLE line tied to $V+$.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing

Clock and Timing Signal Generators

ICM7209	High-frequency clock-generator for 5-volt systems	8-Pin DIP	to 10 MHz	Crystal frequency, plus 8 divider stage
ICM7213	Oscillator and frequency divider	14-Pin DIP (plastic)	to 10 MHz	1pps, 1ppm, 10 Hz, composite

Clocks

Part Number	Circuit Description	Typical Operating Voltage	Package
ICM1115	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output $f_{osc} = 4.19MHz$	1.5V	8 pin DIP
ICM1115A	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output $f_{osc} = 4.19MHz$		
ICM1115B	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output $f_{osc} = 4.19MHz$		
ICM7038A	Analog quartz clock circuit with simple alarm. For synchronous motors.	3.0V	8 pin DIP
ICM7038B	Analog quartz clock circuit with simple alarm. For synchronous motors.	1.5V	8 pin DIP
ICM7050	Analog quartz clock circuit with complex alarm. For bipolar stepper motors. 47 ms pulse width. 1Hz rate $f_{osc} = 4.19MHz$	1.5V	8 pin DIP
ICM7051A	Analog quartz clock circuit for automotive applications—synchronous motors. 64 Hz square wave	12.0V	8 pin DIP
ICM7051B	Analog quartz clock circuit for automotive applications—bipolar stepper motors 31 ms pulse width. 1Hz rate		
ICM7070L	Analog quartz clock circuit with complex alarm. For bipolar stepper motors, 31 ms pulse width @ 0.5 Hz $f_{osc} = 32$ kHz	1.5	8 pin DIP
ICM7223	4 Digit LCD Alarm Clock with Snooze.	1.5V	40 pin DIP
ICM7223D	Direct drive Cricket alarm. 24 hour format by bond option. For 32.768 kHz quartz crystal.		
ICM7223A	4 Digit LCD Clock Radio circuit with Sleep Timer. Snooze and Alarm. Low battery indicator. Radio Enable. For 32.768 kHz quartz crystal.	9.0V	40 pin DIP
ICM7223VF	4 Digit Vacuum Fluorescent Clock Radio/Auto Clock circuit with Sleep Timer. Alarm. Snooze. and Radio Enable. For 32.768 kHz quartz crystal.	12.0V	40 pin DIP

Notes: All Analog clock circuits are designed for use with a 4.19 MHz quartz crystal, with the exception of the ICM7223 series which uses a 32.768 kHz crystal.
Clock circuits are normally purchased in package form; each is also available as dice.
All Analog clock circuits are mask programmable for oscillator frequency, output frequency and pulse width, and alarm frequency. Consult the factory for details.

Stopwatches

Part Number	Circuit Description	Crystal Frequency	Package
ICM7045	8 Digit 4 Function LED stopwatch circuit. Features Hours:Minutes:Seconds.100ths. Provides Time Out, Taylor, Split and Rally modes. Direct drive for LEDs. May be used as 24-hour clock.	6.55 MHz	28 pin DIP
ICM7215	6 Digit 4 Function LED stopwatch circuit. Features Minutes:Seconds.100ths. Provides Time out, Taylor and Split modes. Direct drive for LEDs.	3.28 MHz	24 pin DIP

Notes: All stopwatches may be purchased as an Evaluation Kit (EV KIT) which includes the IC and the appropriate quartz crystal. All operate at 2.5 to 4.5 volts, and source 15 mA current to the segments of the LEDs.

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INTERSIL

CMOS OSCILLATOR/DIVIDER/DRIVERS SELECTION GUIDE

(Includes circuits used in quartz analog clock and watch applications)

PRODUCT NUMBER	MASK VARIANT	CRYSTAL FREQUENCY (MHz)	MOTOR DRIVE OUTPUT	OUTPUT PULSE CHARACTERISTICS Width (ms)	Freq. (pulses per sec)	ALARM FREQUENCY (Hz)	NOMINAL VOLTAGE (V)	TYPICAL CURRENT (μA)	PACKAGE[4]
ICM7038A	—	4.19	Synchronous	7.8 [1]	64	512	3.0	90	8-pin DIP
ICM7038B	—	4.19	Synchronous	7.8 [1]	64	512	1.5	40	8-pin DIP
ICM7213	—	4.19	Multiple	7.8 31.2 125	1 16 1 per min.	1024+16+2	3.0	100	14-pin DIP
ICM7050A	ITS9044-1	4.19	Unipolar	15.6	1	1024	1.5	40	8-pin DIP
ICM7050	—	4.19	Bipolar	46.9	0.5	2048+8+1	1.5	40	8-pin DIP
ICM7051A	ITS9042-1	4.19	Bipolar	7.8 [1]	64	—	4.5-13.5	500	8-pin DIP
ICM7051B	—	4.19	Bipolar	31.2	0.5	—	4.5-13.5	500	8-pin DIP
ICM7070L[2]	—	32 kHz	Bipolar	31.2	0.5	2048+8+1	1.5	3	8-pin DIP
ICM7245A[2]	—	32 kHz	Bipolar	9.7	0.5	—	1.5	0.4	8-pin DIP
ICM7245B[2]	—	32 kHz	Bipolar	7.8	0.5	—	1.5	0.4	8-pin DIP
ICM7245D[2]	—	32 kHz	Bipolar	7.8	1 per 10 sec	—	1.5	0.4	8-pin DIP
ICM7245E[2]	—	32 kHz	Bipolar	7.8	1 per 12 sec	—	1.5	0.4	8-pin DIP
ICM7245F[2]	—	32 kHz	Bipolar	7.8	1 per 20 sec	—	1.5	0.4	8-pin DIP
ICM7245U[2]	—	32 kHz	Unipolar	3.9	1	—	1.5	0.4	8-pin DIP
ICM1115A	—	4.19	Bipolar	1000 [1]	0.5	64	1.5	80	8-pin DIP
ICM1115B	—	4.19	Bipolar	1000 [1]	0.5	64	1.5	40	8-pin DIP

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All Intersil analog quartz products are mask programmable. Options include:

- Crystal frequency (32 kHz, 1 MHz, etc.)
- Pulse width (500 msec to 3.9 msec)
- Pulse frequency (64 Hz to 0.5 Hz)
- Alarm frequency (64 Hz to 4096 Hz, including complex
- Motor drive characteristics
- Oscillator characteristics, including fixed capacitors (ICM7050

Notes: [1] Square Wave.
[2] Includes a fixed value capacitor on oscillator input.
[3] Includes snooze.
[4] All Intersil analog quartz products may be ordered in die form.

ICM7038 Family CMOS Analog Quartz Clock Circuit

Synchronous Motor Applications

FEATURES

- **Battery operation: 1.2 to 3.6V devices**
- **Very low power: 30μA typical (1.5V parts)**
- **High output current drive: 1 mA minimum**
- **Zero output bridge DC component (50% duty cycle square wave)**
- **All inputs fully protected — no special handling precautions required**
- **Wide operating temperature range: −20°C to +70°C**

GENERAL DESCRIPTION

The ICM7038 family of synchronous motor drivers is designed to operate from a 1.5V battery, and performs the functions of oscillator, frequency divider and output driver. In addition a power driver is tapped off from the thirteenth divider for use as an alarm driver.

Specifically the ICM7038 family uses an inverter oscillator having all biasing components on chip. Binary dividers permit frequency division from 4 MHz down to 64 Hz. The output from the divider network drives a bridge output circuit which provides a 50% duty cycle AC square wave having virtually zero DC component for driving a synchronous single phase motor. The total output drivers saturation is typically 200 ohms providing efficient operation of synchronous motors. The alarm output will drive a transducer (piezoelectric or speaker).

TABLE OF OPTIONS

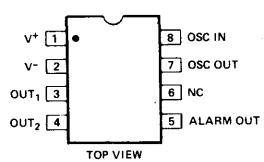
The ICM7038 may be modified with alternative metal masks to provide any number of binary divider stages up to a maximum of 19 and supply voltages from 1.2 V to over 3.6V together with various output options. Consult your Intersil representative or the factory for further information. The alarm output can be tapped off from any of the latter divider stages.

(See table for standard options).

Part Number	Binary Dividers	Nominal Output Frequency	Nominal Supply Voltage
ICM7038A	16	64 Hz	3.0V
ICM7038B	16	64 Hz	1.5V

PIN CONFIGURATION

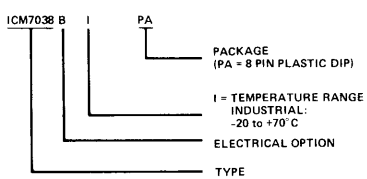
(OUTLINE DRAWING PA)



TOP VIEW

PIN 1 IS DESIGNATED BY EITHER A DOT OR A NOTCH.

ORDERING INFORMATION



ORDER DEVICES BY FOLLOWING PART NUMBER—
ICM7038B I PA

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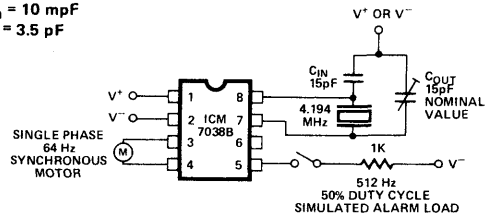
ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit(1) 300mW
Supply Voltage:
ICM7038A 5V
ICM7038B 3V
Output Voltage(2) ..... V^- to V^+
Input Voltage(2) ..... V^- to V^+
Storage Temperature ..... −30°C to +125°C
Operating Temperature ..... −20°C to +70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

TEST CIRCUIT

QUARTZ CRYSTAL PARAMETERS
f = 4,194,304 Hz
R_S = 35Ω
C_m = 10 mpF
C_0 = 3.5 pF



NOTES:
1. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
2. Except for instantaneous static discharges all terminals may exceed the supply voltage (2.0V max) by ±0.5 volt provided that the currents in these terminals are limited to 2 mA each.

OPERATING CHARACTERISTICS

(V^+ = 3.0V (ICM7038A) or 1.5V (ICM7038B), f_{osc} = 4,194,304 Hz, test circuit 1, T_A = 25°C, unless otherwise specifed.

Parameter	Symbol	Conditions	7038A/C/F			7038B/D/E/G			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Supply Current	I^+			90	150		30	60	μA
Guaranteed Operating Voltage Range	V^+	−20°C ≤ to ≤ 70°C	2.2		3.6	1.2		1.8	V
Total Output Saturation Resistance	R_{SAT}	p + n Output Transistors, I_{OUT} = 0.5mA		230	400		200	700	Ω
Alarm Output Saturation Resistance	R_{AL}	I_{OUT} = 1mA		200	400		300	800	Ω
Oscillator Stability	f_{STAB}	Over V^+ range $C_{IN} = C_{OUT}$ = 15pF		1			1		ppm
Oscillator Start-Up Time	t_{START}	V^+ = min.			1.0			1.0	sec

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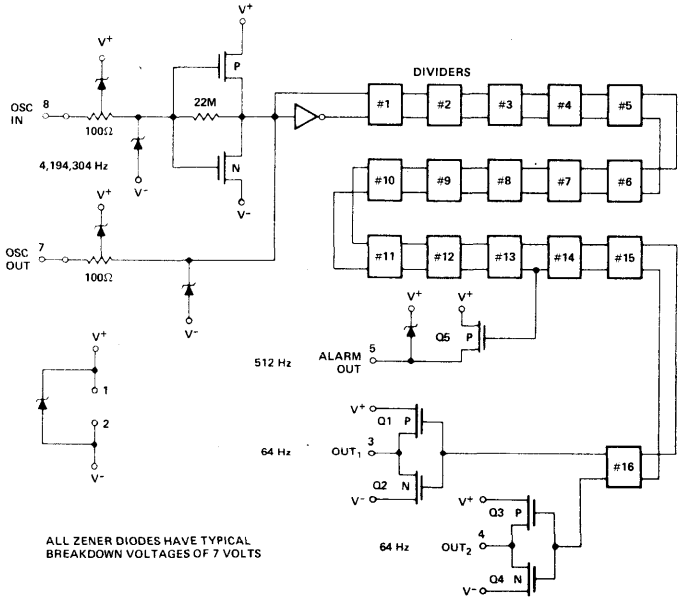
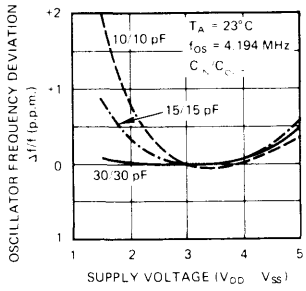
SCHEMATIC DIAGRAM (ICM7038B)

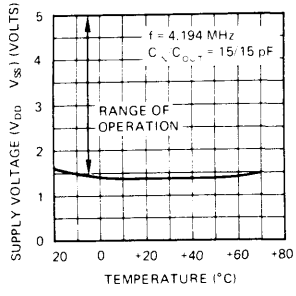


TYPICAL OPERATING CHARACTERISTICS (ICM7038A)

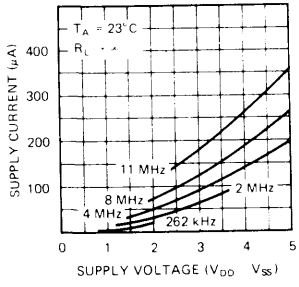
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



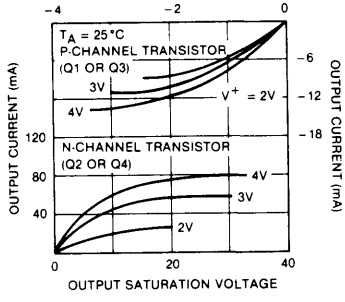
MINIMUM OPERATING SUPPLY VOLTAGE VS. TEMPERATURE



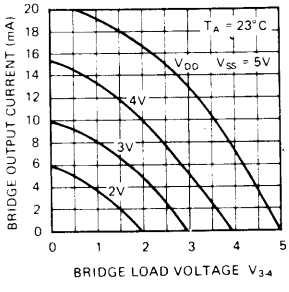
SUPPLY CURRENT VS. SUPPLY VOLTAGE



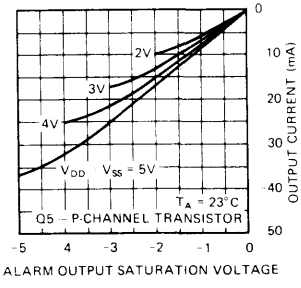
OUTPUT CURRENT VS. OUTPUT SATURATION VOLTAGE



BRIDGE OUTPUT CURRENT VS. BRIDGE OUTPUT VOLTAGE

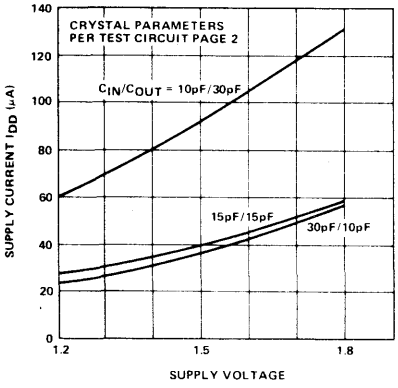


ALARM OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE

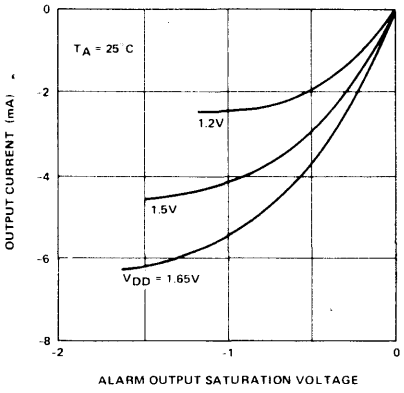


TYPICAL OPERATING CHARACTERISTICS (ICM7038B)

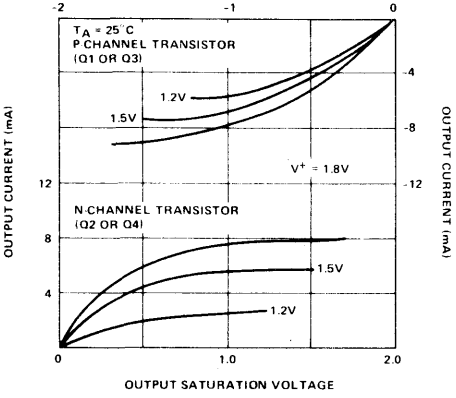
SUPPLY CURRENT VS. SUPPLY VOLTAGE



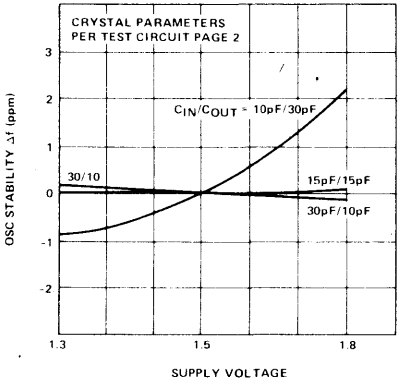
ALARM OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE



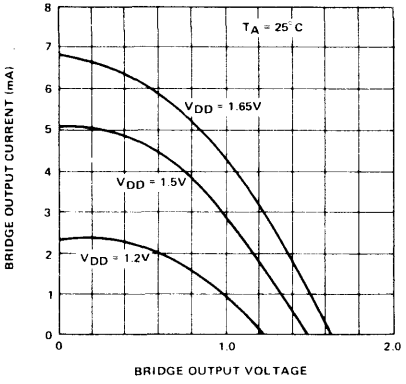
OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE



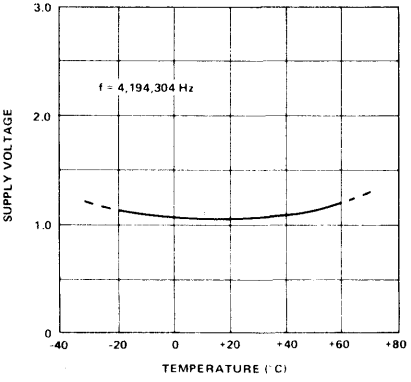
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT VS. BRIDGE OUTPUT VOLTAGE



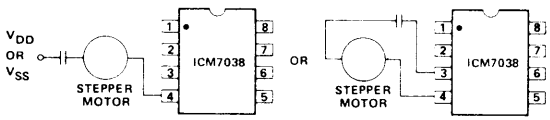
MINIMUM OPERATING SUPPLY VOLTAGE VS. TEMPERATURE



APPLICATION NOTES

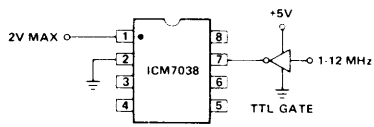
GENERAL DESCRIPTION

The ICM7038 Family has been designed primarily for quartz clock and timer applications using oscillator frequencies between 2.0 and 10 MHz. The design objectives were exceptional oscillator frequency stability, very low power, wide supply voltage range and wide temperature range. The oscillator contains all components except the tuning components and quartz crystal. Three outputs are provided. The two principal outputs are intended to be used to drive a single phase synchronous motor in a bridge configuration. As such, because of the matching of the transistors in the two outputs, the output DC component is extremely small. Stepper motors may also be used by placing a capacitor in series with the motor and using either a single output or the bridge output.



Alternatively outputs 3 and 4 may be used to drive TTL logic directly for timer applications.

The alarm output is taken from the output of the thirteenth divider and can source 1 mA at a low saturation voltage.



The ICM7038 may be used as a straight divider by driving directly into the oscillator output (pin no. 7) with a low impedance square wave drive. As such it may be used over the frequency range 1 MHz to 10 MHz.

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7038 is designed to operate with crystals having a load capacitance of 10 to 12 pF. This allows nominal capacitor values of 15/15 pF or 20/20 pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however, the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor is provided on chip, which has a maximum value at start up. Oscillator tuning should be done at the oscillator output.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \qquad C_L = \frac{C_{IN}C_{OUT}}{C_{IN}+C_{OUT}}$$

g_m required for startup

$$g_m = \omega^2 C_{IN}C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_O = static capacitance of the crystal
C_{IN} = input capacitance
C_{OUT} = output capacitance
C_L = load capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 50 μmhos

ICM7045
CMOS Precision Decade Timers

FEATURES

- **Total integration: includes oscillator, divider, decoder driver on chip**
- **Wide operating supply range: 2.5V ≤ V⁺ ≤ 4.5V**
- **Low operating power consumption: 0.9 mW @ 3.6V supply with display off**
- **High output current drive: 18 mA peak current per segment with 12.5% duty cycle.**
- **Leading zero suppression: timer stopwatch applications**
- **Fractional second suppression: 24-hour clock application**
- **Short duration short circuit protection on all inputs and outputs at 3.6V supply**
- **Versatility of applications: precision timer, 4 mode stopwatch, 24-hour clock**
- **Uses 6.5536 MHz quartz crystal for high accuracy**

GENERAL DESCRIPTION

The ICM7045 is a fully integrated precision decade timer fabricated using Intersil's low voltage metal gate C-MOS technology. The oscillator, frequency divider, multiplexer, decoder, segment and digit output buffers are all included on-chip. The circuits are designed to interface directly with fully multiplexed 8-digit 7-segment common cathode LED displays. The normal supply voltage is 3.6V, equivalent to a stack of three nickel cadmium batteries.

This circuit is designed for use as a digital timer, 4-function stopwatch and 24 hour clock; the only external components required are the display, batteries, 6.5536 MHz crystal, turning capacitor and 4 switches.

The ICM7045 divides the oscillator frequency in sixteen binary stages to a frequency of 100 Hz; some of these intermediate outputs are used to generate the multiplex waveforms at a 12.5% duty cycle/800 Hz rate. The 100 Hz signal is then processed in the counters and multiplexed in the decoders.

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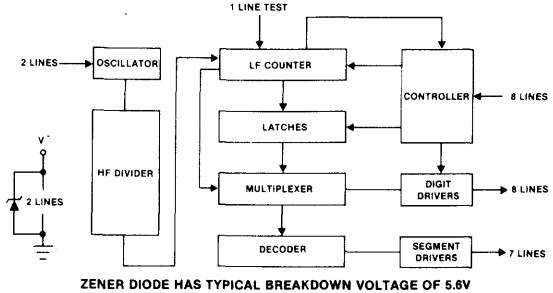
BLOCK DIAGRAM



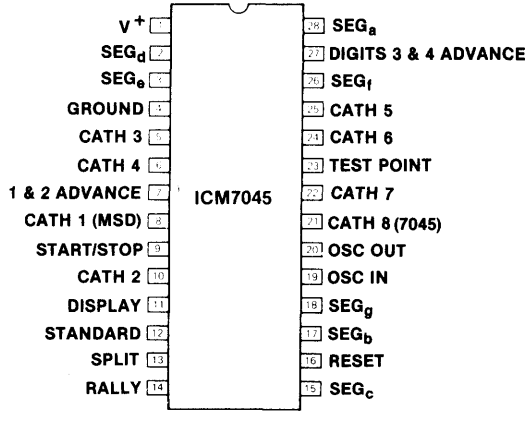
ZENER DIODE HAS TYPICAL BREAKDOWN VOLTAGE OF 5.6V

ORDERING INFORMATION

ICM7045 I DI — Package
28 Pin Plastic DIP
Temperature Range
I = Industrial −20°C to +85°C
Type

Order Dice by Following Part Number — ICM7045/D

PIN CONFIGURATION (outline dwg DI)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1) 1W
Supply Voltage . . . . . + 5.5V
Input Voltage . . . . . Equal to, but never in excess of the supply voltages
Output Voltage . . . . . Equal to, but never in excess of the supply voltages
Digit Drive Output Current 150mA/digit
Storage Temperatures . . . . . − 55 °C to + 125 °C
Operating Temperatures . . . . . − 20 °C to + 85 °C
Lead Temperature (Soldering, 10 sec) . . . . . 300 °C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

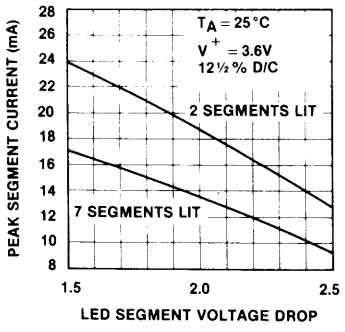
TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V+ = 3.6V$, $T_A = 25\,°C$ Parameters listed are absolute value

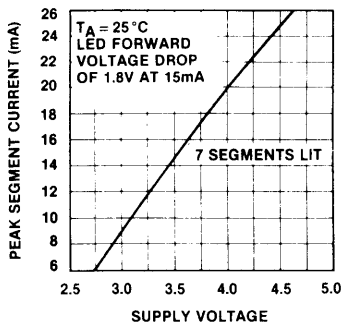
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$I+$	Display Off		180	2000	μA
		7 Segments Lit $V_F = 1.8V$	70	105		mA
		2 Segments Lit $V_F = 1.8V$	28	42		mA
Operating Voltage	V^+	$-20\,°C < T_A < 85\,°C$	2.5		4.5	V
Segment Current Drive	I_{SEG}	7 Segments I.T., $V_F = 1.8V$, 12.5% Duty Cycle				
Instantaneous			10	15		mA
Average			1.25	1.825		mA
Segment Current Drive		2 Segments Lit, $V_F = 1.8V$ 12.5% Duty Cycle				
Instantaneous			14	21		mA
Average			1.75	2.625		mA
Min. Switch Actuation Current, Any Switch	I_{SW}		50			μA
Digit Driver Leakage Current	I_{DLK}				200	μA
Segment Driver Leakage Current	I_{SLK}				200	μA
Typical Oscillator Stability	f_{STAB}	$3V \le V^+ \le 4V$, $C_{TUNING} = 15pF$		1.0		ppm
Oscillator Start Up Time	t_{start}	$V^+ = 3.6V$			0.1	sec
		$V^+ = 2.5V$			1.0	sec
Oscillator Input Capacitance	C_{IN}			17		pF

TYPICAL PERFORMANCE CURVES

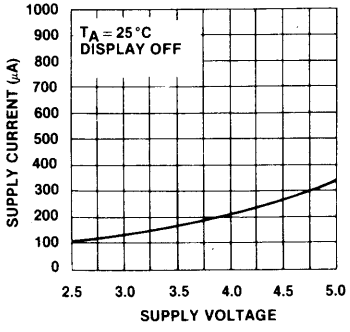
PEAK SEGMENT CURRENT DRIVE VS. LED SEGMENT VOLTAGE DROP



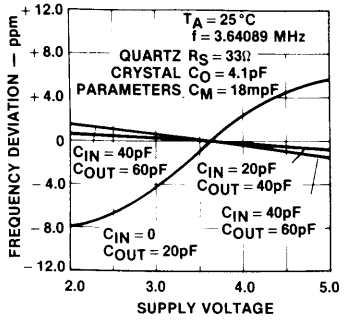
PEAK SEGMENT CURRENT VS. SUPPLY VOLTAGE

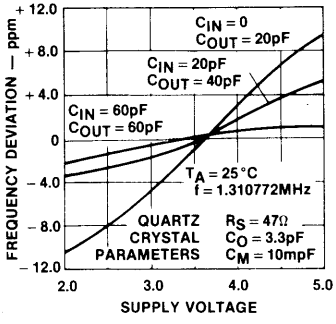


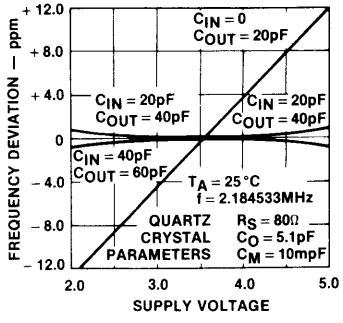
SUPPLY CURRENT VS. SUPPLY VOLTAGE



OSCILLATOR STABILITY VS. SUPPLY VOLTAGE FOR 3 DIFFERENT QUARTZ CRYSTALS



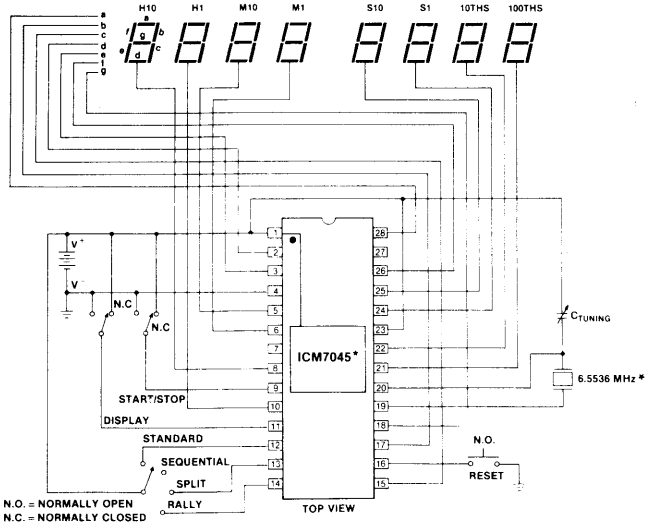




7

ICM7045

Quartz Crystal Parameters
f = 6.5536 MHz
R_s = 40Ω
C_1 = 15mpF
C_O = 3.5pF



NOTE: Specify quartz crystal to have nominal frequency value when tuned by a total parallel capacitance value of 12 pF or less.

Figure 1: Four Stopwatch Modes

FUNCTIONAL OPERATION

STOPWATCH/TIMER OPERATION

The control inputs used in the complete stopwatch application are: (refer to fig. 1)

START/STOP	RESET	SPLIT
DISPLAY	STANDARD	RALLY

START/STOP and DISPLAY are designed for connection to single pole double throw switches to insure operation free of contact bounce.

The switch connected to RESET can be normally open single pole single throw. STANDARD, SPLIT and RALLY are control points with internal pull down resistors to V^-.These are designed to be connected to a rotary function switch which will connect no more than one of these points to V^+. If STANDARD (SPLIT, RALLY) is connected to V^+ the stopwatch is said to be in the STANDARD (SPLIT, RALLY) mode. If all three are left open, the stopwatch is in the SEQUENTIAL mode.

RESET FUNCTION

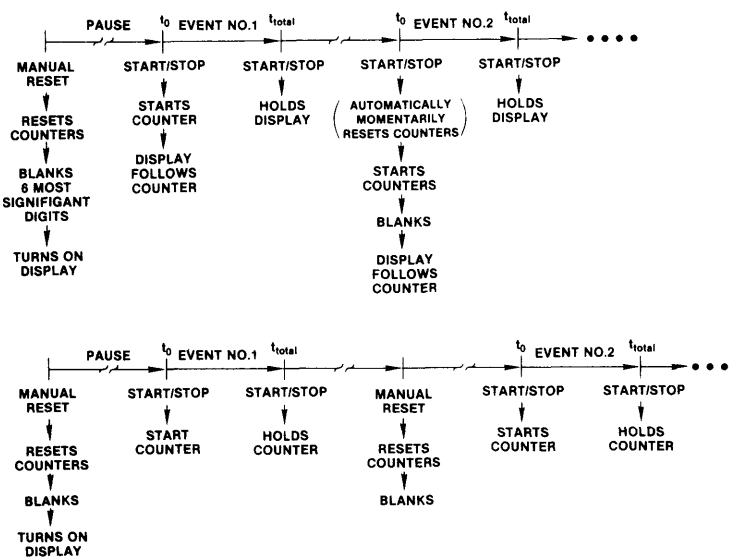
When the stopwatch is turned on, the RESET will normally be activated. This puts the stopwatch in a ready condition by:

1. Resetting all circuitry
2. Blanking seconds, minutes, hours
3. Showing 00 in the two least significant digits.
4. Turning on the display if it was previously turned off

The display of just two zeros in the two least significant digits gives the complete assurance that the stopwatch is "ready to go".

STANDARD MODE

In the STANDARD mode, after a reset has taken place, START/STOP is activated at time t_0. The clock and display are moving simultaneously. A second activation of START/STOP stops the clock and holds the display at time t_{total}. This completes an event. For timing a second event there are two options. One is to activate START/STOP at the start of the second event. This will momentarily reset the counter and display so that the timing of the second event proceeds from zero. Another activation of START/STOP stops the counter and display at time t_{total} to end the second event. The other option is to activate RESET after the first event is over. Then the second event proceeeds similarly to the first event. As is clear from this description, RESET can be used at any time to reset the stopwatch, including when a timing is in progress. The DISPLAY input can be activated to turn the display off and on. If the display is off when RESET is activated, it will reset and turn on. Turning off the display for timing long events will result in a very substantial power saving.

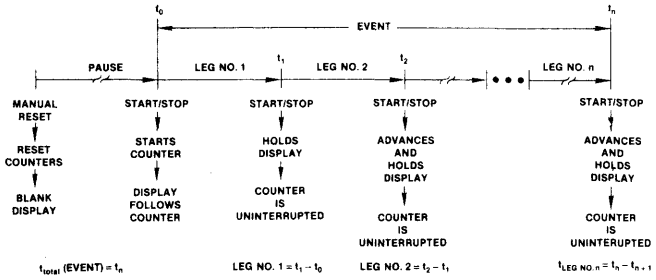


SEQUENTIAL MODE

The sequential mode of the stopwatch is designed for timing events consisting of more than one leg (such as relays, multilap races, etc.). After the initial reset the START/STOP is activated at t_0 to start the event. A second activation of START/STOP at time t_1 stops the display and allows t_1 to be read out, while the clock resets and starts counting again instantaneously. At time t_2 an activation of START/STOP enters t_2 (the time of leg 2) into the display. This sequence can continue indefinitely. Assuming the total event has n legs, the total elapsed time is then equal to the sum of the n times read out:

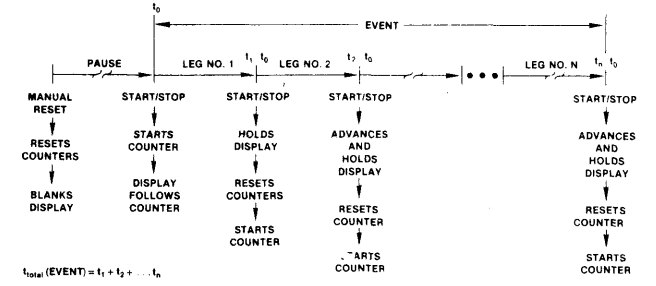
$$t_{total} = t_1 + t_2 \ldots + t_n$$

If it is desired to see the moving clock after a time has been recorded, the DISPLAY switch can be activated to release the display hold and catch up with the moving clock. The display cannot be turned off in the sequential mode. RESET can be activated at any time to reset clock and display.



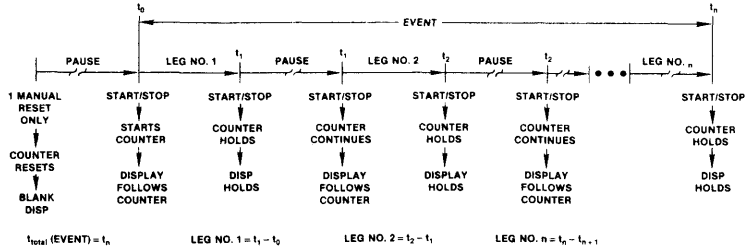
SPLIT MODE

The split mode is another mode for timing multileg events. In contrast to the sequential mode, the timing in the split mode is cumulative. From a reset condition, the START/STOP switch is activated at t_0 to start the counter and display running. A second activation at t_1 stops the display and allows t_1 to be read out while counter continues timing. A third activation at t_2 advances the display with the total elapsed time from t_0 to t_2 showing. Finally, at time t_n the total elapsed time of the event is entered in the display. The time of one leg of the event can be obtained by subtraction. The display can be synchronized to the counter (catch-up function) at any time by activating the display switch. To reset the timer, activate reset. The display cannot be turned off in the SPLIT mode.



RALLY MODE

The rally mode is designed for timing of events with interruptions. Consider an n leg event where the legs may be separated by intervals which should not be timed. The rally mode starts with a RESET. At time t_0 the stopwatch is started by activating START/STOP. After this point the RESET function is disabled to prevent accidental resets during long timing intervals. At time t_1 a START/STOP pulse stops counter and display. From here on each leg time is added to the total by a START/STOP pulse at the beginning of the leg and at the end. The individual leg times are determined by subtraction. The display can be turned on and off with the display switch.



CLOCK OPERATION

The control inputs used in a possible 24-hour clock configuration are (refer to fig. 2):

START/STOP
MINUTES ADVANCE
HOURS ADVANCE
RALLY

START/STOP, MINUTES ADVANCE and HOURS ADVANCE are designed for connection to single pole double throw switches; this assures contact bounce elimination on these inputs. To avoid an additional switch for the DISPLAY input, the RALLY input should be connected to V^+ through a 20k resistor and to V^- through a 0.01μF capacitor. These components insure that the display is on when power is applied to the circuit. The most convenient setting procedure is:

1. If clock is not running when power is applied activate START/STOP switch.
2. Depress MINUTES ADVANCE switch to obtain correct minutes setting, one minute count per activation.
3. Depress HOURS ADVANCE switch to obtain correct HOURS setting, one hour count per activation.

It is possible to set the clock more accurately or to correct small time errors by using START/STOP in combination with MINUTES ADVANCE. If the clock is, for instance, 20 seconds slow, activate the MINUTES ADVANCE once, then activate the START/STOP, wait 40 seconds and activate the START/STOP again. If the clock is 20 seconds fast, the START/STOP switch should be activated to stop the clock, then after 20 seconds activated again to restart the clock. Other clock configurations are possible (see Application Notes).

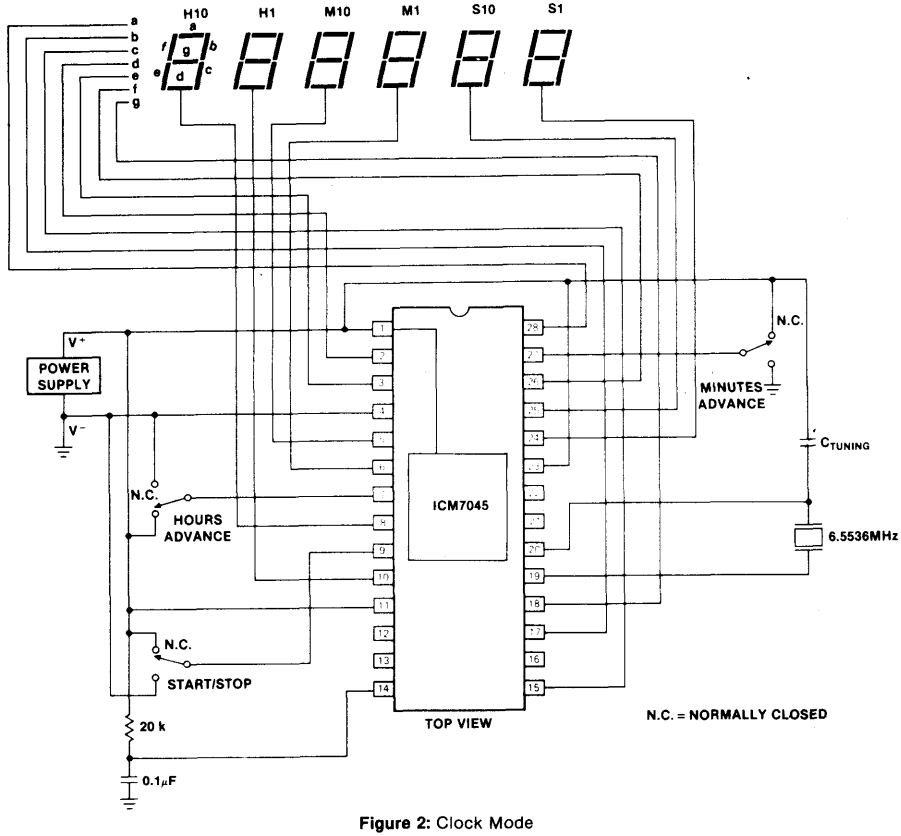


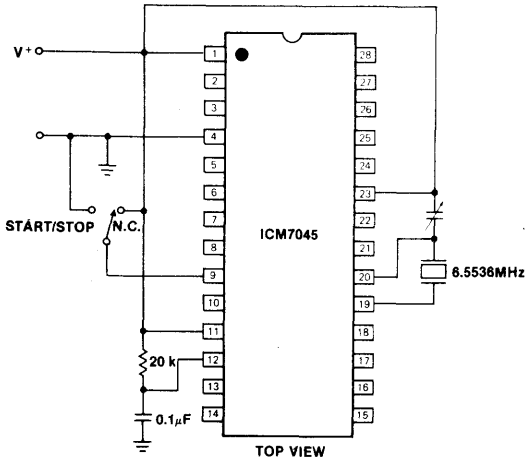
Figure 2: Clock Mode

APPLICATION NOTES

The ICM7045 have been designed with versatility of applications in the digital timer/stopwatch/24-hour clock field as the major objective. The simplicity of operating modes allow for an extremely practical, easy to use stopwatch, at the same time permit the design of a variety of simple lapse timer, stopwatch and clock circuits; a few of these will be shown and discussed briefly here.

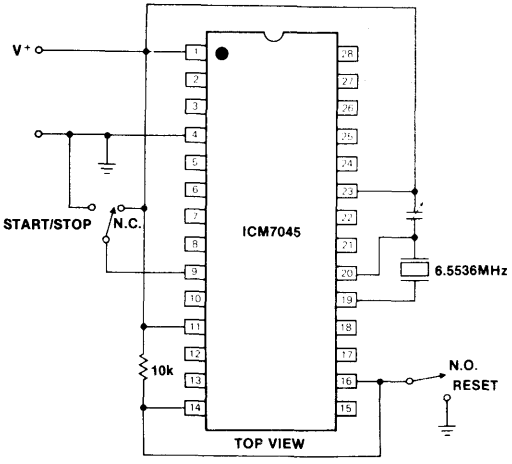
TIMER CIRCUIT I

This simple circuit (display connections not shown) allows interval timing up to 24 hours with a resolution of 0.01 second. Each interval is timed by one start and one stop pulse on the start/stop line. The start pulse for the next interval to be timed automatically resets the timer. Leading zero suppression is automatic.



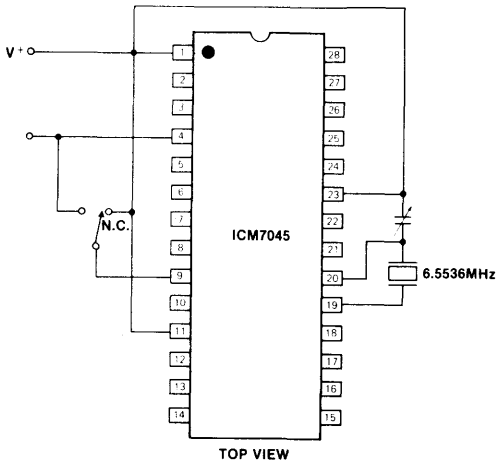
TIMER CIRCUIT II

This circuit allows cumulative timing of intervals. Each interval is timed by one start and one stop pulse on the start/stop line. Each subsequent interval timed adds to the total line displayed. The reset switch allows the timer to be reset to zero to start another sequence of intervals. Note that the time between the end of one interval and the start of the reset is not recorded nor added to the total.



TIMER CIRCUIT III

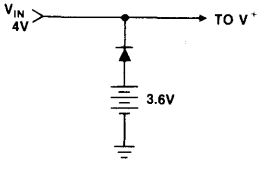
This circuit allows interval timing with a single pulse on the start/stop line. Each pulse enters the time elapsed since the previous pulse into the display, resets the timer and starts the timer for the next interval.



CLOCK CIRCUIT I

The standard clock circuit is shown and described in fig. 2. The clock accuracy with a stable voltage supply will depend mostly on the temperature and aging characteristics of the crystal.

The power supply can be modified to give battery standby power.

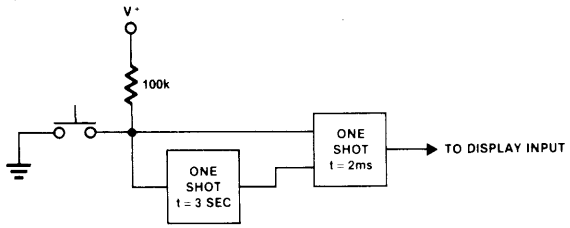


The standby circuit should be designed to provide the *specified minimum voltage* to the ICM7045.

OTHER CLOCK CIRCUITS

The basic clock circuit can be modified for various special applications. If it is desired to turn the display on and off, then connect the display input to an additional SPDT switch, while omitting the capacitor/resistor combination on the STANDARD Input.

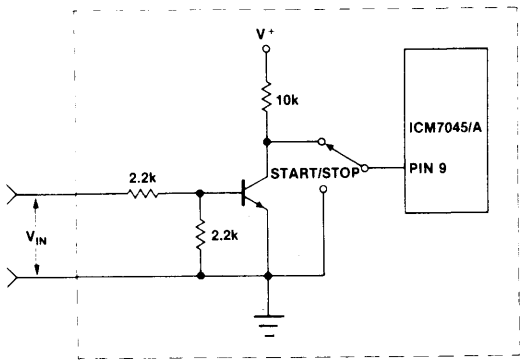
This input can then be wired directly to V^+. This 24-hour clock version might be applicable to vehicles, boats, etc. where a battery is available to supply the display off clock current, while the display can be turned on with the ignition. Another possible configuration would connect a special circuit to the DISPLAY input which generates a double pulse about 3 seconds apart:



This means depressing the switch will turn on the clock's display for 3 seconds. This allows design of a battery operated "on demand" digital 24-clock.

STOPWATCH EXTERNAL SYNC CIRCUIT

If the stopwatch is connected as shown in fig.1, a few additional components will allow external synchronization of the stopwatch in any mode:



NOTE: Be sure to minimize the distance between the transistor and the ICM7045 to prevent noise from being generated along this connection. *Noise spikes absolutely must not exceed the supply voltages.*

The external sync signal source must supply a positive pulse to activate the START/STOP input. The minimum voltage of this pulse is about 1.2V in the circuit as shown, but the triggering level can be changed by modifying the input resistor ratio. The output impedance of the external sync signal source should be no greater than 4k ohms.

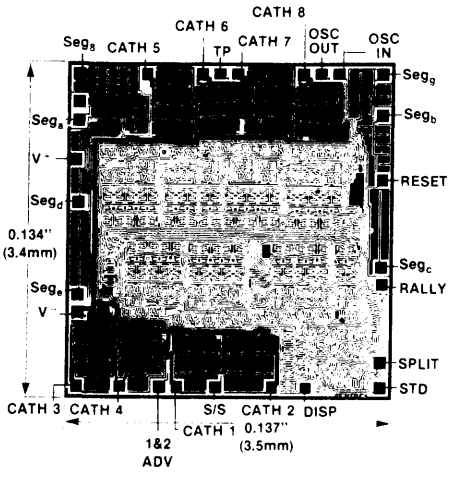
OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary MOS inverter with on-chip feedback resistors and an on-chip fixed input capacitor of 22pF. For the 6.5536 MHz crystal needed for normal timing using the ICM7045, it is suggested that the nominal load capacitance be kept under 12pF to keep total loading on the oscillator to a reasonable level. The actual trimmer range and the nominal load capacitance needed will have to be determined from the total stray capacitance of the particular circuit (including ICM7045 with package, PC board, etc.) and the tuning tolerance of the chosen crystal.

The series resistance of the crystal should also be kept to a low value (typically less than 50 ohms) to achieve adequate low voltage operation.

Oscillator tune up can be most easily performed using a pull-up resistor of 10k ohms on the fractional seconds digit, using period average tune for 1.25ms (800Hz).

CHIP TOPOGRAPHY



7

ICM7050
ICM1115
Quartz Clock Circuits
Bipolar Stepper Motor Applications

FEATURES

- **Single battery operation**
- **Very low current - typically 40μA at 4.19MHz**
- **Reset or stop function, inhibited during output**
- **Extremely low output saturation resistance: less than 100 ohms**
- **Complex direct drive alarm: 1Hz + 8Hz + 2048Hz**
- **Custom options available**

ORDERING INFORMATION

DEVICE	MOTOR OUTPUT	ALARM OUTPUT
ICM7050	47ms @ 0.5 Hz	Complex
ICM1115	0.5 Hz Square Wave	64 Hz Tone

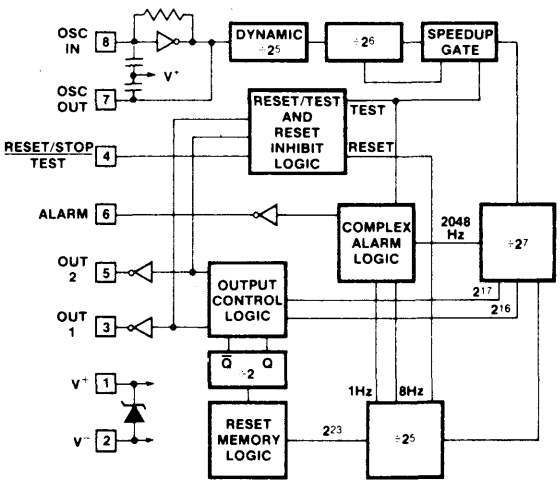
Note: These devices require a crystal frequency of 4.19 MHz. Consult ICM7070 data sheet for 32.768 kHz devices.

*See **PART NUMBER CHANGES** below.

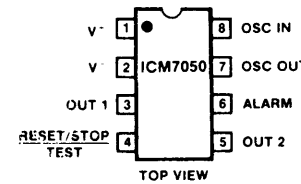
GENERAL DESCRIPTION

The ICM7050/ICM1115 are single battery analog quartz clock circuits intended for use with bipolar stepper motors and fabricated using Intersil's low voltage metal gate CMOS process. The circuits consist of a divider chain, output gating, output buffers and an oscillator which, when using the specified 4.19MHz crystal and capacitors, provides excellent stability. The high frequency portion of the divider chain consists of dynamic dividers, while the remainder are static. The dynamic dividers feature low power consumption and operating voltage, but limit low frequency operation. The 2^{23} divider chain is tapped at the 2^{11}, 2^{19}, and 2^{22} points to provide a complex alarm of 1Hz, 8Hz, and 2048Hz driving an output inverter. Several standard motor drive waveforms are available, and the large output inverters provide the low impedance necessary to drive the motor. A reset inhibit function is provided so that if the RESET occurs during an output pulse, resetting will not take place until the pulse is completed. RESET may also be used as a stop for synchronization to a time signal or tester. Motor drive will continue 1 sec. after RESET is released.

BLOCK DIAGRAM



PIN CONFIGURATION (outline dwg PA)



TOP VIEW

ORDERING INFORMATION

ICM7070 | PA

- PA: Package — See Outline Drawing
- |: Temperature Range: Industrial —20°C to +70°C
- ICM7070: Type

Order Devices by Following Part Number — ICM7050IPA, ICM1115AIPA, ICM1115BIPA

CUSTOM OPTIONS

The ICM7050 input and output configurations may be customized for:

- On-chip oscillator capacitance up to 20 pF at OSC IN or OSC OUT
- Output pulse frequency from 0.5 Hz to 64 Hz (standard crystal freq.)
- Output pulse width from 0.98 msec to 50% duty cycle
- Alarm output up to three binary frequencies from 1 Hz to 2048 Hz

Consult factory for mask programming charge and minimum order requirements.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1)	300mW
Supply Voltage	3V
Output Voltage (Note 2)	Equal to but never
Input Voltage (Note 2)	exceeding the supply voltage
Storage Temperature	−30°C to +125°C
Operating Temperature	−20°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

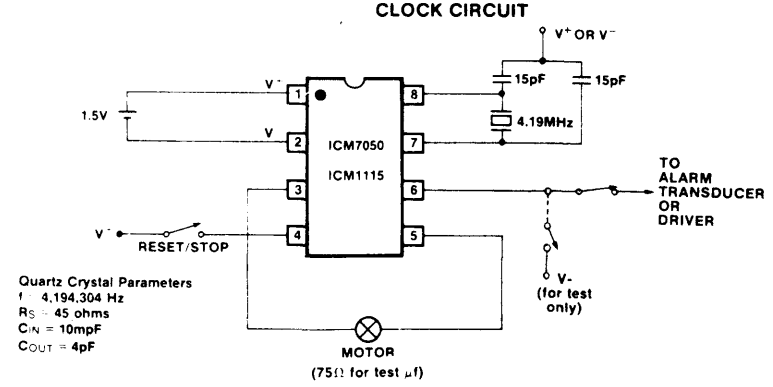
ELECTRICAL CHARACTERISTICS

($V+ = 1.5V$, f_{osc} = 4,194,304Hz test circuit, $T_A = 25°C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 3) except ICM1115A	I^+	No Load		40	60	μA
ICM1115A Only				80	120	
Operating Voltage	V^+	$-20°C < T_A < 70°C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	I_L = 4mA		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, I_L = 1mA		400	700	Ω
		N, I_L = 2mA		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \le V^+ \le 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec
Oscillator Transconductance (Note 3)	g_m	ICM7050	75	200		μmho
		ICM1115A	150	400		
		ICM1115B	75	200		

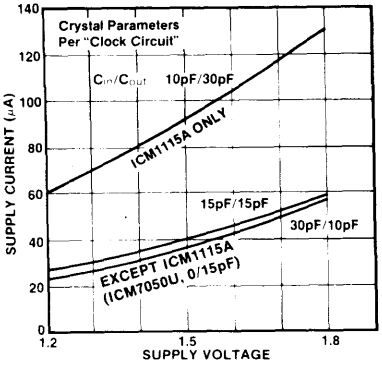
NOTE 3: Two options are available with the ICM1115. The ICM1115B is designed to be used with crystals whose load capacitance is 12 pF or less. Using input and output capacitors of 15 to 20 pF, this device will provide stable operation at very low supply current. For applications with larger load capacitance (15 to 20 pF), the ICM1115A ensures that an increased oscillator current is available to guarantee startup and operation over the voltage range. Using input and output capacitors of 30 to 40 pF, the ICM1115A will offer good stability at a supply current approximately twice that of the ICM1115B.

TYPICAL APPLICATION (also TEST CIRCUIT)

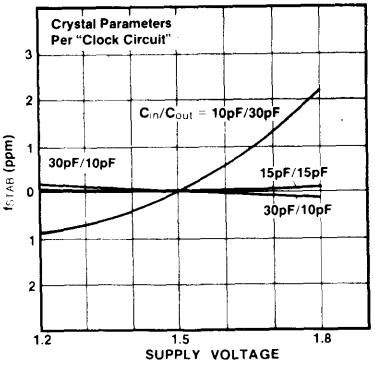


TYPICAL OPERATION CHARACTERISTICS

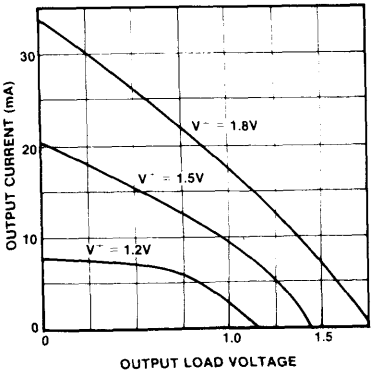
SUPPLY CURRENT vs SUPPLY VOLTAGE



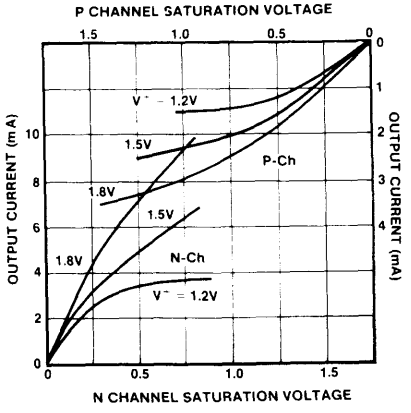
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



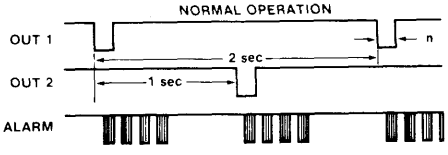
OUTPUT CURRENT vs OUTPUT LOAD VOLTAGE



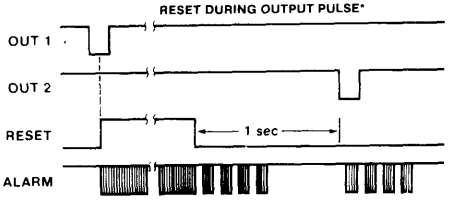
ALARM OUTPUT CURRENT vs SATURATION VOLTAGE



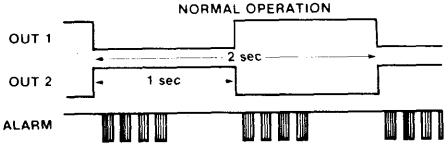
OUTPUT WAVEFORMS (ICM7050)

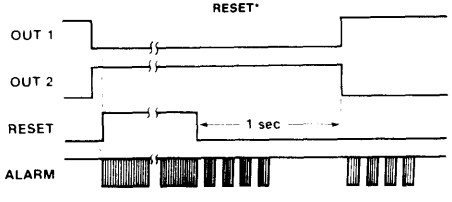


n = 47 msec for ICM7050



OUTPUT WAVEFORMS (ICM1115)





*Shown during OUTput 1; exchange OUTput 1 and OUTput 2 for opposite case.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7050 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15/15pF or 20/20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip. Oscillator tuning should be done at the OSCillator OUTput.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

g_m required for startup

$$g_m = \omega^2 C_{in}C_{out}R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance
C_{out} = output capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 50μmhos.

OSCILLATOR TUNING METHODS

When tuning the oscillator two methods can be used. The first method would be to monitor the output pulse at either OUT 1 or OUT2 with a counter set to measure the period. The oscillator trimmer would then be adjusted for a reading of 2.000000 secs. A second method would be to put the device in the **reset** mode by pulling the RESET pin to V+ and then monitor the ALARM output with a counter set to measure average period. The ALARM output is a continuous 2048Hz when in the **reset** mode, which gives a period of 488.28125μs.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input,the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

TEST MODE OPERATION

Pulling the RESET/TEST input to —7V switches the device into the **test** mode to speedup automatic testing. When in the **test** mode the output rate is increased 16 times, from 1Hz to 16Hz, with a corresponding reduction in pulse width. The ALARM output changes to a composite waveform of 16Hz and 128Hz. The circuit can be **reset** while in the **test** mode by shorting the ALARM output to V⁻.

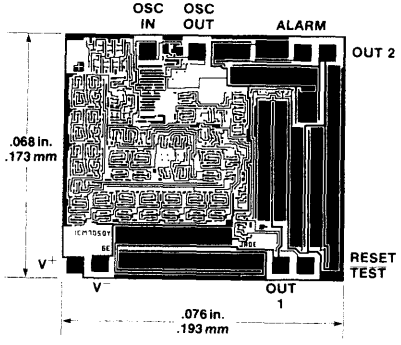
ALARM CONSIDERATIONS

The ALARM output inverter is large enough to directly drive transducers requiring up to 2mA of current. If more current is needed, a PNP buffer should be used*. A slight flutuation in the supply current of 0.5μA to 1.0μA will be seen; this is a result of 2048Hz driving the relatively large gate capacitance of the alarm output transistors.

*See Intersil Application Bulletin A031 for details.

7

CHIP TOPOGRAPHY



ICM7051
CMOS Auto Clock Circuit

FEATURES

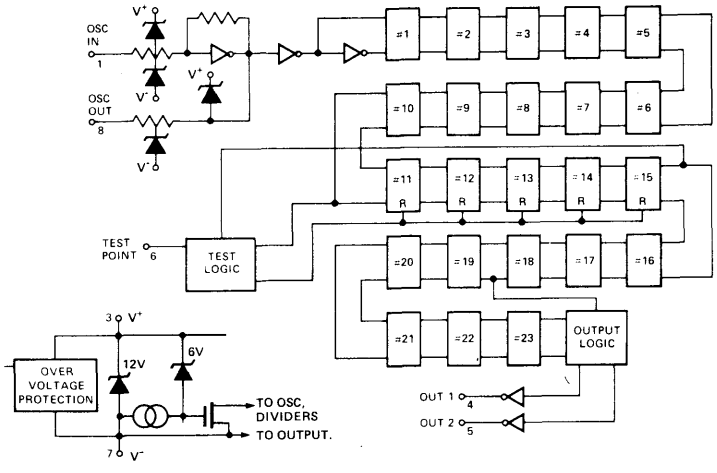
- **Wide operating supply voltage and temperature ranges**
- **Excellent oscillator stability**
- **Short circuit protected bridge output with low ON resistance**
- **Oscillator feedback resistor on-chip**
- **All inputs fully protected**
- **Nominal 12.6 volt zener on chip**
- **64Hz output for synchronous motor applications (ICM7051A)**
- **1 Hz output with 31.2 ms output pulse width for stepper motor applications (ICM7051B)**
- **Typical power dissipation < 4 mW at 12 volts**

GENERAL DESCRIPTION

The ICM7051A/B is an auto clock circuit fabricated using Intersil's standard metal gate CMOS process. Included on-chip are the oscillator, dividers, output drivers and over-voltage protection circuitry. The oscillator of the ICM7051A/B has the feedback component on-chip, and when used with the specified crystal parameters will give excellent stability. The binary dividers of the ICM7051 allow division from 4.19MHz and drive a bridge output which provides an alternating 31.2ms output pulse at 1Hz for the ICM7051B (0.5Hz each side) or a 64Hz square wave output for the ICM7051A. The bridge output consists of two large inverters with the output ON resistance of the N and P channel devices together being less than 100 ohms with V_{BATT} equal to 13.5 volts and load current equal to 10mA.

The ICM7051 series contains an on-chip zener which, when used with an external resistor and capacitor, will provide protection against over-voltage transients that may occur in an automobile environment.

SCHEMATIC DIAGRAM



ORDERING INFORMATION

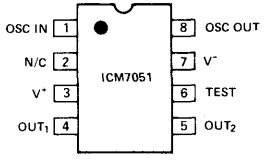
ICM7051A
ICM7051B — I — PA

- PA: PACKAGE — PA = 8 PIN MINIDIP
- I: TEMPERATURE RANGE — -20°C to +85°C
- ICM7051A/B: TYPE

Order dice by following part numbers: ICM7501A/D. ICM7051B/D

Note: The ICM7051A was formerly known as ITS 9042-1.

PIN CONFIGURATION (outline dwg PA)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{BATT}, see TEST CIRCUIT) ..... -12 to +25V (Note 1)
..... -0.5 to +13.5V
Output Voltage and T.P. Input ..... Not to exceed supply voltage
Storage Temperature ..... -40°C to +125°C
Operating Temperature ..... -20°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation (Note 2) ..... 0.5 Watt
Latch up holding current (Note 3) 100mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Stress duration not to exceed 2 min.
Note 2: This value of power dissipation refers to that of the package and will not be normally obtained under normal operating conditions.
Note 3: A destructive latch up mode is possible if an input or output is forward biased with respect to either the positive or negative supplies. The ICM7051 has an absolute maximum latch up holding current of 100mA. This means the device, when operated at ambient temperature, will return to its normal operating state after an inadvertant input transient, if the supply current is limited to less than the absolute maximum latch up holding current of the device.

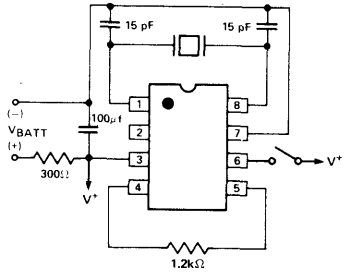
OPERATING CHARACTERISTICS

V_{BATT} = 13.5V, T_A = 25°C, f_{OSC} = 4.194304MHz, R_L = 1.2 kΩ, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supply Current	I^+	No Load	V_{BATT} = 13.5V			7	mA
			V^+ = 7.0V			1	
Supply Voltage Range (Note 4)	V_{BATT}	T_A = 25°C		4.5	>3.5	22	V
		-20°C ≤ T_A ≤ +85°C		7.0		17	
Output Resistance (n+p)	R_{OUT}	I_O = 10mA				100	Ω
		V^+ = 5V, I_O = 5mA			130		
Zener Voltage	V_Z	I_Z = 5mA		11		14	V
Oscillator Stability	f_{STAB}	6V ≤ V^+ ≤ V_Z				2	ppm
Oscillator Start Up Time	t_{START}	6V ≤ V^+ ≤ V_Z				1	sec
Output Leakage Current	I_{OLK}	All Outputs				100	μA
Oscillator Transconductance	gm	V^+ ≥ 6.0V			250		μmho
		V^+ ≥ 3.0V		25	100		

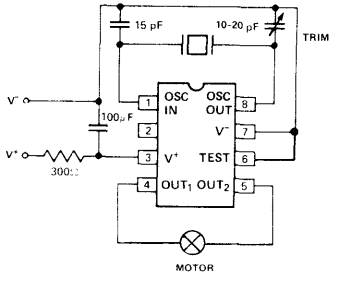
Note 4: In Test Circuit only. V^+ should not exceed V_Z.

TEST CIRCUIT



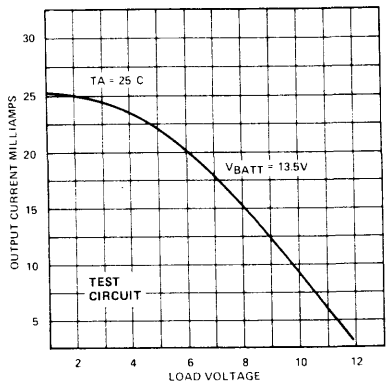
TYPICAL AUTO CLOCK

Quartz Crystal Parameters
R_S = 100Ω
C_m = 0.012 pF
C_O = 5 pF
f = 4.194,304 Hz

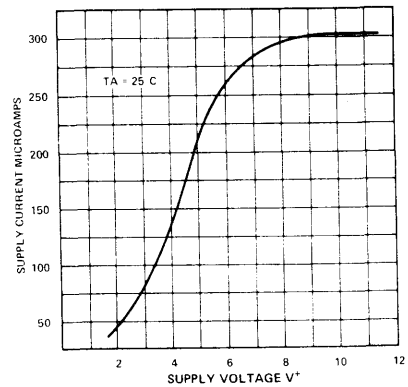


TYPICAL OPERATING CHARACTERISTICS

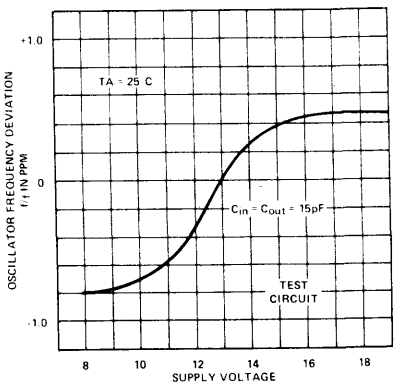
Output Current as
a Function of Load Voltage



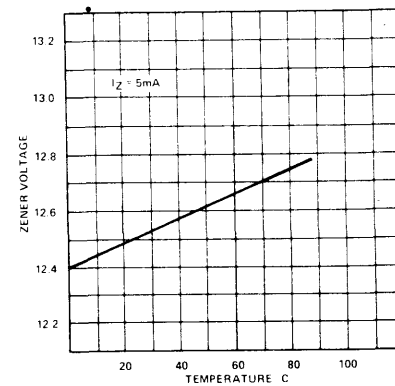
Supply Current as
a Function of Supply Voltage



Oscillator Stability as
a Function of Supply Voltage

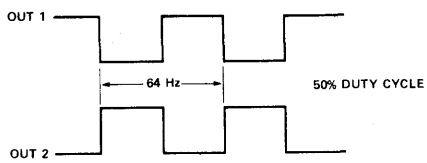


Zener Voltage as
a Function of Temperature

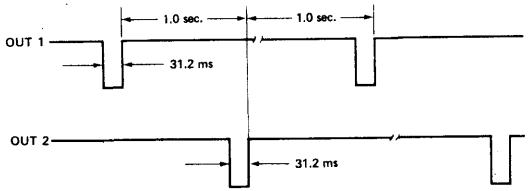


OUTPUT WAVEFORMS

ICM 7051A



ICM 7051B



The ICM7051 uses a TEST point to facilitate testing. This pin has an on-chip pulldown resistor, and for normal operation is at V^-. Connecting this pin to V^+ will give a 32 times speed-up of the outputs.

CUSTOM VERSIONS

The ICM7051 may be modified with alternative metal masks to provide a different number of dividers, various pulse widths, increased oscillator transistors or optional V zener pad for use with an external zener diode. The ICM7051 can be adapted for use with different synchronous motors as well as a variety of stepping motors. Consult factory for details.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7051 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15/15pF or 20/20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

To tune the oscillator, the best method is to monitor the output pulse at either OUT1 or OUT2 with a counter set to measure the period. The oscillator trimmer is then adjusted for a reading of 15.625 msec for the ICM7051A, or 2.0000 secs for the ICM7051B. Note that different output frequencies can be obtained by varying the crystal frequency over a range of 1 to 10MHz. In particular, a 60Hz output will result if a 3.93216MHz crystal is used with the ICM7051A.

The follwing expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

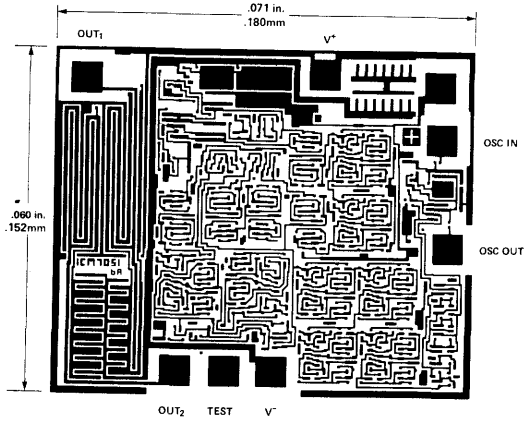
g_m required for startup

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance
C_{out} = output capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed about 1/2 the value of the oscillator at the relevant supply voltage.

CHIP TYPOGRAPHY



ICM7070L

Quartz Clock Circuits Bipolar Stepper Motor Applications

FEATURES

- **Single battery operation**
- **Very low current - typically 3 μA**
- **Reset or stop function, inhibited during output**
- **Extremely low output saturation resistance: less than 100 ohms**
- **Complex direct drive alarm: 1Hz + 8Hz + 2048Hz**
- **On chip oscillator input capacitor**
- **Custom options available**

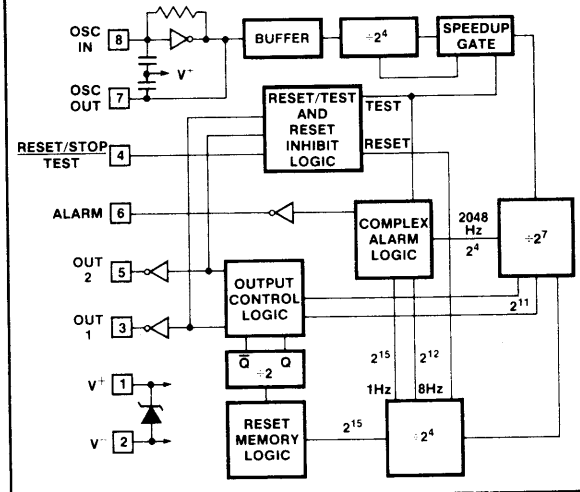
DEVICE	MOTOR OUTPUT
ICM7070L	31ms @ 0.5 Hz

Note: These devices require a crystal frequency of 32.768 kHz. Consult ICM7050 family data sheet for 4.19 MHz devices.

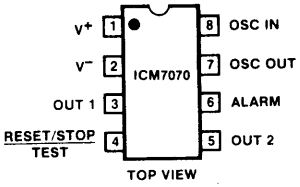
GENERAL DESCRIPTION

The ICM7070 is a single battery analog quartz clock circuits intended for use with bipolar stepper motors and fabricated using Intersil's low voltage metal gate CMOS process. The circuit consists of a divider chain, control gating, output buffers and an oscillator which, when using the specified 32 kHz crystal and capacitors, will provide excellent stability. The 2^{15} divider chain is tapped at the 2^{15}, 2^{12}, and 2^{4} points to provide a complex alarm of 1Hz, 8Hz, and 2048Hz driving an output inverter. Several standard motor drive waveforms are available, and the large output inverters provide the low impedance necessary to drive the motor. A reset inhibit function is provided so that if the RESET occurs during a (non-square wave) output pulse, resetting will not take place until the pulse is completed. RESET may also be used as a stop for synchronization to a time signal or tester. Output will begin 1 sec. after RESET goes low again, and in the correct sequence.

BLOCK DIAGRAM

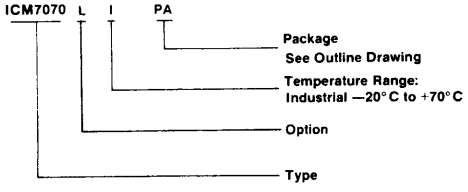


PIN CONFIGURATION (outline dwg PA)



TOP VIEW

ORDERING INFORMATION



CUSTOM OPTIONS

The ICM7070 input and output configurations may be customized for:

- On-chip oscillator capacitance up to 20pF at OSC IN or OSC OUT
- Output pulse frequency from 0.5 Hz to 64 Hz standard crystal freq.
- Output pulse width from 0.98 ms to 50% duty cycle
- Alarm output up to three binary frequencies from 1 Hz to 2048 Hz

Consult factory for mask programming charge and minimum order requirements.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1)	300mW
Supply Voltage	3V
Output Voltage (Note 2)	Equal to but never
Input Voltage (Note 2)	exceeding the supply voltage
Storage Temperature	−30°C to +125°C
Operating Temperature	−20°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

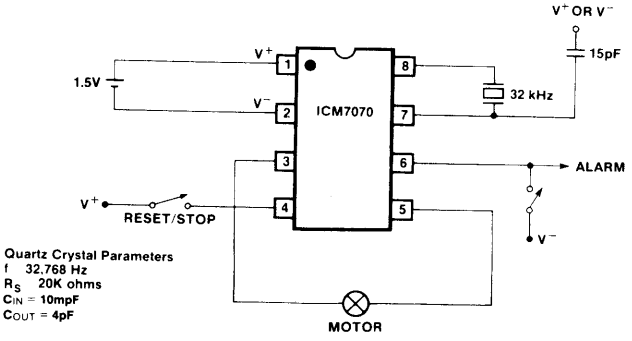
ELECTRICAL CHARACTERISTICS

($V+ = 1.5V$, fosc = 32,768 Hz test circuit, $T_A = 25°C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+	No Load		3	6	μA
Operating Voltage	V^+	$-20°C < T_A < +70°C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	$I_L = 4mA$		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, $I_L = 1mA$		400	700	Ω
		N, $I_L = 2mA$		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \leq V^+ \leq 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec
Oscillator Input Capacitance	C_{IN}		16	20	24	pF
Oscillator Transconductance	g_m		2	7		μmho

TYPICAL APPLICATION

CLOCK CIRCUIT



Quartz Crystal Parameters
f 32.768 Hz
R_S 20K ohms
C_{IN} = 10mpF
C_{OUT} = 4pF

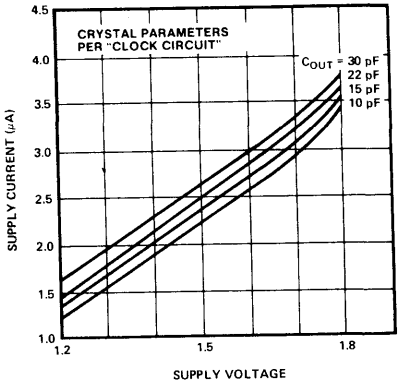
NOTES:

RESET/STOP: If pin 4 is not used, it should be tied to V−

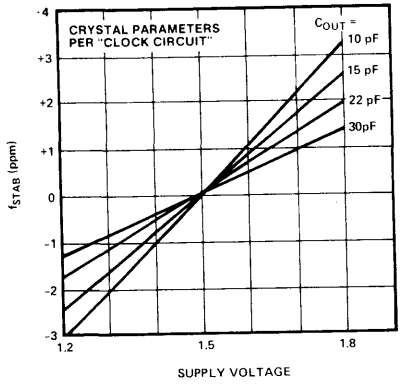
OUTPUT FREQUENCIES: Crystal frequencies from 20 to 100 kHz may be used to obtain different output frequencies. See **Oscillator Considerations** for suitable crystal parameters.

TYPICAL OPERATION CHARACTERISTICS

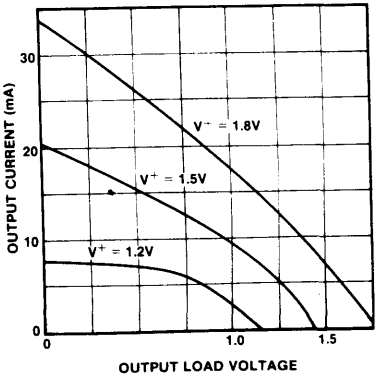
SUPPLY CURRENT vs SUPPLY VOLTAGE



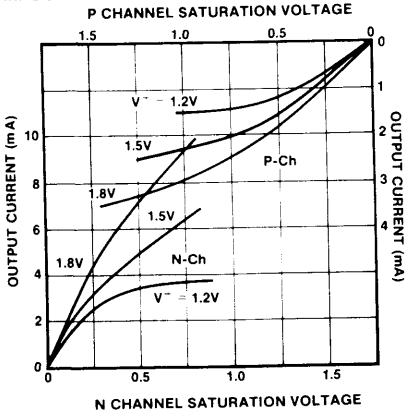
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



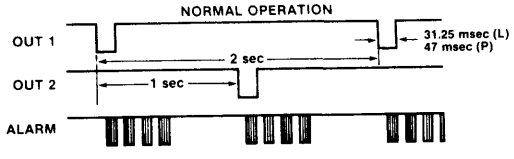
OUTPUT CURRENT vs OUTPUT LOAD VOLTAGE

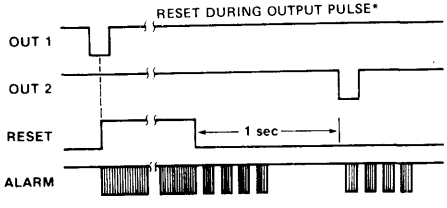


ALARM OUTPUT CURRENT vs SATURATION VOLTAGE



OUTPUT WAVEFORMS (ICM7070L)





APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7070 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15pF or 20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip. Oscillator tuning should be done at the oscillator output.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

g_m required for startup

$$g_m = \omega^2 C_{in}C_{out}R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance
C_{out} = output capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 20 μmhos.

OSCILLATOR TUNING METHODS

When tuning the oscillator two methods can be used. The first method would be to monitor the output pulse at either OUT 1 or OUT 2 with a counter set to measure the period. The oscillator trimmer would then be adjusted for a reading of 2.000000 secs. A second method would be to put the device in the **reset** mode by pulling the RESET pin to V^+ and then monitor the ALARM output with a counter set to measure average period. The ALARM output is a continuous 2048Hz when in the **reset** mode, which gives a period of 488.28125μs.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. the Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

TEST MODE OPERATION

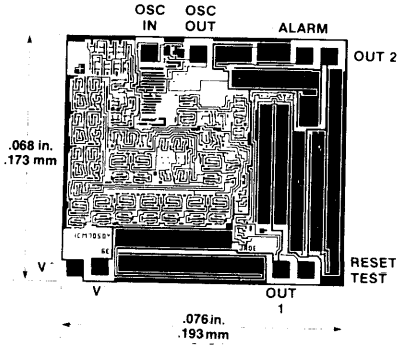
Pulling the RESET/TEST input to —7V switches the device into the **test** mode to speed up automatic testing. When in the **test** mode the output rate is increased 4 times, from 0.5Hz to 2Hz, with a corresponding reduction in pulse width. The ALARM output changes to a composite waveform of 4Hz and 32Hz. The circuit can be reset while in the **test** mode by shorting the ALARM output to V^-.

ALARM CONSIDERATIONS

The ALARM output inverter is large enough to directly drive transducers requiring up to 2mA of current. If more current is needed, a PNP buffer should be used*. A slight fluctuation in the supply current of 0.5μA to 1.0μA will be seen; this is a result of the 2048Hz drive to the relatively large gate capacitance of the alarm output transistors.

*See Intersil Application Bulletin A031 for details.

CHIP TOPOGRAPHY



ICM7206 CMOS Touch Tone™ Encoder

FEATURES

- **Low cost system with minimum component count**
- **Fully integrated oscillator uses 3.58 MHz color TV crystal**
- **High current bipolar output driver**
- **Low output harmonic distortion**
- **Wide operating supply voltage range: 3 to 6 volts**
- **Uses inexpensive single contact per key calculator type keyboard (ICM7206/C/D)**
- **Extremely low power ≤ 5.5mW with a 5.5V supply**
- **Single and dual tone capabilities**
- **Multiple key lockout**
- **Disable output: provides output switch function whenever a key is pressed**
- **Custom options available**

GENERAL DESCRIPTION

The Intersil ICM7206/A/B/C/D are 2-of-8 sine wave tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate programmable dividers, a D/A converter, and a high level output driver.

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58 MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately -3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

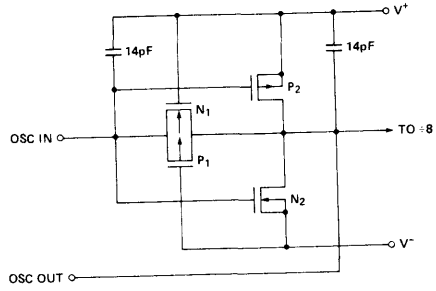
The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to V^+.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to V^+. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its' source is connected to V^+.

The 7206B requires a 4 x 4 double contact keyboard with the common line tied to V^-. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE output consists of an n-channel open drain FET with its' source tied to V^-.

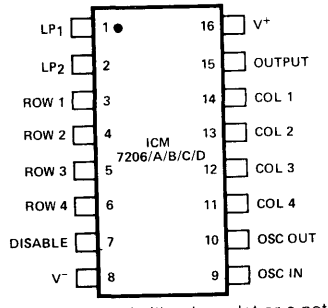
The 7206C uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will be on only during the time that a key is depressed.. The DISABLE output consists of an n-channel open drain FET with its source tied to V^-.

The 7206D uses a single contact 3 x 4 or 4 x 4 keyboard. The oscillator will be on only during the time that a key is depressed. DISABLE output consists of a p-channel open drain FET with its source tied to V^+.



ICM7206 Oscillator

PIN CONFIGURATION (OUTLINE DRAWING PE)



Pin 1 is designated either by a dot or a notch.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7206 JPE	-40° C to +85° C	Plastic
ICM7206A JPE	-40° C to +85° C	Plastic
ICM7206B JPE	-40° C to +85° C	Plastic
ICM7206C JPE	-40° C to +85° C	Plastic
ICM7206D JPE	-40° C to +85° C	Plastic
ICM7206/D	-40° C to +85° C	DICE
ICM7206A/D	-40° C to +85° C	DICE
ICM7206B/D	-40° C to +85° C	DICE
ICM7206C/D	-40° C to +85° C	DICE
ICM7206D/D	-40° C to +85° C	DICE

INTERSIL

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) 6.0V
Supply Current V^- (terminal 8) 25mA
Supply Current V^+ (terminal 16) 40mA
Disable Output Volt. (term. 7) .. Not more pos. than V^+ nor more neg. than −6V with respect to V^+
Output Volt. (term. 15). Not more pos. than +5V with respect to V^+, nor more neg. than −1.0 with respect to V^-
Output Current (terminal 15) 25mA
Power Dissipation 300mW
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

NOTE 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2. The ICM7206 family has a zener diode connected between V^+ and V^- having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.5V$, Test Circuit, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	R_L disconnected			450	1000	μA
Guaranteed Operating Supply Voltage Range (Note 3)	V_{OP}	$-40°C \le T_A \le +85°C$		3.0		6.0	V
Peak to Peak Output Voltage	V_{OUT}	C_1, C_2 disconnected — Low Band		0.90	1.15	1.45	V
RMS Output Voltage		$R_L = 1k\Omega$, no filtering — High Band		1.10	1.40	1.70	V
		$R_L = 1k\Omega$, $f_{OUT} = 697Hz$	C_2 Only		480		mV
			C_1 to C_2		480		mV
			No filtering		490		mV
		$R_L = 1k\Omega$, $f_{OUT} = 1633Hz$	C_1		490		mV
			C_1 to C_2		580		mV
			No filtering		655		mV
Skew Between High and Low Band Output Voltages		$R_L = 1k\Omega$, C_1, C_2 disconnected			2.5	3.0	dB
Output Impedance	Z_O	$R_L = 1k\Omega$	Operating		90	200	Ω
			Quiescent		25		KΩ
Total Output Harmonic Distortion	THD1	Either Hi or Low Bands			20	25	%
		No Low Pass Filtering					%
Total Output Harmonic Distortion	THD2	$R_L = 1k\Omega$, $C_1 = .002\mu F$	$f_{OUT} = 697Hz$		2.3	10	%
		$C_2 = 0.02\mu F$	$f_{OUT} = 1633Hz$		1.0	10	%
Maximum Output Voltage Level	V_{OH}	$R_L = 1k\Omega$				4.6	V
Minimum Output Voltage Level	V_{OL}	$R_L = 1k\Omega$					V
Keyboard Input Pullup Resistors	R_{IN}	Terminals 3,4,5,6,11,12,13,14		0.5			
Keyboard Input Capacitance	C_{IN}	Terminals 3,4,5,6,11,12,13,14		35	100	150	KΩ
Guaranteed Oscillator Frequency Range (Note 4)	f_{OSC}	$3 \le (V^+ - V^-) \le 6V$				5	pF
Guaranteed Oscillator Frequency Range		$4V \le (V^+ - V^-) \le 6V$		2.0		4.5	MHz
System Startup Time on Application of Power	t_{on}	ICM7206, ICM7206A		2.0		7	MHz
System Startup Time on Application of Power and Key Depressed Simultaneously		ICM7206B, ICM7206C, ICM7206D			10		ms
DISABLE Output Saturation Resistance (ON STATE)	R_D	See Logic Table for Input Conditions Current = 4mA				7	ms
DISABLE Output Leakage (OFF STATE)	I_{OLK}	See Logic Table for Input Conditions			330	700	Ω
Oscillator Load Capacitance	C_{OSC}	Measured between terminals 9 & 10, no supply voltage applied to circuit $-40°C \le T_A \le 85°C$				10	μA
Guaranteed Output Frequency Tolerance	f_O	Any output frequency Crystal tolerance ±60ppm Crystal load capacitance CL = 30pF			7		pF
Oscillator Startup Time ICM7206B, C, D	t_{start}	$V^+ = 3V$ (Note 5)				±0.75	%
						7	ms

NOTE 3: Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.

NOTE 4: The ICM7206 family uses dynamic high frequency circuitry in the initial 2^3 divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.

NOTE 5: After row input is enabled.

TRUTH TABLE

LINE	ROWS (1) ACTIVATED	COLS (2) ACTIVATED	OUTPUT (TERMINAL #15)	DISABLE (TERMINAL #7)	COMMENTS
1	0	0	Off	Off	Quiescent State
2	1	1	$f_{row} + f_{col}$	On	Dual Tone
3	1	2 or 3 (incl. col #4)	f_{row}	On	Single Tone
4	2 or 3	1	f_{col}	On	Single Tone
5	2 or 3	2 or 3 (excl. col #3)	D.C. Level	On	No Tone
6	1	4 or 3 (must excl. col #4)	f_{row}, 50% Duty Cycle	f_{row}, 50% Duty Cycle	f_{row} Test
7	4	1	f_{col}, 50% Duty Cycle	f_{col}, 50% Duty Cycle	f_{col} Test
8	0	1 or 2 or 3 or 4	Off	Off	n/a*
9	1	0	902Hz + f_{row}	On	n/a*
10	2 or 3	0	902Hz	On	n/a*
11	4	0	902Hz, 50% Duty Cycle	902Hz, 50% Duty Cycle	n/a*
12	2 or 3 or 4	4	D.C. Level	Indeterminate	Multiple Key Lockout
13	4	2 or 3 or 4	D.C. Level	Indeterminate	Multiple Key Lockout

*n/a — not applicable to telephone calling.

Note 1: Rows are activated for the ICM7206/C by connecting to a negative supply voltage with respect to V^- (terminal 16) at least 33% of the value of the supply voltage (V^+-V^-). For the ICM7206A rows (and columns) are activated by connecting to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+-V^-). The rows and columns of the ICM7206B are activated by connecting to a negative supply voltage.

Note 2: Columns (ICM7206) are activated by being connected to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+-V^-).

COMMENTS

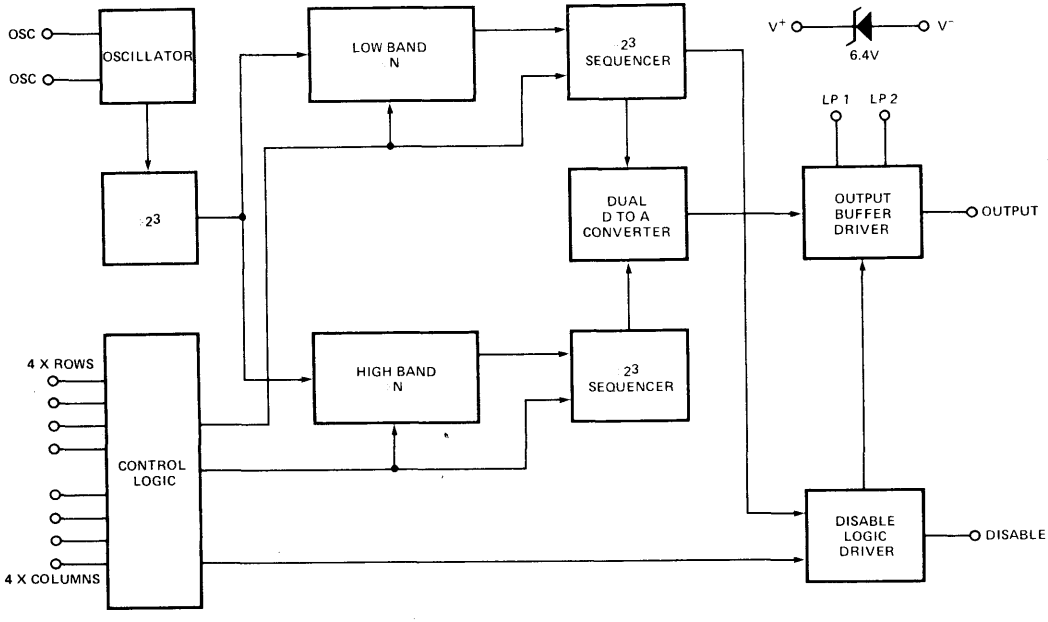
All combinations of row and column activations are given in the truth table. Lines 1 thru 7 and 12, 13 represent conditions obtainable with a matrix keyboard. Lines 8 thru 11 are given only for completeness and are not pertinent to telephone dialing.

Lines 6 and 7 show conditions for generating 50% duty cycle full amplitude signals useful for rapid testing of the row and column frequencies on automatic test equipment. In all other cases, output frequencies on terminal 15 are single or dual 4 level synthesized sine waves.

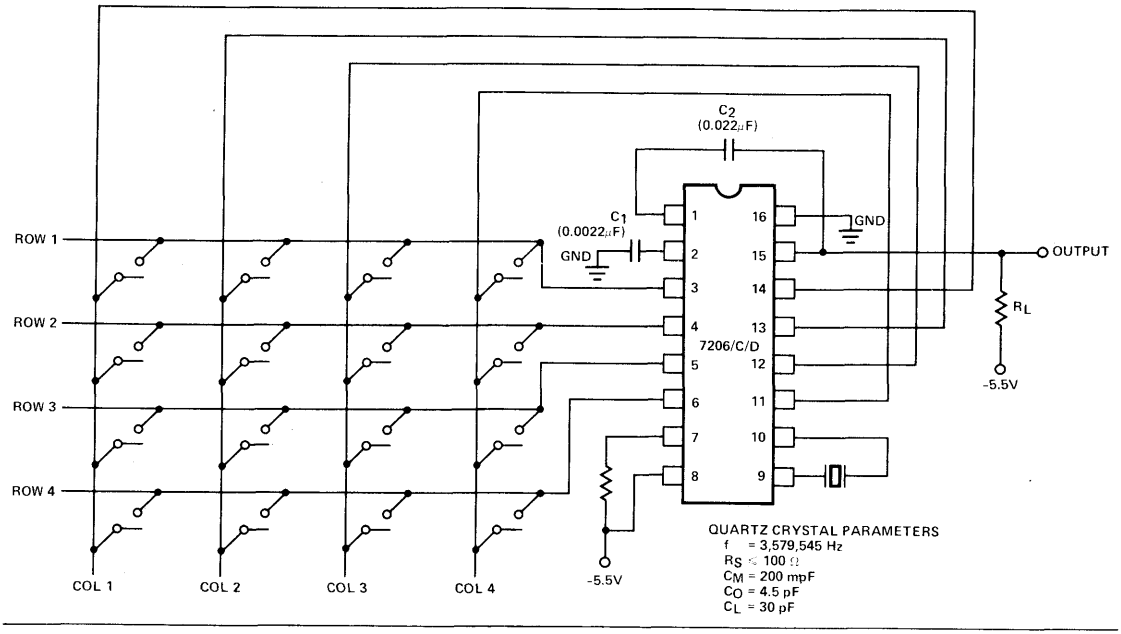
A 'DC LEVEL' on terminal 15 may be any voltage level between approximately 1.2 and 4.3 volts with respect to V^- (terminal 8) for a 5.5 volt supply voltage.

The impedance of the OUTPUT (terminal 15) is approximately 20K ohms in the OFF state. The 'DISABLE OUT-OUT' ON and OFF conditions are defined in the TYPICAL OPERATING CHARACTERISTICS.

SCHEMATIC DIAGRAM

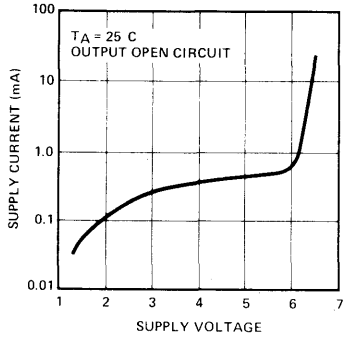


TEST CIRCUIT (single contact keyboard devices shown)

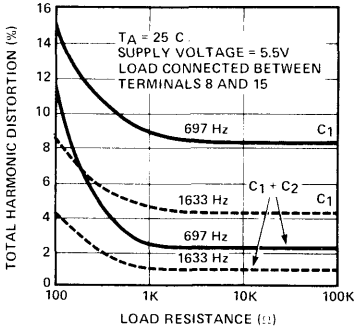


TYPICAL OPERATING CHARACTERISTICS

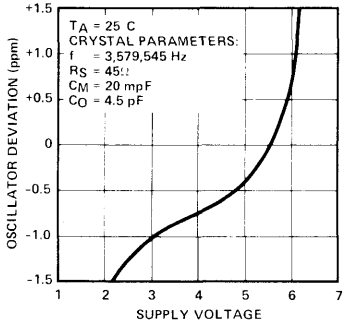
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



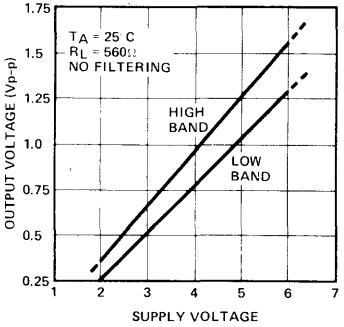
TOTAL HARMONIC DISTORTION AS A FUNCTION OF LOAD RESISTANCE

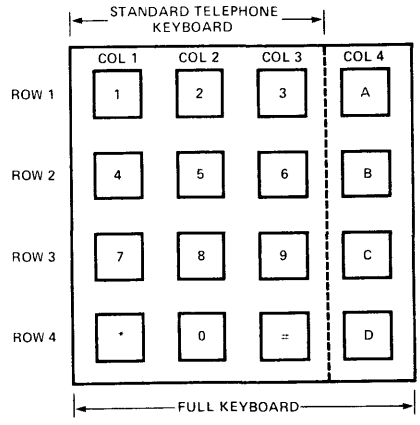


OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE



PEAK TO PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE





KEY	LOW BAND FREQ. Hz	HI BAND FREQ. Hz
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
*	941	1209
0	941	1336
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

FIGURE 1: Keyboard Frequencies

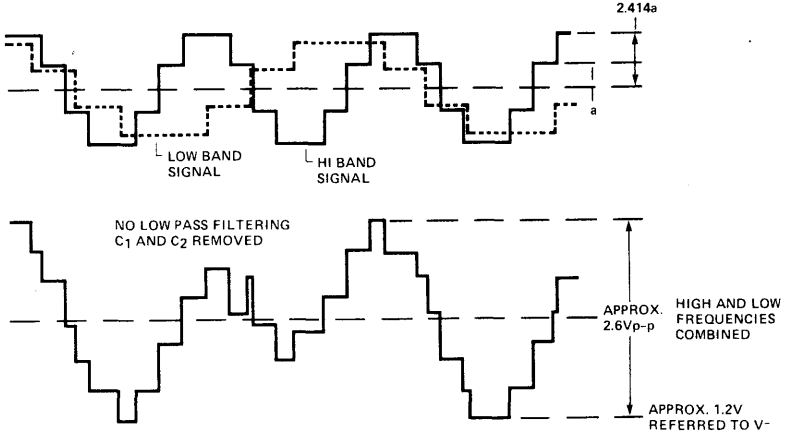


FIGURE 2

Figure 2 shows individual currents of a low band and high band frequency pair into the summing node A (see Figure 3) and the resultant voltage waveform.

DESIRED FREQUENCY Hz	ACTUAL FREQUENCY Hz	FREQUENCY DEVIATION %	DIVIDE BY N RATIO
697	699.13	+0.30	80
770	766.17	-0.50	73
852	847.43	-0.54	66
941	947.97	+0.74	59
1209	1215.88	+0.57	46
1336	1331.68	-0.32	42
1477	1471.85	-0.35	38
1633	1645.01	+0.74	34

APPLICATION NOTES

1. Device Description

The ICM7206 family is manufactured with a standard metal gate C-MOS technology having proven reliability and excellent reproducability resulting in extremely high yields. The techniques used in the design have been developed over many years and are characterized by wide operating supply voltage ranges and low power dissipation.

To minimize chip size, all diffusions used to define source-drain regions and field regions are butted up together. This results in approximately 6.3 volt zener breakdown between the supply terminals, and between all components on chip. As a consequence, the usual C-MOS static charge problems and handling problems are not experienced with the ICM7206.

The oscillator consists of a medium size C-MOS inverter having on chip a feedback resistor and two capacitors of 14pF each, one at the oscillator input and the other at the oscillator output. The oscillator is followed by a dynamic $\div 2^3$ circuit which divides the oscillator frequency to 447,443Hz. This is applied to two programmable dividers each capable of division ratios of any integer between 1 and 128, and each counter is controlled by a ROM. The outputs from the programmable counters drive sequencers (divide by 8) which generate the eight time slots necessary to synthesize the 4-level sine waves.

The control logic block recognizes signals on the row and column inputs that are only a small fraction of the supply voltage, thereby permitting the use of a simple matrix single contact per key keyboard, rather than the more usual two contacts per key type having a common line. The row and column pullup resistors are equal in value and connected to the opposite supply terminals (ICM7206/C only; for the ICM7206A all pullup resistors are connected to the V^- terminal and for the ICM7206B they are tied to the V^+. Therefore, connecting a row input to a column input generates a voltage on those inputs which is one half of the supply voltage.

The ICM7206 family employs a unique but extremely simple digital to analog (D to A) converter. This D to A converter produces a 4 level synthesized sine wave having an intrinsic total harmonic distortion level of approximately 20%. Figure 3 shows a single channel D to A converter. The current sources Q_2 and Q_3 are proportioned in the ratio of 1:1.414. During time slots 1 and 8 both S_1 and S_2 are off, during time slots 2 and 7 only S_1 is on, during time slots 3 and 6 only S_2 is on, and during time slots 4 and 5 both S_1 and S_2 are on. The resultant currents are summed at node A, buffered by Q_4 and further buffered by R_3, R_4 and Q_5. Switch S_3 allows the output to go into a high impedance mode under quiescent conditions.

Node A is the common summing point for both the high and low band frequencies although this is not shown in Figure 3.

The synthesized sine wave has negligible even harmonic distortion and very low values of third and fifth harmonic distortion thereby minimizing the filtering problems necessary to reduce the total harmonic distortion to well below the 10% level required for touch tone telephone encoding. Figure 4 shows the low pass filter characteristic of the output buffer for $C_1 = 0.0022\mu F$ and $C_2 = 0.022\mu F$. A small peak of 0.4dB occurs at 1100Hz with sharp attention (12dB per octave) above 2500Hz. This type of active filter produces a sharper and more desirable knee characteristic than would two simple cascaded RC networks.

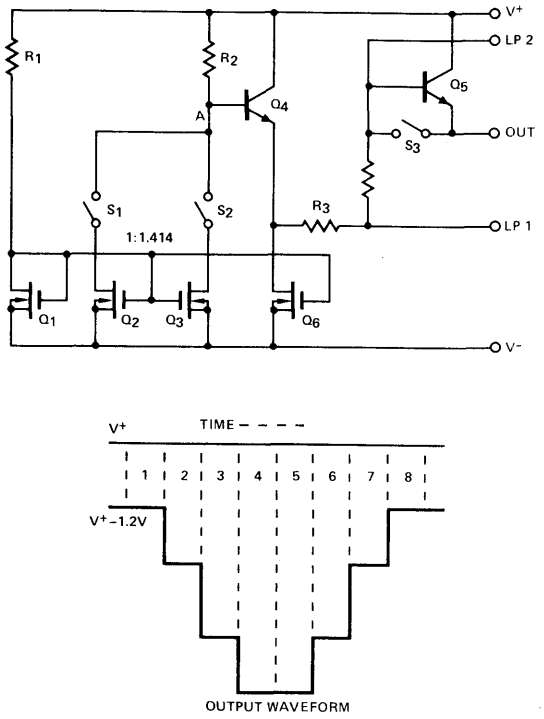


FIGURE 3: D to A Converter and Output Buffer

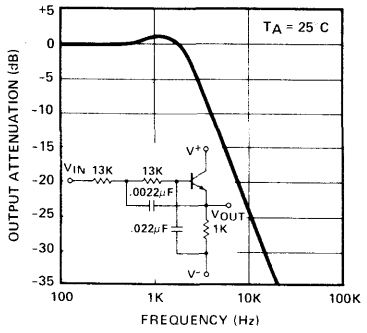


FIGURE 4: Frequency Attentuation Characteristics of the Output Buffer

2. Latchup Considerations

Most junction isolated C-MOS integrated circuits, especially those of moderate or high complexity, exhibit latchup phenomena whereby they can be triggered into an uncontrollable low impedance mode between the supply terminals. This can be due to gross forward biasing of inputs or outputs (with respect to the supply terminals), high voltage supply transients, or more rarely by exceptional fast rate of rise of supply voltages.

The ICM7206 family is no exception, and precautions must be taken to limit the supply current to those values shown in the ABSOLUTE MAXIMUM RATINGS. For an example, do not use a 6 volt very low impedance supply source in an **electrically extremely noisy** environment unless a 500 ohm current limiting resistor is included in series with the V^- terminal. For normal telephone encoding applications no problems are envisioned, even with low impedance transients of 100 volts or more, if circuitry similar to that shown in the next section is used.

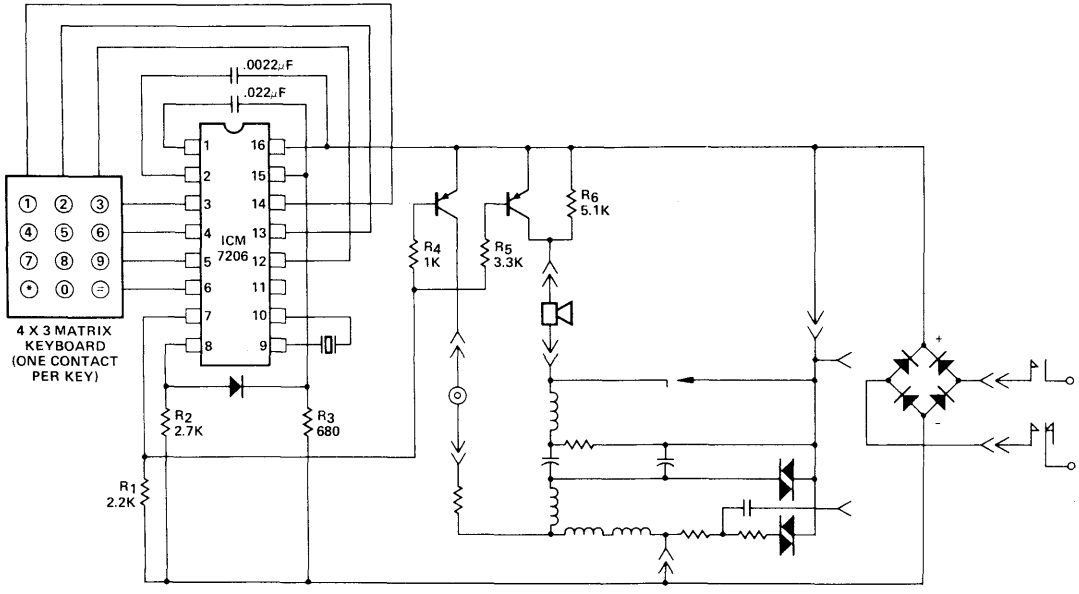
3. Typical Application (Telephone Handset)

A typical encoder for telephone handsets is shown in Figure 5. This encoder uses a single contact per key keyboard and provides all other switching functions electronically. The diode connected between terminals 8 and 15 prevents the output going more than 1 volt negative with respect to the negative supply V^- and the circuit operates over the supply voltage range from 3.5 volts to 15 volts on the device side of the bridge rectifier. Transients as high as 100 volts will not cause system failure, although the encoder will not operate correctly under these conditions. Correct operation will resume immediately after the transient is removed.

The output voltage of the synthesized sine wave is almost directly proportional to the supply voltage (V^+–V^-) and will increase with increase of supply voltage until zener breakdown occurs (approximately 6.3 volts between terminals 8 and 16) after which the output voltage remains constant.

4. Portable Tone Generator

The ICM7206A/B require a two contact key keyboard with the common line connected to the positive supply (neg for ICM7206B) (terminal 16). A simple diode matrix may be used with this keyboard to provide power to the system whenever a key is depressed, thus avoiding the need for an on/off switch. In Figure 6 the tone generator is shown using a 9 volt battery. However, if instead, a 6 volt battery is used, the diode D_4 is not required. It is recommended that a 470 ohm resistor still be included in series with a negative (positive) supply to prevent accidental triggering of latchup.



NOTE: If dual contact keyboard is used, common should be left floating.

FIGURE 5: Telephone Handset Touch Tone Encoder

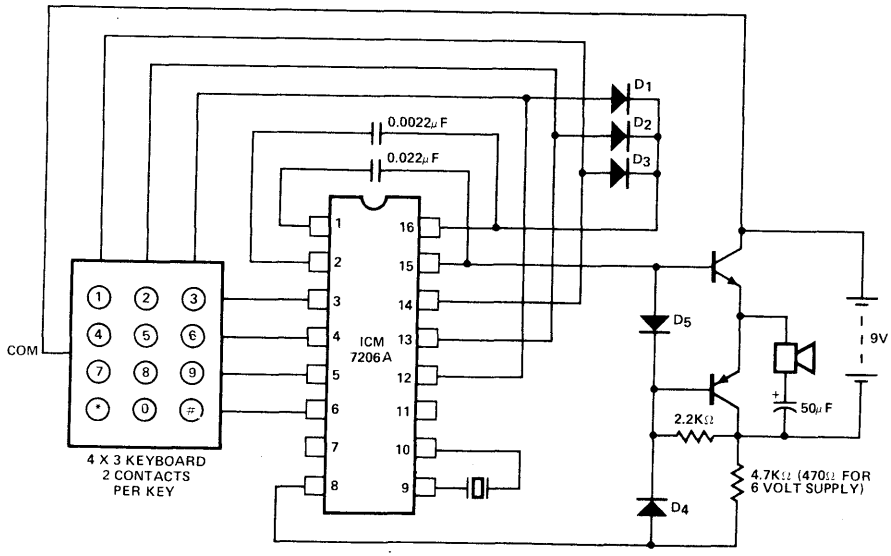


FIGURE 6: Portable Tone Generator

OPTIONS

(For additional information consult the factory)

Options can be achieved using metal mask additions to provide the following.

1) The sequence or position of either the row or column terminals can be interchanged i.e., row 1 terminal 3 could become terminal 11, etc.

2) Any frequency oscillator from approximately 0.5MHz to 7MHz can be chosen. Note that the accuracy of the output frequencies will depend on the exact oscillator frequency. For instance, a 1 MHz crystal could be used with worst case output frequency error of 0.8%. Or, if high accuracy is required, ±0.25%, oscillator frequencies of 5,117,376Hz or 2,558,688Hz could be selected. ROM's are used to program the dividers.

3) The 'DISABLE' output may be changed to an inverter or an uncommitted drain n-channel transistor.

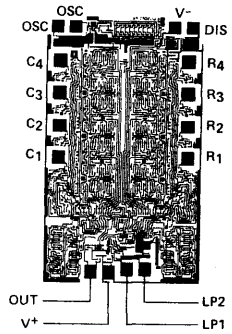
4) The oscillator may be disabled until a key is depressed.

7

CHIP TOPOGRAPHY

Chip Dimensions
0.60" (1.524mm)x0.101"
(2.565mm)

Chip may be die attached using conventional eutictic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.



ICM7209
CMOS Clock Generator

FEATURES

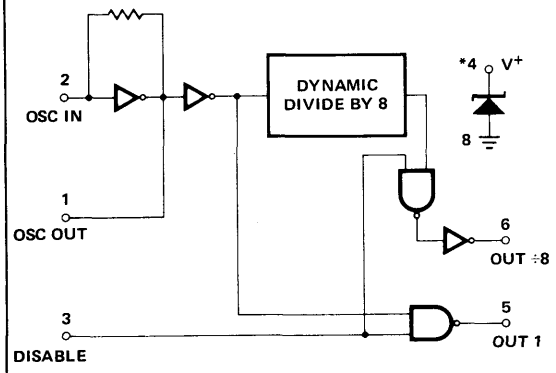
- **High frequency operation — 10MHz guaranteed**
- **Easy to use oscillator — requires only a quartz crystal and two capacitors**
- **Bipolar, MOS and CMOS compatibility**
- **High output drive capability — 5 x TTL fanout with 10ns rise and fall times**
- **Low power — 50mW at 10MHz**
- **Choice of two output frequencies — osc., and osc. ÷8 frequencies**
- **Disable control for both outputs**
- **Wide industrial temperature range — −20°C to +85°C**
- **All inputs fully protected — circuits may be handled without any special precautions**

GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

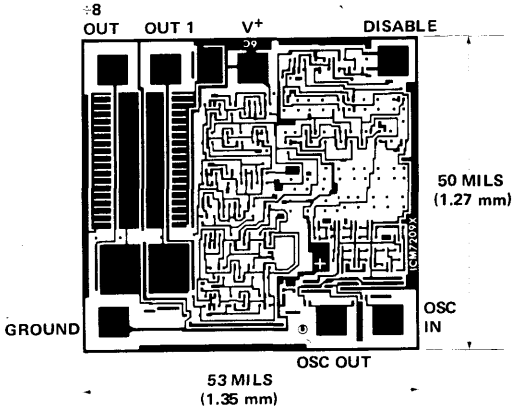
The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

SCHEMATIC DIAGRAM

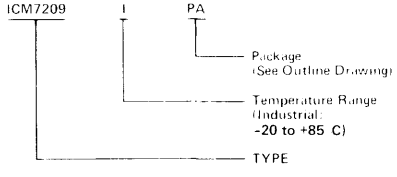


*ZENER VOLTAGE IS TYPICALLY 6.3 VOLTS

CHIP TOPOGRAPHY



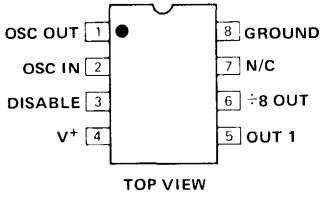
ORDERING INFORMATION



Order Devices by Following Part Number ICM7209 I PA

Order Dice by Following Part Number ICM7209/D

PIN CONFIGURATION (OUTLINE DRAWING PA)



TOP VIEW

Pin 1 is designated by either a dot or a notch.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (25°C) 300mW
Supply Voltage ..... 6 V
Output Voltages ..... Equal to or less than supply
Input Voltages ..... Equal to or less than supply
Storage Temp. ..... -55°C to +125°C
Operating Temp. Range ..... -20°C to +85°C
Lead Temp. (Soldering, 10 seconds) ..... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5V \pm 10\%$, test circuit, f_{osc} = 10MHz, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply Current	I^+	Note 1 No Load		11	20	mA
Disable Input Capacitance *	C_D				5	pF
Disable Input Leakage	I_{ILK}	Either '1' or '0' state			±10	μA
Output Low State	V_{OL}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads			0.4	V
Output High State	V_{OH}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	4.0	4.9		V
Output Rise Time (Note 3)	t_r	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	ns
Output Fall Time (Note 3)	t_f	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	ns
Minimum OSC Frequency for ÷8 Output	f_{osc}	Note 2	2			MHz
Output ÷8 duty cycle		Any operating frequency Low state : High state		7:9		MHz
Oscillator Transconductance	gm		80	200		μmho

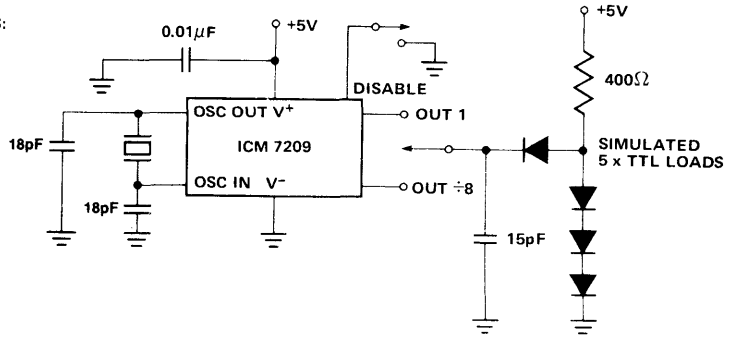
NOTE 1: The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.

NOTE 2: The ÷8 circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.

NOTE 3: Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

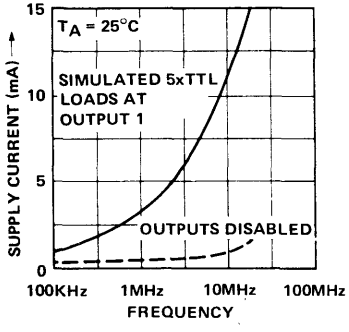
TEST CIRCUIT

CRYSTAL PARAMETERS:
C_M = 5mpF
R_S = 15 ohms
C_O = 3pF
C_L = 10pF
f = 10 MHz

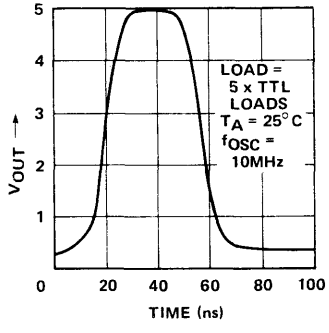


TYPICAL OPERATING CHARACTERISTICS

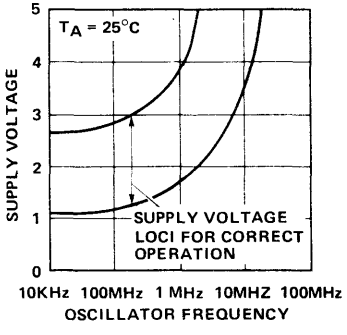
SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



TYPICAL OUT 1 RISE AND FALL TIMES



SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF ÷8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY



Rise and fall times of OUT ÷8 are similar to those of OUT 1.

7

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a C-MOS inverter with a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10KHz) to 10MHz.

The oscillator circuit consumes about 500μA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

THE ÷8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to store voltage levels instead of latches (which are used in static dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see graph under TYPICAL OPERATING CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consist of C-MOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other C-MOS gates operating with a 5 volt supply, or TTL compatible MOS gates.

The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

COMMENTS ON THE DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be dramatically reduced.

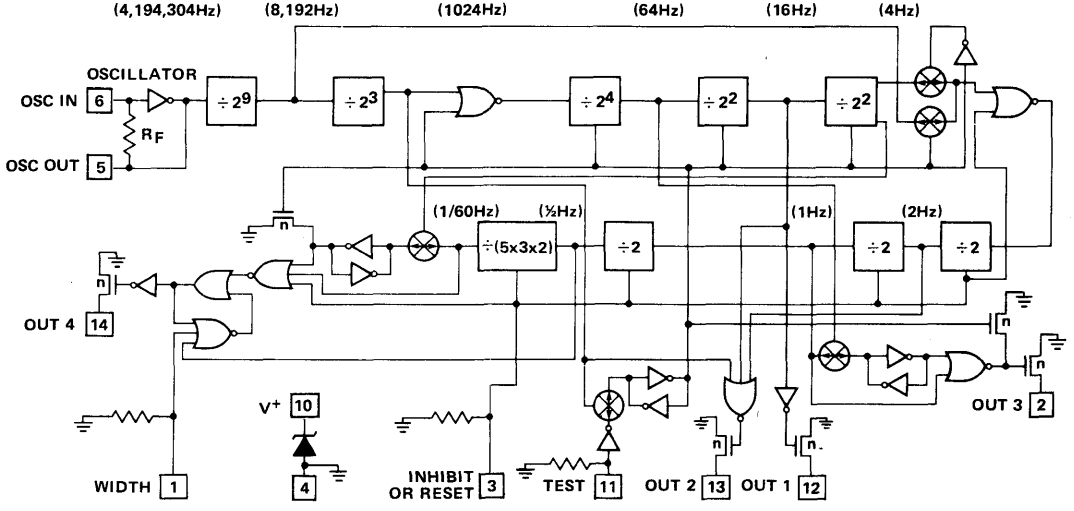
ICM7213
One Second/One Minute Precision Clock and Reference Generator

FEATURES
- **Guaranteed 2 volts operation**
- **Very low current consumption: Typ. 100μA @ 3V**
- **All outputs TTL compatible**
- **On chip oscillator feedback resistor**
- **Oscillator requires only 3 external components: fixed capacitor, trim capacitor, and a quartz crystal**
- **Output inhibit function**
- **4 simultaneous outputs: one pulse/sec, one pulse/min, 16Hz and composite 1024 + 16 + 2Hz outputs**
- **Test speed-up provides other frequency outputs**
- **Input static protection — no special handling required**

GENERAL DESCRIPTION
The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304 MHz crystal will produce a variety of output frequencies including 2048 Hz, 1024 Hz, 34.133 Hz, 16 Hz, 1 Hz, and 1/60 Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate C-MOS technology which uses 6.4 volt zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (see Figure 2).

BLOCK DIAGRAM



ORDERING INFORMATION

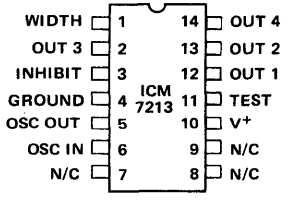
ICM7213 I PD

- PD — Package: PD = 14 Pin Plastic
- I — Temperature Range: -20°C to +85°C
- ICM7213 — Type

Order Devices by Following Part Number
ICM7213IPD

Order Dice by Following Part Number
ICM7213D

PIN CONFIGURATION (OUTLINE DRAWING PD)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.0V
Output Current (Any output) 20mA
All Input and Oscillator Voltages (Note 1) ..... Equal to but not greater than the supply voltage
All Output Voltages (Note 1) ..... $0 \leq V_O \leq +6$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -40°C to +125°C
Power Dissipation (Note 2) 200mW
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: The ICM7213 like most C-MOS devices, may enter a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting.

NOTE 2: Derate linearly power rating of 200mW at 25°C to 50mW at 70°C.

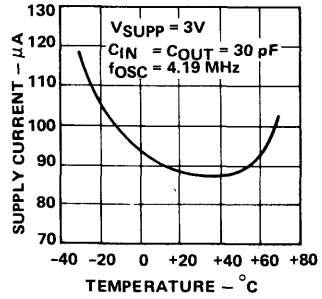
OPERATING CHARACTERISTICS

TEST CONDITIONS: $V+ = 3.0V$, $f_{osc} = 4.194304$ MHz, Test Circuit, $T_A = 25°C$ unless otherwise specified

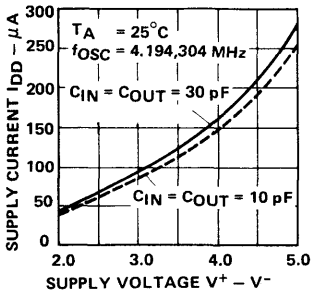
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+			100	140	μA
Guaranteed Operating Supply Voltage Range	V_{OP}	-20°C < T_A < 85°C	2		4	V
Output Leakage Current	I_{OLK}	Any output, V_{OUT} = 6 Volts			10	μA
Output Sat. Resistance	R_{OUT}	Any output, I_{OLK} = 2.5mA		120	200	Ω
Inhibit Input Current	I_I	Inhibit terminal connected to V^+		10	40	μA
Test Point Input Current	I_{TP}	Test point terminal connected to V^+		10	40	
Width Input Current	I_W	Width terminal connected to V^+		10	40	
Oscillator g_m	g_m	V^+ = 2V	100			umho
Oscillator Frequency Range (Note 3)	f_{osc}		1		10	MHz
Oscillator Stability	f_{STAB}	2V < V^+ < 4V		1.0		ppm
Oscillator Start Time	t_s	V^+ = 3.0 volts		0.1		sec
		V^+ = 2.0 volts		0.2		

NOTE 3: The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible. See application notes.

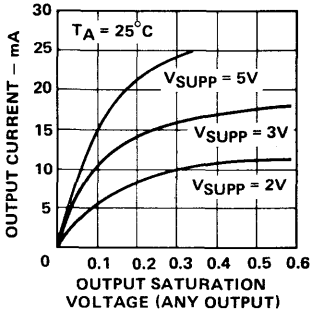
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



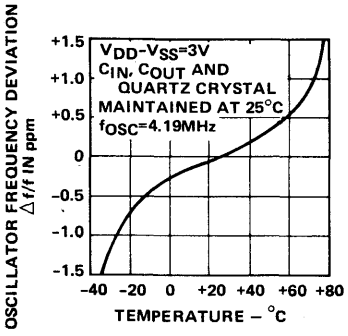
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



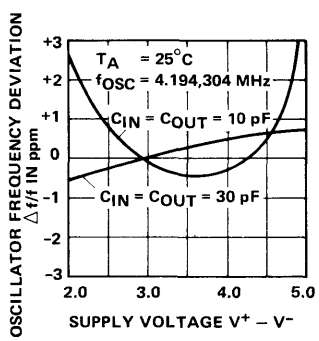
OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



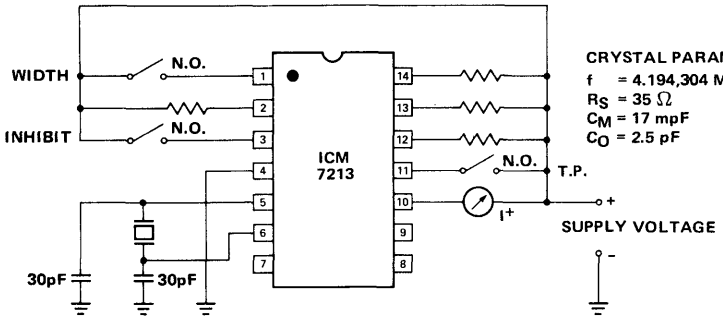
OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



7 TEST CIRCUIT



OUTPUT DEFINITIONS

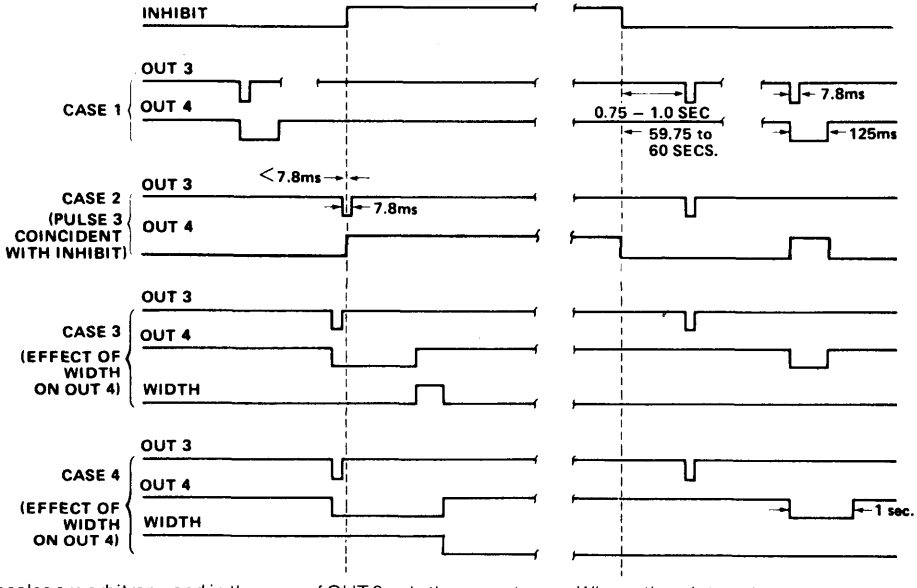
TABLE I.

INPUT STATES*			PIN 12	PIN 13	PIN 2	PIN 14
TEST	INHIBIT	WIDTH	OUT 1	OUT 2	OUT 3	OUT 4
L	L	L	16Hz ÷2^{18}	$\overline{1024 + 16 + 2}$Hz (÷2^{12}÷2^{18}÷2^{21}) composite	1Hz, 7.8mS ÷2^{22}	1/60Hz, 1 Sec. ÷ (2^{24} x 3 x 5)
L	L	H	16Hz ÷2^{18}	$\overline{1024 + 16 + 2}$Hz (÷2^{12}÷2^{18}÷2^{21}) composite	1Hz, 7.8mS ÷ 2^{22}	1/60Hz, 125ms
L	H	L	16Hz ÷2^{18}	$\overline{1024 + 16}$Hz (÷2^{12}÷2^{18}) composite	OFF	OFF
L	H	H	16Hz ÷2^{18}	$\overline{1024 + 16}$Hz (÷2^{12}÷2^{18}) composite	OFF	SEE WAVEFORMS
H	L	L	ON	$\overline{4096 + 1024}$Hz (÷2^{10}÷2^{12}) composite	2048Hz ÷2^{11}	34.133Hz, 50% D.C. ÷(213 x 5 x 3)
H	L	H	ON	$\overline{4096 + 1024}$Hz (÷2^{10}÷2^{12}) composite	2048Hz ÷2^{11}	34.133Hz, 50% D.C. ÷(213 x 5 x 3)
H	H	L	ON	1024Hz ÷2^{12}	ON	OFF
H	H	H	ON	1024Hz ÷2^{12}	ON	OFF

NOTE: When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

OUTPUT WAVEFORMS

EFFECT OF INHIBIT INPUT TEST connected to ground or left open.



All time scales are arbitrary, and in the case of OUT 3 only the pulses coinciding with the negative edge of OUT 4 are shown. Where time intervals are relevant they are clearly shown.

APPLICATIONS

1. Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to 1/60Hz using a 4,194,304Hz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.

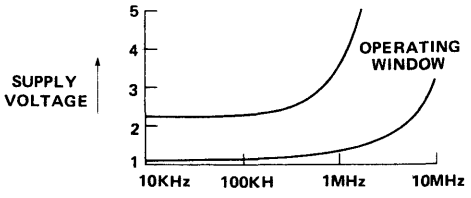
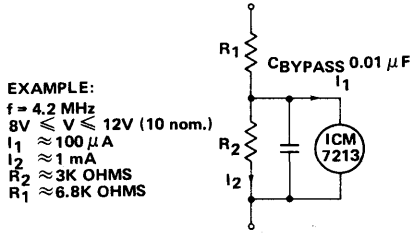


FIGURE 1: Window of Correct Operation

The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.



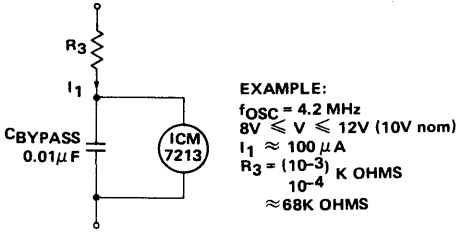


FIGURE 2: Biasing Schemes with High Voltage Supplies

2. Logic Family Compatability

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

3. Oscillator Considerations

The oscillator consists of a C-MOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 30pF and the oscillator tuning capacitor should range between approximately 16 and 60pF.

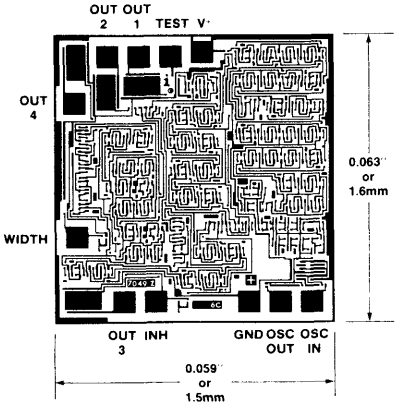
Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

4. Control Inputs

The TEST input inhibits the 2^{18} output and applies the 2^9 output to the 2^{21} divider, thereby permitting a speedup of the testing of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1 sec, or to change the state of OUT 4 from ON to OFF during INHIBIT.

CHIP TOPOGRAPHY



ICM7215
6-Digit 4-Function LED Stopwatch Circuit

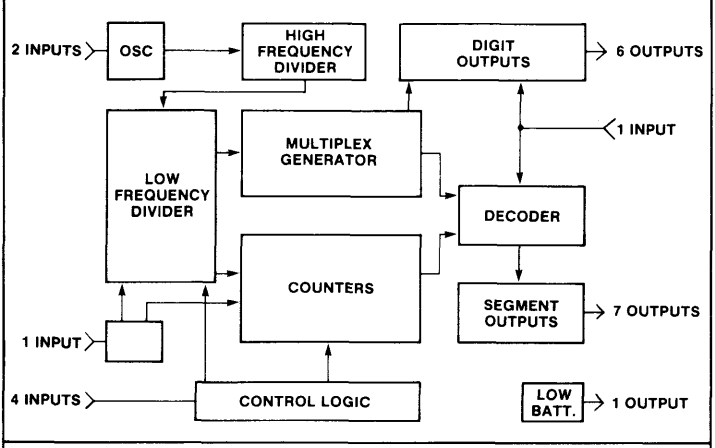
FEATURES

- **Four functions: start/stop/reset, split, taylor, time out**
- **Six digit display: ranges up to 59 minutes 59.99 seconds**
- **High LED drive current: 13mA peak per segment at 16.7% duty cycle with 4.0 volt supply**
- **Requires only three low cost SPST switches without loss of accuracy: start/stop, reset, display unlock**
- **Chip enable pin turns off both segment and digit outputs; can be used for multiple circuits driving one display**
- **Low battery indicator**
- **Digit blanking on seconds and minutes**
- **Wide operating range: 2.0 to 5.0 volts**
- **1KHz multiplex rate prevents flickering display**
- **Can be used easily in four different single function stopwatches or two two-function stopwatches: start/stop/reset with time-out, split with taylor. The component count for a three- or four-function stopwatch will be slightly greater.**
- **Retrofit to ICM7205 for split and/or taylor applications**

GENERAL DESCRIPTION

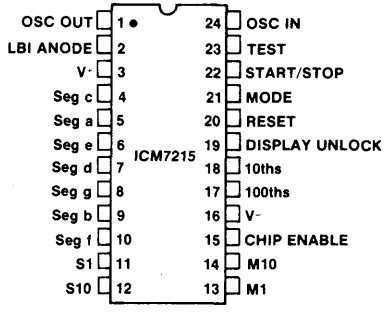
The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED. The only components required for a complete stopwatch are the display, three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an on-off switch. For a two function stopwatch, or to add a display off feature, one additional slide switch is required. The circuit divides the oscillator frequency by 2^{15} to obtain 100Hz, which is fed to the fractional seconds, seconds and minutes counters, while an intermediate frequency is used to obtain the 1/6 duty cycle 1.07KHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP.

BLOCK DIAGRAM



PIN CONFIGURATION

(OUTLINE DRAWING PG)



ORDERING INFORMATION

Order devices by following part number ICM7215 I PG
Order dice by following part number ICM7215/D

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 5.5 V
Power Dissipation (Note 1) ..... 0.75 W
Operating Temperature ..... −20°C to +70°C
Storage Temperature ..... −55°C to +125°C
Input and Output Voltage ..... equal to but never exceeding the supply voltage

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS:

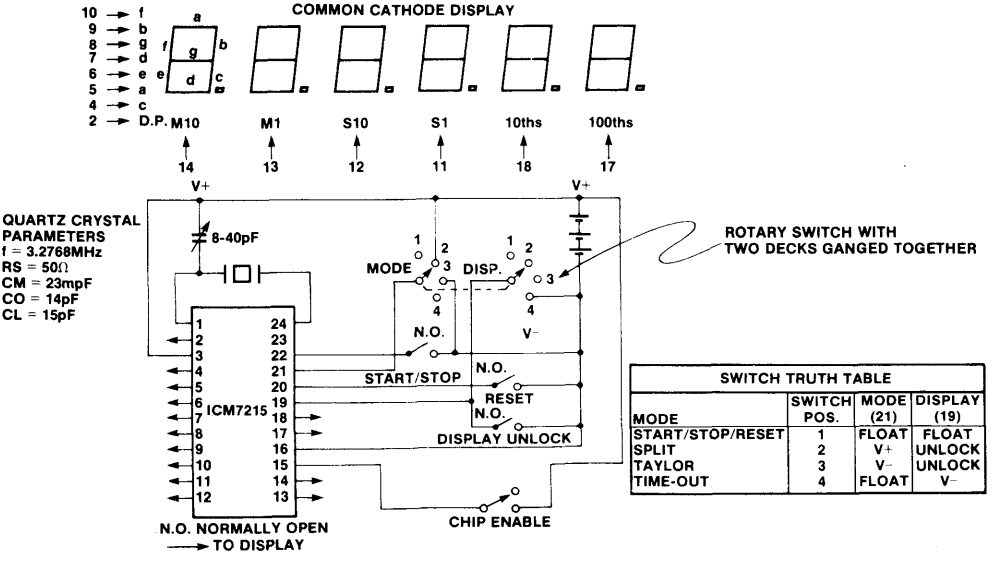
TEST CONDITIONS: $T_A = +25°C$, stopwatch circuit, $V^+ = 4.0V$ unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V^+	$-20°C \le T_A \le +70°C$	2.0		5.0	V
Supply Current	I^+	Display off		0.6	1.5	mA
Segment Current	I_{SEG}	5 segments lit				mA
Peak		1.8 Volts across display	9.0	13.2		mA
Average				2.2		mA
Switch Actuation Current	I_{SW}	All inputs except chip enable		20	50	µA
Switch Actuation Current		Chip enable		50	200	µA
Digit Leakage Current	I_{DLK}	$V_{DIG} = 2.0V$			50	µA
Segment Leakage Current	I_{SLK}	$V_{SEG} = 2.0V$			100	µA
Low Battery Indicator Trigger Voltage	V_{LBI}		2.2		2.8	V
LBI Output Current	I_{LBI}	$V^+ = 2.0V$, $V_{LBI} = 1.6V$		2.0		mA
Oscillator Stability	f_{STAB}	$V^+ = 2.0V$ to $V^+ = 5.0V$		6		PPM
Oscillator Transconductance	g_m	$V^+ = 2.0V$	120			µmho
Oscillator Input Capacitance	C_{OSCI}		24	30	36	pF

NOTE 1: The output devices on the ICM7215 have very low impedance characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA. This will not damage the device momentarily, but if the short circuit condition is not removed immediately probable device failure will occur.

7

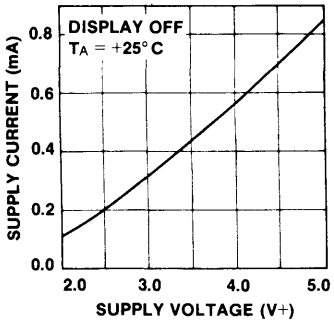
STOPWATCH CIRCUIT



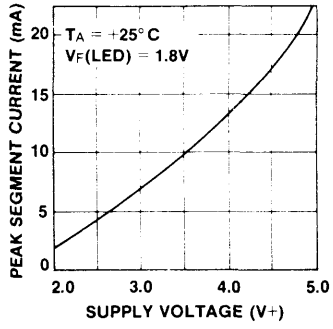
SWITCH TRUTH TABLE			
MODE	SWITCH POS.	MODE (21)	DISPLAY (19)
START/STOP/RESET	1	FLOAT	FLOAT
SPLIT	2	V+	UNLOCK
TAYLOR	3	V−	UNLOCK
TIME-OUT	4	FLOAT	V−

TYPICAL PERFORMANCE CHARACTERISTICS

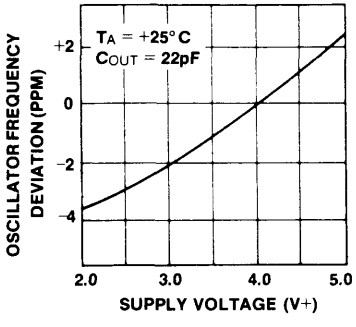
SUPPLY CURRENT VS VOLTAGE



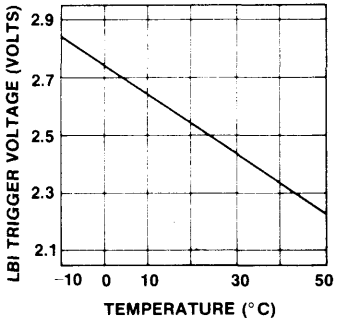
SEGMENT CURRENT VS SUPPLY VOLTAGE



OSC. STABILITY VS SUPPLY VOLTAGE



LOW BATTERY INDICATOR (LBI) TRIGGER VOLTAGE VS TEMPERATURE



7

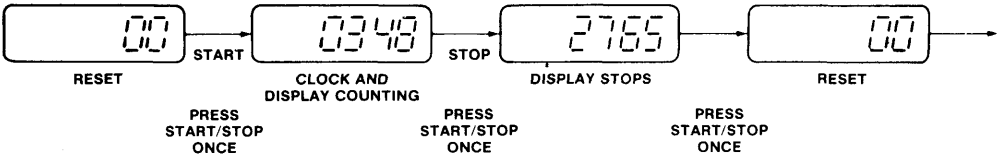
FUNCTIONAL OPERATION

Turning on the stopwatch will bring up the reset state with the fractional seconds displaying 00 and the other digits blanked. This display always indicates that the stopwatch is ready to go.

The display can be turned off in any mode by connecting the chip enable input to V+.

START/STOP/RESET MODE

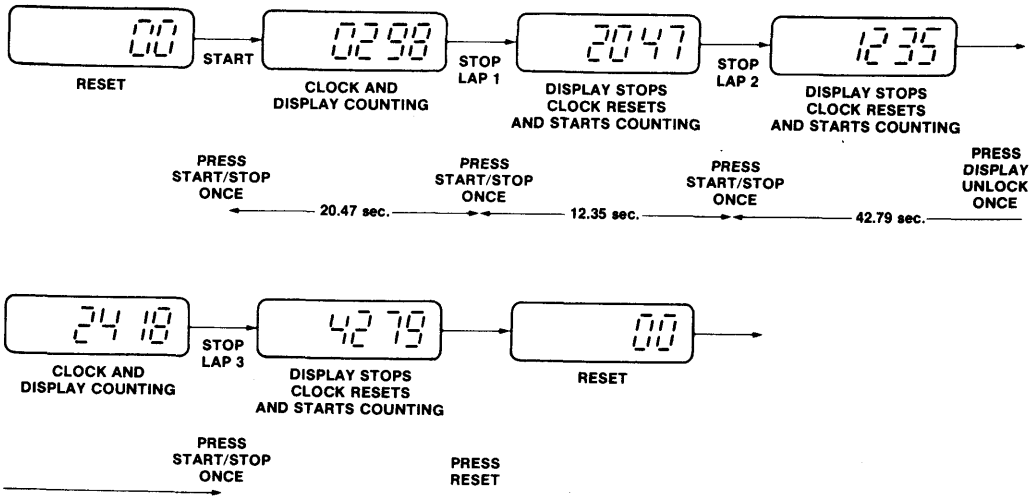
When the mode input is floating and the display input is floating or connected to V+ the circuit is in the start/stop/reset mode.



The start/stop/reset mode can be used for single event timing in a one-button stopwatch; an additional switch can be used to provide an instant reset. To time another event, the display must be reset before the start of the event. Seconds will be displayed after one second, minutes after one minute. The range of the stopwatch is 59 minutes 59.99 seconds, and if an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.

TAYLOR OR SEQUENTIAL MODE

When the mode input is connected to V−, the stopwatch is in the taylor or sequential mode.

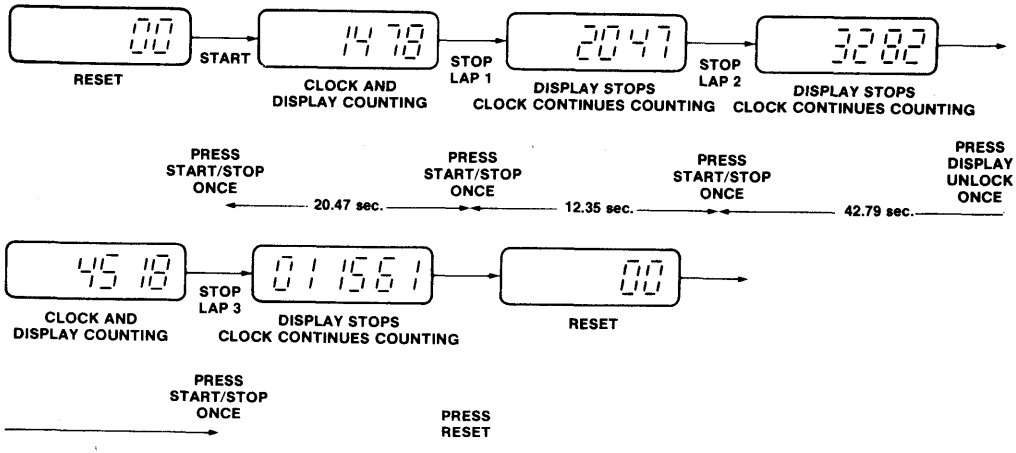


Each split time is measured from zero in the taylor mode; i.e., after stopping the watch, the counters reset momentarily and start counting the next interval. The time displayed is that elapsed since the last activation of start/stop. The display is stationary after the first interval unless the display unlock is used to show the running clock. Reset can be used at any time.

7

SPLIT MODE

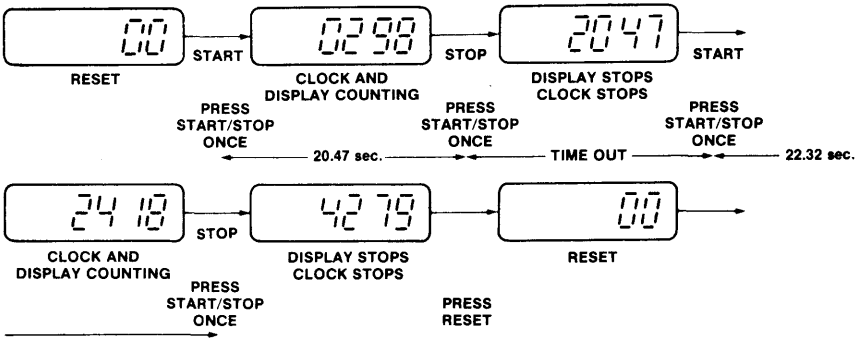
When the mode input is connected to V+ the stopwatch is in the split mode.



The split mode differs from the taylor in that the lap times are cumulative in the split mode. The counters do not reset or stop after the first start until reset is activated. Time displayed is the cumulative time elapsed since the first start after reset. Display unlock can be used to let the display 'catch up' with the clock, and reset can be used at any time.

TIME OUT MODE

When the mode input is floating and the display input is tied to V⁻, the stopwatch is in the time-out mode.



In the time-out mode the clock and display alternately start and stop with activations of the start/stop switch. Reset can be used at any time. The display unlock button is bypassed in this mode.

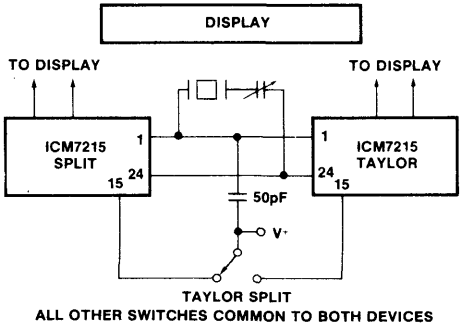
APPLICATION NOTES

LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers, and designed to provide a trigger voltage of approximately 2.5 volts at room temperature. Normal AA type batteries will provide many hours of accurate timekeeping after the indicator comes on, however the wide voltage spread between the LBI voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

CHIP ENABLE

The chip enable input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the chip enable input is floating or connected to V⁻, the display is enabled, and when the tied to V⁺ the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the taylor mode. The circuit below indicates how the user can obtain lap and cumulative readings of the same event.



SWITCH CHARACTERISTICS

The ICM7215 is designed for use with SPST switches throughout. On the display unlock and reset inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any length of time however short. Switch bounce on these inputs does not need to be specified. The start/stop input, however, responds to an edge and so requires a switch with less than 15ms of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.

LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to the 7215. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

OSCILLATOR DESIGN

The oscillator of the ICM7215 includes all components on chip except the 3.2768 MHz crystal and the trimming capacitor. The oscillator input capacitance has a nominal value of 30pF, and the circuit is designed to work with a crystal with a load capacitance of approximately 15pF. If the crystal has characteristics as shown on page 3, an 8-40pF trimming capacitor will be adequate for a tuning tolerance of ±30PPM on the crystal. If the crystal's static capacitance is significantly lower, a narrower trimming range may be selected.

After deciding on a crystal and a nominal load capacitance, take the worst case values of C_{in}, C_{out} and R_S and calculate the g_m required by:

$$g_m = \omega^2 C_{in} C_{out} R_S \left\{1 + \frac{C_o (C_{in} + C_{out})}{C_{in} C_{out}}\right\}^2$$

C_o = static capacitance
R_S = series resistance
C_{in} = input capacitance
C_{out} = output capacitance
ω = 2π x crystal frequency

The resulting g_m should be less than half the g_m specified for the device. If it is not, a lower value of crystal series resistance and/or load capacitance should be specified.

OSCILLATOR TUNING

Tuning can be accomplished by using the 10th or 100th seconds with the device reset. The frequency on the cathode should be tuned to 1066.667 Hz, which is equivalent to a period of 937.5 microseconds. Note that a frequency counter cannot be connected directly to the oscillator because of possible loading.

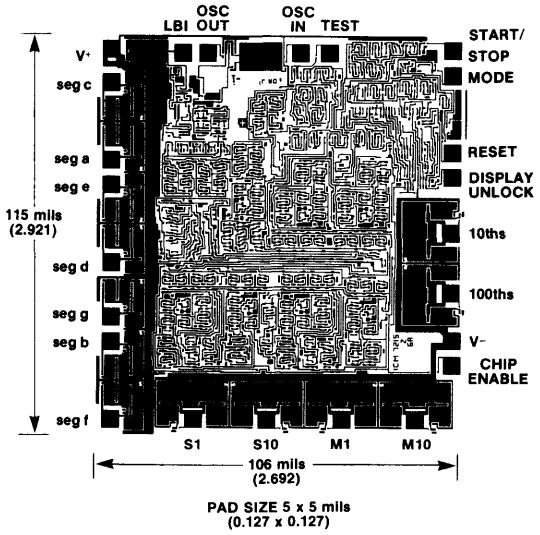
TEST POINT

The test point input is used for high speed testing of the device. When the input is pulsed low, a latch is set which speeds up counting by a factor of 32; each pulse on the test point rapidly advances both minutes and seconds in a parallel mode. To accurately rapid advance the signal applied to the test point must be free of switch bounce. The circuit is taken out of the test mode by using either reset or start/stop.

REPLACING THE ICM7205 WITH THE ICM7215

The ICM7215 is designed to be compatible with circuits using the ICM7205. If the 7205 is used only in the split mode no changes are required. If the 7205 is used in the taylor mode and the split taylor input (pin 21) is left open, a jumper from pin 21 to V- must be added when converting to the 7215. A jumper may also be needed if the 7205 is used with a split/taylor switch. Once the jumper has been added the board can be used with either device.

CHIP TOPOGRAPHY



ICM7223
4-Digit LCD Clock Circuit with Snooze Alarm

FEATURES

- **3-1/2 or 4 digit display with AM/PM and alarm flags**
- **12/24 hour user selectable formats**
- **Direct alarm drive @ 3V p-p, with complex (cricket) alarm tone**
- **8 minute snooze (Dice programmable from 2 to 14 minutes in two minute increments)**
- **Single battery operation (1.5V)**
- **Low current — 6 μA maximum**
- **On-chip fixed oscillator input capacitor**
- **32 kHz oscillator requires only quartz crystal and trimming capacitor**
- **Voltage tripler for large displays**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7223IPL	-20°C to +70°C	40 Pin Plastic DIP
ICM7223D/D	-20°C to +70°C	DICE

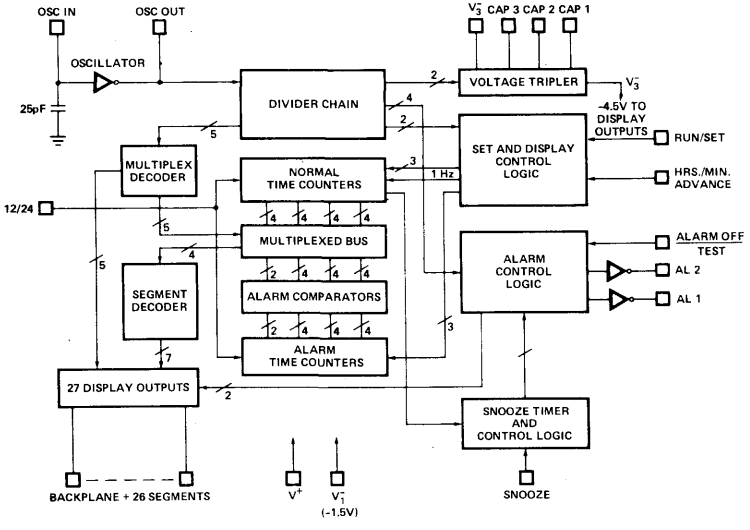
GENERAL DESCRIPTION

The ICM7223 is a fully integrated 4-digit LCD clock circuit with 24 hour alarm and 8 minute snooze timer. For high accuracy and low power consumption a 32.768 KHz quartz watch crystal is used as the time base, and the number of external components has been reduced to a minimum.

The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered, thereby permitting synchronization of the clock to the nearest second. Seconds are not displayed.

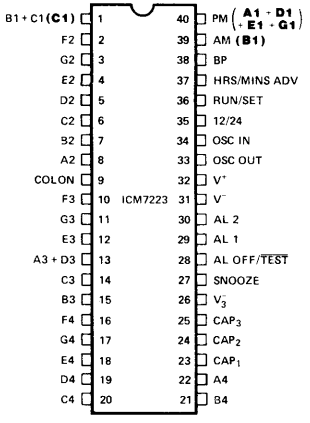
The ICM7223 is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life.

BLOCK DIAGRAM



PIN CONFIGURATION

(OUTLINE DRAWING PL)



PARENTHESES AND **BOLD TYPE** INDICATE 24 HOUR OPERATION

7

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -10°C to +60°C
Power Dissipation[1] ..... 100 mW
Supply Voltage[2]
$V^+ - V_1^-$ 2.0V
$V^+ - V_3^-$ 5.5V
Input Voltage (Osc. In, Test, Set, Display) ..... $V^- \leq V_{IN} \leq V^+$
Output Voltage (Osc. Out, 512) ..... $V_1^- \leq V_{OUT} \leq V^+$
(All Other Pins) ..... $V_3^- \leq V_{OUT} \leq V^+$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

OPERATING CHARACTERISTICS

TEST CONDITIONS: V^+-V^- = 1.55V, voltage tripler connected, T_A = 25°C, Test Circuit, unless otherwise specified, voltages and currents are shown as absolute values.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V^+	V^- = 0V -10°C < T_A < 60°C	1.2		1.8	Volts
Supply Current	I^+	Display Disconnected		4	6	μA
Tripler Output Voltage	V_3^-	I_3 = 0.0 μA	4.2			V
		I_3 = 1.0 μA	4.1			
Segment Drive Current	I_{SEG}	V_{SAT} = 0.2V (Both Directions)	5			μA
Backplane Drive Current	I_{BP}	V_{SAT} = 0.1V (Both Directions)	20			μA
Switch Actuation Current	I_{SW}	V_{SW} = V^+ or V_{SW} = V_3^-		3	5	μA
Alarm Saturation Resistance	$R_{AL(ON)}$	P-CH at 1 mA P-CH		350	500	Ω
		N-CH at 0.5 mA N-CH		1500	1800	
Oscillator Stability	f_{STAB}	V^- = 0V, 1.20V ≤ V^+ ≤ 1.55V, C_{OUT} = 25 pF		2		PPM
Oscillator Input Current[3]	I_{OSCI}	'OSC IN' Connected to V^+ 'OSC OUT' Open Circuit		0.2		μA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		μmho

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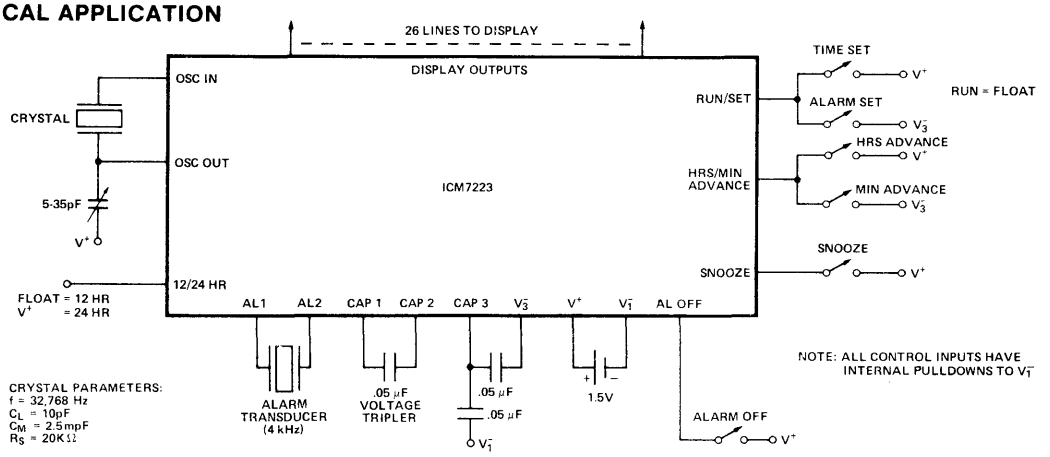
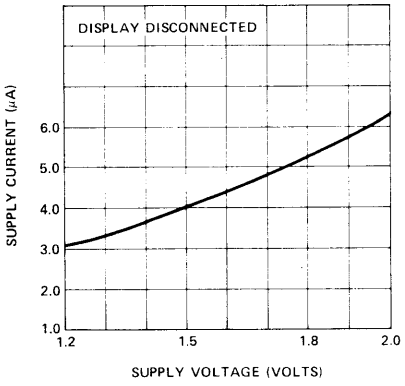
Notes:
1. The ICM7223 is fully short circuit protected on all inputs and outputs. However, if by forward biasing an input or output the device is put into a latchup condition, power dissipation must be limited to 100 mW to prevent destruction of the device.
2. The ICM7223 is intended for use with two power supplies, one of which is derived from an external battery V_1^- and the other is generated internally by the voltage multiplier (V_3^-). The common point of the two supplies is the most positive, V^+. If desired the circuit can be supplied with an external V_3^- by disconnecting the multiplier capacitors, or V_3^- and V_1^- can be tied together (for a 1.5 volt display for instance).
3. The integrated oscillator biasing components have a nonlinear characteristic depending on the instantaneous values of the input and output voltages of the oscillator and the supply. Under oscillator startup conditions this component has a maximum value.

TYPICAL APPLICATION

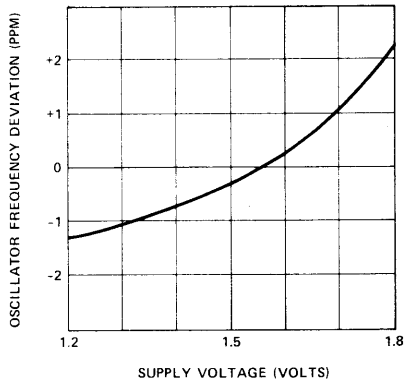


TYPICAL PERFORMANCE CHARACTERISTICS

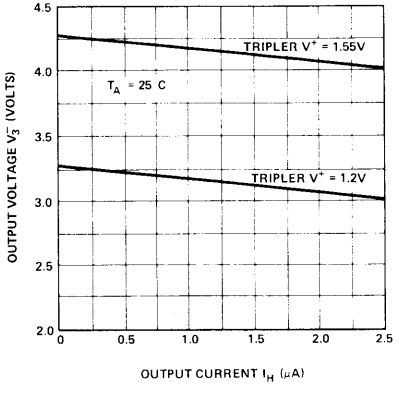
SUPPLY CURRENT VS. SUPPLY VOLTAGE



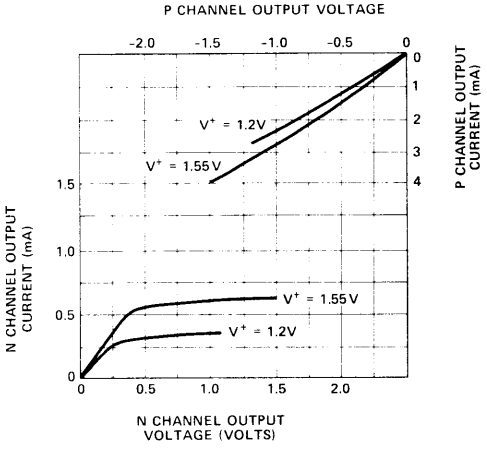
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



VOLTAGE MULTIPLIER OUTPUT VOLTAGE VS. OUTPUT CURRENT



ALARM DRIVER OUTPUT CURRENT VS. OUTPUT VOLTAGE



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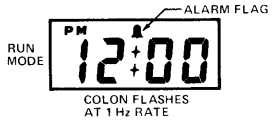
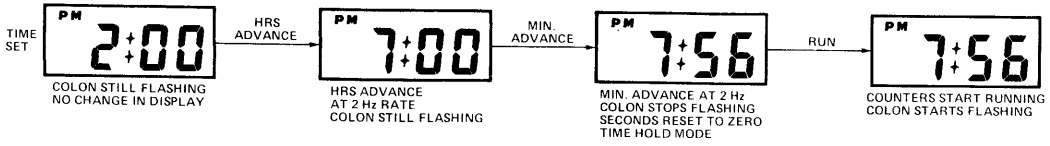
NORMAL CLOCK OPERATION



In normal operation, hours and minutes are displayed with the colon flashing at a 1 Hz rate. An AM and a PM indicator flag is provided in the 12 hour mode, while in the 24 hour mode, the pads used for the AM/PM flags are utilized to drive the segments which produce the numeral "2" in the tens of hours digit. The alarm flag will be on if the alarm is enabled, and off if the alarm is not enabled; (Alarm Off input at V^+).

TIME SETTING

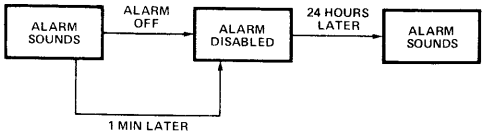


NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.

ALARM OPERATION



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The alarm comparator provides a 24 hour alarm in both 12 and 24 hour modes. When the time of day and alarm times are equal, the alarm outputs are enabled, providing that the ALARM OFF input is at V_T^-. If the ALARM OFF input is at V^+, the alarm outputs will not be enabled. The alarm outputs provide a push-pull, or bridge, configuration for direct drive of a piezoelectric transducer, and if increased drive (loudness) is desired, a coil and external NPN transistor may be used. The external transistor should be driven by the ALARM 1 output. The coil DC resistance should be 100Ω or greater, to limit the peak current to less than 13 mA.

The alarm signal is a complex waveform that generates the Intersil Cricket sound. The alarm output will automatically stop after one minute unless either the ALARM OFF or the SNOOZE input is used. The alarm transducer should be selected to provide maximum output (loudness) at 4 kHz, that is, it should be resonant at 4 kHz.

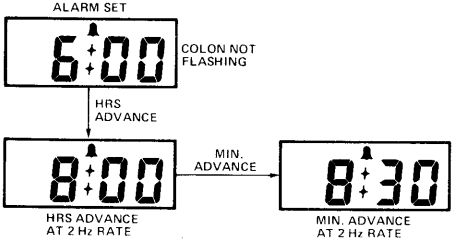
SNOOZE OPERATION

A momentary closure of the SNOOZE switch to V^+ will silence the alarm and start the snooze timer. The Snooze input must be activated during the one minute the alarm is sounding in order to start a Snooze cycle. After 8 minutes the alarm will again sound, and will continue for 2 minutes and stop unless ALARM OFF is used or another Snooze cycle is activated. The Snooze may be repeated as many times as desired.

NOTE: In die form, all the SNOOZE input pads are available, allowing the manufacturer or user to select snooze times from 2 to 14 minutes in 2 minute steps. These pads are identified as SN1, SN2 and SN3. See the following table for the selection of Snooze times:

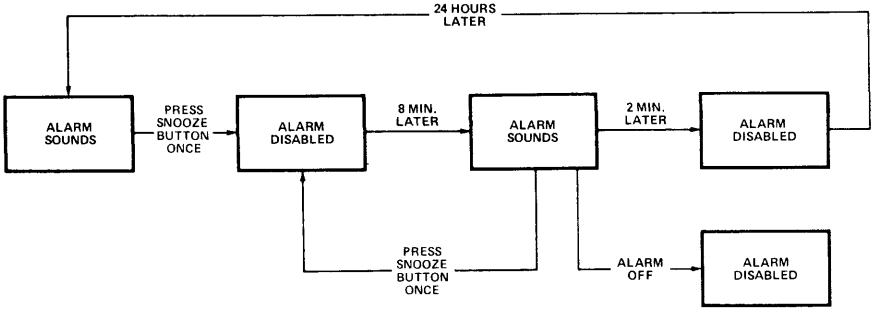
INPUT CODE (1 = V^+)			SNOOZE
SN3	SN2	SN1	TIME
0	0	0	None
0	0	1	2 minutes
0	1	0	4 minutes
0	1	1	6 minutes
1	0	0	8 minutes
1	0	1	10 minutes
1	1	0	12 minutes
1	1	1	14 minutes

ALARM SETTING



The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the RUN/SET switch is in the Alarm Set position.

SNOOZE OPERATION



NOTE: IF ALARM OFF IS LEFT AT V^+ THE ALARM WILL NOT SOUND 24 HOURS LATER.

APPLICATION NOTES

ALARM DRIVE

The ICM7223 alarm output transistors are capable of directly driving a piezoelectric ceramic transducer at 3 volts peak-to-peak. Any transducer that does not require more than 1 mA of peak current may also be used. The transducer should generate maximum output at 4 kHz. If a louder sound is desired, buffering (using an NPN transistor and 5 mho coil) or sound enhancement techniques such as a resonant cavity or diaphragm will be required. See Application Bulletin A031 for details.

TEST MODE

The high speed test mode for automatic testing is entered by pulling the ALARM OFF/TEST Input to -7 volts referenced to $V\overline{1}$. In this state the HRS/MIN ADVANCE input will advance the appropriate counters at the rate that the input is toggled. The colon will appear to stop flashing as it is changing state more rapidly than the display can respond. In the run mode the minutes will change at a 4.27 Hz rate, as the clock has been speeded up by a factor of 256 Hz. The backplane frequency will be 512 Hz. The voltage tripler drive frequencies remain the same as in normal modes.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

VOLTAGE MULTIPLIER

The ICM7223 voltage multiplier may be utilized only in a tripler configuration; only four pins, and three external capacitors are required. The connection of the capacitors differs from that used in standard watch circuit type voltage multipliers, therefore close attention should be paid to substrate design to ensure the proper connection of the capacitors.

OSCILLATOR

The oscillator of the ICM7223 is designed for low frequency operation at very low currents from a 1.55 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2\,(C_O + C_L)} \; ; \; C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance of Crystal
C_m = Motional Capacitance of Crystal

The g_m required for startup calculated should not exceed 50% of the g_m guaranteed for the device.

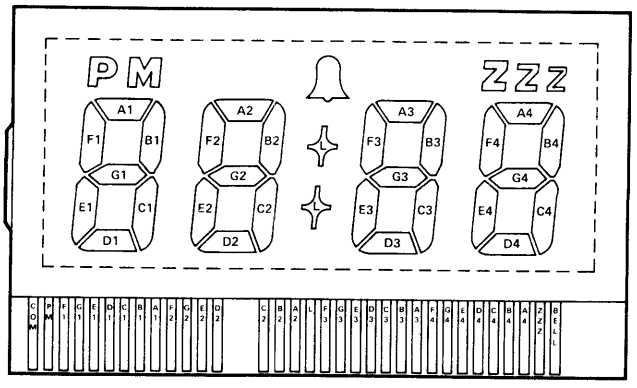
POWER UP RESET

An on chip circuit is provided that will reset all counters and flip-flops to a known state when power is first applied. The alarm and timekeeping counters will be reset to 1:00 am in the 12 hr. mode and 0:00 in the 24 hr. mode. This function is not tested during automatic testing, as it does not affect normal circuit operation.

ICM7223

DISPLAY

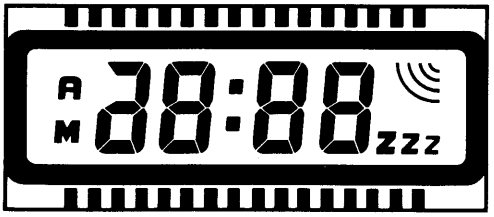
MOTOROLA	MLC406
BECKMAN	737-01
LADCOR	LAD-001
HAMLIN	3411
TIMEX	T1001
COCKROFT	CII202



DISPLAY FONT

NUMBERS

COCKROFT CII201



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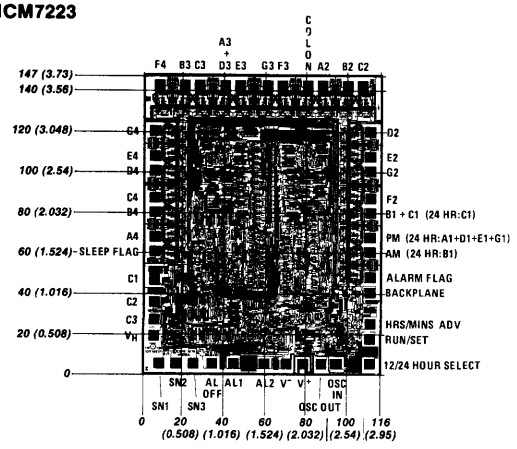
CHIP TOPOGRAPHY

ICM7223



CHIP DIMENSIONS: 116 x 147 mils (2.95 x 3.73 mm)

ICM7223A 3-1/2 Digit LCD Battery Operated Clock Circuit With Snooze and Sleep Timers

FEATURES

- **Single 9V transistor battery operation**
- **3-1/2 digit display with AM/PM, SLEEP and ALARM flags**
- **Direct alarm drive with complex (cricket) alarm tone**
- **Programmable snooze**
- **Programmable sleep timer with RADIO ENABLE OUTPUT**
- **Wide operating voltage range — 4 to 15 volts**
- **Low current — 15μA @ 9V**
- **On-chip fixed oscillator input capacitor**
- **Uses standard 32.768 KHz crystal**
- **Low battery indicator (display flashes at 1 Hz)**
- **Display and alarm test**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7223AIPL	-20°C to +85°C	40 Pin Plastic DIP
ICM7223A/D	-20°C to +85°C	DICE

GENERAL DESCRIPTION

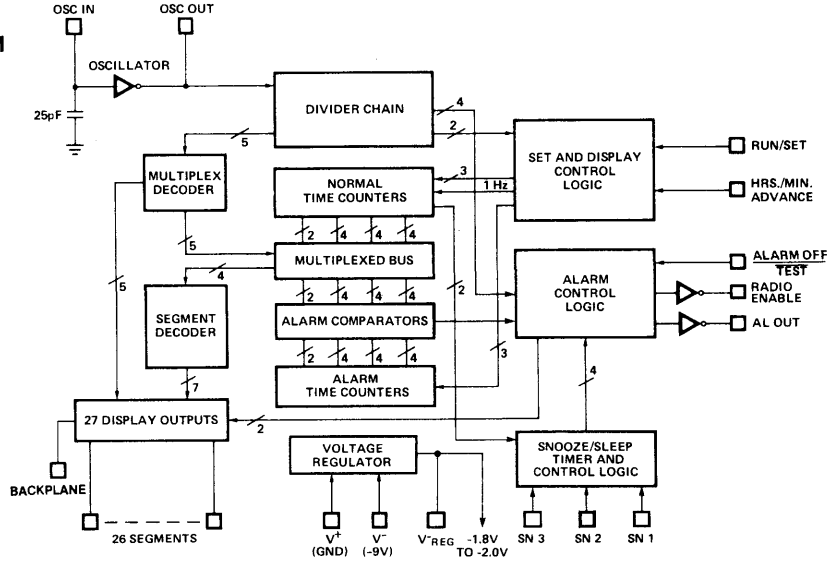
The ICM7223A is a fully integrated 3-1/2 digit LCD clock circuit with 24 hour alarm, and sleep and snooze timers. For high accuracy and low power consumption a 32.768 kHz quartz watch crystal is used as the time base, while the number of external components has been reduced to a minimum. This circuit is intended for use in 9V clock-radio systems where both the clock and the radio operate from the same battery.

The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered; this permits synchronization of the clock to the nearest second. Seconds are not displayed.

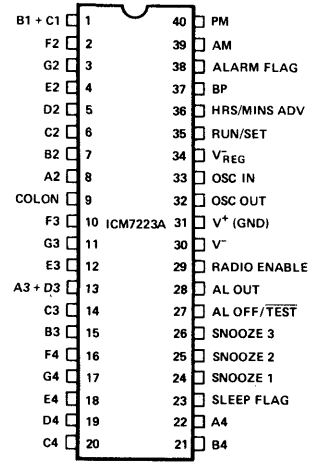
The alarm employs a snooze timer that may be programmed from 2 to 14 minutes in two minute increments; the sleep timer may be set from 8 to 56 minutes in 8 minute increments. The alarm outputs consist of a complex (cricket) alarm tone to directly drive a speaker of piezoelectric transducer, and a radio enable output which allows control of a clock radio. Low battery voltage is indicated by the display flashing at a 1 Hz rate whenever the battery voltage falls below about 5.6V.

The ICM7223A is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life. Current drain at 9 volts is typically 15μA with a maximum of 25μA.

BLOCK DIAGRAM



PIN CONFIGURATION (outline dwg PL)



NOTE: CONSULT FACTORY IF 24 HOUR TIME DISPLAY IS DESIRED.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -20°C to +85°C
Power Dissipation[1] ..... 500 mW
Supply Voltage 18V
Input Voltage
(OSC IN, SN_1, SN_2, SN_3) ..... $-2V \le V_{IN} \le V^+ + 0.3V$
(RUN/SET, HRS/MIN ADV, AL OFF/$\overline{TEST}$) ..... $V^- - 0.3V \le V_{IN} \le V^+ + 0.3V$
Output Voltage
(OSC OUT) ..... $-2V \le V_{OUT} \le V^+$
(AL OUT, RADIO ENABLE, All Segment Drivers) ..... $V^- \le V_{OUT} \le V^+$

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

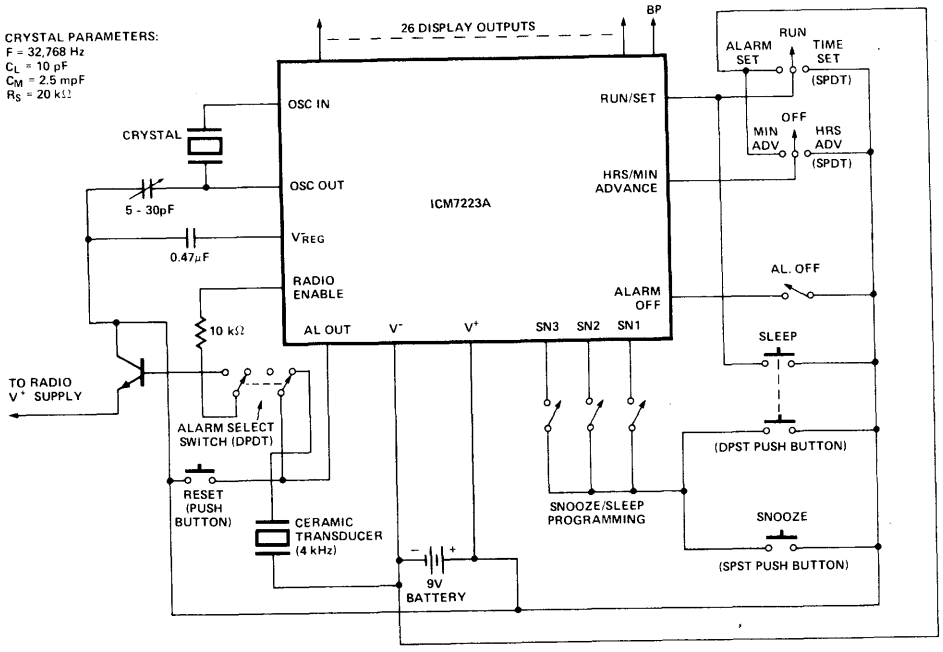
OPERATING CHARACTERISTICS

All testing at 25°C; All numbers stated in absolute value; $V^+ = 9V$ unless otherwise specified.

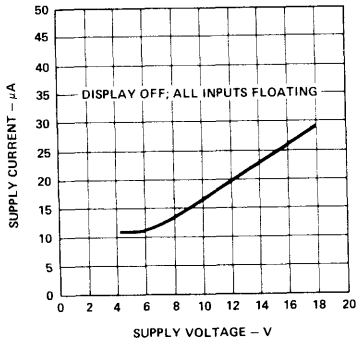
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supply Voltage Range Timekeeping Accurate	V^+		4		18	V
Supply Current	1^+	$V^+ = 9V$		15	25	μA
Oscillator Input Current(3)	I_{OSCI}	'OSC IN' Connected to V^+ 'OSC OUT' Open Circuit		0.2		μA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		μmho
Oscillator Stability	f_{STAB}	$5V \le V_{SUPPLY} \le 15V$		0.7	1.0	ppm
Alarm Saturation Resistance	$R_{AL(on)}$	P-ch at 10mA		220	300	Ω
		N-ch at 10 mA		100	150	Ω
Segment Drive Current	I_{SEG}	$V_{SAT} = 0.2V$ (Both Directions)	5			μA
Backplane Drive Current	I_{BP}	$V_{SAT} = 0.1V$ (Both Directions)	20			μA
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$		10	30	μA
		$V_{SW} = V^-$		10	30	μA

NOTES: 1. This value of power dissipation is that of the package and will not be obtained under normal operating conditions.

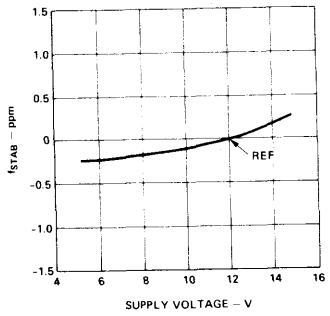
TYPICAL CLOCK RADIO APPLICATION



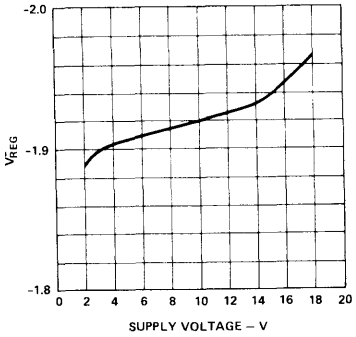
SUPPLY CURRENT vs. SUPPLY VOLTAGE



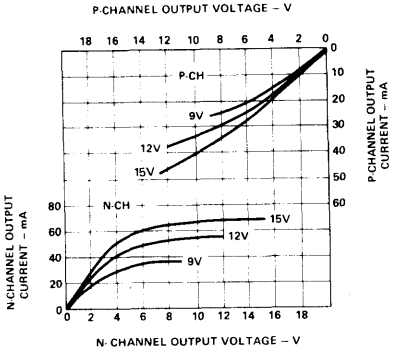
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



VOLTAGE REGULATOR OUTPUT vs. SUPPLY VOLTAGE

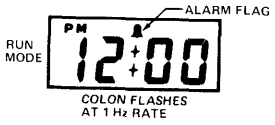


ALARM DRIVER OUTPUT CURRENT vs. OUTPUT VOLTAGE



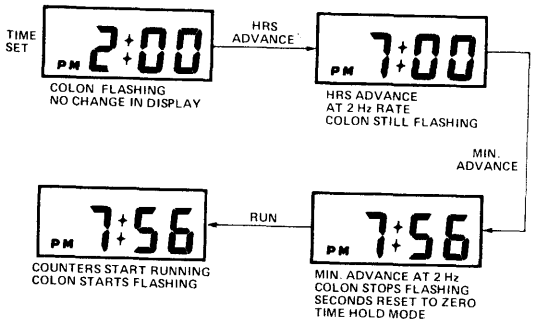
NORMAL CLOCK OPERATION

In normal operation hours and minutes are displayed with the colon flashing at a 1 Hz rate. AM and PM indicators are provided. The alarm flag will be on if the ALARM OFF input is at V^-, and off with the ALARM OFF input at V^+. Time is displayed in a 12 hour format with AM/PM annunciators.



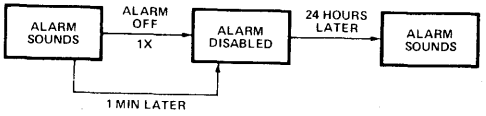
TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.



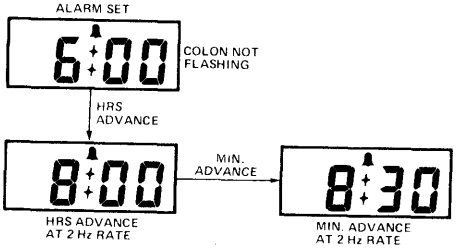
NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

ALARM OPERATION



The alarm comparator provides a 24 hour alarm by taking into account AM and PM. When the time of day and alarm times agree, and the ALARM OFF input is floating, the ALARM and RADIO ENABLE outputs are activated; the alarm sounds and the RADIO ENABLE line goes to V^+. Momentarily tying the ALARM OFF input to V^+ will silence both the alarm and the radio. The alarm will automatically shut off after one minute if ALARM OFF is not used; the RADIO ENABLE will stay HIGH until either the ALARM OFF or SNOOZE inputs are used. The SNOOZE input must be applied within one minute in order to begin a snooze cycle.

ALARM SETTING

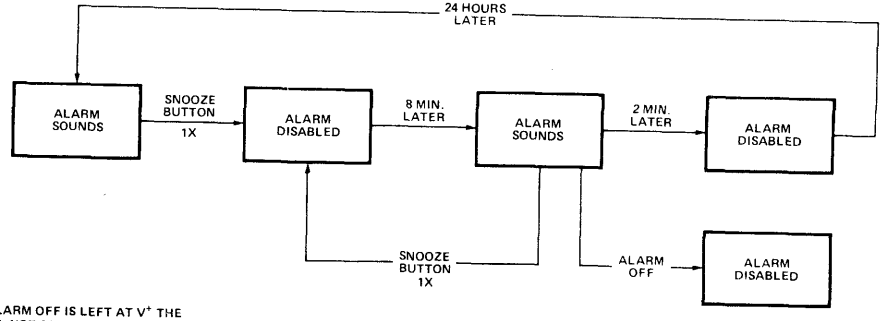


The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the RUN/SET switch is in the Alarm Set position.

SNOOZE OPERATION

To begin a snooze cycle, the SNOOZE input must be momentarily shorted to V^+ during the one minute that the alarm is sounding or the RADIO ENABLE line is high. When this is done the alarm will be silenced and the snooze timer started; the alarm will sound again after the selected snooze time. Unless the ALARM OFF input is used, the alarm will automatically shut off after two

SNOOZE OPERATION



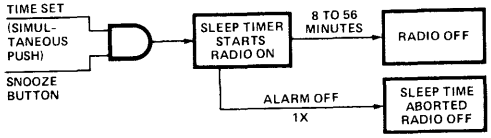
NOTE: IF ALARM OFF IS LEFT AT V^+ THE ALARM WILL NOT SOUND 24 HOURS LATER.

minutes. The RADIO ENABLE will remain on until the ALARM OFF line is activated, however, a second snooze cycle can be initiated with the SNOOZE switch. This can only be done if the SNOOZE is activated while the alarm is sounding.

The snooze times are programmable in 7 steps from 2 to 14 minutes. Programming is accomplished with binary coding on the three SNOOZE inputs, as shown in the following table:

INPUT CODE (1 = V⁻)			SNOOZE TIME	SLEEP TIME
SN3	SN2	SN1		
0	0	0	None	None
0	0	1	2 minutes	8 minutes
0	1	0	4 minutes	16 minutes
0	1	1	6 minutes	24 minutes
1	0	0	8 minutes	32 minutes
1	0	1	10 minutes	40 minutes
1	1	0	12 minutes	48 minutes
1	1	1	14 minutes	56 minutes

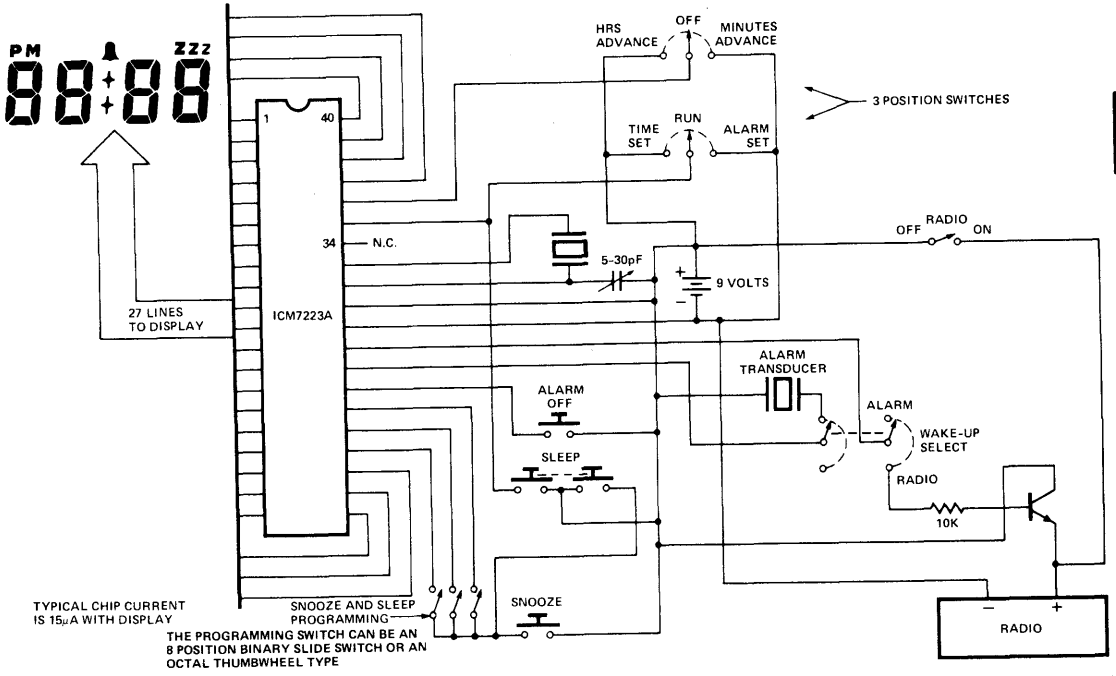
SLEEP TIMER OPERATION



The sleep timer may be activated at any time except during a snooze cycle or when the alarm is sounding. The sleep timer is started by setting the RUN/SET switch in the SET position and momentarily activating the SNOOZE switch. Sleep times are programmed with the snooze inputs; see table on previous page.

Another method for sleep timer activation is to use a single DPST pushbutton switch, with one pole connected to the RUN/SET switch and the other to the common side of the SNOOZE programming switch. The other side of the switches is tied to V^+. (See typical application, page 3). This method allows the use of a "dedicated" sleep button, which may be recessed to prevent accidental activation.

When the sleep timer is activated the RADIO ENABLE output is set high to turn on a radio and the sleep flag appears on the display. At the end of the programmed sleep time the RADIO ENABLE output is returned to V^- and the sleep flag disappears.



ICM7223A 12HR LCD SNOOZE ALARM CLOCK RADIO CIRCUIT WITH SLEEP TIMER.
(9 volt single battery operation)

LOW BATTERY INDICATION

The ICM7223A is provided with a completely integrated low battery indicator. When the supply voltage drops below about 5.6V the display will begin flashing at a 1 Hz rate. Actual trigger points vary from chip to chip, but will usually be in the range of 5.2V to 6V. Time keeping will not be affected.

CHIP RESET

Power up reset is not provided on the 7223A, as interaction between the V^+ and V^- inputs and the voltage regulator in noisy environments could cause spurious resetting. Resetting the circuit to a known state, 1:00 AM, can be accomplished by momentarily connecting the ALARM OUT output to V^+; this can be done with a NO SPST switch. This same method may be employed to clear the 7223A in the event that it powers up in an illegal state. The switch should be made accessible to the user for use when changing batteries.

TEST MODE OPERATION

This mode, provided for high speed automatic testing, is entered by shorting ALARM OFF to V^-. The minutes will then advance at a 4.27 Hz rate and setting can be accomplished by the application of a digital input to the hrs — mins advance input. The counter will then advance once per pulse. Note that in the test mode there is no debounce protection on the HRS/MINS ADVANCE input.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

OSCILLATOR

The oscillator of the ICM7223A is designed for low frequency operation at very low currents from a 9 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \; ; \; C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S	=	Series Resistance of Crystal
f	=	Frequency of the Crystal
Δf	=	Frequency Shift from Series Resonance Frequency
C_O	=	Static Capacitance of Crystal
C_{IN}	=	Input Capacitance
C_{OUT}	=	Output Capacitance
C_L	=	Load Capacitance of Crystal
C_m	=	Motional Capacitance of Crystal

The (calculated) g_m required for startup should not exceed 50% of the g_m guaranteed for the device.

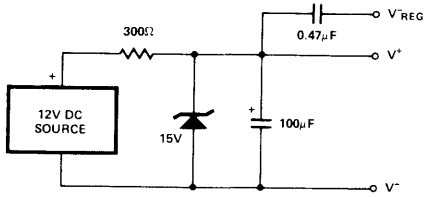
ALARM DRIVE

The ICM7223A will directly drive any suitable audio transducer (piezoelectric ceramic, or magnetic speaker) with a peak frequency response of 4 kHz with V^+ = 9V and a peak current of 10 mA. The volume should be more than adequate; no buffering should be required.

POWER SUPPLY CONSIDERATIONS

The ICM7223A contains an on-chip CMOS voltage regulator which operates all timing and counting logic circuitry at about 1.8 to 2.0V below V^+. This provides low current operation over a voltage range of 4-15V and also improves oscillator stability. The LCD maximum operating voltage will be the limiting factor in most cases, therefore the supply voltage will rarely exceed 12V.

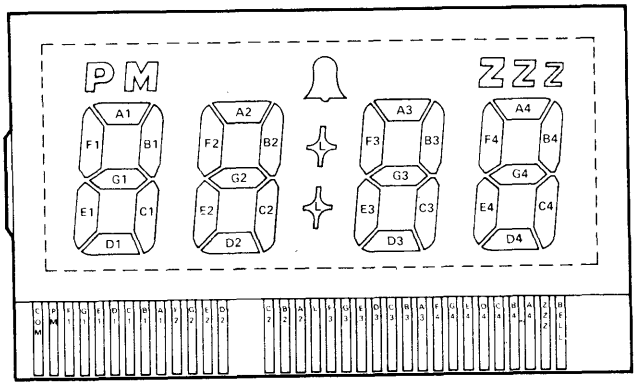
For applications which involve power supplies with high noise levels or transients, it will be necessary to provide supply filtering. The voltage regulator output (V^-_{REG}) should be decoupled to V^+ with a 0.22μF to 0.47μF capacitor, and the V^+ and V^- lines should be low-pass-filtered using a 300Ω resistor and 100μF capacitor. Note that a zener diode in parallel with the filter cap will limit voltage spikes to 15V, and should be included if the common "24V survival" required for automotive use is desired.



ICM7223A

DISPLAY

MOTOROLA	MLC406
BECKMAN	737-01
LADCOR	LAD-001
HAMLIN	3411
TIMEX	T1001
COCKROFT	CII202

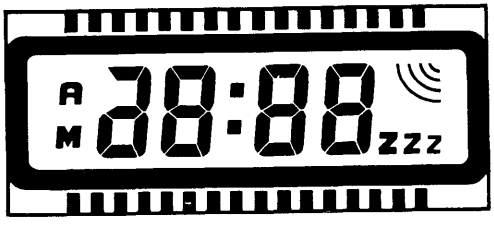


DISPLAY FONT

NUMBERS

1 2 3 4 5 6 7 8 9 0

COCKROFT CII201

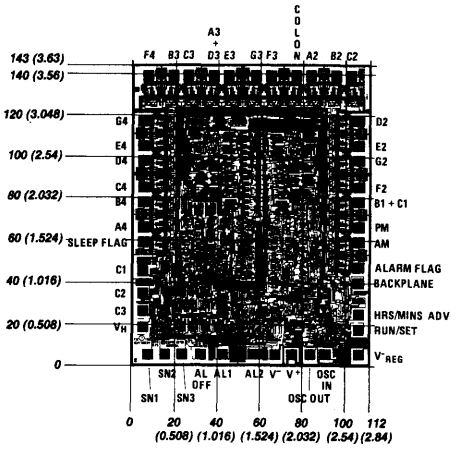


7

ICM7223A

CHIP TOPOGRAPHY

ICM7223A



CHIP DIMENSIONS: 112 x 143 mils (2.84 x 3.63 mm)

ICM7223VF
3-1/2 Digit Vacuum Fluorescent Clock Circuit With Snooze Timer and Sleep Timer

FEATURES

- **3-1/2 digit display with AM/PM, sleep timer, and alarm flags**
- **Direct alarm drive with complex (cricket) alarm tone plus radio enable for clock radio applications**
- **8 minute repeatable programmable snooze**
- **Programmable sleep timer**
- **Wide operating voltage range — 4 to 15 volts**
- **Low current — 12μA @ 12V with display off**
- **On-chip fixed oscillator input capacitor**
- **Uses standard 32.768 kHz crystal**
- **Display control blanks display for auto and travel clock applications**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7223VFIPL	-20°C to +85°C	40 Pin Plastic DIP
ICM7223VF/D	-20°C to +85°C	Dice

GENERAL DESCRIPTION

The ICM7223VF is a fully integrated 3-1/2 digit Vacuum Fluorescent clock circuit with 24 hour alarm, and sleep and snooze timers. For high accuracy and low power consumption a 32.768 kHz quartz watch crystal is used as the time base, while the number of external components has been reduced to a minimum. The vacuum fluorescent display outputs are static, or non-multiplexed, thereby eliminating radio frequency interference (RFI).

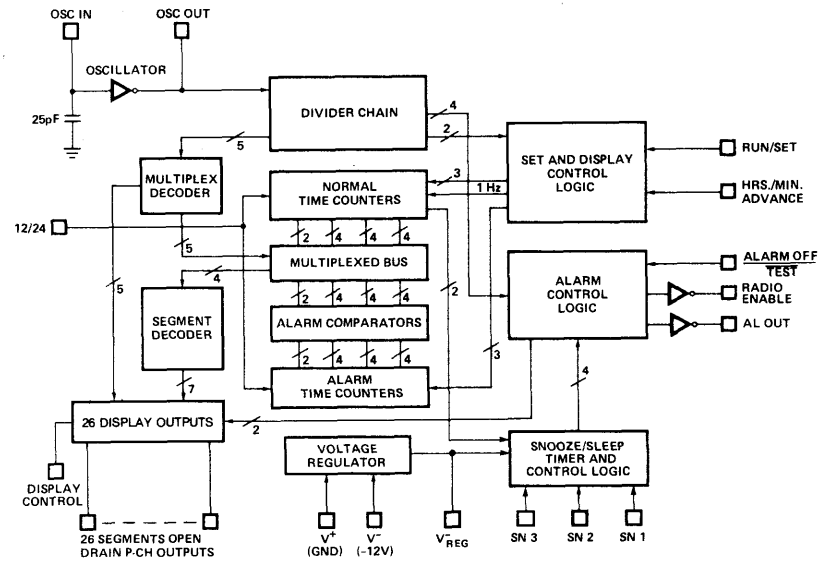
The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered; this permits synchronization of the clock to the nearest second. Seconds are not displayed.

The alarm employs a snooze timer that may be programmed from 2 to 14 minutes in two minute increments; the sleep timer may be set from 8 to 56 minutes in 8 minute increments. The alarm outputs consist of a complex (cricket) alarm tone to directly drive a speaker or piezoelectric transducer and a radio enable output which allows control of a clock radio.

The ICM7223VF is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life. Current drain at 12 volts is typically 12μA with a maximum of 25μA (display off).

7

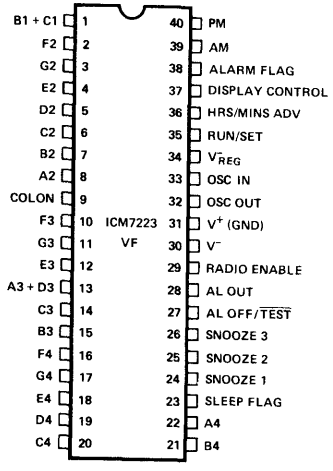
BLOCK DIAGRAM



ICM7223VF

INTERSIL

PIN CONFIGURATION (OUTLINE DRAWING PL)



NOTE: CONSULT FACTORY IF 24 HOUR TIME DISPLAY IS DESIRED.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -20°C to +85°C
Power Dissipation[1] ..... 500 mW
Supply Voltage ($V^+ - V^-$) 18V
Input Voltage
(OSC IN, SN_1, SN_2, SN_3) ..... $-2V \le V_{IN} \le V^+ + 0.3V$
(RUN/SET, HRS/MIN ADV, AL OFF/$\overline{TEST}$) ..... $V^- - 0.3V \le V_{IN} \le V^+ + 0.3V$
Output Voltage
OSC OUT ..... $-2V \le V_{OUT} \le V^+$
AL OUT, RADIO ENABLE ..... $V^- \le V_{OUT} \le V^+$
All Segment Drivers ..... $V^+ - 35V \le V_{OUT} \le V^+$

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

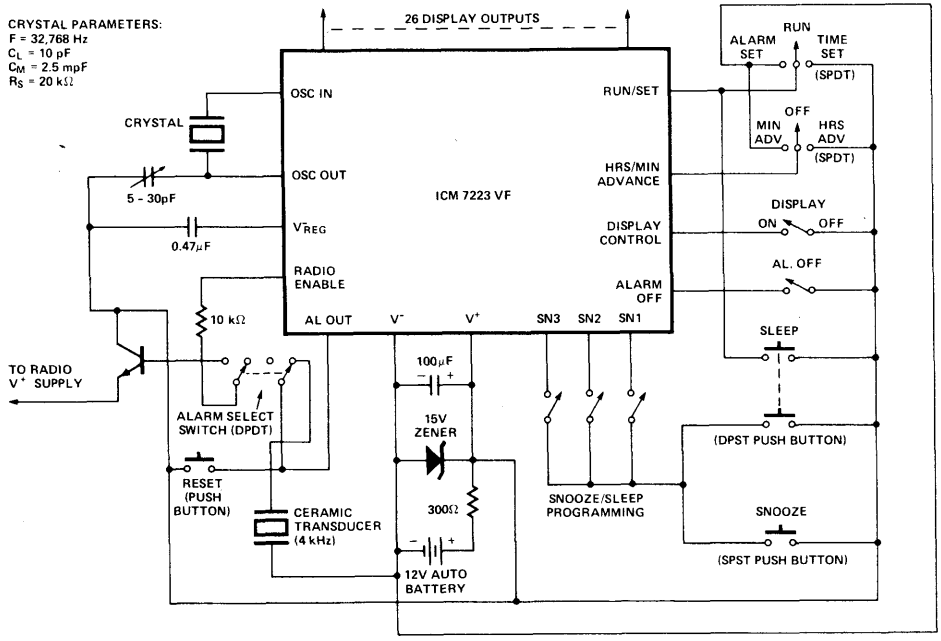
OPERATING CHARACTERISTICS All testing at 25°C; All numbers stated in absolute value

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supply Voltage Range Timekeeping Accurate	V^+		4		15	V
Supply Current	I^+	Display OFF $V^+ - V^- = 12V$		12	25	μA
Supply Current Display ON[2]		$V^+ - V^- = 12V$, Display Test, NEC LD8164		3		mA
Segment Output Saturation Resistance	R_{SEG}	I_{DS} = 1mA P-ch		1000	1500	Ω
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Stability	f_{STAB}	$5V \le V_{SUPPLY} \le 15V$		0.7	1.0	ppm
Alarm Saturation Resistance	$R_{AL(on)}$	P-ch at 10mA		220	300	Ω
		N-ch at 10mA		100	150	Ω
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$		10	30	μA
		$V_{SW} = V^-$		10	30	μA

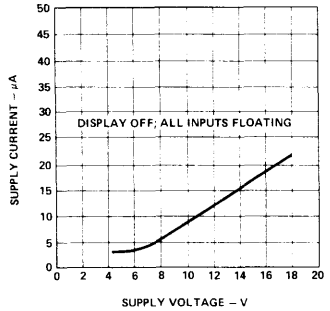
NOTES: 1. This value of power dissipation is that of the package and will not be obtained under normal operating conditions.
2. Chip current plus display anode current only; does not include display filament or grid currents.

7

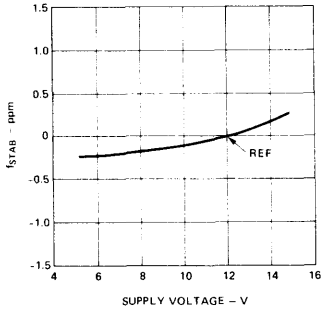
TYPICAL CLOCK RADIO APPLICATION



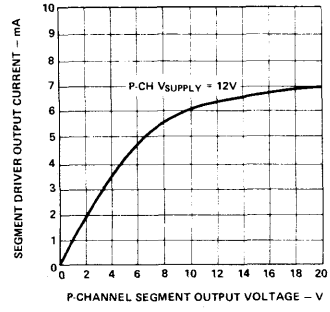
SUPPLY CURRENT vs. SUPPLY VOLTAGE



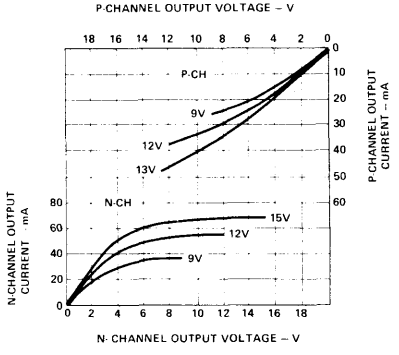
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



SEGMENT DRIVER OUTPUT CURRENT vs. DRAIN VOLTAGE



ALARM DRIVER OUTPUT CURRENT vs. OUTPUT VOLTAGE

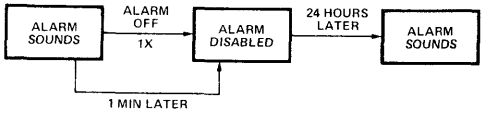


NORMAL CLOCK OPERATION

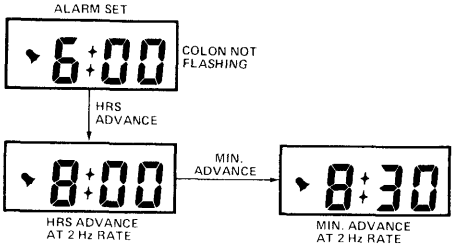
In normal operation hours and minutes are displayed with the colon flashing at a 1 Hz rate. AM and PM indicators are provided. The alarm flag will be on if the ALARM OFF input is floating, and off with the ALARM OFF input at V^+. Time is displayed in a 12 hour format with AM/PM annunciators.

ALARM OPERATION

The alarm comparator provides a 24 hour alarm by taking into account AM and PM. When the time of day and alarm times agree, and the ALARM OFF input is floating, the ALARM and RADIO ENABLE outputs are activated; the alarm sounds and the RADIO ENABLE line goes to V^+. Momentarily tying the ALARM OFF input to V^+ will silence both the alarm and the radio. The alarm will automatically shut off after one minute if the ALARM OFF is not used; the RADIO ENABLE will stay HIGH until either the ALARM OFF or SNOOZE inputs are used. The SNOOZE input must be applied within one minute in order to begin a snooze cycle.



ALARM SETTING



The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the RUN/SET switch is in the Alarm Set position.

SNOOZE OPERATION

To begin a snooze cycle, the SNOOZE input must be momentarily shorted to V^+ during the one minute that the alarm is sounding or the RADIO ENABLE line is high. When this is done the alarm will be silenced and the snooze timer started; the alarm will sound again after the selected snooze time. Unless the ALARM OFF input is used, the alarm will automatically shut off after two minutes. The RADIO ENABLE will remain on until the ALARM OFF line is activated, however, a second snooze cycle can be initiated with the SNOOZE switch. This can only be done if the SNOOZE is activated while the alarm is sounding.

The snooze times are programmable in 7 steps from 2 to 14 minutes. Programming is accomplished with binary coding on the three SNOOZE inputs, as shown in the following table:

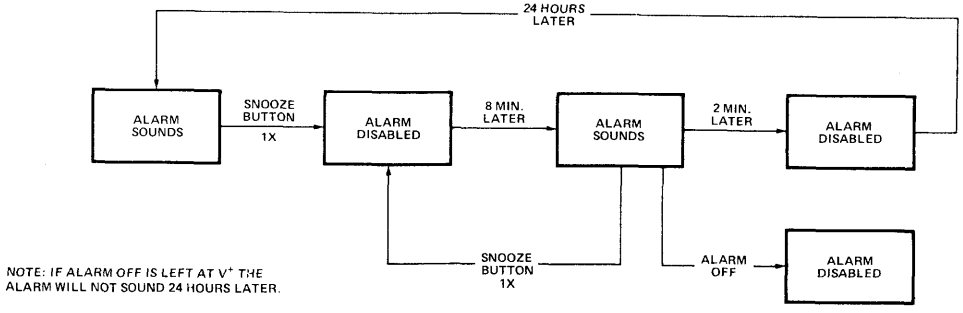
INPUT CODE (1 = V^+)			SNOOZE TIME	SLEEP TIME
SN3	SN2	SN1		
0	0	0	None	None
0	0	1	2 minutes	8 minutes
0	1	0	4 minutes	16 minutes
0	1	1	6 minutes	24 minutes
1	0	0	8 minutes	32 minutes
1	0	1	10 minutes	40 minutes
1	1	0	12 minutes	48 minutes
1	1	1	14 minutes	56 minutes

SLEEP OPERATION

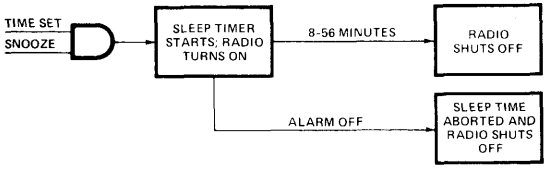
The sleep timer may be activated at any time except during a snooze cycle or when the alarm is sounding. The sleep timer is started by setting the RUN/SET switch in the SET position and momentarily activating the SNOOZE switch. Sleep times are programmed with the snooze inputs; see table on previous page.

Another method for sleep timer activation is to use a single DPST pushbutton switch, with one pole connected to the RUN/SET switch and the other to the common side of the SNOOZE programming switch. The other side of the switches is tied to V^+. (See typical application, page 3). This method allows the use of a "dedicated" sleep button, which may be recessed to prevent accidental activation.

SNOOZE OPERATION

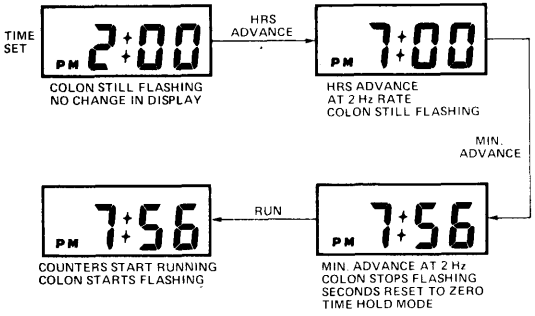


When the sleep timer is activated the RADIO ENABLE output is set high to turn on a radio. At end of the programmed sleep time the RADIO ENABLE output is returned to V^-.



TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.



NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

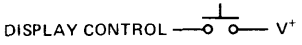
DISPLAY

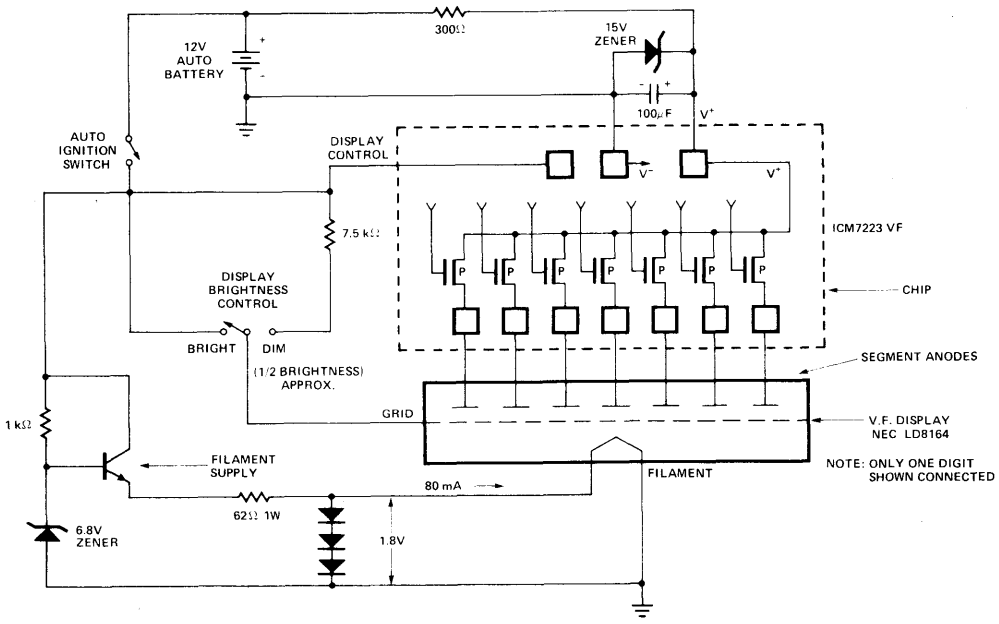
The ICM7223VF is designed for use only with 12V direct drive (non-multiplexed) 3½ digit vacuum fluorescent displays such as the NEC LD8164 or equivalent. (But see "LED Display Driving" under DESIGN CONSIDERATIONS.)

DESIGN CONSIDERATIONS

DISPLAY CONTROL

This input allows the display to be blanked (turned off) when low current operation is desirable, such as when an auto clock is being used with the engine turned off. For normal operation connect DISPLAY CONTROL to V^+; to turn off display allow the input to float. A SPST switch can be used for those times when it is desired to turn on the display with the engine off.





ICM7223VF VACUUM FLUORESCENT DISPLAY CONNECTION EXAMPLE; AUTO CLOCK APPLICATION

LED DISPLAY DRIVE

It is possible to drive high efficiency common cathode LED displays with the 7223VF as long as the total display current does not exceed 100mA (or 4mA per segment), as excessive on-chip heating may occur. Operation is not guaranteed for extended periods, since the package power dissipation limits are likely to be exceeded. When driving LED displays with the 7223VF, use of the DISPLAY CONTROL as a "time demand" is highly recommended.

CHIP RESET

Power up reset is not provided on the 7223VF, as interaction between the V^+ and V^- inputs and the voltage regulator in noisy environments could cause spurious resetting. Resetting the circuit to a known state, 1:00 AM, can be accomplished by momentarily connecting the ALARM OUT output to V+; this can be done with a NO SPST switch. This same method may be employed to clear the 7223VF in the event that it powers up in an illegal state.

TEST MODE OPERATION

This mode, provided for high speed automatic testing, is entered by shorting ALARM OFF to V^-. The minutes will then advance at a 4.27 Hz rate and setting can be accomplished by the application of a digital input to the hrs — mins advance input. The counter will then advance once per pulse. Note that in the test mode there is no debounce protection on the HRS/MINS ADVANCE input.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

7

OSCILLATOR

The oscillator of the ICM7223VF is designed for low frequency operation at very low currents from a 12 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2 \cdot (C_O + C_L)} \; ; \; C_L = \frac{C_{IN}\, C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance of Crystal
C_m = Motional Capacitance of Crystal

The (calculated) g_m required for startup should not exceed 50% of the g_m guaranteed for the device.

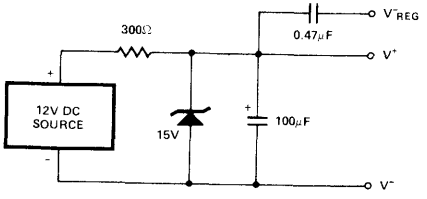
ALARM DRIVE

The ICM7223VF will directly drive any suitable audio transducer (piezoelectric ceramic, or magnetic speaker) with a peak frequency response of 4 kHz with V^+ = 12V and a peak current of 10 mA. The volume should be more than adequate; no buffering should be required.

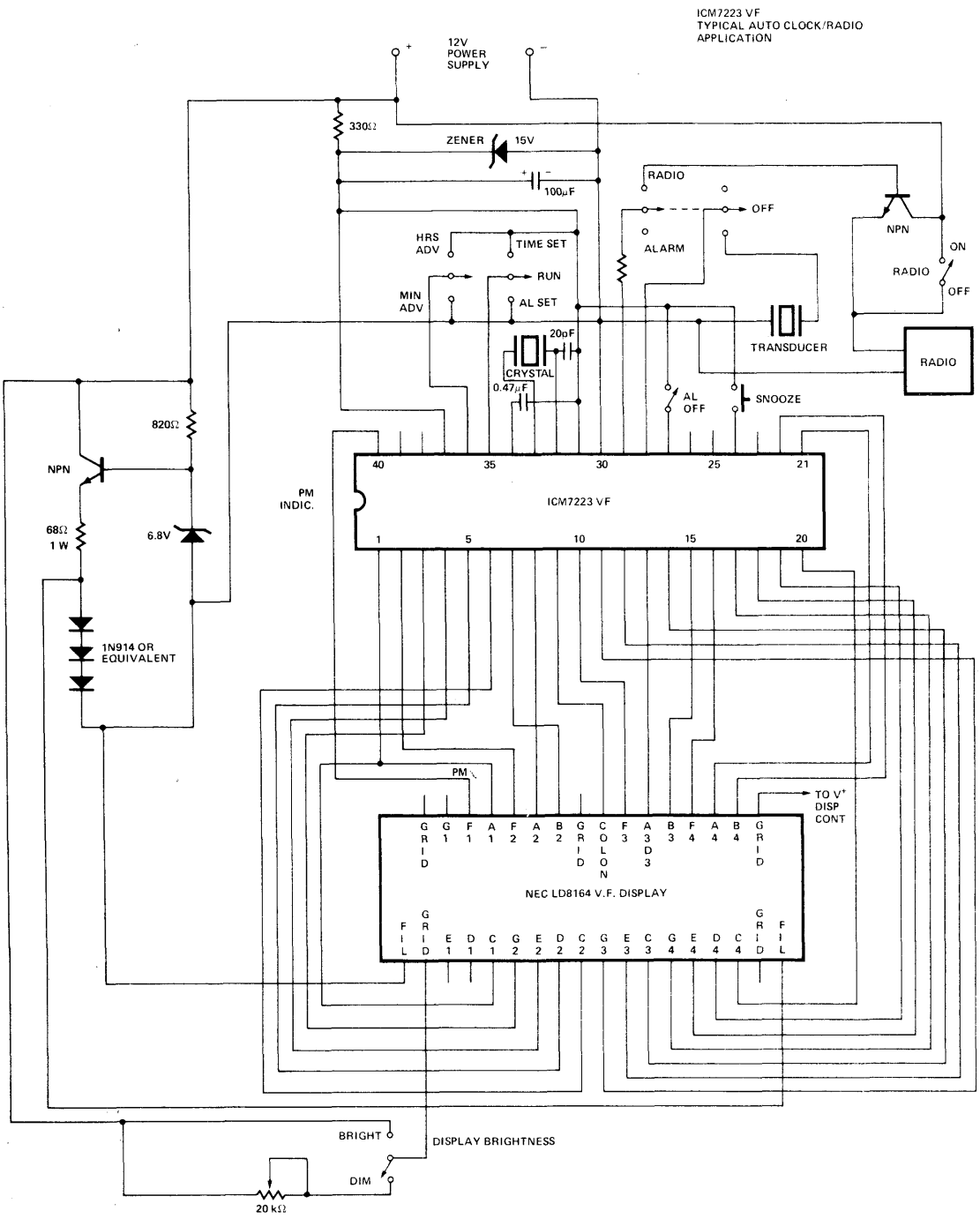
POWER SUPPLY CONSIDERATIONS

The ICM7223VF contains an on-chip CMOS voltage regulator which operates all timing and counting logic circuitry at about 1.8 to 2.0V below V^+. This provides low current operation over a voltage range of 4-15V and also improves oscillator stability.

For applications which involve power supplies with high noise levels or transients, it will be necessary to provide supply filtering. The voltage regulator output (V^-_{REG}) should be decoupled to V^+ with a 0.22μF to 0.47μF capacitor, and the V^+ and V^- lines should be low-pass-filtered using a 300Ω resistor and 100μF capacitor. Note that a zener diode in parallel with the filter cap will limit voltage spikes to 15V, and should be included if the common "24V survival" required for automotive use is desired.

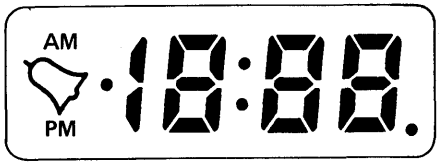


TYPICAL CLOCK RADIO APPLICATION



TYPICAL DISPLAY (FIP5E15S)

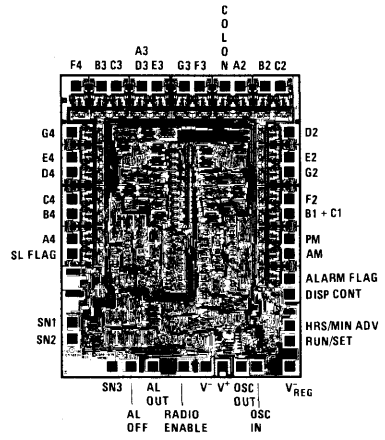
Other displays (by NEC):
- FIP 5B8S
- LD 8196
- LD 8164



DISPLAY FONT

NUMBERS

CHIP TOPOGRAPHY



CHIP DIMENSIONS: 116 x 147 mils (2.95 x 3.73 mm)

ICM7241 CMOS Frequency Divider 4.19 MHz to 32 kHz

FEATURES

- **Single battery operation (1.2 - 1.8V)**
- **Low power consumption — typ. 40μA @ 1.5V**
- **Oscillator biasing resistor included on-chip**

GENERAL DESCRIPTION

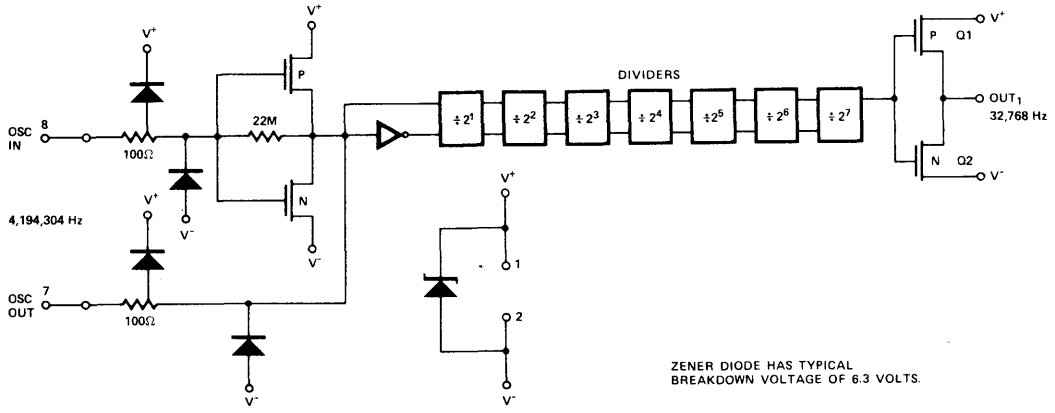
The ICM7241 is a fully integrated oscillator, 2 divider and output driver which efficiency converts 4.194304 MHz to 32.768kHz using a minimum of power. Only three external components are necessary for complete oscillator operation; a 4.194304 MHz crystal, a fixed input capacitor, and an output trimmer capacitor. The output has a low enough impedance to satisfy most drive requirements.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit[2] . 300 mW
Supply Voltage 3V
Output Voltage[1]
Input Voltage[1]
Storage Temperature ..... -30°C to +125°C
Operating Temperature ..... -20°C to 70°C

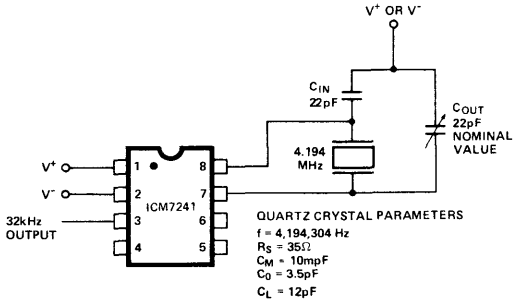
NOTES:
1. Except for instantaneous static discharges all terminals may exceed the supply voltage (2.0V max) by ±0.5 volt provided that the currents in these terminals are limited to 2 mA each.
2. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

SCHEMATIC DIAGRAM

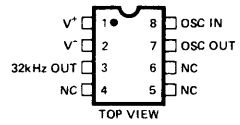


ZENER DIODE HAS TYPICAL BREAKDOWN VOLTAGE OF 6.3 VOLTS.

TYPICAL CONNECTION



PIN CONFIGURATION (outline dwg PA)



PIN 1 IS DESIGNATED BY EITHER A DOT OR A NOTCH.

ORDERING INFORMATION

Order devices by following part number: ICM7241

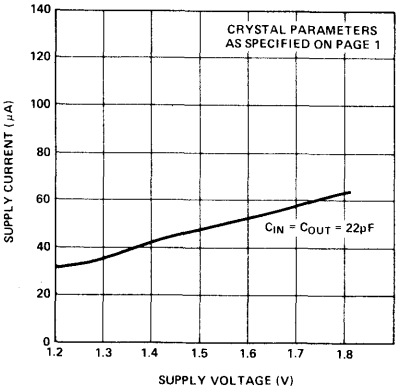
TYPICAL OPERATING CHARACTERISTICS

V^+ = 1.5V, fosc = 4,194,304 Hz, T_A = 25°C, unless otherwise specified. All numbers in absolute values.

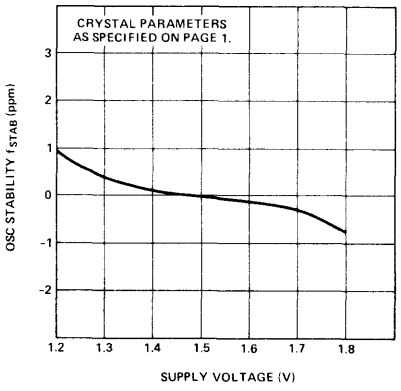
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I^+			40	70	μA
Guaranteed Operating Voltage Range	V^+	-20°C ≤ to ≤ 70°C	1.2		1.8	V
P-Ch Output Saturation Resistance	R_{SAT}	I_{OUT} = .5mA		680	2	kΩ
N-Ch Output Saturation Resistance	R_{SAT}	I_{OUT} = .5mA		240	1	kΩ
Oscillator Stability	f_{STAB}	1.2V < V^+ < 1.6V C_{IN} = C_{OUT} = 15pF		1		ppm
Oscillator Start-Up Time	t_{start}	V^+ = 1.2V			1.0	sec

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

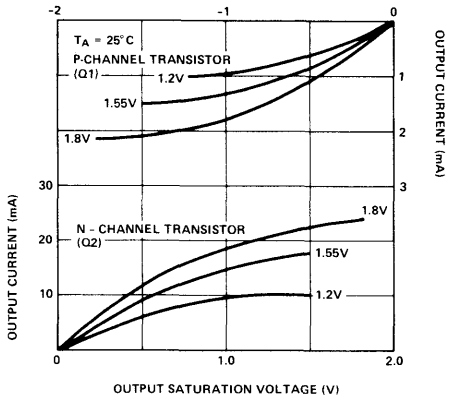
SUPPLY CURRENT vs. SUPPLY VOLTAGE



OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



OUTPUT CURRENT (SOURCE) vs. OUTPUT SATURATION VOLTAGE



ICM7245 Quartz Analog Watch Circuit

FEATURES

- **Very low current consumption: 0.4μA at 1.55 volt typical**
- **32 kHz oscillator requires only quartz crystal and trimming capacitor**
- **Bipolar stepper drive with low output ON resistance: 200 ohms maximum (7245 A/B/D/E/F)**
- **Unipolar stepper drive with very low output ON resistance: 50 ohms maximum (7245U)**
- **Extremely accurate: oscillator stability typically 0.1 ppm**
- **STOP function for easy time synchronization**
- **TEST input for highspeed testing**
- **Wide temperature range: -20° C to +70° C**
- **On chip fixed oscillator capacitor: 20pF ±20%**

TABLE OF OPTIONS

Device Number	Bipolar/ Unipolar	Pulse Width (ms)	Pulse Frequency	Oscillator Capacitor
ICM7245A	B	9.7	1Hz	COUT
ICM7245B	B	7.8	1Hz	CIN
ICM7245D	B	7.8	0.1Hz (1 pulse/ 10 seconds)	COUT
ICM7245E	B	7.8	0.0833Hz (1 pulse/ 12 seconds)	CIN
ICM7245F	B	7.8	0.05Hz (1 pulse/ 20 seconds)	CIN
ICM7245U	U	3.9	1Hz	CIN

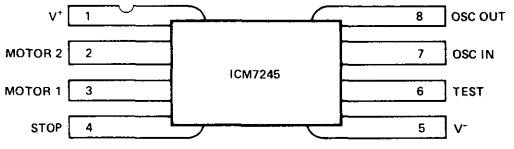
GENERAL DESCRIPTION

The ICM7245 is a very low current, low voltage microcircuit for use in analog watches. It consists of an oscillator, dividers, logic and drivers necessary to provide either bipolar or unipolar drive for minimum-component count watches. The oscillator is extremely stable over wide ranges of voltage and temperature, and thus combines high accuracy with low system power. The ICM7245 is fabricated using Intersil's low threshold metal-gate CMOS process.

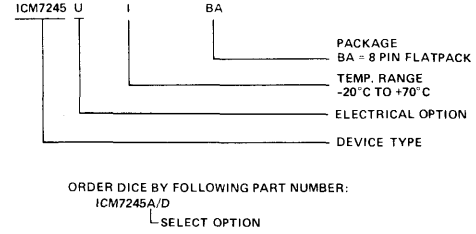
The inverter oscillator contains all components on-chip except for the tuning capacitor and quartz crystal. The binary divider consists of 15 stages, the last 5 of which may be reset. If a reset (stop) occurs during an output pulse, the duration of the pulse is not affected. When the reset is released, the first output occurs approximately 1 second later. For the bipolar version, memory reset logic is included to make sure the first pulse after a "stop" occurs on the opposite output from the one just before the "stop".

The bipolar bridge output consists of two large inverters, normally high. The output ON resistance of the P and N channel devices in series is 200Ω maximum @ 1 mA. In unipolar operation, the output is made up of a single normally high inverter. The ON resistance of the N-channel device is 50Ω maximum @ 3 mA.

PIN CONFIGURATION (OUTLINE DRAWING BA)



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -40°C to +125°C
Operating Temperature ..... -20°C to +70°C
Power Dissipation (Note 1) ..... 25 mW
Supply Voltage ($V^+ - V^-$) ..... 3.0 volts
Lead Temperature (Soldering, 10 sec) ..... 300°C
Input Voltages ..... $V^- - 0.3 < V_{IN} < V^+ + 0.3$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Note 1.: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

TYPICAL OPERATING CHARACTERISTICS

$V^+ - V^- = 1.55V$, $f_{osc} = 32{,}768$ Hz, circuit in Figure 1, $T_A = 25°C$, unless otherwise stated.
Numbers are in absolute values.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	No Load		0.4	0.8	μA
Operating Voltage	$V^+ - V^-$	$0°C < T_A < 50°C$	1.2		1.8	V
Oscillator Transconductance	g_m	Start-up	15			μmho
Oscillator Capacitance	C_{OSC}		16	20	24	pF
STOP Input Current	I_{STOP}				0.3	μA
TEST Input Current	I_{TEST}				10	μA
Oscillator Stability	f_{STAB}	$\Delta(V^+ - V^-) = 0.6V$		0.1		ppm
Supply Current During Stop	I^+	'STOP' Connected to V^+			1.0	μA
Output Saturation Resistance	R_O	Bipolar (N-CH. + P-CH) $I_L = 1$ mA			200	Ω
Output Saturation Resistance P-CH	R_{O-P}	Unipolar $I_L = 3$ mA			200	Ω
Output Saturation Resistance N-CH	R_{O-N}	Unipolar $I_L = 3$ mA			50	Ω

7

TYPICAL WATCH CIRCUIT

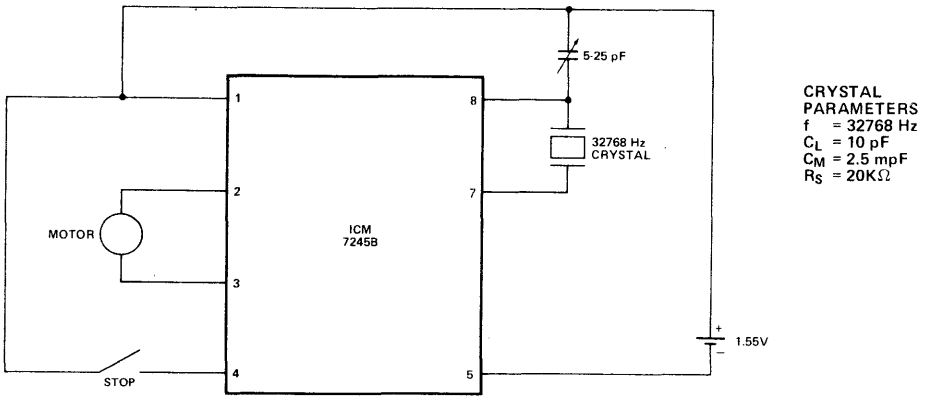
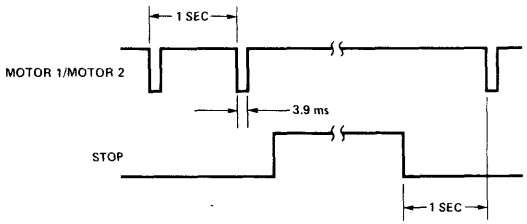


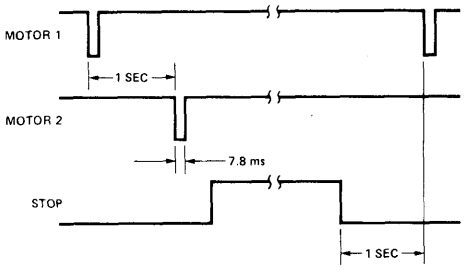
Figure 1.

WAVEFORMS

(ICM7245U)

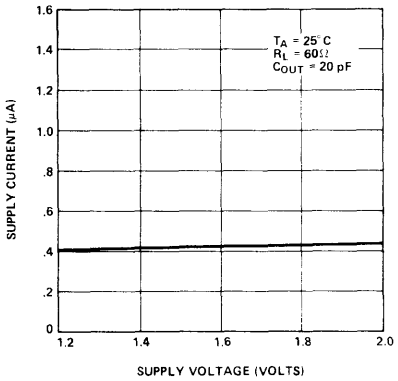


(ICM7245B)

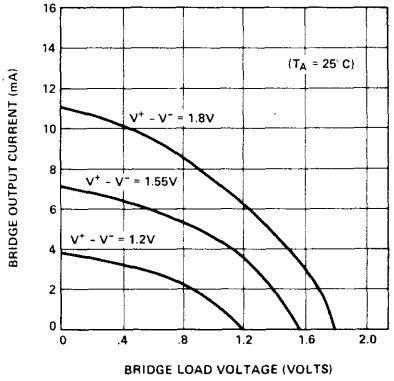


TYPICAL OPERATING CHARACTERISTICS

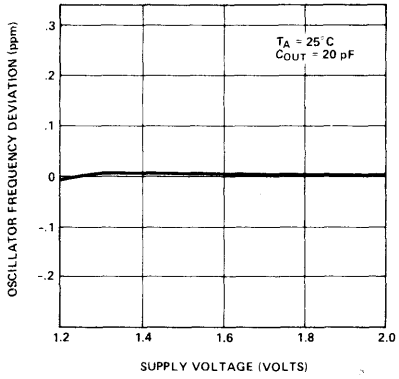
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT AS A FUNCTION OF LOAD VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATION NOTES

OSCILLATOR

The oscillator of the ICM7245 is designed for low frequency operation at very low current from a 1.55 volt supply. The oscillator is of the inverter type, using a non-linear feedback resistor having maximum resistance under start-up conditions. The nominal load capacitance of the crystal should be less than 12 pF, with a preferred range of 7-10 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure start-up and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \; ; \; C_L = \frac{C_{IN}\, C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for start-up

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance
C_m = Motional Capacitance of Crystal

The g_m required for start-up calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT

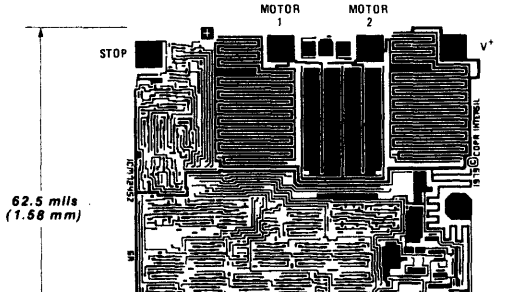
The TEST input, when connected to V^-, causes the ICM7245B/U to speed-up the outputs by 16 times. On long period output versions (12, 20, 60 sec) the speed-up factor will be larger. This allows easy testing of the finished watch module. The pulse width is not affected by the speed-up of the pulse frequency.

CUSTOM VERSIONS

The ICM7245 may be modified with alternative metal masks to provide different number of dividers, various pulse widths, and different output configurations.

In addition, MOS capacitors on-chip up to a total of 50 pF may be connected to either the input and/or the output of the oscillator. Consult your Intersil representative or the factory for further information.

CHIP TOPOGRAPHY



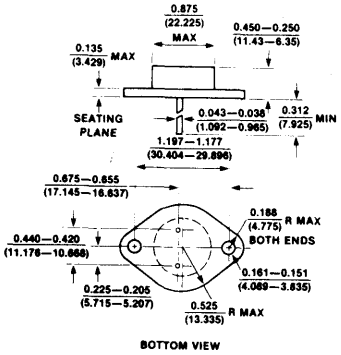
DIE SIZE = 62.5 x 62.5 MILS (1.58 x 1.58 mm)
BOND PAD SIZE = 5x5 MILS (.127 x .127 mm)

Appendix

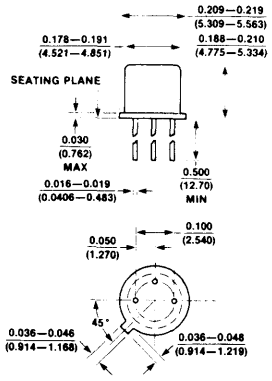
	Page
Packaging Dimensions	B-2
Thermal Resistance	B-11
High Reliability Processing	B-12
Application Note Summary	B-20
Evaluation (EV) Kit Information	B-22
Chip Ordering Information	B-23
Intersil Part Numbering System	B-29
Sales Offices, Distributors, and Representatives	B-31

PACKAGE OUTLINES

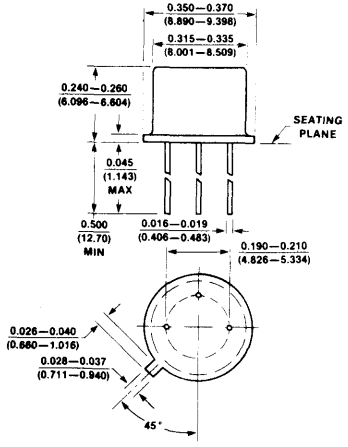
All dimensions given in inches and (millimeters).



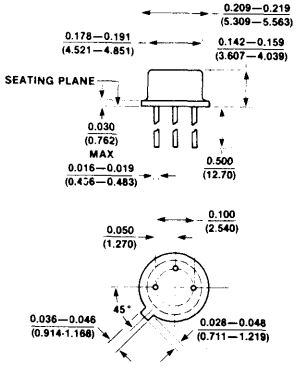
TO-3



TO-18

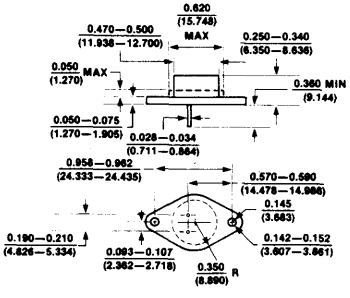


TO-39

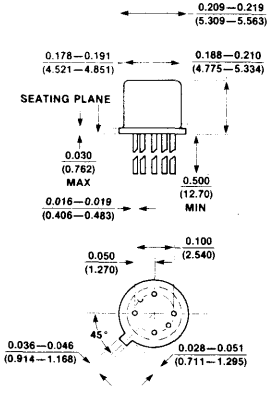


TO-52 (SQ*, SR)

*SQ denotes a two lead package; center lead missing.

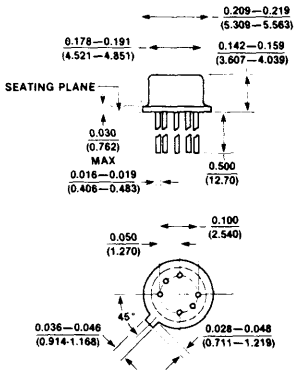


TO-66

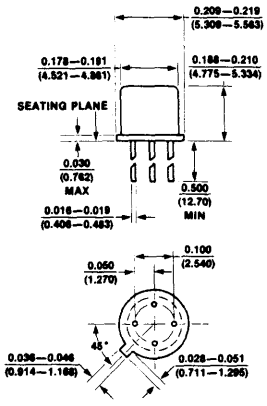


TO-71

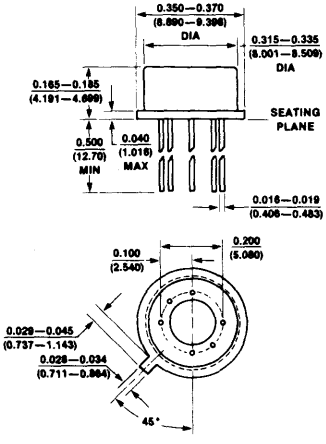
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



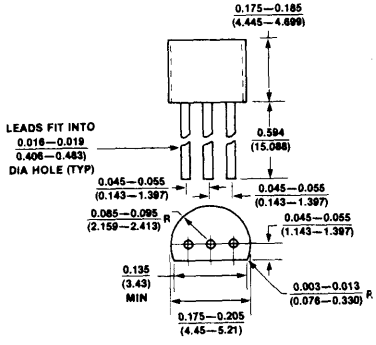
TO-71 LOW PROFILE (UT)



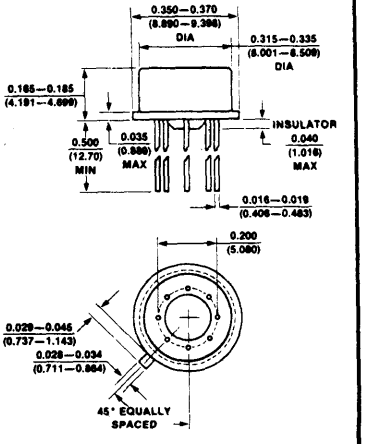
TO-72 (US)



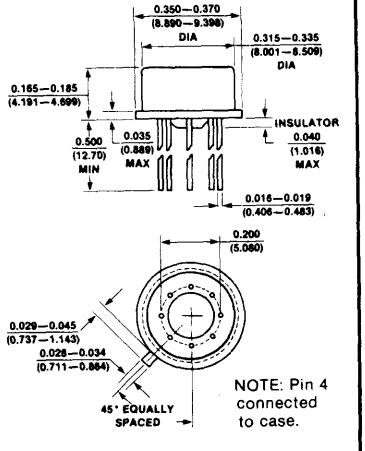
TO-78



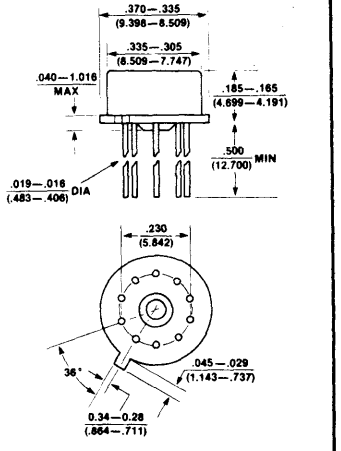
TO-92 (ZR)



TO-99 (TV)



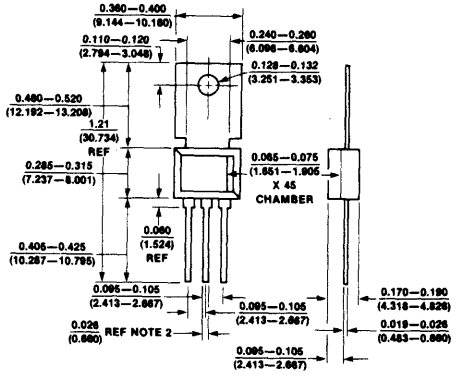
TO-99 (TY)



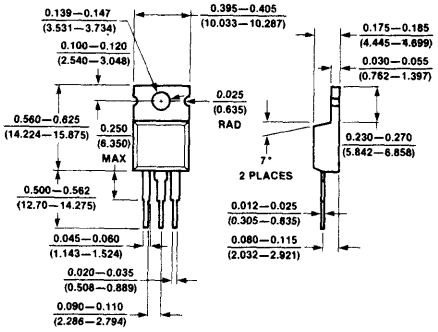
TO-100 (TW, TX)

B

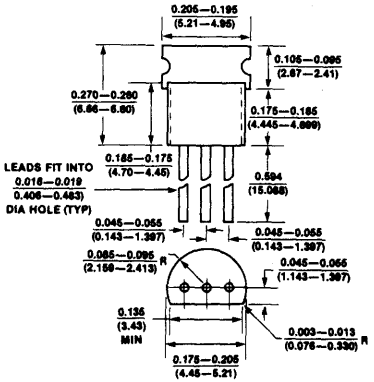
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



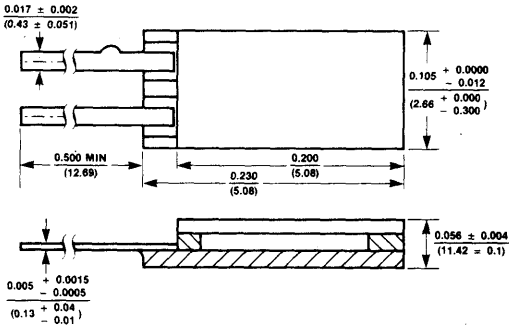
TO-202



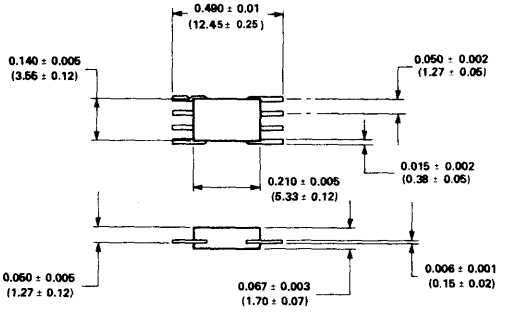
TO-220



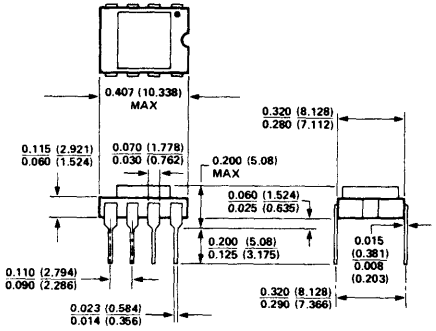
TO-237 (AR)



2 LEAD CERAMIC (DH)

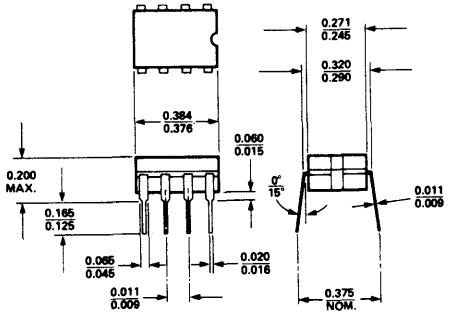


8 LEAD FLATPACK (BA)

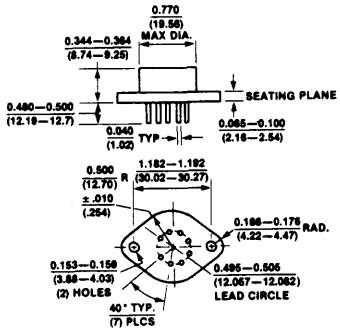


8 LEAD CERAMIC (DA)

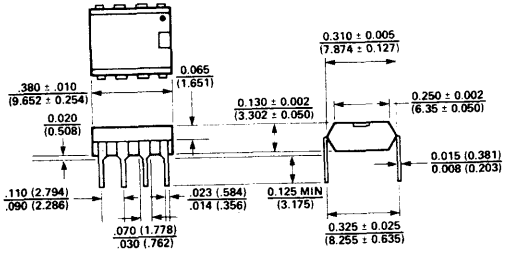
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



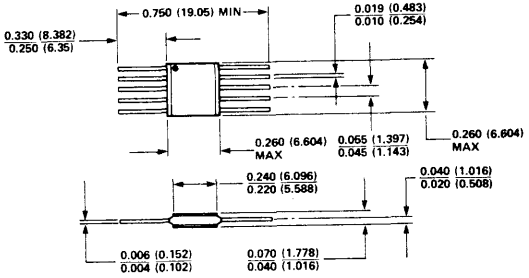
8 LEAD CERDIP (JA)



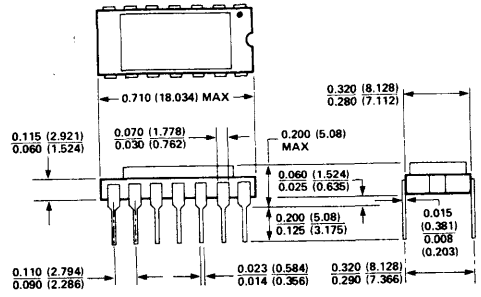
8 LEAD TO-3 CAN (KA)



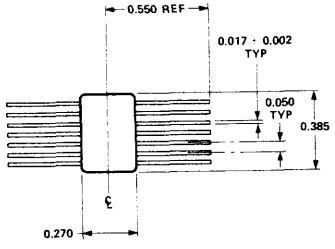
8 LEAD PLASTIC (PA)



10 LEAD FLATPACK (FB)

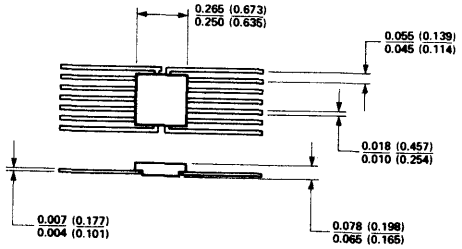


14 LEAD CERAMIC (DD)

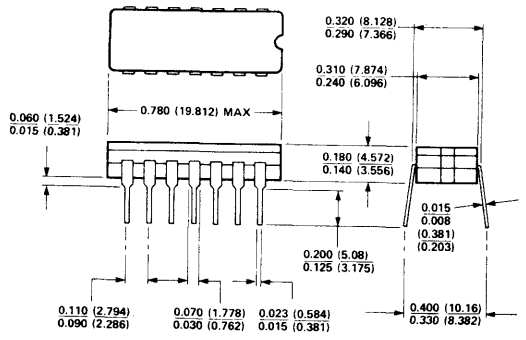


14 LEAD FLATPACK (FD-1)

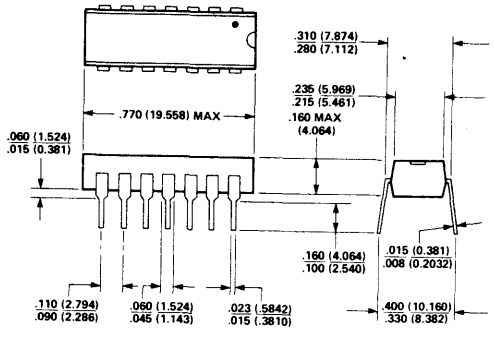
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



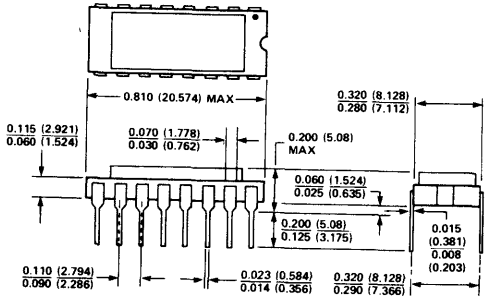
14 LEAD FLATPACK (FD-2)



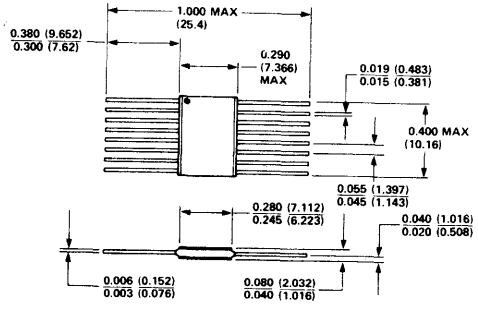
14 LEAD CERDIP (JD)



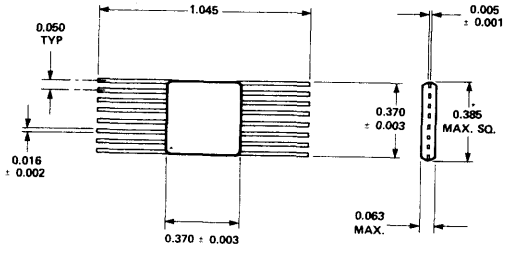
14 LEAD PLASTIC (PD)



16 LEAD CERAMIC (DE)

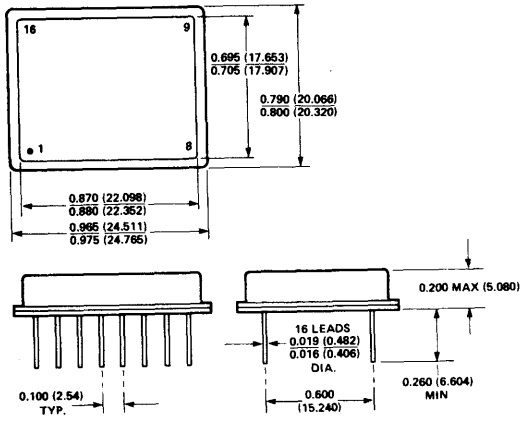


16 LEAD FLATPACK (FE-1)

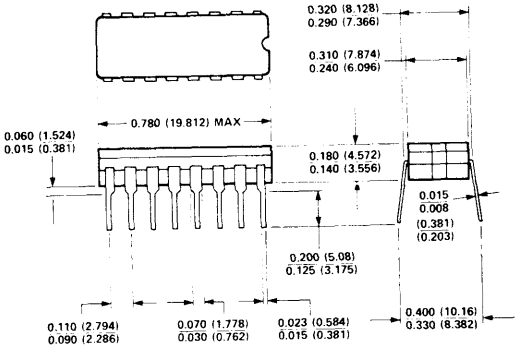


16 LEAD FLATPACK (FE-2)

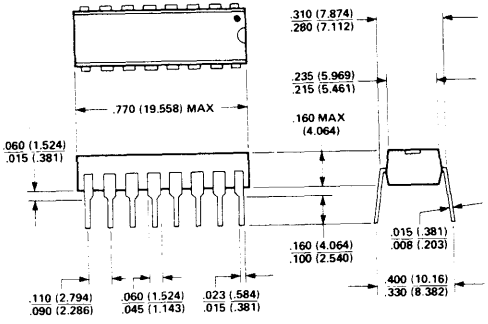
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



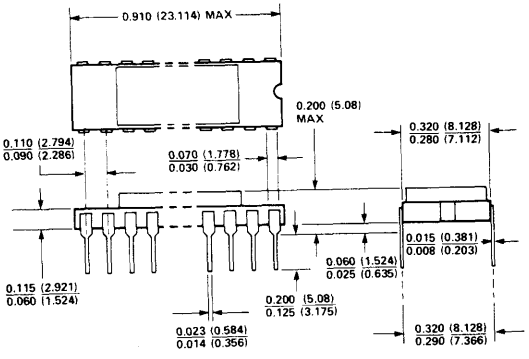
16 LEAD (.6 x .7) CERAMIC (IE)



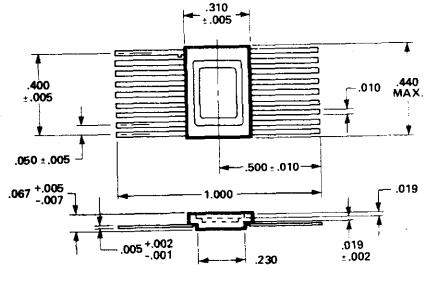
16 LEAD CERDIP (JE)



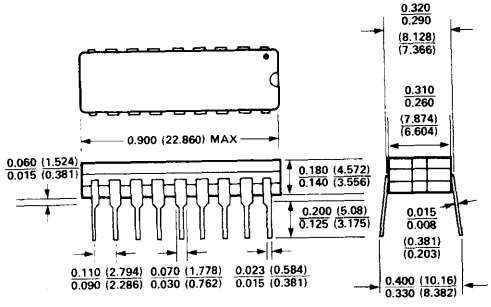
16 LEAD PLASTIC (PE)



18 LEAD CERAMIC (DN)

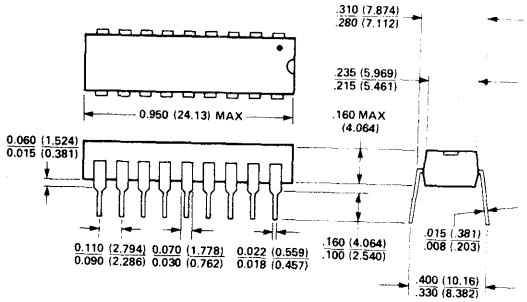


18 LEAD FLATPACK (FN)

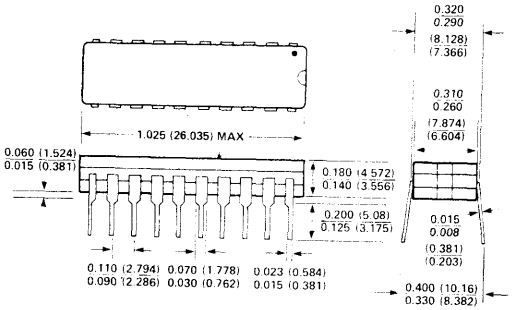


18 LEAD CERDIP (JN)

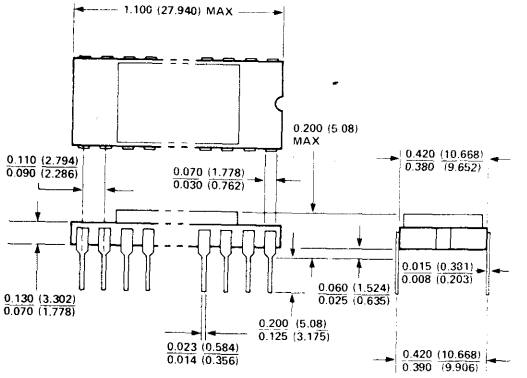
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



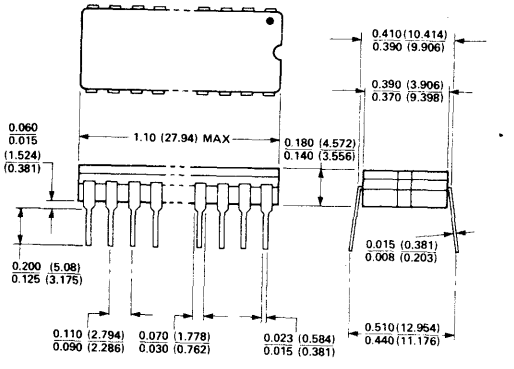
18 LEAD PLASTIC (PN)



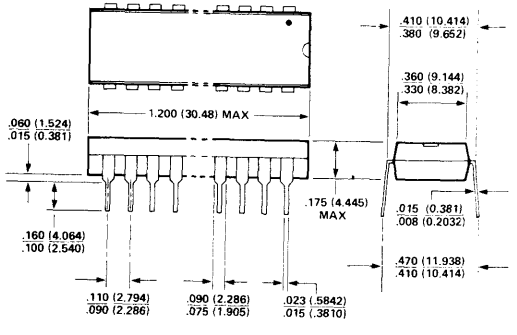
20 LEAD CERDIP (JP)



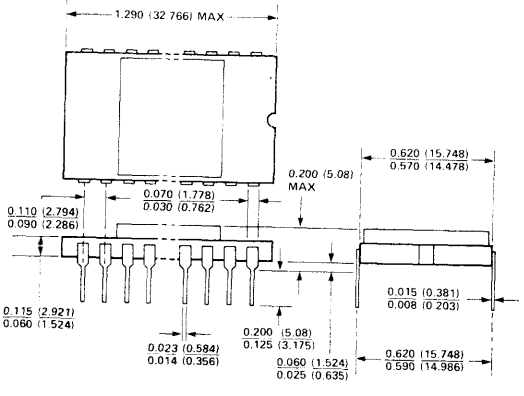
22 LEAD CERAMIC (DF)



22 LEAD CERDIP (JF)

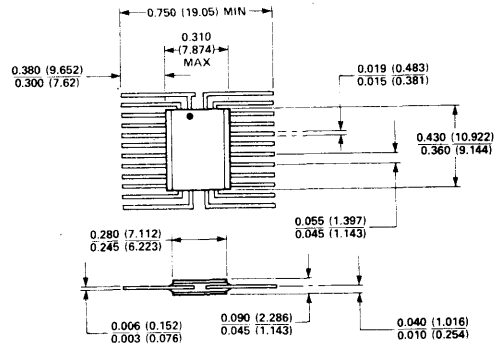


22 LEAD PLASTIC (PF)

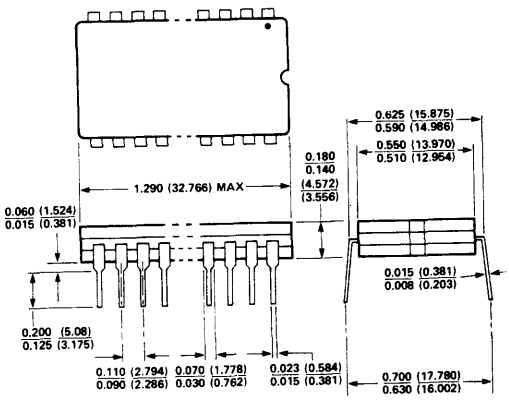


24 LEAD CERAMIC (DG)

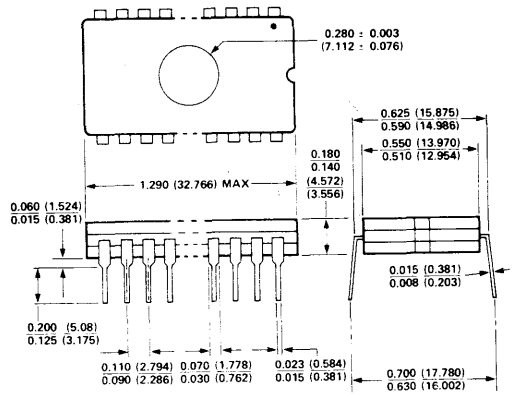
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



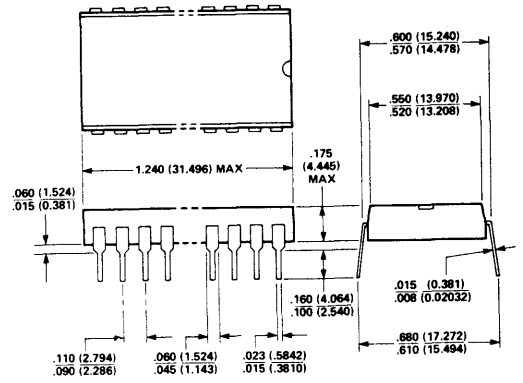
24 LEAD FLATPACK (FG)



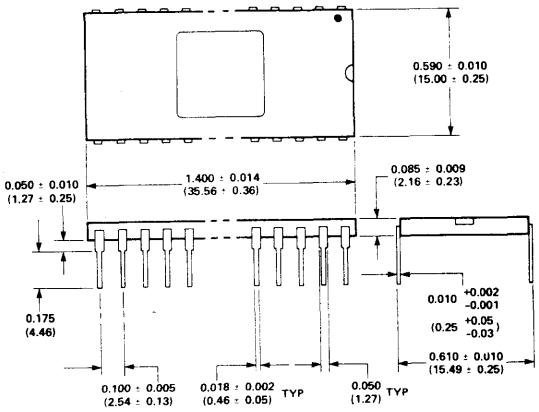
24 LEAD CERDIP (JG)



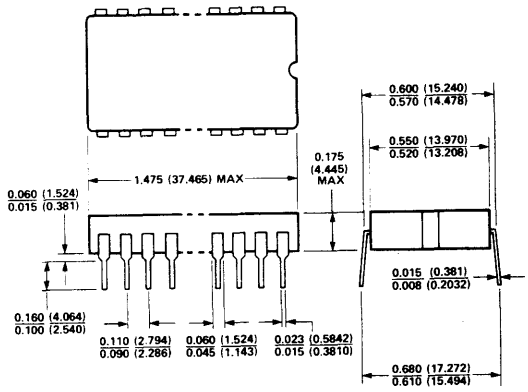
24 LEAD CERDIP WITH WINDOW (JG/W)



24 LEAD PLASTIC (PG)



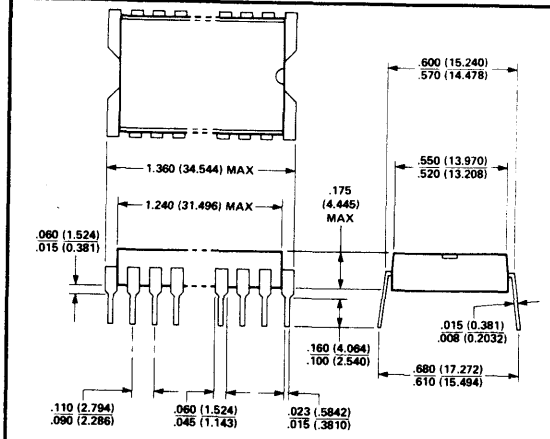
28 LEAD CERAMIC (DI)



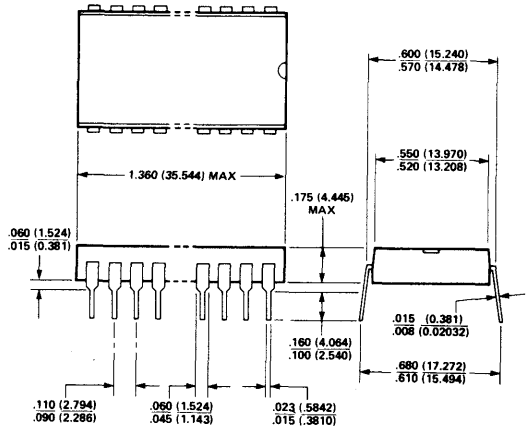
28 LEAD CERDIP (JI)

B

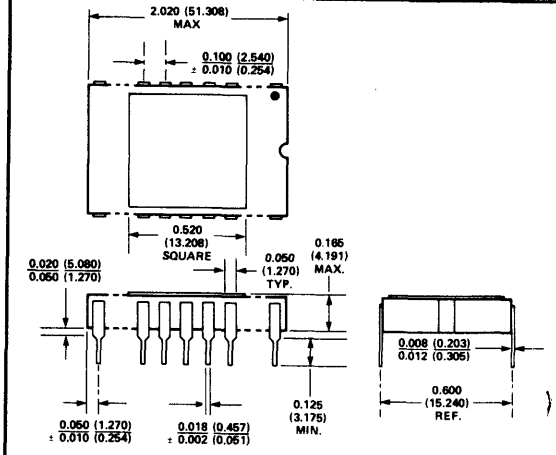
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



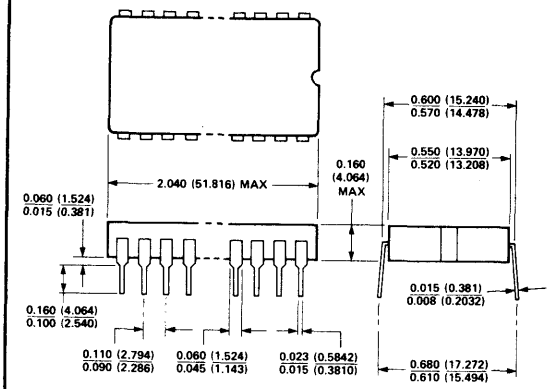
28 LEAD PLASTIC (PI-1)



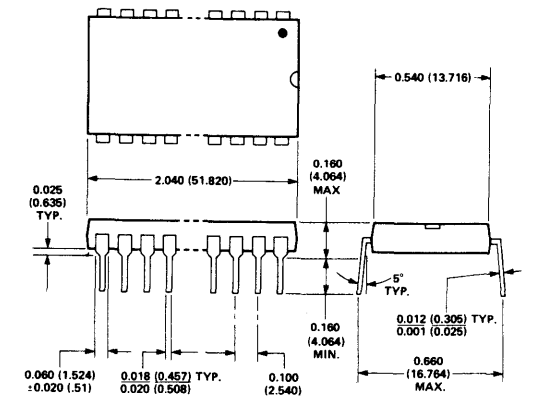
28 LEAD PLASTIC (PI-2)



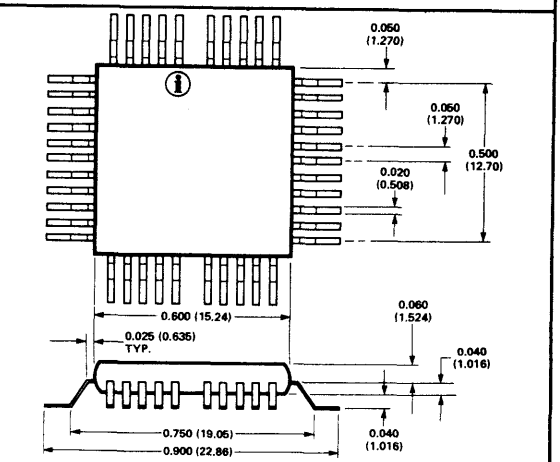
40 LEAD CERAMIC (DL)



40 LEAD CERDIP (JL)



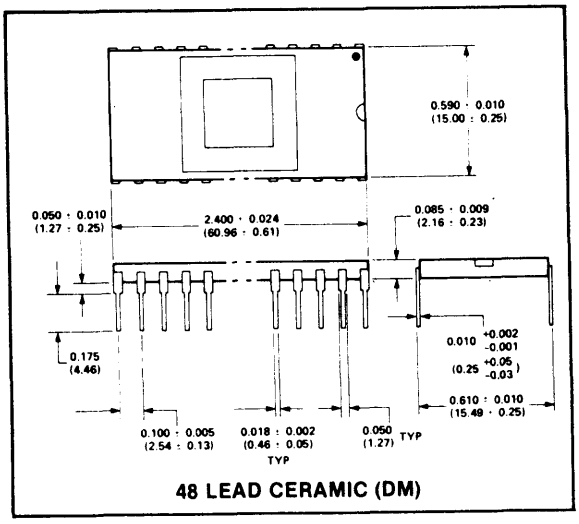
40 LEAD PLASTIC (PL)



42 PIN FLATPACK (BH)

B

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



48 LEAD CERAMIC (DM)

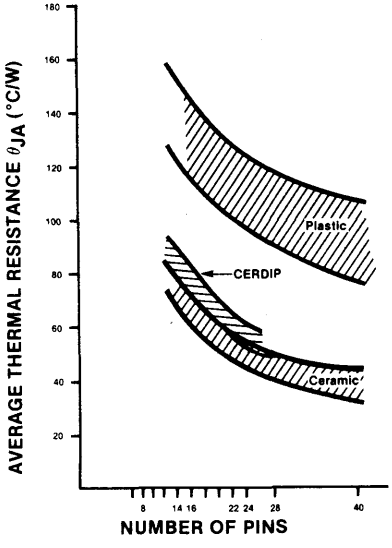
THERMAL RESISTANCE θJA

The junction-to-ambient thermal resistance values of dual in-line packaging systems used in GE Intersil CMOS integrated circuits are graphically illustrated in Figure 1. Each envelope represents the typical range of values for plastic, CERDIP or ceramic sidebraze package types as a function of size. The values were obtained while operating in a "still-air" environment and inserted into low-cost sockets mounted on printed circuit cards.

Thermal resistance is influenced by a number of factors including die size, cavity size and die bonding. In order to present a comprehensive characterization of these variables, a range of values is provided rather than a single point.

Since most CMOS devices dissipate insignificant power, it is not likely that thermal resistance will be a critical design factor. In those situations where high dc currents or high-speed operation is required, the junction temperatures should be estimated through the use of this data and by knowing the actual power being dissipated by the device.

Figure 1 — THERMAL RESISTANCE OF DIP PACKAGES



B

100% INTEGRATED CIRCUIT PROCESSING

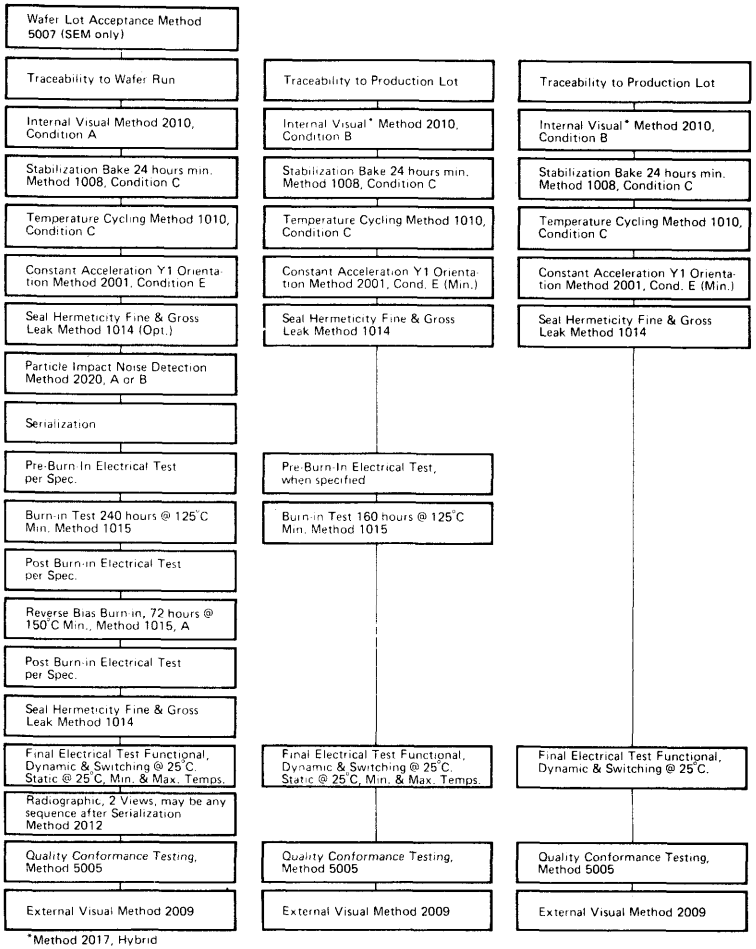
Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

100% DISCRETE DEVICE PROCESSING

Intersil also offers several QPL-approved discrete products carrying the JANTX designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

MIL-STD-883B SCREENING AND QUALITY CONFORMANCE PROGRAMS, METHODS 5004 AND 5005

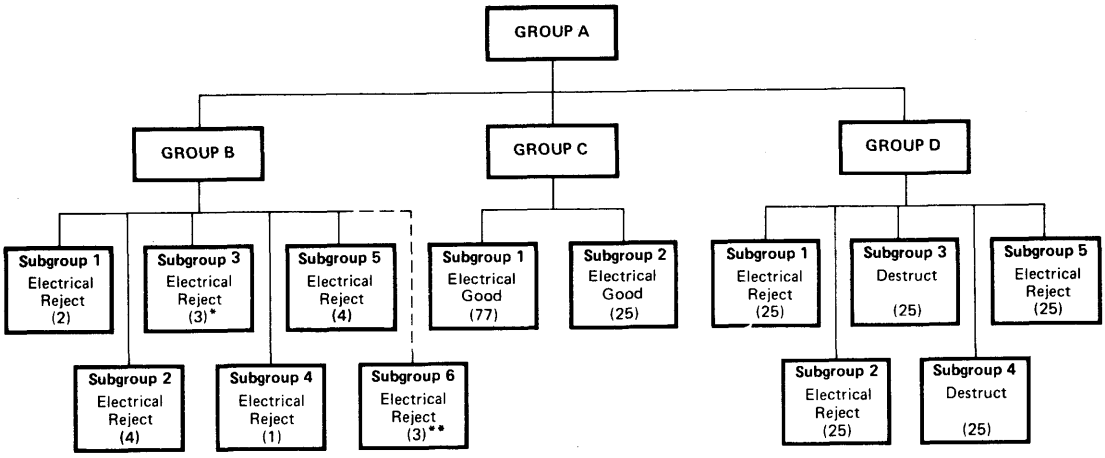
The following flow chart details screening activities as carried out by Intersil for Class S, B and C requirements.



*Method 2017, Hybrid

QUALITY CONFORMANCE INSPECTION, CLASSES B AND C

The following diagram presents quality conformance inspection methods for Classes B and C as performed at Intersil.



*Sample must have had temp/time exposure specified for burn-in. LTPD of 15 applies to number of leads inspected except that in no case shall less than 3 devices be used.

**Required only when a package contains a dessicant.

NOTES:

1. Group A and B inspections are required on individual inspection lots as a condition for acceptance for delivery.
2. Samples shall be randomly selected from the assembled inspection lot in accordance with appendix B of MIL-M-38510. Specified screen requirements of method 5004 are not required to have been completed for Intersil's standard generic data program, but will be performed when required by customer drawing. Where use of electrical rejects is permitted, and unless otherwise specified, they need not have been subjected to the temperature/time exposure of burn-in.
3. Group C (chip-related test) shall be performed periodically at 3 month intervals.
4. Group D (package related tests) shall be performed periodically at 6 month intervals.
5. Where end point measurements are required but no parameters have been identified, the critical final electrical parameters specified for 100% screening shall be used as end point measurements.
6. Subgroups within a group may be performed in any order but individual tests within a subgroup shall be performed in the sequence indicated.

B

QUALITY CONFORMANCE

The following steps are carried out when quality conformance testing is performed on a lot from which samples are taken.

QUALITY CONFORMANCE – CLASSES B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	3-5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	8-10 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Non-destructive, shippable samples (102 units).

NOTE 2: Destructive tests:

Moisture resistance. Subgroup 3 sample size	25 units
Variable-frequency vibration. Subgroup 4 sample size	25 units
Total Destroyed	50 units

QUALIFICATION TESTING

When qualification testing is required, it will be equivalent to quality conformance testing, with the exception that Group A must be read and recorded on all applicable subgroups for the number of electrically-good units which will be required for samples for Groups C and D.

QUALIFICATION TESTING – GROUPS B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	184 (Read & Record)	5	5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	10-12 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Shippable samples.

NOTE 2: 50 destroyed samples, subgroups 3 and 4.

LIMITED USAGE QUALIFICATION

A customer may elect to take advantage of a "Limited Usage" qualification per MIL-M-38510, in order to reduce the number of samples required. The following conditions must be met for eligibility for the "Limited Usage" qualification:

1. A maximum quantity of 500 microcircuits is included in a single order.
2. A maximum quantity of 2000 microcircuits is included in a given equipment-acquisition contract or program.
3. A maximum quantity of 2000 microcircuits is to be procured during a 12-month period for a given circuit type and vendor.

Microcircuits which qualify for limited usage cannot be assigned a JAN part number. Variable data will be taken only when specified in a customer drawing.

LIMITED USAGE QUALIFICATION – CLASS B[1]

	SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related, Non-Destructive)	10 Good Electrical Parts	0	8-10 weeks
Group D (Package Related, Destructive)	25 (15 Good, 10 Electrical Rejects)	0	4 weeks

(1) Mil-M-38510, Paragraph 4.4.4; MIL-STD-883, Method 5005.

GLOSSARY OF MILITARY/AEROSPACE HIGH-REL DEFINITIONS/TERMINOLOGY

ACCELERATED BURN-IN – Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150° C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA – Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE – Technique used to define manufacturing and test processes at time of order placement. Baselining usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs. Other terminology associated with baselining include "Critical Process Changes", "Minor Process Changes", and "Major Process Changes".

BURN-IN – A screening operation. Devices are subjected to high temperature (typically 125° C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

CLASS S, B AND C INTEGRATED CIRCUITS – These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-M-38510. Classes, S, B and C are sometimes referred to as "Levels S, B and C." The Classes cover:

CLASS S – For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.

CLASS B – For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap visual, etc.

CLASS C – For ground support equipment. Contains only environmental screening requirements with pre-cap visual. No burn-in required.

In all classes, LTPD (Lot Tolerance Percent Defective) is the sampling plan measurement criteria.

CORRECTIVE ACTION – Those actions which a given supplier (or user) agrees to perform so that a detected problem does not reoccur.

DESC – Defense Electronic Supply Center, located in Dayton, Ohio. The command includes two major subgroups, with functions as follows:

DESC-ECS – This group performs specification engineering work. After the original specifications are created at RADC, DESC-ECS implements and monitors the specifications. DESC-ECS is the industry's main interface on existing specifications.

DESC-EQM – The group which supervises supplier certifications and qualifications per MIL-M-38510. The group to which the industry submits applications when desiring to have devices qualified (QPL'd) on an existing JAN slash sheet. DESC-EQM surveys supplier facilities and grants line certification as various requirements are met. Also reviews manufacturer's qualification test data and issues JAN QPL's accordingly.

DESC-EQT – Same as EQM, except handles transistors per MIL-S-19500.

DESC LINE CERTIFICATION – The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

DIE SHEAR TESTS – A sample test. Mounted chips are exercised to destruction. Degree of die adherence to lead frame is observed. Corrective action taken if required.

DPA – Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

GENERIC DATA – Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order.

GROUP A – Sample electrical tests which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

GROUP B – A collection of package-related environmental and "wear-and-tear" tests. Defined in Test Method 5005 for integrated circuits. For Class S screening, additional life tests are required, and are performed on every lot per MIL-M-38510. For diodes and transistors, Group B consists of both environmental and life tests, as defined in MIL-S-19500.

GROUP C – For Class B and C integrated circuits, only Group C includes life testing and temperature cycling/constant acceleration die-related sample tests. Defined in Test Method 5005 and performed every three months per MIL-M-38510.

GROUP D – A collection of additional environmental package-related sample tests as defined in Test Method 5005. Performed every six months per MIL-M-38510. For classes S, B, & C.

JAN – "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX – A JAN-qualified diode or transistor which has been subjected to additional screening (burn-in) tests. MIL-S-19500 only.

JAN TXV – A JAN-qualified diode or transistor which, in additional to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits. MIL-S-19500 only.

"M38510" CIRCUITS – Until a recent revision to MIL-M-38510, it was a common practice for users and suppliers alike to specify or offer integrated circuits marked "M38510/XXX" without a J or JAN prefix. This part numbering system indicated a device which was "near-JAN", "quasi-JAN" or "non-JAN". The practice tended to cause confusion between these devices and parts in full conformance to JAN levels. MIL-M-38510 now prohibits such marking with the exception of two special instances:

- When JAN QPL supplier for a given product does not exist, the government will permit "M38510/XXX" marking. While a customer may specify such marking, the supplier must furnish the government with evidence that the parts meet all applicable requirements.
- For certain parts destined for use in some programs, "M38510/XXX" marking is permissible, but orders for such parts must be accompanied by appropriate DESC certification letter.

M38510/XXX – Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-M-38510 – The general military specification for integrated circuits.

MIL-S-19500 – The general military specifications for diodes and transistors.

MIL-S-19500/XXX – Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 – Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

MIL-STD-883 – Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, , hermeticity, storage life, etc.

NPFC – Naval Publications and Forms Center, Philadelphia. Printing and distribution source for military specifications.

NON-STANDARD PARTS – In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL – Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

OPERATING LIFE TEST – Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA – Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA – Percent Defective Allowable. Criteria sometimes applied to burn-in screening. A 10% PDA (the most common type) means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

PDS – Parameter Drift Screening. Measures the changes (Δs) in electrical parameters through burn-in. Common for Class S devices.

PIND – Particle Impact Noise Detection. This is an audio screening test to locate and elminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY – The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL – A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY – Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABLIITY – Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours at a 60% confidence level at 25°C") or MTBF (mean time between failure in hours). MTBF is the reciprocal of Failure Rate.

QPL – Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist for MIL-M-38510:

PART II QPL – This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided after 90 days whenever any one supplier is granted a PART I QPL.

PART I QPL – A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QPLTT – Qualified Product List Throughput Time. That period which required to obtain device qualification. QPLTT is a function of (1) whether a JAN slash sheet exists; (2) whether a competitor already holds a Part I QPL; and (3) whether the applicant's production line is certified by DESC.

Following is a worst-case example, where a JAN slash sheet does not exist and government line certification has not been granted. QPLTT will be approximately 39.5 months, if the JAN slash sheet already exists, QPLTT will be cut to about 10.5 months. If the applicant already has line certification, QPLTT will be about 2 months to obtain Part II status.

Total time required to obtain a Part I QPL adds about 7 months to QPLTT; in a worst-case example, about 46 months will be required.

QUALIFYING ACTIVITY – Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING – Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D. For diodes and transistors, this usually means testing to Groups A, B and C.

QUALITY CONFORMANCE TESTING – These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

RADC – Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA – Same as variable data.

REWORK PROVISION – For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), lead straightening or bending, re-marking, and cleaning.

S & V – Survivability and Vulnerability. Pertains to the ability of a device to resist radiation dosage.

SCREENING – Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc. For integrated circuits, Test Method 5004 defines screening flow.

SEM INSPECTION – Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects. A common inspection for Class S devices.

SERIALIZATION – The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs – Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

SOURCE INSPECTION – Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can occur at one or more of the following points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection. Simple and inexpensive; little delivery impact.
- Throughout. Very expensive and time-consuming.

STANDARD PARTS – In government terminology, JAN parts.

TRACEABILITY – A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA – Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.

WIRE PULL TESTS – Bond wire pull tests will be specified in two modes:

DESTRUCTIVE WIRE PULL – Generally performed periodically in assembly on a sample basis. Wires are pulled to destruction and the break point force is recorded. Corrective action is taken as required.

NON-DESTRUCTIVE WIRE PULL – Option for class 5 microcircuits, wire bonds are pulled to a max of 70% of the preseal minimum bond strengths for the applicable material on 100% of the lot.

Ordering Information for MIL-STD-883B Processed Devices

The following Intersil devices are available as a standard with Class B screening per method 5004 of MIL-STD-883B. To order, add 833B after the device number as shown below.

Part Number	Part Number	Part Number	Part Number
AD532SD/883B	DG112AL/883B	DG162AK/883B	DGM185AL/883B
AD532SH/883B	DG116AK/883B	DG162AL/883B	DGM187AA/883B
AD550M-12/883B	DG116AL/883B	DG163AK/883B	DGM187AK/883B
AD550S/883B	DG118AK/883B	DG163AL/883B	DGM187AL/883B
AD550T/883B	DG118AL/883B	DG164AK/883B	DGM188AA/883B
AD550U/883B	DG120AK/883B	DG164AL/883B	DGM188AK/883B
AD590JH/883B	DG120AL/883B	DG180AA/883B	DGM188AL/883B
AD590KH/883B	DG121AK/883B	DG180AK/883B	DGM190AK/883B
AD590LH/883B	DG123AK/883B	DG180AL/883B	DGM190AL/883B
AD590MH/883B	DG123AL/883B	DG181AA/883B	DGM191AK/883B
AD7520SD/883B	DG125AK/883B	DG181AK/883B	DGM191AL/883B
AD7520TD/883B	DG125AL/883B	DG181AL/883B	
AD7520UD/883B	DG126AK/883B	DG182AA/883B	G115AK/883B
AD7521SD/883B	DG126AL/883B	DG182AK/883B	G115AL/883B
AD7521TD/883B	DG129AK/883B	DG182AL/883B	G116AK/883B
AD7521UD/883B	DG129AL/883B	DG183AK/883B	G116AL/883B
AD7523SD/883B	DG133AK/883B	DG183AL/883B	G117AK/883B
AD7523TD/883B	DG133AL/883B	DG184AK/883B	G117AL/883B
AD7523UD/883B	DG134AK/883B	DG184AL/883B	G118AK/883B
AD7533SD/883B	DG134AL/883B	DG185AK/883B	G118AL/883B
AD7533TD/883B	DG139AK/883B	DG185AL/883B	G119AK/883B
AD7533UD/883B	DG139AL/883B	DG186AA/883B	G119AL/883B
AD7541SD/883B	DG140AK/883B	DG186AK/883B	G123AK/883B
AD7541TD/883B	DG140AL/883B	DG186AL/883B	G123AL/883B
ADC0801LD/883B	DG141AK/883B	DG187AA/883B	G125AK/883B
ADC0802LD/883B	DG141AL/883B	DG187AK/883B	G125AL/883B
ADC0803LD/883B	DG142AK/883B	DG187AL/883B	G126AK/883B
	DG142AL/883B	DG188AA/883B	G126AL/883B
D112AK/883B	DG143AK/883B	DG188AK/883B	G127AK/883B
D112AL/883B	DG143AL/883B	DG188AL/883B	G127AL/883B
D113AK/883B	DG144AK/883B	DG189AK/883B	G128AK/883B
D113AL/883B	DG144AL/883B	DG189AL/883B	G128AL/883B
D120AK/883B	DG145AK/883B	DG190AK/883B	G129AK/883B
D120AL/883B	DG145AL/883B	DG190AL/883B	G129AL/883B
D121AK/883B	DG146AK/883B	DG191AK/883B	G130AK/883B
D121AL/883B	DG146AL/883B	DG191AL/883B	G130AL/883B
D123AK/883B	DG151AK/883B	DG200AA/883B	G131AK/883B
D123AL/883B	DG151AL/883B	DG200AK/883B	G131AL/883B
D125AK/883B	DG152AK/883B	DG200AL/883B	G132AK/883B
D125AL/883B	DG152AL/883B	DG201AK/883B	G132AL/883B
D129AK/883B	DG153AK/883B	DGM182AA/883B	
D129AL/883B	DG153AL/883B	DGM182AK/883B	ICL7109MDL/883B
	DG154AK/883B	DGM182AL/883B	ICL7650MJD/883B
DG111AK/883B	DG154AL/883B	DGM184AK/883B	ICL7650MTV/883B
DG111AL/883B	DG161AK/883B	DGM184AL/883B	ICL7660MTV/883B
DG112AK/883B	DG161AL/883B	DGM185AK/883B	ICL8007AMTV/883B

Part Number
ICL8007MTY/883B
ICL8013AMTZ/883B
ICL8013BMTZ/883B
ICL8013CMTZ/883B
ICL8018AMJD/883B
ICL8018MJD/883B
ICL8019AMJD/883B
ICL8019MJD/883B
ICL8020AMJD/883B
ICL8020MJD/883B
ICL8021MTY/883B
ICL8022MFD/883B
ICL8022MJD/883B
ICL8023MJE/883B
ICL8038AMJD/883B
ICL8038BMJD/883B
ICL8049BCJE/883B
ICL8069ACSQ/883B
ICL8069BCSQ/883B
ICL8069CMSQ/883B
ICL8069DMSQ/883B
ICL8211MTY/883B
ICL8212MTY/883B
ICM7555MTV/883B
ICM7556MJD/883B
IH181MFD/883B
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IH182MFD/883B
IH182MJD/883B
IH182MTW/883B
IH184MFD/883B
IH184MJE/883B
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IH185MJE/883B
IH187MFD/883B
IH187MJD/883B
IH187MTW/883B
IH188MFD/883B
IH188MJD/883B
IH200AK/883B
IH200AL/883B
IH200MJE/883B
IH201MJE/883B
IH202MJE/883B
IH5003MFD/883B
IH5003MJD/883B
IH5004MFD/883B
IH5004MJD/883B
IH5005MFD/883B
IH5005MJD/883B
IH5006MFD/883B
IH5006MJD/883B
IH5007MFD/883B
IH5007MJD/883B

Part Number
IH5009MJD/883B
IH5010MJD/883B
IH5011MJE/883B
IH5012MJE/883B
IH5013MJD/883B
IH5014MJD/883B
IH5015MJE/883B
IH5016MJE/883B
IH5017MJD/883B
IH5018MJD/883B
IH5019MJE/883B
IH5020MJE/883B
IH5021MJD/883B
IH5022MJD/883B
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IH5024MJE/883B
IH5025MJD/883B
IH5026MJD/883B
IH5027MJE/883B
IH5028MJE/883B
IH5029MJD/883B
IH5030MJD/883B
IH5031MJE/883B
IH188MTW/883B
IH190MFD/883B
IH190MJE/883B
IH191MFD/883B
IH191MJE/883B
IH200AA/883B
IH5032MJE/883B
IH5033MJD/883B
IH5034MJD/883B
IH5035MJE/883B
IH5036MJE/883B
IH5037MJD/883B
IH5038MJD/883B
IH5040MFD/883B
IH5040MJE/883B
IH5041MFD/883B
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IH5045MJE/883B
IH5046MFD/883B
IH5046MJE/883B
IH5047MFD/883B
IH5047MJE/883B
IH5048MFD/883B
IH5048MJE/883B

Part Number
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IH5053MJE/883B
IH5108MJE/883B
IH5140MFD/883B
IH5140MJE/883B
IH5141MFD/883B
IH5141MJE/883B
IH5141MTW/883B
IH5142MFD/883B
IH5142MJE/883B
IH5142MTW/883B
IH5143MFD/883B
IH5143MJE/883B
IH5144MFD/883B
IH5144MJE/883B
IH5144MTW/883B
IH5145MFD/883B
IH5145MJE/883B
IH5148MFD/883B
IH5148MJE/883B
IH5148MTW/883B
IH5149MFD/883B
IH5149MJE/883B
IH5150MFD/883B
IH5150MJE/883B
IH5150MTW/883B
IH5151MFD/883B
IH5151MJE/883B
IH5200MFD/883B
IH5200MJD/883B
IH5200MTW/883B
IH5201MJE/883B
IH5208MJE/883B
IH6108MJE/883B
IH6116MJI/883B
IH6201MJE/883B
IH6208MJE/883B
IH6216MJI/883B
IM5603AMFE/883B
IM5624MFE/883B
IM6100-1MJL/883B
IM6100AMJL/883B
IM6101-1MJL/883B
IM6101AMJL/883B
IM6102-1MJL/883B
IM6102AMJL/883B
IM6103-1MJL/883B
IM6103AMJL/883B

Part Number
IM6402-1MJL/883B
IM6402AMJL/883B
IM6403-1MJL/883B
IM6403AMJL/883B
IM6512AMFN/883B
IM6512AMJN/883B
IM6512MFN/883B
IM6512MJN/883B
IM65X08AMFE/883B
IM65X08AMJE/883B
IM65X08MFE/883B
IM65X08MJE/883B
IM65X18AMFN/883B
IM65X18AMJN/883B
IM65X18MFN/883B
IM65X18MJN/883B
IM65X51AMJF/883B
IM65X51MJF/883B
IM65X61AMFN/883B
IM65X61AMJN/883B
IM65X61MFN/883B
IM65X61MJN/883B
IM6653AMJG/883B
IM6653MJG/883B
IM6654AMJG/883B
IM6654MJG/883B
LM100H/883B
LM101AF/883B
LM101AH/883B
LM101H/883B
LM105H/883B
LM107F/883B
LM107H/883B
LM107J-14/883B
LM108AH/883B
LM108AJ/883B
LM108H/883B
LM110F/883B
LM110H/883B
LM111H/883B
LM111J/883B
LM4250H/883B
OP-05AJ/883B
OP-05AY/883B
OP-05AZ/883B
OP-05J/883B
OP-05Y/883B
OP-05Z/883B
OP-07AJ/883B
OP-07AY/883B
OP-07AZ/883B
OP-07J/883B
OP-07Y/883B
OP-07Z/883B
μA723HM/883B

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APPLICATION NOTE SUMMARY

The following are brief descriptions of current Intersil Application notes.

A003 **UNDERSTANDING AND APPLYING THE ANALOG SWITCH**

Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET + driver), J-FET "virtual ground" and J-FET "positive signal" types. Application information included.

A004 **IH5009 LOW COST ANALOG SWITCH SERIES**

Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.

A005 **THE 8007–A HIGH PERFORMANCE FET INPUT OP AMP**

Compares the 8007 with the 741, which is pin compatible and suggests applications such as log-antilog amplifier, sample and hold circuit, photometer, peak detector, etc.

A007 **USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER**

Describes in detail the operation of the 8048 logarithmetic amplifier, and its counterpart, the 8049 antilog amp.

A011 **A PRECISION FOUR QUADRANT MULTIPLIER–THE 8013**

Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.

A013 **EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038**

This note includes 17 of the most asked questions regarding the use of the 8038.

A015 **DESIGN FOR A BATTERY OPERATED FREQUENCY COUNTER**

Describes a low cost battery operated frequency/period counter using the 7207A and 7208. Includes specifications, schematics, PC layout, etc.

A016 **SELECTING A/D CONVERTERS**

Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.

A017 **THE INTEGRATING A/D CONVERTER**

Provides an explanation of integrating A/D converters, together with a detailed error analysis.

A018 **DO'S AND DONT'S OF APPLYING A/D CONVERTERS**

An analysis of proper design techniques using D/A converters.

A019 **4½ DIGIT PANEL METER DEMONSTRATION/INSTRUMENTATION BOARDS**

Describes two typical PC board layouts using the 8052A/7103A 4½ digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.

A020 **A COOKBOOK APPROACH TO HIGH SPEED DATA ACQUISITION AND MICROPROCESSOR INTERFACING**

Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.

A021 **POWER D/A CONVERTERS USING THE ICH 8510**

Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc. Also see A026.

A022 **A NEW J-FET STRUCTURE–THE VARAFET**

Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built-in.

A023 **LOW COST DIGITAL PANEL METER DESIGNS**

Provides a detailed explanation of the 7106 and 7107 3½ digit panel meter IC's, and describes two of the evaluation kits available from Intersil.

A026 **DC SERVO MOTOR SYSTEMS USING THE ICH8510**

This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.

A027 **POWER SUPPLY DESIGN USING THE ICL-8211 AND ICL8212**

Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.

A028 **BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR**

This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a ±4½ digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.

A029 **POWER OP AMP HEAT SINK KIT**

Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.

A030 **THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS**

Describes in detail the operation of the 7104. Includes in digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.

A031 **COIL DRIVE ALARM DESIGN CONSIDERATIONS**

Explains the procedure used when using watch circuits to drive piezoelectric transducers.

A032 **UNDERSTANDING THE AUTO-ZERO AND COMMON MODE PERFORMANCE OF THE ICL7106/7107/7109 FAMILY**

Explains in detail the operation of the ICL7106/7/9 family of A/D Converters.

A046 **BUILDING A BATTERY OPERATED AUTO RANGING DVM WITH THE ICL7106**

Explains principles of auto ranging, problems and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.

A047 **GAMES PEOPLE PLAY WITH A/D CONVERTERS**

Describes 25 different integrating A/D converter applications. Input circuits, conversion modifications, display and microprocessor interfaces are shown in detail.

A050 **USING THE IT500 FAMILY TO IMPROVE THE INPUT BIAS CURRENT OF BIFET OP AMPS**

A brief description of a preamplifier for BIFET OP AMPS.

A051 **PRINCIPLES AND APPLICATIONS OF THE ICL7660 CMOS VOLTAGE CONVERTER**

Describes internal operation of the ICL7660. Includes a wide range of possible applications.

A052 **TIPS FOR USING SINGLE CHIP 3½ DIGIT A/D CONVERTERS**

Answers frequently asked questions regarding the operation of 3½ digit single chip A/D converters. Included are sections on power supplies, displays, timing and component selection.

A053 **THE ICL7650 A NEW ERA IN GLITCH-FREE CHOPPER STABILIZER AMPLIFIERS**

A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.

A054 **DISPLAY DRIVER FAMILY COMBINES CONVENIENCE OF USE WITH MICROPROCESSOR INTERFACABILITY**

Compares and describes the various display drivers. Includes design examples for 7 segment, Alpha-numeric, and bargraph systems.

M011 **AVOIDING PROBLEMS IN CMOS MEMORY OPERATION**

Discusses input overvoltage and SCR latch-up and the multiple address access problem in CMOS RAMs.

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EVALUATION KITS AVAILABLE FROM INTERSIL

PRODUCT DESCRIPTION	PART NUMBER	CONTENTS
3½ Digit LCD Panel Meter Kit	ICL7106EV/KIT	ICL7106 + PC Card + All Passive Components
3½ Digit LED Panel Meter Kit	ICL7107EV/KIT	ICL7107 + PC Card + All Passive Components
3½ Digit Low Power LCD Panel Meter Kit	ICL7136EV/KIT	ICL7136 + PC Card + All Passive Components
4½ Digit A/D Converter Kit	ICL7135EV/KIT	ICL7135 + ICL7660 + ICL8069 + PC Card + Active, Passive Components
4½ Digit LCD Display Driver Kit	ICM7211EV/KIT	ICM7211 + 4½ Digit LCD Display + PC Card + Active, Passive Components
4½ Digit LED Display Driver Kit	ICM7212EV/KIT	ICM7212 + 4½ Digit LED Display + PC Card + Active, Passive Components
4½ Digit VF Display Driver Kit	ICM7235EV/KIT	ICM7235 + 4½ Digit VF Display + PC Card + Active, Passive Components
8 Character Multiplexed LCD Display Driver Kit	ICM7233 EV/KIT	2 of ICM7233 + PC Card + 8 Character Triplexed LCD Display
8 Character Multiplexed LED Display Driver Kit	ICM7243BEV/KIT	ICM7243B + PC Card + 8 Character LED
4½ Digit LCD Display Counter Kit	ICL7224EV/KIT	ICM7224 + ICM7207A + 5.24288 MHz Crystal + 4½ Digit LCD Display + PC Card + Passive Components
4½ Digit LED Display Counter Kit	ICM7225EV/KIT	ICM7225 + ICM7207A + 5.24288 MHz Crystal + 4½ Digit LED Display + PC Card + Passive Components
4½ Digit VF Display Counter Kit	ICM7236EV/KIT	ICM7236 + ICM7207A + 5.24288 MHz Crystal + 4½ Digit VF Display + PC Card + Passive Components
8 Digit Stopwatches		
Hour Decade Timer	ICM7045AEV/KIT H	ICM7045A + 3.640889 MHz Crystal
Minute Decade Timer	ICM7045AEV/KIT M	ICM7045A + 2.184533 MHz Crystal
4 Function/24 Hour Clock	ICM7045EV/KIT	ICM7045 + 6.5536 MHz Crystal
6 Digit Stopwatches		
4 Function	ICM7215EV/KIT	ICM7215 + 3.2768 MHz Crystal
Touch Tone Encoder		
One contact per key	ICM7206EV/KIT	ICM7206 + 3.579545 MHz Crystal
Two contacts per key, common to positive supply	ICM7206AEV/KIT	ICM7206A + 3.579545 MHz Crystal
Common to negative supply, oscillator enabled when key depressed	ICM7206BEV/KIT	ICM7206B + 3.579545 MHz Crystal
8 Digit Frequency/Period Counter		
5 Function	ICM7226AEV/KIT	ICM7226A + 10 MHz Crystal + PC Card + LEDs + All Passive Components
Oscillator Controller		
For application as freq. counter with ICM7208	ICM7207EV/KIT	ICM7207 + 6.5536 MHz Crystal
	ICM7207AEV/KIT	ICM7207A + 5.24288 MHz Crystal
Power Amplifier Kits	ICH8510IEV/KIT	ICH8510I + Socket + Heat Sink
	ICH8510MEV/KIT	ICH8510M + Socket + Heat Sink
	ICH8520IEV/KIT	ICH8520I + Socket + Heat Sink
	ICH8520MEV/KIT	ICH8520M + Socket + Heat Sink
	ICH8530IEV/KIT	ICH8530I + Socket + Heat Sink
	ICH8530MEV/KIT	ICH8530M + Socket + Heat Sink

B

DIE & WAFER ORDERING INFORMATION

FET, MOSFET, AND DUAL TRANSISTOR CHIPS

INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need, Intersil offers a full line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is due to the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy for dice as it can for packaged devices. This is due to equipment limitations and handling problems.

PURCHASE OPTIONS

Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, visually inspected and scribed only.
- Wafers which have been electrically probed, inked, and visually inspected only.

GENERAL PHYSICAL INFORMATION

- Consult individual product information sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.
- Dice are 100% tested to electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

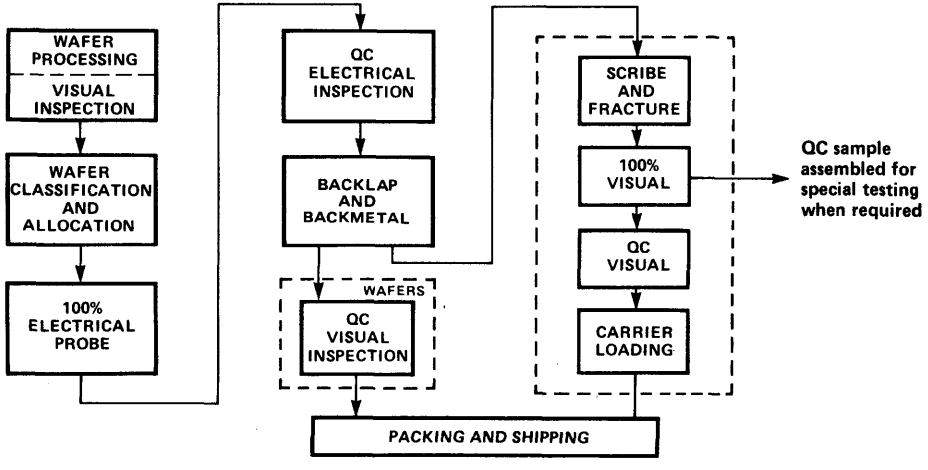
Small Signal Devices

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003" to .006".
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general, dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.

Power FETs

- Chip height ranges from .007" to .020".
- To facilitate die attaching, chips have gold or silver backing.
- Top side metal is aluminum with a thickness of 10,000 - 30,000 angstroms.

CHIP AND WAFER PROCESSING FLOW CHART



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DIE & WAFER ORDERING INFORMATION

RECOMMENDED DICE ASSEMBLY PROCEDURE

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is to boil the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385° C and 400° C with eutectic visible on three sides of the die after attachment.

BONDING:

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430° C.

ELECTRICAL TEST LIMITATIONS

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DUAL BIPOLAR TRANSISTORS

LV_{CEO}	100V max. @ ≤ 1 mA
BV_{CBO}	100V max. @ ≥ 1 μA
BV_{EBO}	100V max. @ ≤ 10 mA
h_{FE}	≤1000 @ ≥ 10 μA
$V_{CE(sat)}$	≥ 10 mV @ ≤ 10 mA
I_{CBO}	≥ 100 pA @ ≤ 100V
$V_{BE1}-V_{BE2}$	≥ 1 mV @ ≥ 10 μA
$I_{B1}-I_{B2}$	≥ 2 nA

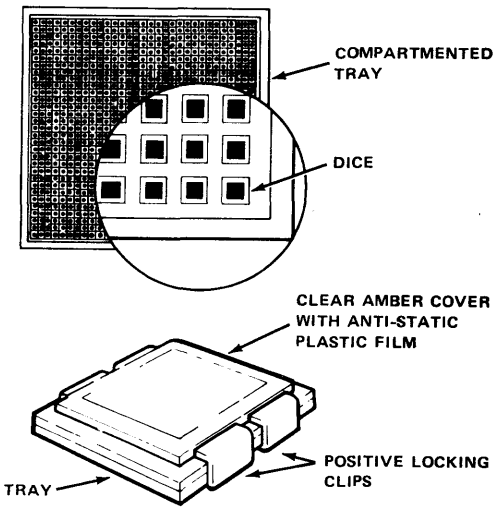
FETS

Breakdown voltage	100V max. @ 1 μA
Pinch-off voltage	0-20V @ ≥ 1 nA
$V_{GS(th)}$	0-20V @ ≥ 10 μA
$r_{DS(on)}$	20 Ω min. @ V_{GS} = 0 (V_{GS} = 30 MOSFETs)
I_{DSS} & I_{DSS}	100 mA max.
g_{fs}	10,000 μMHOS max. @ I_D ≤ 10 mA
$I_{D(off)}$, $I_{S(off)}$, I_{GSS}	100 pA min.
$V_{GS1} - V_{GS2}$ (Duals)	10 mV min.

Electrical testing is guaranteed to a 10% LTPD. AC parameters such as capacitance and switching time cannot be tested in wafer or dice form.

STANDARD DIE CARRIER PACKAGE

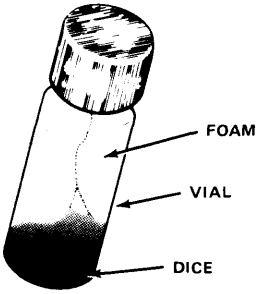
- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection – dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usuable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.



DIE & WAFER ORDERING INFORMATION

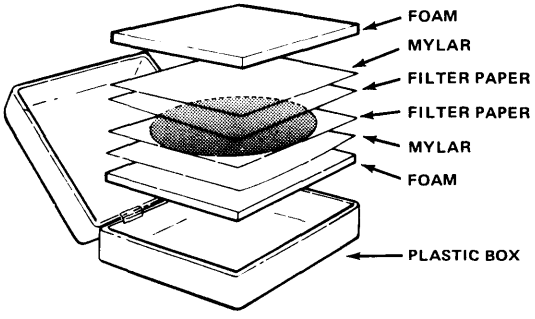
OPTIONAL VIAL PACKAGE

- 100% electrically probed dice with rejects inked but included in vial. Bulk shipment.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lower cost.
- For vial package – replace "D" in catalog number with "V", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/V (2N4416 dice in vial).



OPTIONAL WAFER PACKAGE

- 100% electrically probed – rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package – replace "D" in catalog number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).



NOTE:

Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

ELECTRICAL TEST CAPABILITY

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

Electrical Test Spec.	2N4391 in a TO-18	2N4391 Chip
I_{GSS} @ 25C	100 pA max.	100 pA max.
BV_{GSS}	40V min.	40V min.
$I_{D(off)}$ @ 25C	100 pA max.	100 pA max.
$V_{GS(forward)}$	1V max.	See note 1
$V_{GS(off)}$ or V_P	4V to 10V	4V to 10V
I_{DSS}	50 to 150 mA	50 to 100 mA
$V_{DS(on)}$	0.4V max.	0.4V max.
$r_{DS(on)}$	30Ω max.	30Ω max.
C_{iss}	14 pF max.	Guaranteed by Design
C_{rss}	3.5 pF max.	Guaranteed by Design
t_d	15ns max.	Guaranteed by Design
t_r	5ns max.	Guaranteed by Design
t_{off}	20ns max.	Guaranteed by Design
t_f	15 ns max.	Guaranteed by Design

NOTE 1: This parameter is very dependent upon quality of metallization surface to which chip is attached.

SUMMARY

Of the 14 items specified for the package part, only 7 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is two-fold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe testing can be performed on the packaged devices per individual customer needs. When testing is required other than that called out in the data sheet, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown as follows:

DIE & WAFER ORDERING INFORMATION

FET & DUAL FET PAIRS

1. Leakages to 1 pA (I_{GSS})
2. $r_{DS\ (on)}$ to as low as 4 ohms
3. $I_{D\ (off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. g_{fs} to 10,000 μmho
6. g_{os} to 1 μmho
7. e_n noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz to 100 Hz
8. CMRR to 100 dB
9. $\Delta(V_{GS1}-V_{GS2})/\Delta T$ down to 10μV/°C to an LTPD of 20%
10. g_m match to 5%
11. I_{DSS} match to 5%

TRANSISTOR PAIRS

1. Leakages to as low as 1 pA
2. Beta with collector current up to 50 mA and as low as 100 nA
3. f_T up to 500 MHz with collector currents in the range of 10 μA to 10 mA
4. Noise measurements as low as 5 nV/$\sqrt{Hz}$ from 10 Hz to 100kH
5. $\Delta(V_{BE1}-V_{BE2})/\Delta T$ to 10μV/°C to an LTPD of 20%

VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

B

CMOS INTEGRATED CIRCUIT CHIPS

INTRODUCTION

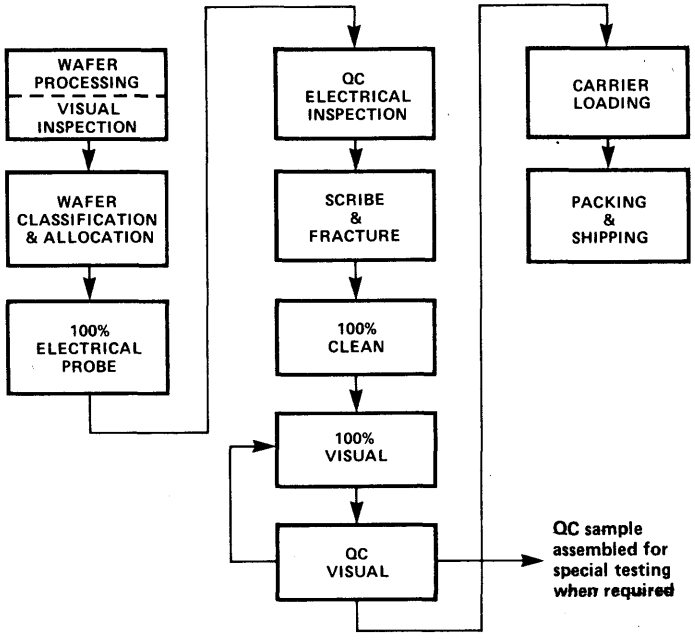
In addition to discrete device chips, Intersil also offers a full line of metal gate CMOS integrated circuits in die form. Die sales, however, present some unique problems. In many cases, chips cannot be guaranteed to the same electrical specifications as can the packaged parts. This is because leakage, noise, AC parameters and temperature testing cannot be guaranteed to the same degree of accuracy for dice as for packaged devices.

GENERAL PHYSICAL INFORMATION

- Chips are available with precise length and width dimensions, ±2 mils in either dimension.
- Chip thickness is 15 mils ±1 mil.
- Bonding pad and interconnect material is aluminum, 10K to 15K Å thick.
- Each die surface is protected by planar passivation and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by an HF etchant; bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.
- Dice are 100% inspected to electrical specifications, then visually inspected according to MIL-STD-883, Method 2010.2, Condition B, with modifications reflecting CMOS requirements.
- Bonding pad dimensions are 4.0 x 4.0 mils minimum.
- Storage temperature is -40°C to +150°C.
- Operating temperature is -20°C to +70°C.
- Guaranteed AQL Levels:

Visual	2.0%
Functional electrical testing	1.0%
Parametric DC testing	4.0%
Untested parameters	10.0%

CMOS INTEGRATED CIRCUIT CHIP PROCESSING FLOW CHART



DIE & WAFER ORDERING INFORMATION

RECOMMENDED DICE ASSEMBLY PROCEDURES

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. However, if cleaning is desired, dice should be subjected to freon TF in a vapor degreaser and then vapor-dried.

RECOMMENDED HANDLING

Intersil recommends that dice be stored in the vacuum-sealed plastic bags which hold the dice carriers. Once removed from the sealed bags, the dice should be stored in a dry, inert-gas atmosphere.

Extreme care should be used when handling dice. Both electrical and visual damage can occur as the result of an unclean environment or harsh handling techniques.

DIE ATTACH

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidization. If a eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C. If hermetic packages are used, epoxy die attach should be carried out with caution so that there will be no "outgassing" of the epoxy.

BONDING

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The wire should be 99.99% pure gold and the aluminum wire should be 99% aluminum/1% silicon. In either case, it is recommended that 1.0 mil wire be used for normal power circuits.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection – dice are in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be used as storage contained for unused dice.
- Carriers hold 25, 100 or 400 dice, depending on die size and quantity ordered.
- Packaging of integrated circuit dice in carriers is identical to illustration shown earlier for discrete device, except that IC chips are not available in vial packs or in wafer form.

CHANGES

Intersil reserves the right in improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect dice electrical limits, pad layouts, or maximum die sizes.

USER RESPONSIBILITY

Written notification of any non-conformance by Intersil of Intersil's dice specifications must be made within 75 days of the shipment date of the die to the user. Intersil assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

PART NUMBERING SYSTEM

Examples of Intersil Part Numbers

BASIC	ELECTRICAL OPTION	TEMP	PKG	PIN	ORDER #
ICH8500	A	C	T	V	ICH8500ACTV
ICL8038	C	C	P	D	ICL8038CCPD
IH5040		M	D	E	IH5040MDE

ON ALL INTERSIL IC PART NUMBERS. THE LAST THREE LETTERS ARE TEMPERATURE, PACKAGE, AND NUMBER OF PINS, RESPECTIVELY.

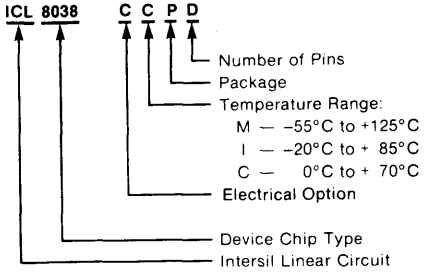
PACKAGE:

A	TO-237
B	Plastic flat-pack
C	TO-220
D	Ceramic dual-in-line
E	Small TO-8
F	Ceramic flat-pack
H	TO-66
I	16 pin (.6 x .7 pin spacing) hermetic hybrid dip
J	Cerdip dual-in-line
K	TO-3
L	Leadless, ceramic
P	Plastic dual-in-line
S	TO-52
T	TO-5 type (also TO-78, TO-99, TO-100)
U	TO-72 type (also TO-18, TO-71)
V	TO-39
Z	TO-92
/W	Wafer
/D	Dice

NUMBER OF PINS:

A	8	P	20
B	10	Q	2
C	12	R	3
D	14	S	4
E	16	T	6
F	22	U	7
G	24	V	8 (0.200" pin circle, isolated case)
H	42		
I	28	W	10 (0.230" pin circle, isolated case)
J	32		
K	35	Y	8 (0.200" pin circle,
L	40		case to pin 4)
M	48	Z	10 (0.230" pin circle,
N	18		case to pin 5)

LINEAR:



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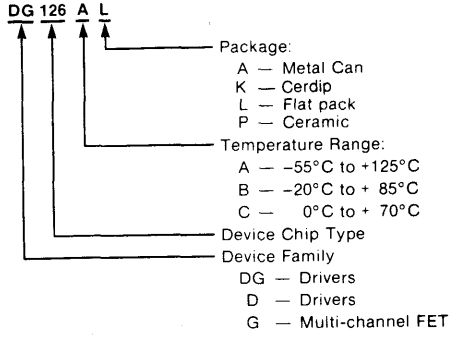
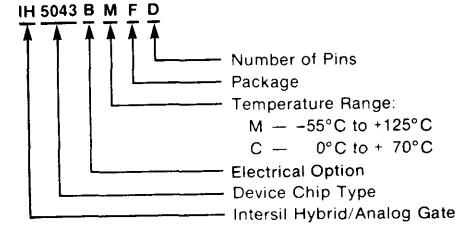
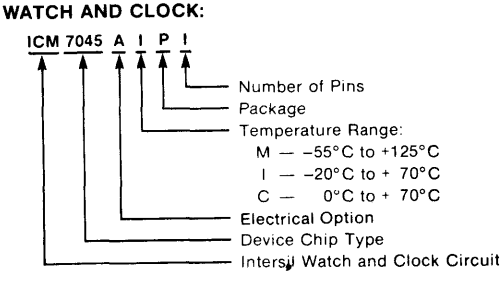




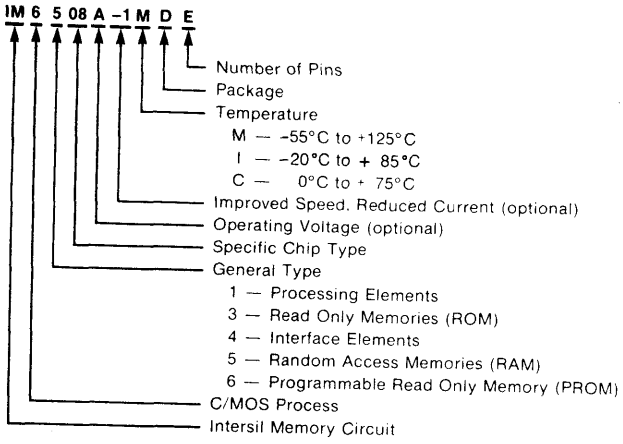
WATCH AND CLOCK:



B

PART NUMBERS AND ORDERING INFORMATION

C/MOS MEMORY:



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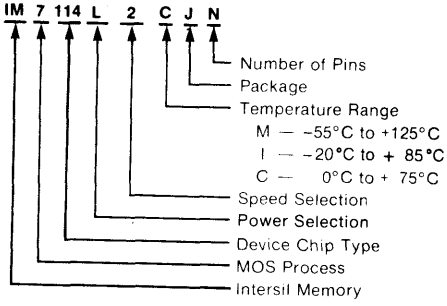

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EXPLANATION OF TERMS, INDICES AND SPECIAL SUBSECTIONS

PRODUCTION DATA SHEET
This is a full, final data sheet, and describes a mature product in full production. Although Intersil reserves the right to make changes in specifications contained in these data sheets at any time without notice, such changes are not common and are usually minor, generally relating to yield and processing improvements. These data sheets are not marked; others are marked preliminary.

PRELIMINARY DATA SHEET
A preliminary data sheet is issued in advance of the availability of production samples and generally indicates that at the time of printing, the device had not been fully characterized. In the case of a second-source part, the specifications are already determined, and a "preliminary" designation indicates the anticipated availability of the device.

ALPHANUMERIC INDEX
This part number index is arranged first by alpha sequence, (ie: ADCxxxx, DGxxx, Gxxx, ICLxxxx, ICMxxxx, etc.) then by numeric sequence (ie: LM100, LM101A, LM102, LM105, etc.) and ignoring package/temperature/pin number suffixes. The basic numbering sequence, is sorted by reading the part number characters from left to right. Reading the left character first (which is usually an alpha character), then the next character to the right and so forth.

BASE NUMBER INDEX
If only the basic part number is known, use the Base Number Index as a locator aid. The Base Number Index is organized in numeric sequence (with alpha prefixes appearing in bold type and numeric characters set in medium type). Devices are arranged in this index according to the numeric value of the first digit on the left, then the value of the second digit, then the third, and so on. For example, device number ICM7218 precedes ICL741, no package/temperature/pin number suffixes are included, but these may be obtained from the specific product data sheet.

FUNCTION INDEX
This is an index of Intersil device types categorized by product grouping and function. The first major subsection, DISCRETES, is further subdivided into categories for JFETs and Special Function devices.

All remaining major subsections (ANALOG SWITCHES/MULTIPLEXERS, DATA ACQUISITION, LINEAR, TIMERS/COUNTERS, TIMEKEEPING/DTMF, MEMORIES and MICROPROCESSORS/PERIPHERALS) are organized alphabetically by function. The Functional Index appears in its entirety in section A, and an appropriate subindex appears at the beginning of each major product section.

CROSS-REFERENCE GUIDES
Two cross-reference guides are provided: one for Discrete Devices and one for Integrated Circuits.

The Discrete Cross-Reference Guide indicates whether Intersil can provide the industry-standard type, or an Intersil preferred part instead.

The IC Alternate Source Cross-Reference Guide lists competitive manufacturer device types for which Intersil makes pin-for-pin replacements. In the left-hand column, the competitive device part number is organized alphabetically by manufacturer. The Intersil pin-for-pin replacement appears in the right hand column.

SELECTOR GUIDES
Selector guide tables appear at the front of each major product category subsection and provides a quick reference of key parameters for devices contained in that section.

DEVICE FUNCTION/PACKAGE CODES
Package dimensions and diagrams explaining device prefix and suffix codes appear in Appendix B.

DIE SELECTION CRITERIA
Many of Intersil's semiconductor products are available in die form. This subsection of Appendix B contains general information on criteria for transistor and integrated circuit die selection, including physical parameters, packaging for shipment, assembly, testing and purchase options.

HIGH-RELIABILITY PROCESSING
This subsection of Appendix B defines Intersil's commitment to 100 percent compliance with MIL-STD-883, MIL-STD-750, MIL-M-38510 and MIL-S-19500 specifications. It also outlines Intersil's programs for quality conformance, quality testing and limited use qualification and includes a glossary of military/aerospace Hi-Rel terms.

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- MULTIPLEXERS
- A/D & D/A CONVERTERS
- LINEAR DEVICES
- DISCRETES/FETs
- TIMERS
- COUNTERS
- DISPLAY DRIVERS
- ROMs/EPROMs
- MICROPROCESSORS AND PERIPHERALS

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